APA750 and A54SX32A LANSCE Neutron Test Report

White Paper

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Executive Summary

The APA750 and A54SX32A (MEC) FPGAs were tested using the WNR neutron beam at Los Alamos National Laboratory. The results are:

- No loss of configuration data was observed in either the APA750 or the A54SX32A.
- No latch-up or upsets to clock or control circuits were observed in either the APA750 or the A54SX32A.
- The only anomalies observed in the APA750 were single event upsets (SEUs) in user flip-flops. The cross section per bit is 3.1×10^{-14} cm^2 for neutron energies > 1.5 MeV and 6.02×10^{-14} cm^2 for neutron energies > 10 MeV.
- The soft error rate (SER) for Flash switches per device is calculated as < 0.051 FITs (failure in time rates) for 95% confidence level if the device is located at sea level in New York City.
- There were no anomalies observed in the A54SX32A. The cross section per user flip-flop is $< 1.24 \times 10^{-13}$ cm^2 for neutron energies > 1.5 MeV and $< 2.4 \times 10^{-13}$ cm^2 for neutron energies > 10 MeV. The SER for antifuse switches per device is calculated as < 0.051 FITs for 95% confidence level if the device is located at sea level in New York City.

During tests, each device received a neutron exposure equivalent to over 675,000 years of exposure to natural atmospheric neutrons at sea level in New York City.

These results indicate that both the ProASIC^{PLUS} (APA) Flash-based FPGAs and the SX-A antifuse-based FPGAs are inherently suitable for applications where the loss of FPGA configuration would have serious consequences for the reliability of the system. Such applications include high-altitude systems such as avionics, and also high-reliability or high-availability ground-based systems such as data storage and carrier-class telecommunications.

Background and Test Objectives

ProASIC^{PLUS} (APA devices) and SX-A devices had been previously tested for single event effects (SEE) using both heavy-ion and proton beams. Test results indicated that both the antifuse and Flash switches are insensitive to proton, and by extrapolation, neutron irradiation. However, industry concern has grown recently surrounding alpha particle-induced and neutron-induced soft errors, or SEUs, in semiconductor devices. For programmable logic devices such as FPGAs, the focus is the susceptibility of the programmable switches. The primary objective is, in the context of the JEDEC standard, JESD89, to confirm that terrestrial neutrons do not induce single event upsets (SEUs) in either the antifuse switch or Flash switch.

Device under Test

The manufacturing source, lot number, date code, and other basic information of the devices under test (DUT) are listed in Table 1.

Table 1: Devices under Test Information

Device	APA750	A54SX32A
Package	PQ208	PQ208
Foundry	UMC	MEC
Technology	0.22 µm CMOS	0.25 µm CMOS
Die Size	10 mm x 11 mm	5.7 mm x 5.5 mm
Die Lot Number	MF228	T25J066
Date Code	0322	0328
Quantity Tested	5	5
Serial Numbers	LAPA1017-1, LAPA1017-2, LAPA1017-3, LAPA1017-4, LAPA1017-5	LSXA1017-1, LSXA1017-2, LSXA1017-3, LSXA1017-4, LSXA1017-5
I/O Configuration	3.3 V CMOS In/3.3 V PCI Out	3.3 V PCI
Test Design	GF50	TMR

Test Methods

The test follows the guidance of *Accelerated terrestrial cosmic ray secondary test procedures* in *JESD89*, pages 25 to 40.

Neutron Irradiation

The irradiation uses the neutron beam of the Weapons Neutron Research (WNR) facility at Los Alamos National Laboratory. DUT LAPA1017-1, -2, and -3, and LSXA1017-1, -2, and -3 were irradiated by a 3 cm-diameter beam and the rest of the DUTs were irradiated by an 8 cm-diameter beam. The flux is independent of the beam size; it fluctuates with a small variation with time. A counter measures the number of counts per run. The facility provides the information of the neutron fluence per count for every 24 hours. Table 2 lists the neutron fluence per count of the 3 cm beam and 8 cm beam respectively. The fluence of each run can be obtained by multiplying the number of counts and the neutron fluence per count.

Table 2: Neutron fluence per count

Energy Spectrum	3 cm Beam	8 cm Beam
> 1.5 MeV	298,305 neutron/cm^2•count	32,575.6 neutron/cm^2•count
> 10 MeV	153,340 neutron/cm^2•count	16,851.7 neutron/cm^2•count

APA750 Test Logic Design

The test logic in the APA750 DUTs, called GF50, consists of two identical 200-flip-flop, first-in-first-out shift registers that use a common clock. The shift registers are labeled DOS and DOH, respectively.

A54SX32A Test Logic Design

The logic design in the A54SX32A DUTs is called TMR. It has four 100-flip-flop, first-in-first-out shift registers, labeled DOS, DOC, DOH and DOVH, in which a common clock is used. DOS and DOC shift

registers use a regular flip-flop for each bit, while DOH and DOVH registers use a triple module redundant (TMR) flip-flop configuration, where each register is implemented using three flip-flops.

Instrumentation

The instrumentation tests two DUTs simultaneously. In each run, an APA750 DUT on a ProASIC^{PLUS} board and an A54SX32A DUT on an SX-A board were tested in parallel.

The test signal generation and data collection are automated by using a PC as the command-control console. The operator uses GUI software to conduct the testing by commanding the communications between an I/O-counter board in the PC and DUT boards in the irradiation area. Figure 1 on page 5 shows a block diagram illustrating how SEUs are measured. The I/O-counter board selects the signal generated by the control chip. The signal pattern is clocked through the DUT shift registers and then compared with the original pattern. Since the irradiation only strikes the DUT chip, the occurrence of SEUs will produce signal pulses at the comparator output. One SEU in the DUT shift register will be counted as one error. The error counts during each run will keep accumulating until a reset button is depressed. Each shift register uses one counter; the APA750 has two counters and the A54SX32A has four.

The data generator can generate one, zero, and checkerboard patterns. The clock frequency was set at 2 MHz. The design has a self-testing mechanism so that a data-pattern change during clocking will generate a constant error count. This self-testing was exercised during each long testing run (approximately 10–12 hours) to ensure the testing validity. The nominal biases for both APA750 DUT and A54SX32A are 3.3V/2.5V on V_{CCI}/V_{CCA}.

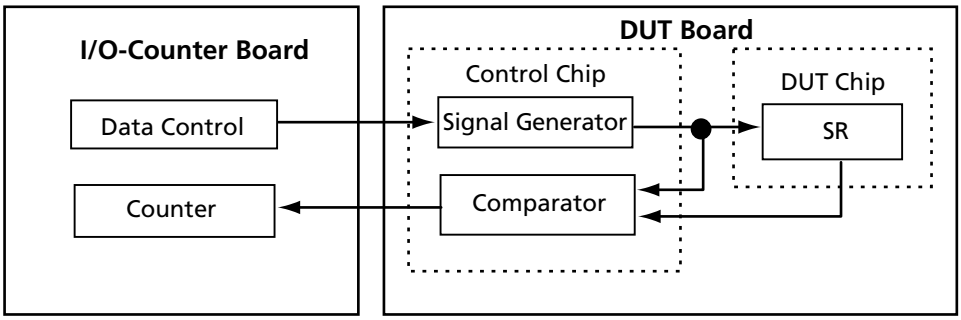


Figure 1: Schematic Showing SEU Error-Detecting Mechanism

Physical Setup

The ProASIC^{PLUS} board and SX-A board, which are both the same size, were stacked in parallel and perpendicular to the neutron beam. A laser beam was used to align and center the DUTs. DUT boards were inside the radiation area and connected to the I/O-counter board by long twisted ribbon cables. The testing ambient temperature was the same as the room temperature, approximately 20°C.

Test Results and Discussions

APA750

Functionality and I_{CC}

The self-testing was exercised multiple times during each run to verify the functionality of the DUT during irradiation. The first DUT was monitored about every hour and the following DUTs were monitored about every two hours. Every DUT passed every functional check throughout the irradiation. The I_{CC} was monitored visually. No I_{CC} change was observed in any DUT.

SEU and Other SEE

Table 3 summarizes the test data of the APA750. Only two upsets were observed in the whole experiment. The cross section per bit is obtained as 3.1×10^{-14} cm^2 for neutron energies > 1.5 MeV and 6.02×10^{-14} cm^2 for neutron energies > 10 MeV. No other SEE was observed in any DUT.

Table 3: Flip-Flop Upsets in DUR Shift Registers

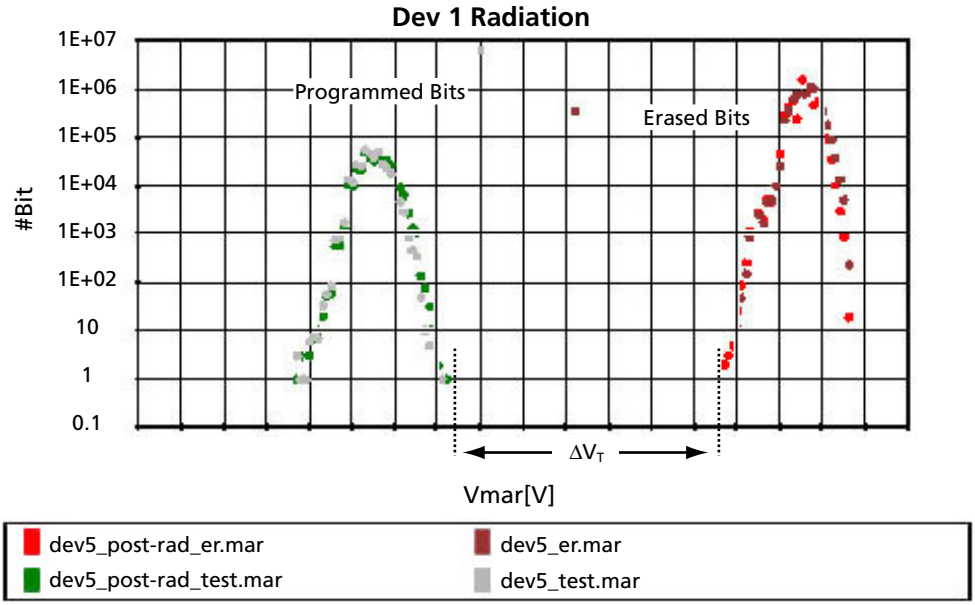
DUT	Fluence (neutron/cm^2)		Flip-flop Upsets	
	> 1.5 MeV	> 10 MeV	DOS	DOH
LAPA1017-1	3.58×10^{10}	1.84×10^{10}	1	0
LAPA1017-2	3.58×10^{10}	1.84×10^{10}	0	0
LAPA1017-3	3.03×10^{10}	1.56×10^{10}	0	0
LAPA1017-4	2.57×10^{10}	1.33×10^{10}	1	0
LAPA1017-5	3.36×10^{10}	1.74×10^{10}	0	0

Neutron Effects on Flash Switches

The pre- and post-irradiated threshold voltage (V_T) of every Flash switch was measured to evaluate the neutron-induced effect. The data show that in every DUT, the number of programmed bits (360,475) was not changed by neutron irradiation. Figure 2 on page 7 shows the pre- and post-irradiation V_T distributions of the programmed bits and that of the erased bits in DUT LAPA1017-1. The changes of these distributions due to the irradiation are within a few tenths of a volt near the distribution tails. The most important parameter, the separation between the V_T of the programmed bits and V_T of the erased bits, is practically not affected by the irradiation. The minimum separation (ΔV_T in Figure 2) of each DUT maintains 6 V or more after the irradiation. The same conclusion applies to the test results of the other DUTs, whose pre- and post-irradiation V_T distributions are shown in Figure 3 on page 7 to Figure 6 on page 9. The measurement of pre- and post-irradiation data is separated by about a month. The effect of elapsed time and tester noise may produce the same magnitude of the observed variances. A control group will be tested in the future to ascertain if the observed minute variances are really due to the neutron-induced effect.

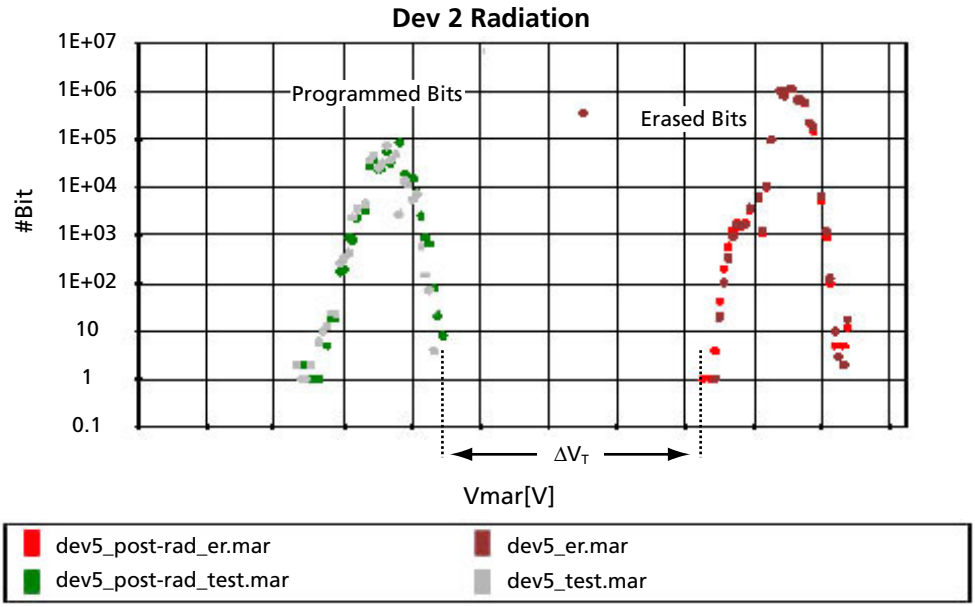
Soft Error Rate (SER) Statistics of Floating-Gate Switches

Sea level at New York City is used as the reference location for the SER statistics. Using > 10 MeV, the neutron flux New York City is 0.0039 neutrons/cm^2•sec. The total number of tested device-hours normalized to New York City is thus 5.92×10^9 device-hours. Note that in the device-hour unit, a device means a DUT. Since there is no failure due to Flash switches, the failure rate of Flash switches per device is < 0.051 FITs for 95% confidence level. For ProASIC^{PLUS} devices of different sizes, FIT rates can be obtained by linearly scaling this FIT rate with the number of switches.



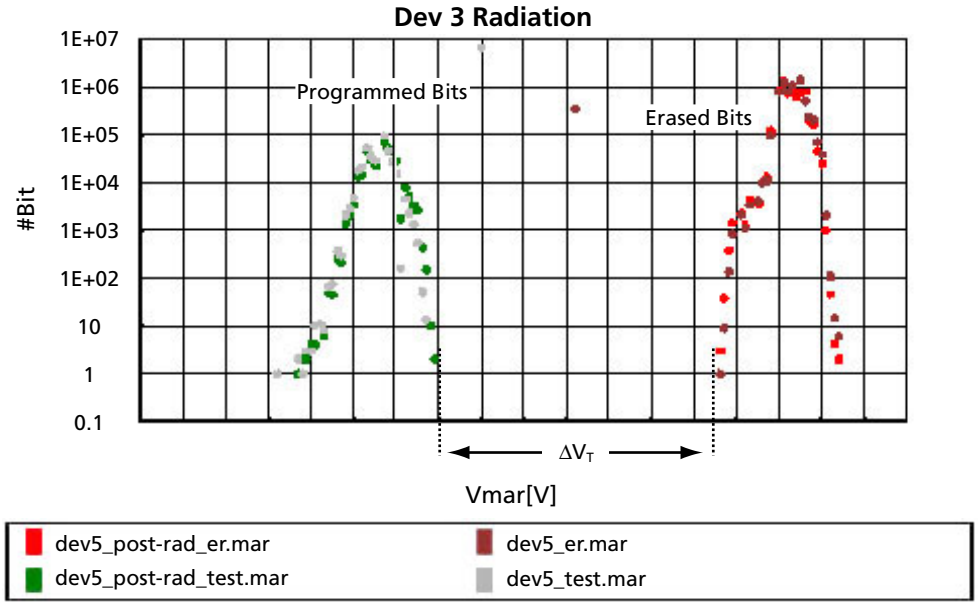
In post-irradiation DUT, the minimum separation between the distributions (ΔV_T) is over 6V. The radiation-induced degradation of this separation is small and indistinguishable from the testing noise.

Figure 2: Pre- and Post-irradiation V_T Distributions of DUT LAPA1017-1



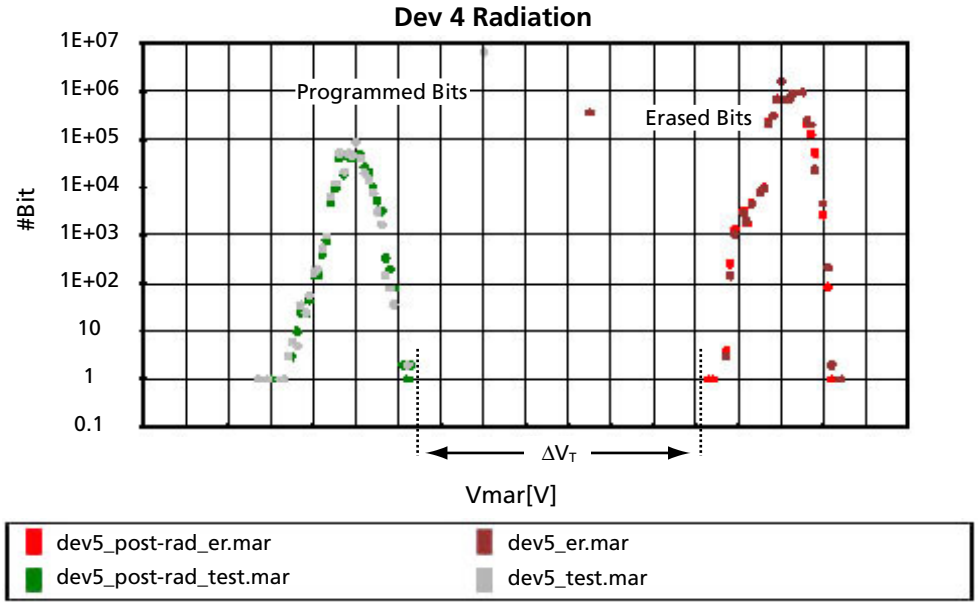
In post-irradiation DUT, the minimum separation between the distributions (ΔV_T) is over 6V. The radiation-induced degradation of this separation is small and indistinguishable from the testing noise. Note that the abscissa scale is different from that of Figure 2 on page 7.

Figure 3: Pre- and Post-irradiation V_T Distributions of DUT LAPA1017-2.



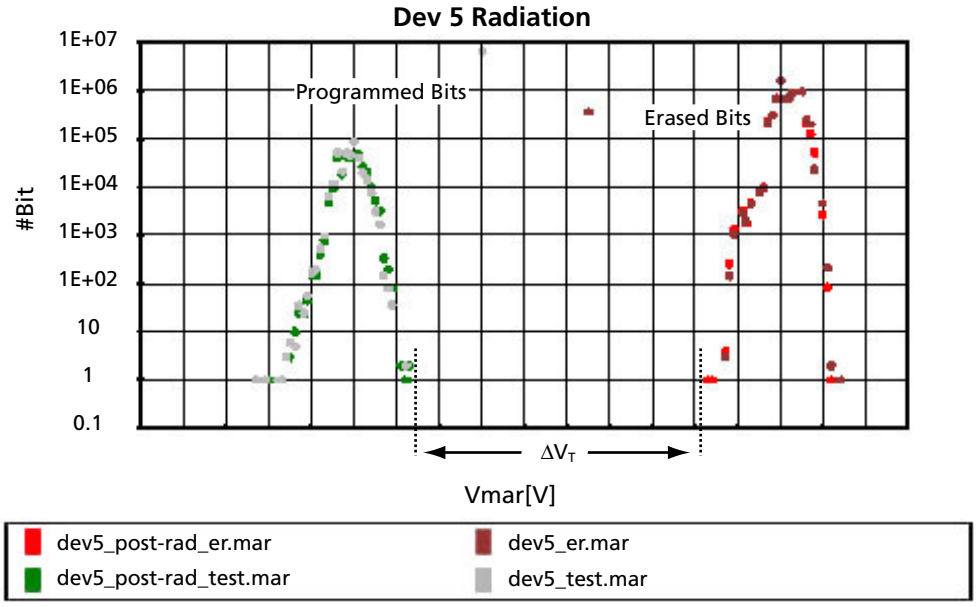
In post-irradiation DUT, the minimum separation between the distributions (ΔV_T) is over 6V. The radiation-induced degradation of this separation is small and indistinguishable from the testing noise.

Figure 4: Pre- and Post-irradiation V_T Distributions of DUT LAPA1017-3



In post-irradiation DUT, the minimum separation between the distributions (ΔV_T) is over 6V. The radiation-induced degradation of this separation is small and indistinguishable from the testing noise.

Figure 5: Pre- and Post-irradiation V_T Distributions of DUT LAPA1017-4



In post-irradiation DUT, the minimum separation between the distributions (ΔV_T) is over 6V. The radiation-induced degradation of this separation is small and indistinguishable from the testing noise.

Figure 6: Pre- and post-irradiation V_T distributions of DUT LAPA1017-5

A54SX32A

Functionality and I_{CC}

The self-test circuit was exercised multiple times during each run to check the functionality of the DUT during irradiation. Every DUT passed every functional check throughout the irradiation. The I_{CC} was monitored visually, and no I_{CC} change was observed in any DUT.

SEU and Other SEE

Table 3 on page 5 summarizes the A54SX32A test data. Due to bad connections on the board, only two shift-registers DOS and DOVH could be monitored during irradiation. No upsets were observed in any shift-register in any DUT. Since only DOS consists of regular flip-flops, the cross section is obtained per DOS flip-flop. The SEU rate is obtained as $< 1.24 \times 10^{-13}$ cm^2 for neutron energies > 1.5 MeV and $< 2.4 \times 10^{-13}$ cm^2 for neutron energies > 10 MeV. No other SEE was observed in any DUT.

Table 4: Flip-flop upsets in shift registers of the DUTs

DUT	Fluence (neutron/cm^2)		Flip-flop upsets	
	> 1.5 MeV	> 10 MeV	DOS	DOVH
LSXA1017-1	3.58×10^{10}	1.84×10^{10}	0	0
LSXA1017-2	3.58×10^{10}	1.84×10^{10}	0	0
LSXA1017-3	3.03×10^{10}	1.56×10^{10}	0	0
LSXA1017-4	2.57×10^{10}	1.33×10^{10}	0	0
LSXA1017-5	3.36×10^{10}	1.74×10^{10}	0	0

Neutron Effects on Antifuse Switches and the SER Statistic

The antifuse switch is intrinsically immune to neutrons. The non-programmed antifuse switch is a capacitor, and the programmed antifuse switch is a metallic link. Nevertheless, the same SER statistics used in the APA750 can be applied here.

New York City is used as the reference location for the SER statistics. Using > 10 MeV, the neutron flux at New York City is 0.0039 neutrons/cm^2•sec. The total tested device-hours normalized to New York City is thus 5.92 x 10^9 device-hours. Since there was no observable failure due to antifuse switches, the failure rate of antifuse switches per device is < 0.051 FITs for 95% confidence level.

Summary and Conclusion

Five devices each of the APA750 Flash-based FPGAs and the A54SX32A antifuse-based FPGAs were subjected to neutron irradiation in the WNR facility at Los Alamos National Laboratory. The total exposure of each device to neutrons was equivalent to 5.92 x 10^9 device hours (or 675,800 device years) exposure to atmospheric neutrons at sea level in New York City. No upsets to the device configuration switches in either the Flash-based or antifuse-based FPGAs were detected.

These results indicate that both the ProASIC^{PLUS} (APA) Flash-based FPGAs and the SX-A antifuse-based FPGAs are ideally suited to applications where neutron exposure is an environmental hazard. Such applications include atmospheric avionics applications, ground level data storage and transmission applications, such as storage area networking, and carrier-class telecommunications and networking applications.

For more information, visit our website at **http://www.actel.com**

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