Jitter and Phase Noise Analysis of Actel's eX Devices

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Introduction

What was deemed as acceptable performance for system clocks and references in high-speed communication and measurement systems in past years, may not now be sufficient to support future applications that require high-speed synchronous equipment. Emerging protocols such as RapidIO, OC-N, and Hypertransport and PCI-Express that require complex CDR schemes are increasing the demands on the levels of acceptable performance required from applications.

Jitter is one of the most important and least understood measurements of clock performance. In the end, jitter determines whether your development project and end product will succeed from a time-to-market and performance perspective.

Telcordia's (Bellcore) GR-1244 specification states:

"Jitter is defined in GR-499-CORE as the short-term variations of a digital signal's significant instants (e.g., optimum sampling instants) from their ideal positions in time. Short-term variations are phase oscillations of frequencies greater than a demarcation point that is specified for each interface rate. For DS1 signals, the demarcation point is 10 Hz, and jitter is measured through the equivalent of a single pole high-pass filter having a pole frequency of 10 Hz. Jitter may be specified and measured in terms of either the rms or peak-to-peak variations that occur. In addition, it is usually given in units of UIs, but may also be expressed in terms of phase-time (e.g., nanoseconds)."

The reduction of these short-term signal variations is the foundation for high performance telecom applications. Low noise components are the first step towards achieving these signal reduction goals. When interfaces and protocols are discussed, the term "clock budgets" is becoming widely used as a term for describing these high performance applications. As protocols like RapidIO, Hypertransport and PCI-Express, and OC-N become widely available, these clock budgets are reducing in size. These reductions in clock budgets and periods are beginning to limit the options of engineer's when it comes to component selection.

In the past, due to their excessive jitter generation, programmable logic devices (PLDs) have only been used on a limited basis as a direct clock generator output. Actel's FPGA antifuse technology provides an exception to this rule. Actel discovered that its eX device family could operate as a clock source output with minimal effort and possessed the bandwidth to run complex detection circuits in excess of 160 MHz at a reasonable cost. This discovery resulted from test data indicating that the eX device adds minimal jitter and phase noise to the source input from the reference clock source.

Measurement Background

Phase noise is the frequency domain measurement of phase modulated noise on an RF carrier and is normalized to a 1Hz bandwidth. The spectrum analyzer is used to chart the measurement graph. This measurement is used to show the frequency of the noise on the carrier, and the amplitude of the noise at that frequency. On the phase noise graph, the frequencies toward the left are the frequencies approaching the carrier frequency. The frequencies toward the right are a departure from the carrier frequency. The amplitude measured can show spurious noise as well as the noise at the domain's frequency. Spurious noise in the measurement can come from external signals, such as computing equipment or radio stations in the area. If a phase noise plot is made of 155.52 MHz and a local police station is using 155.40 MHz, it is possible to measure an intermittent spur at a 120 kHz offset. Phase noise is not a real time measurement, it is averaged over several sweeps. The more times the measurement is averaged, the more defined a line is made for the noise. This produces less ambiguity in the measurement but requires more time to take the measurement.

Phase noise can degrade the effectiveness of data transmission by creating timing errors where the data is not timed properly at the receiving end. These timing errors depend on how much noise there is and how high the frequency has

been multiplied. When the eX64 device is analyzed as a buffer, the accuracy with which the eX64 will replicate the signal edge position of the input signal in the time domain is measured. To analyze how the noise is distributed, this measurement is made in the frequency domain.

For example, in SONET, there is particular interest in the noise of the signal offset from 12 kHz to 20 MHz. Replicating the signal at the input requires the eX64 device to accurately trigger off of the same edge point at each and every edge. Variations in this response will result in a less predictable output and a higher level of phase noise in the output.

A phase noise measurement system can be made on a phase noise measurement machine which consists of a quadrature phase detector, controller, audio spectrum analyzer, and an RF reference (Figure 1).

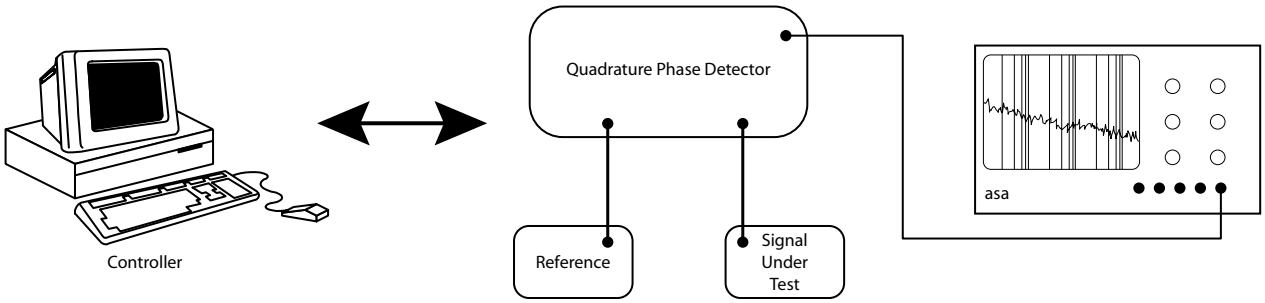

Figure 1: Phase Noise Measurement System

The audio spectrum analyzer should cover the range frequencies under review. For example, if a range of 10 Hz to 1 MHz offset frequencies is under review on a 100 MHz RF signal, then an audio spectrum analyzer of at least 10 Hz to 1MHz is needed for the measurement. Therefore, a 1 MHz spectrum analyzer can also be used for microwave-frequency phase noise measurements as long as the required offset is less than 1 MHz. The reference is used at the signal under test frequency and is tuned to output a phase that is in quadrature with the signal under test. The reference should be significantly better than the phase noise of the signal under test, since noise from the reference can have an effect on the results as well as the device being tested. The quadrature phase detector converts the phase variations from the two oscillators into a DC signal, which can be AC coupled and amplified to represent the instantaneous phase changes and rates of changes. Even though the phase detector outputs a basic DC signal, the AC components of that signal are stripped off for analysis in the spectrum analyzer. This transforms the time domain phase error into a frequency domain signal for measurement. Since noise measurements are different for incremental bandwidth changes, the noise level at a reference 1Hz bandwidth is analyzed. This ensures that measurements can be portable and allows different noise measurements to be directly compared without the need to transform bandwidth properties. Also, the DC information is used to electrically control the frequency of the reference to keep the signals in quadrature. The phase detector normally acts as a phase locked loop where the loop bandwidth is much lower than the lowest end of the measured frequency range of the phase noise measurement. This ensures that the system loop does not affect the measurement.

Figure 2 and Figure 3 illustrate two phase noise plots that were measured with the system in Figure 1 on page 3.

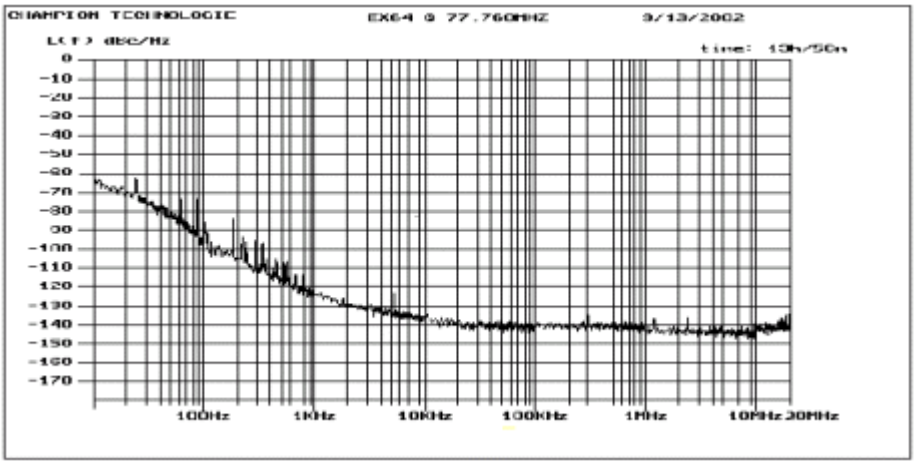

Figure 2: ex64

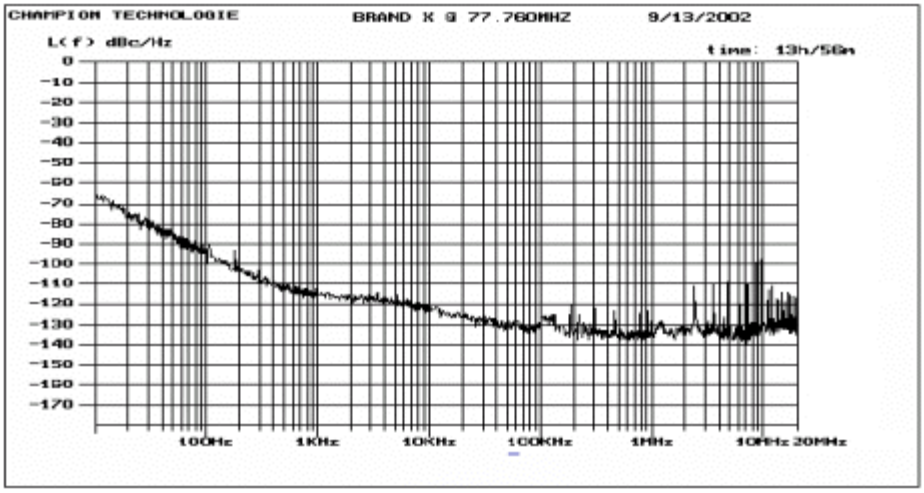

Figure 3: Brand X

Example Standard Timing Requirements

A key aspect of SONET equipment systems is that the network is based on synchronous clocking for the entire network system. This means that issues the asynchronous systems normally compensate for cannot be tolerated in a network using a synchronous clocking scheme. Distributing a synchronous clock to all the components of a communications network is an incredibly difficult task. This is where jitter and phase noise have become critical components in synchronizing all the sub-components of the network. Various components in the system have hierarchy timing requirements that are rated as “Stratum Levels.” Depending on where the sub-component is located in the network, a higher or lower accuracy and stability will be required for that particular clock source. In the case of SONET, Stratum Level 1 is the most accurate timing requirement and the source for all other lower levels in the communications network.

Table 1 shows the hierarchy for the Stratum Levels required for SONET equipment to function properly in the network.

Table 1 • Stratum Level Hierarchy

Level	Free-Run Accuracy	Holdover Stability	Minimum Pull-in and Hold-in Range	Filtering	Output Phase Transients
1	±1 × 10 -11	N/A	N/A	N/A	N/A
2	±1.6 × 10 -8 (±0.025 Hz@ 1.544 MHz)	±1 × 10 -10 /day	±1.6 ×10 -8	Yes, 0.001 Hz	MTIE =150 ns
TNC	±1.0 × 10 -7	±1.5 × 10 -9 /day	±1.0 ×10 -7	Yes, 0.1 Hz	MTIE =1.0 µs
3E	±4.6 × 10 -6 (±7.1 Hz @ 1.544 MHz)	±1.2 × 10 -8 for the initial 24 hrs of holdover	±4.6 ×10 -6	Yes, 0.001 Hz	MTIE =150 ns
3	±4.6 × 10 -6 (±7.1 Hz @ 1.544 MHz)	<255 slips (±3.7 ×10 -7) for the initial 24 hrs of holdover	±4.6 ×10 -6	Yes, 3 Hz	MTIE =1.0 µs
SMC	±20 × 10 -6 (±31 Hz @ 1.544 MHz)	±4.6 × 10 -6 for the initial 24 hrs of holdover	±4.6 ×10 -6 or ±20 ×10 -6	Yes, 0.1 Hz	MTIE =1.0 µs

The requirements for an accurate and stable clock are extremely stringent. As SONET (OC-N) timing requirements increase in bandwidth, the clocking periods for these source synchronous systems are decreasing. Because of this, the components required to operate at these clock periods or Unit Intervals (UIs) must perform at proportional jitter outputs to the overall UI of the measured period that is specified in the SONET specification. This jitter output in the specification must maintain a level of less than 1ps for offsets between 12 kHz and 20 MHz.

Testing

For comparative purposes, a test program was developed to determine the performance of the Actel solution and a leading competitive PLD. A semi-uniform design was implemented in both devices to evaluate the signal outputs that are buffered and divisions from the VCXO source. Figure 4 shows the Actel test circuit.

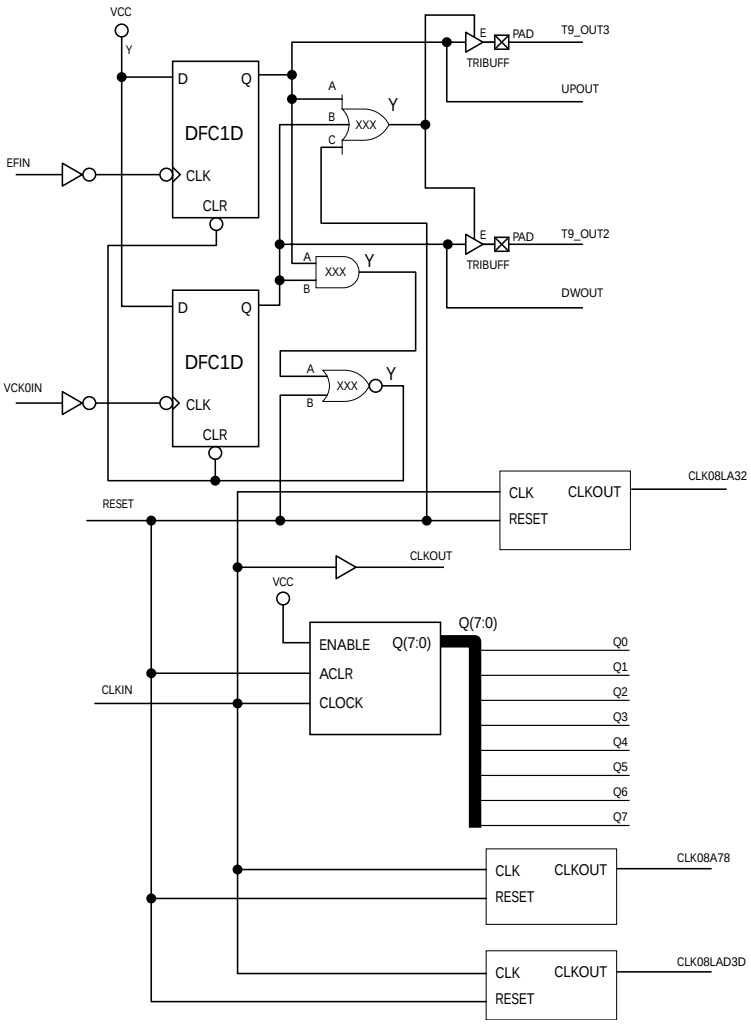

Figure 4: Actel Test Circuit

The above circuit was used to determine various performance qualities of the Actel eX device and the competitive PLD. One difference between the Actel test circuit and the competitive device is the CLKDBLR blocks. These three blocks were used for clock doubling of the VCXO input on CLOCKIN. There are three different blocks for an optimized output at the three tested frequencies, 32.768, 77.76, and 131 MHz. For each frequency input, the clock-doubling block in Figure 4 provided an appropriate clean doubled clock output at a 45 - 55% duty cycle. These three blocks were built with behavioral VHDL code with instantiated Actel delay buffers. Further optimization is possible to tighten the duty cycle to 50%, but this was not the purpose of the testing.

These two components are similar in both test circuits, the 8-bit counter that was built with Actel's ACTgen Macrobuilder and the buffer. The counter was used as a frequency divider for the CLOCKIN input. This CLOCKIN input was also fed straight through the eX device to a buffered output pin CLOCKOUT for jitter measurements.

The flip-flops and combinatorial cells are used to verify the performance of Actel's tristate buffers. The PLD device does not have this output feature for the same density.

The overall circuit in Figure 4 on page 6 utilized the following cells for the eX64-TQ100 device:

Table 2 • Cells for the eX64-TQ100 Device

Cells	Used	Total	Utilization Percentage
Sequential	16	64	25.00%
Combinatorial	42	128	32.81%
Logic	58	192	30.21% (seq+comb)
I/O w/ Clocks	21	38	
Clock	2	2	
HCLOCK	0	1	

Actel's Libero™ Integrated Design Environment (IDE) was used to develop the design for the eX device, and a BP Microsystems programmer was used to program the eX64. The competitor's CPLD was designed and programed in much the same way in order to test the results of the CPLD output performance. The utilization for this design with an 8-bit counter was nine macro-cells and nine product terms. The design for the competitive device was much smaller without the three clock-doubler circuits and tristate test function. However, the power numbers for the Actel device are much lower even though the design is more complicated and runs at higher frequencies.

Figure 5 on page 8 indicates the test setup required two oscilloscopes and a variable power supply. The actual test board included a LDO regulator from National and F1533 oscillators from Champion Technologies, Inc. This test setup was not optimized for layout since this was a generic prototype board that was used for evaluation of new technologies.

The digital storage oscilloscope, which was used for these measurements, is a sampling storage oscilloscope that provides a comprehensive jitter measurement over time. The signal parameters that were measured over time are RMS jitter, Pk-Pk jitter, distance from the trigger edge, and statistical standard deviation from the center. The scope provides a graphical display of the edge being measured, and a graphical histogram of this edge for symmetry analysis and indication of multi-modal peaks. Figure 6 on page 8 is a sample display of the Digital Storage Oscilloscope used for the testing. The measurement is on the first possible rising edge after the scope triggers. The first column at the bottom indicates the window of measurement is in mV and the time window is in ns. The second column displays the mean edge of the measurements, the RMS jitter, the pk-pk jitter, and the number of sample edges being measured. The third column is the standard deviation and the number of waveforms included in that measurement

Figure 6 on page 8 displays a phenomenon for the rising edge called a "bimodal histogram." Even though a solid line is visible for the edge, this display is a summation of multiple samples. The histogram provides the user with an indication of the distribution of the samples in relation to each other. In this particular case, the histogram is displaying two peaks. This means that the samples are concentrated at two points and that there could be potential problems with power supply noise, circuit layout, and/or application issues.

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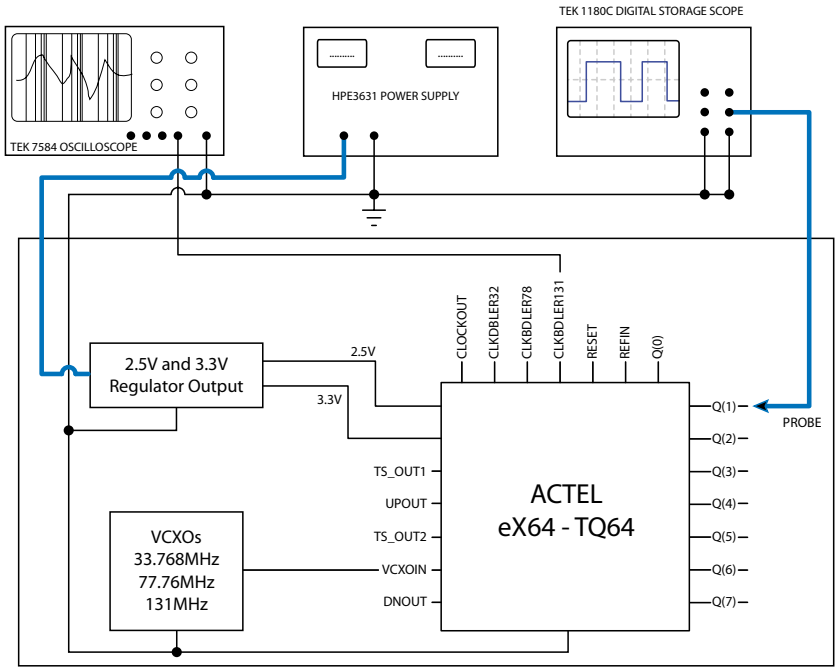

Figure 5: Test Setup

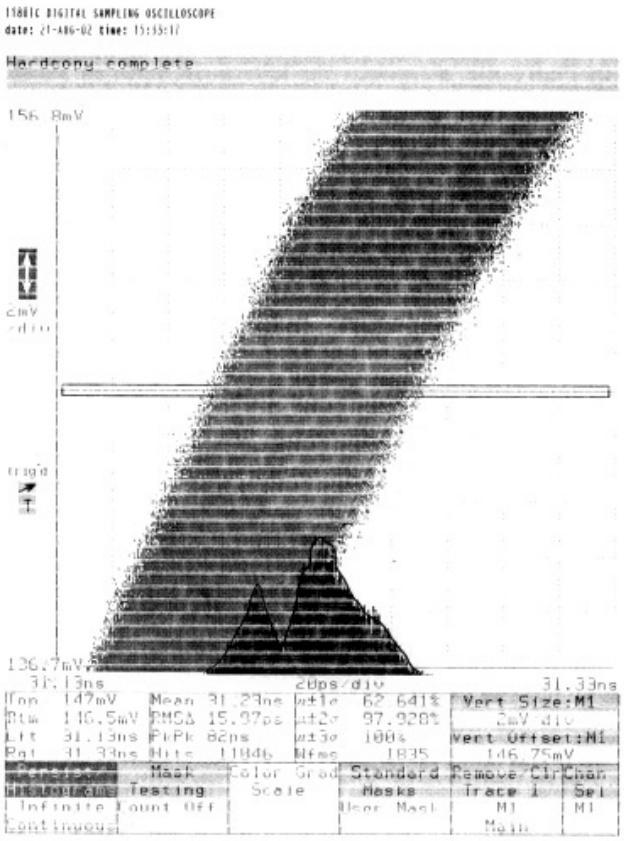

Figure 6: Sample Display of the Digital Storage Oscilloscope

This method of measurement, the histogram function, is one of the most straightforward ways to display jitter. This renders the actual values of the time difference from the rising edge of one cycle to the rising edge of the next trigger point depicted as a histogram displaying the statistics of the signal periods. This method does not take into account changes in amplitude, wave shape, or pulse period.

The results are outlined in several reference frequencies used in the test in Table 3, Table 4, and Table 5.

Table 3 • Test 1[1]

Pin Description	Pin #	Dir.	Jitter (RMS ps)	Jitter (pk-pk ps)	Measurement Range (mV)	Notes
VCXOIN	48	IN	10.38	---	141.2 - 140.8	30.92ns out for rising edge
CLOCKOUT	63	OUT	9.653	---	141.2 - 140.8	31.25ns out for rising edge
Q(0)	50	OUT	18.3	---	148 - 147.6	61.79ns out for rising edge (Bimodal)
Q(1)	49	OUT	4.576	---	145.7 - 145.3	122.9ns out for rising edge
Q(2)	38	OUT	4.235	---	149.5 - 149.0	245ns out for rising edge
Q(3)	51	OUT	4.32	---	152.5 - 152.1	489.1ns out for rising edge (Bimodal)
Q(4)	42	OUT	6.48	---	151.7 - 151.3	977.5ns out for rising edge
Q(5)	39	OUT	7.503	---	141.2 - 140.8	1.954ms out for rising edge
Q(6)	29	OUT	7.276	---	148.7 - 148.5	
Q(7)	34	OUT	10	---	136.7 - 136.3	7.814us out for rising edge
REFIN	60	IN				
RESET	28	IN				
TS_OUT1	27	OUT	---	---	---	
TS_OUT2	24	OUT	---	---	---	
UPOUT	53	OUT	---	---	---	
DNOUT	54	OUT	---	---	---	
VCXO output						32.768 MHz
V_{CCA}						2.5V input
V_{CCI}						3.3V input
Circuit Current						17mA

1. Layout software driven. Notice that this may not have been optimal after looking at the close proximity of the high frequency outputs Q(0), Q(1), and Q(3). Also, there was not a lot of bypassing for power noise. Caps were added to reduce the power supply noise.
All of these tests were performed at ambient temperature in the laboratory.
All tests used High Slew Rate Outputs from the eX device

Table 4 • Test 2[1]

Pin Description	Pin #	Dir.	Jitter (RMS ps)	Jitter (pk-pk ps)	Measurement Range (mV)	Notes
VCXOIN	48	IN	19.69	146	132.4 - 132.2	4th Cycle Out
CLOCKOUT	63	OUT	18	105	155.4 - 155.2	3rd Cycle Out
Q(0)	50	OUT	10.54	69.2	147.9 - 147.7	Bimodal Histogram
Q(1)	49	OUT	22	117	149.9 - 149.7	Extreme Power Supply Noise
Q(2)	38	OUT	9.2	52	147.9 - 147.7	
Q(3)	51	OUT	12	59	147.9 - 147.7	Bimodal Histogram
Q(4)	42	OUT	4.8	32	147.9 - 147.7	Extreme Power Supply Noise
Q(5)	39	OUT	13	67	147.9 - 147.7	Power Supply Prevalent
Q(6)	29	OUT	7.62	44	147.9 - 147.7	
Q(7)	34	OUT	9.78	52	149.4 - 149.2	
CLKDBLER32	26	OUT	---	---	---	
CLKDBLER78	20	OUT	---	---	---	
CLKDBLER131	24	OUT	---	---	---	Output 262 MHz Sawtooth
REFIN	60	IN				
RESET	28	IN				
TS_OUT1	27	OUT	---	---	---	
TS_OUT2	43	OUT	---	---	---	
UPOUT	53	OUT	---	---	---	
DNOUT	54	OUT	---	---	---	
VCXO output						131 MHz
V_{CCA}						2.5V input
V_{CCI}						3.3V input
Circuit Current						171mA

1. Investigated power supply output and discovered that the supply was noisy. After further troubleshooting, it was found that another circuit was on the same power supply output. The other circuit was removed and a few of the noisy outputs were tested. This reduced the jitter and the noise generated on the output signals of the counter outputs.
   The counter output register layout was modified by hand placement as close to the outpad as possible. Notice that this was not optimal after looking at the close proximity of the high frequency outputs Q(0), Q(1), and Q(3). Its is possible that the bimodal condition on Q(0) and Q(3) is generated by crosstalk at this frequency since the logic and routing resources are in such close proximity to each other.
   All of these tests were performed at ambient temp in the laboratory.

Table 5 • Test 3[1]

Pin Description	Pin #	Dir.	Jitter (RMS ps)	Jitter (pk-pk ps)	Measurement Range (mV)	Notes
VCXOIN	48	IN	8.3	72.8	150.4 - 150.2	26.24ns out for rising edge
CLOCKOUT	63	OUT	15	53	147.9 - 147.7	26.28ns out for rising edge (Multimode(5))
Q(0)	50	OUT	21.1	117	141.4 - 141.2	26.29ns out for rising edge (Multimode(7))
Q(1)	49	OUT	18.5	95	147.2 - 147.0	51.65ns out for rising edge (Multimode(7))
Q(2)	38	OUT	5	35	147.9 - 147.7	103.4ns out for rising edge
Q(3)	51	OUT	3.3	24.8	148.7 - 148.5	206.4ns out for rising edge
Q(4)	42	OUT	4.6	29	147.9 - 147.7	412.1ns out for rising edge
Q(5)	39	OUT	6.6	49	147.9 - 147.7	823.4ns out for rising edge
Q(6)	29	OUT	5.54	44	148.7 - 148.5	1.646us out for rising edge
Q(7)	34	OUT	6	42	153.7 - 153.4	3.293us out for rising edge
CLKDBLER32	26	OUT	---	---	---	
CLKDBLER78	20	OUT	11	115	89.9 - 89.7	Output 155.52 MHz
CLKDBLER131	24	OUT	---	---	---	
REFIN	60	IN				
RESET	28	IN				
TS_OUT1	27	OUT	---	---	---	
TS_OUT2	43	OUT	---	---	---	
UPOUT	53	OUT	---	---	---	
DNOUT	54	OUT	---	---	---	
VCXO output						77.76 MHz
V_{CCA}						2.5V input
V_{CCI}						3.3V input
Circuit Current						56mA (12mA OSC)

1. The counter output register layout was modified by hand placement as close to the outpad as possible. Notice that outputs Clockout, Q(0), and Q(1) have multimode outputs. This was very interesting since the modes were distinct with dead space separation. It was like there were multiple signals coming out on the output pad. What also makes this interesting is the pk-pk measurements for these outputs are higher than the VCXO, but the worst output is 60% greater. These signals may also result from bad placement. The overall RMS signals are still low.
   All of these tests were done at ambient temperature in the arbitrator.

Results

The test results of the eX64 samples meet the criteria specified in the SONET requirements of GR-253 jitter generation. The phase noise of the 77.760 MHz buffered output from the eX64 device, the cumulative jitter level from 12 kHz to 20 MHz was better than 0.7ps. The jitter output for the competing CPLD with a similar implemented logic usage is over 14 ps. Clearly, the CPLD is not an option for the implementation as a buffer, but with the output capabilities of the eX devices it is definitely an option for an engineer to investigate. To implement the buffer with a CPLD, the VCXO output must be buffered externally to the CPLD to obtain the specified jitter performance. This requires additional components and reduces the functionality of the CPLD.

Multiple eX64 units were tested to verify that the results are replicable with hand and software-driven placement.

Some notable features or differences that were discovered are:

1. Current consumption of the eX64 was lower than the CPLD with more functionality in the eX64. The idle current of the ex64 is less than a milliamp, the current increases incrementally when clocking at 77.76 MHz. The ex64 current draw measurement at 77.76 MHz is ~ 28mA compared to ~ 60mA for the CPLD. When the clock frequency input was increased to 131 MHz for the eX device, the current draw was 91mA with the clock doubler output running at 262 MHz.
2. The register-to-register clock frequency capability of the standard speed grade for the eX device is 160 MHz and the static timing analysis for the competing CPLD is 90 MHz.
3. eX is offered in a higher density for the same package, which enables the engineer to expand the application capabilities without relayout of the system board and migration to a larger package.
4. The ability of the eX I/O ring to drive 2.5V, 3.3V, or 5.0V is a distinct advantage over the competitive device.

"Appendix A" presents additional results and result verification.

Conclusion

The antifuse devices are superior to the competitive CPLD devices in power consumption, frequency performance, and architectural flexibility. As a low jitter generation output device, external buffers are not required which reduces component count, cost, and manufacturing. The fact that HCMOS frequencies of over 100 MHz are required in many communications designs, a device which handles over 200 MHz I/O is important to a designer.

With the capabilities of the internal performance, flexible architecture, simple I/O structure and density to package ratio the eX device can greatly enhance the following aspects of an application:

1. Control Function
2. Accurate Sensing for Alarms
3. Phase Detection and Control
4. Buffering for Multiple Clock Outputs
5. Signal I/Os
6. Accurate Frequency Synthesis

From a business perspective, these enhancements and capabilities provide the designer with a more cost effective and reliable end product with less components and heat dissipation issues.

Appendix A

Figure 7 shows a measurement of the 77.76 MHz VCXO output with the CPLD output un-programmed. The histogram output is fairly symmetric and uniform and the RMS jitter is <12ps.

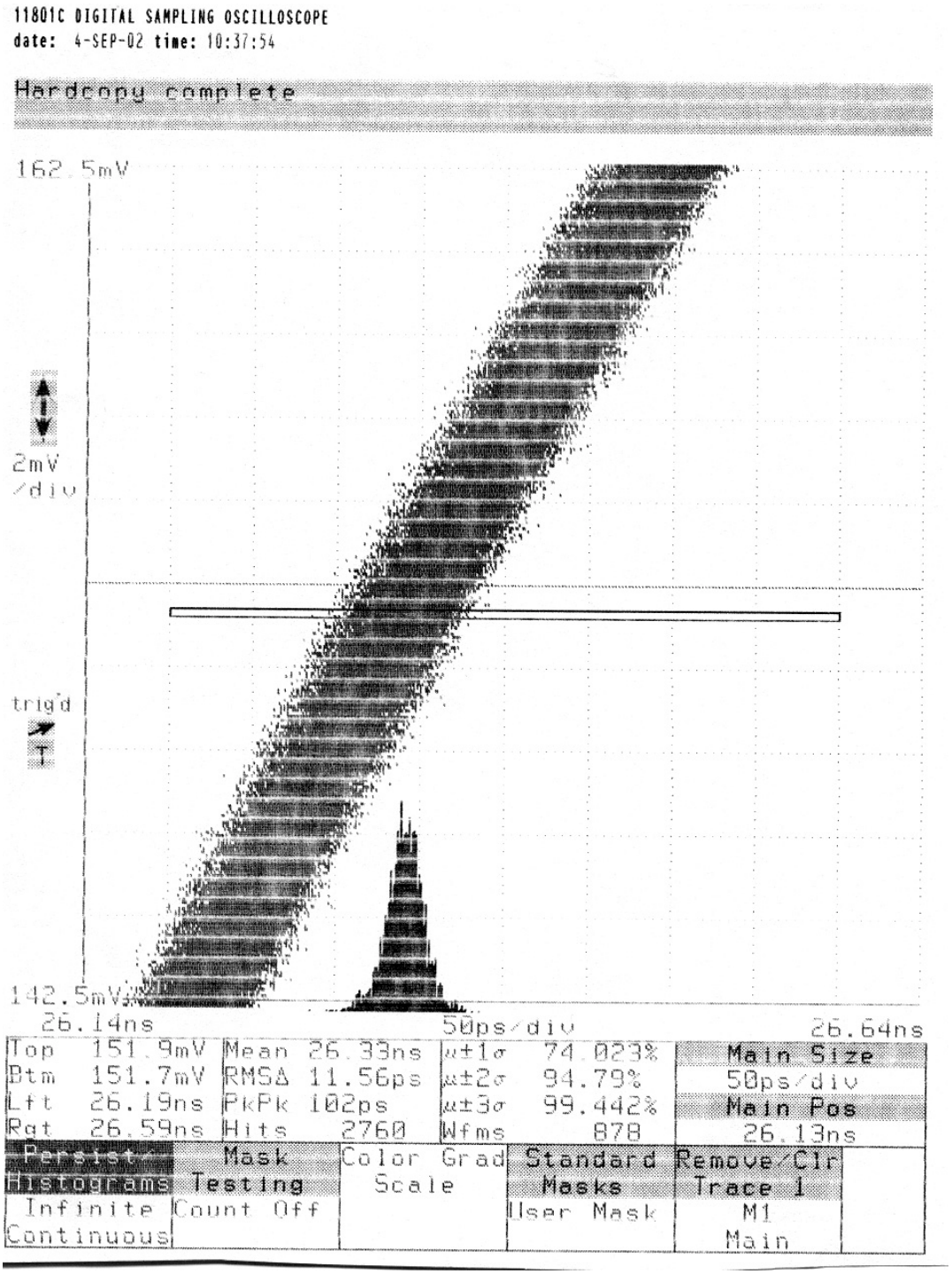

Figure 7: 77.76 MHz VCXO Output with the CPLD Output Unprogrammed

Figure 8 shows a measurement of the 77.76 MHz VCXO output with the CPLD output programmed. The histogram output is extremely noisy and randomly jumping around. The RMS jitter has also increased five times with the CPLD compromising the output of the VCXO with a jitter output of ~63ps.

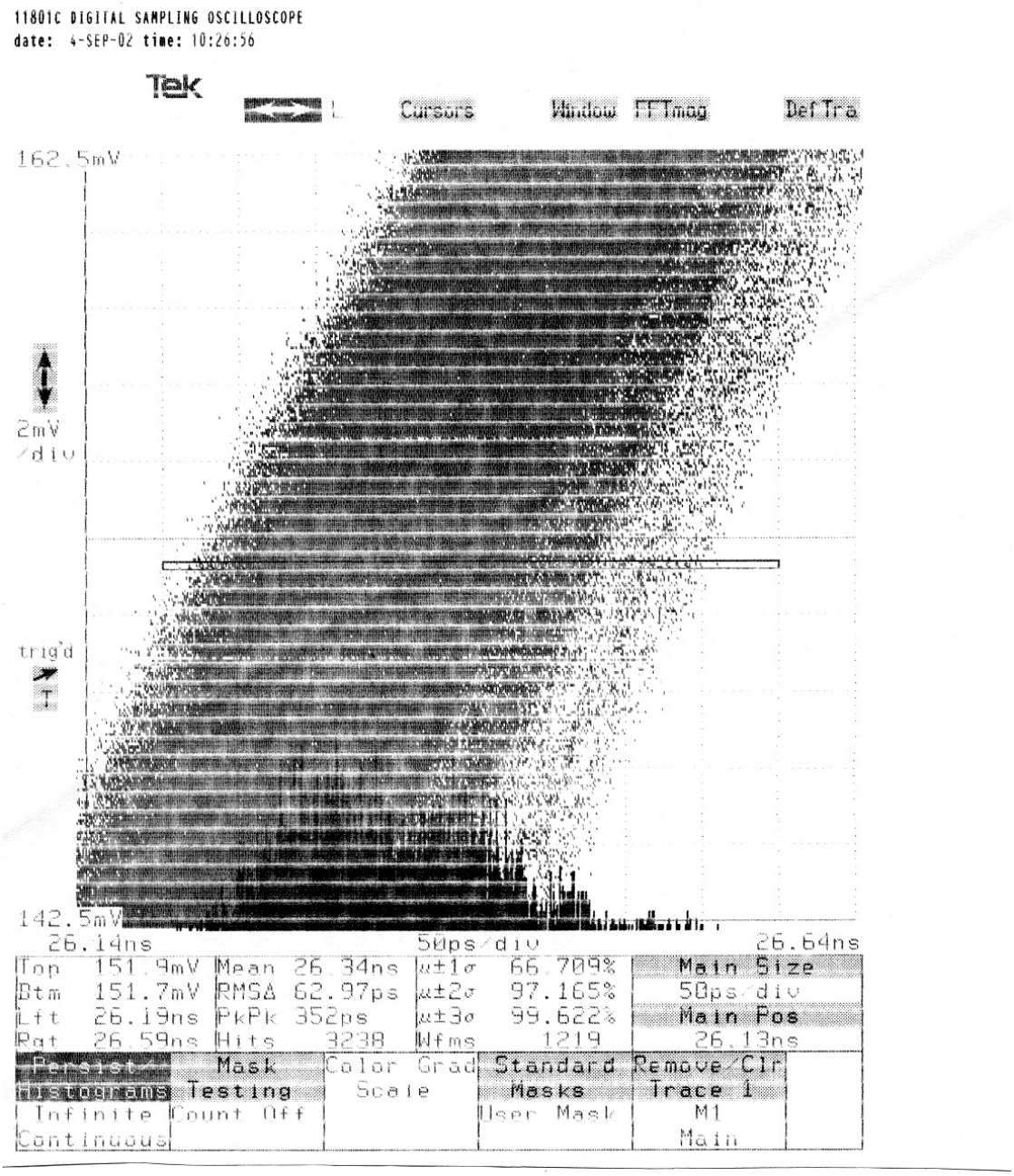

Figure 8: 77.76 MHz VCXO Output with the CPLD Output Programmed.

Figure 9 shows a measurement of the 77.76 MHz VCXO output with the CPLD output programmed. The histogram output is somewhat noisy and randomly jumping around. The RMS jitter has also increased to approximately two times with the CPLD having a jitter output of ~21ps.

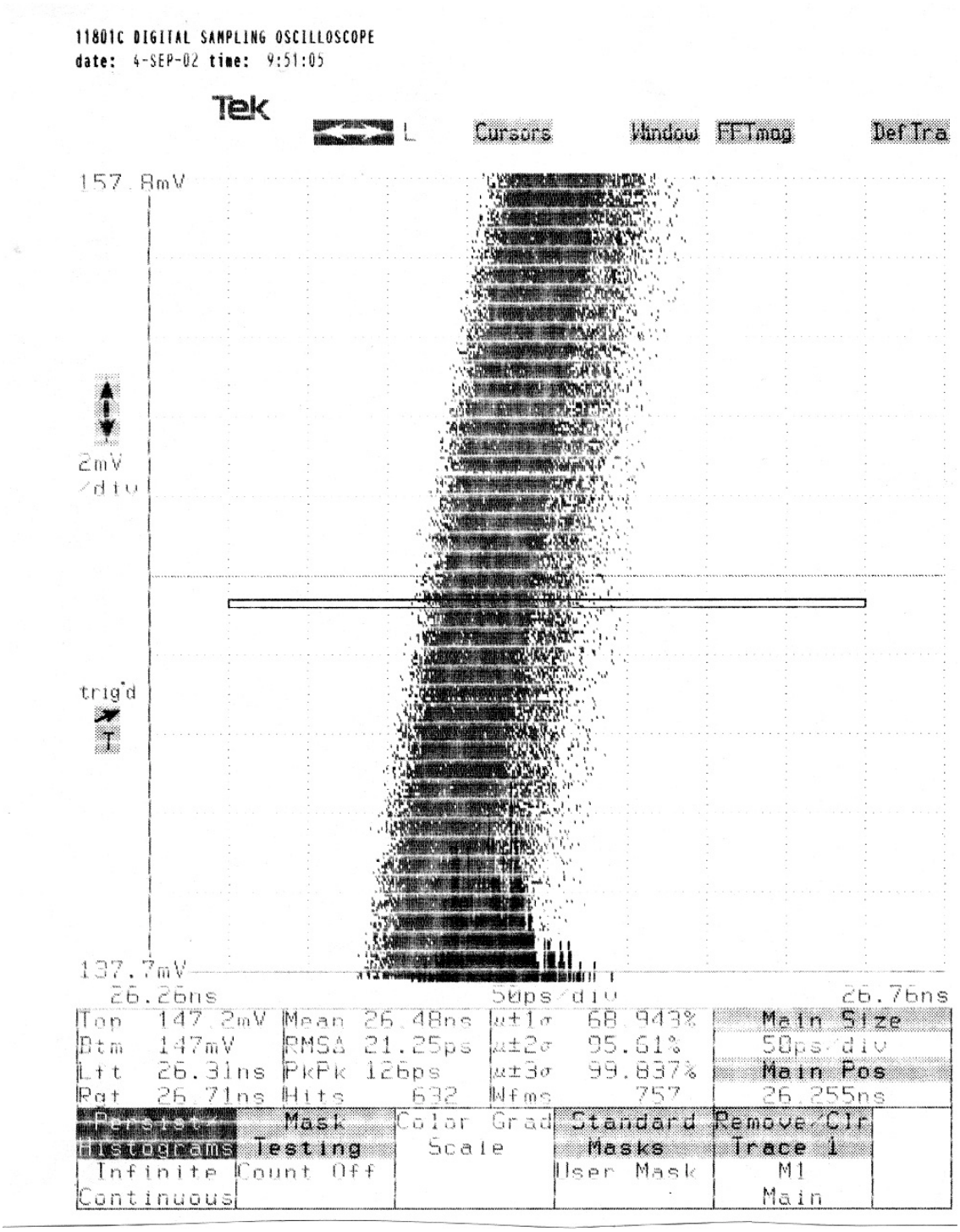

Figure 9: 77.76 MHz VCXO Output with the CPLD Output Programmed

Figure 10 shows a measurement of the 77.76 MHz VCXO output with the CPLD output programmed. The histogram output is noisy and randomly jumping around. The RMS jitter has also increased to approximately two times with the CPLD having a jitter output of ~17ps.

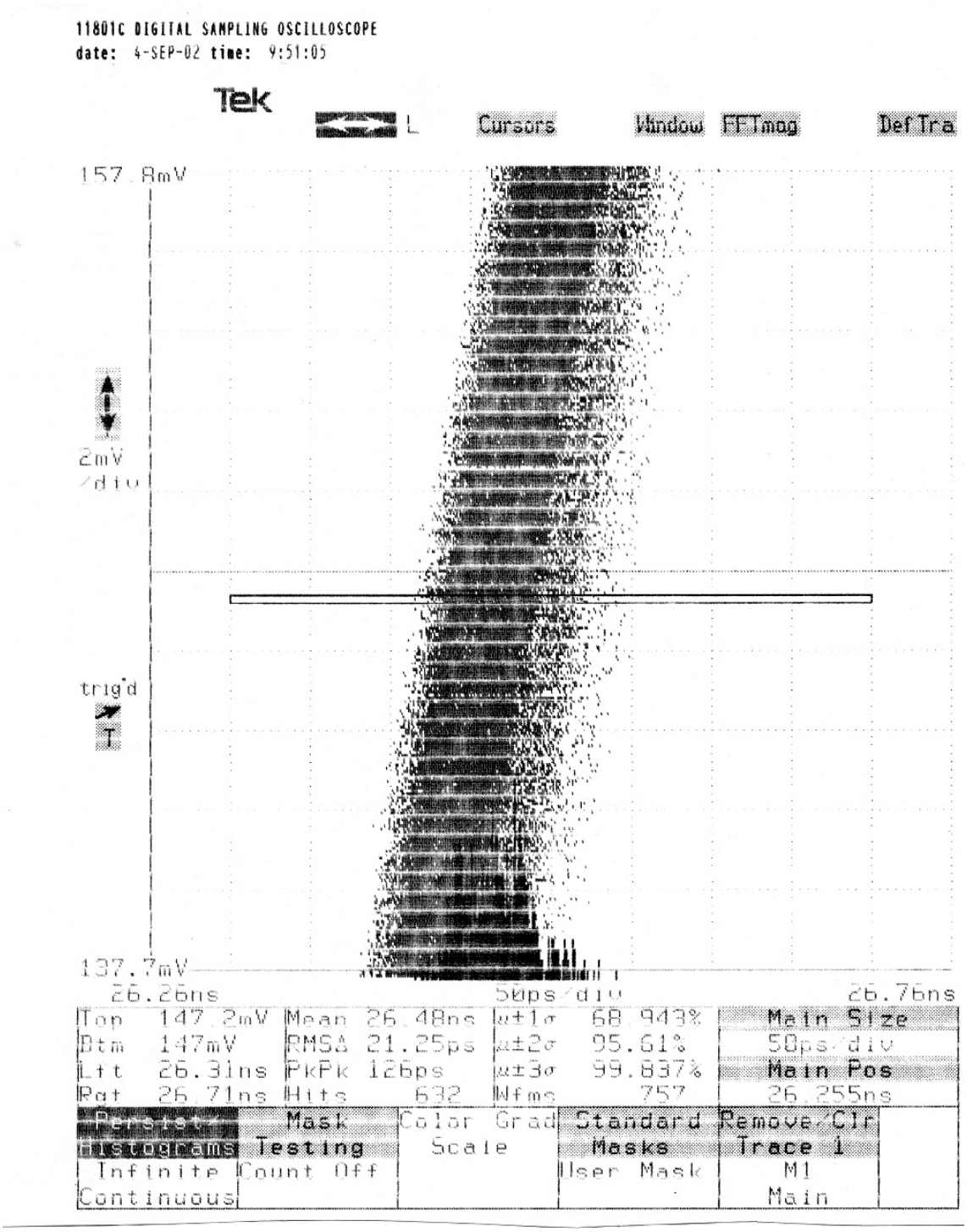

Figure 10: 77.76 MHz VCXO Output with the CPLD Output Programmed

Figure 11 shows a measurement of the 77.76 MHz VCXO output with the CPLD output programmed. The histogram output is somewhat noisy and randomly jumping around. The RMS jitter has also increased to approximately two times with the CPLD having a jitter output of ~21ps.

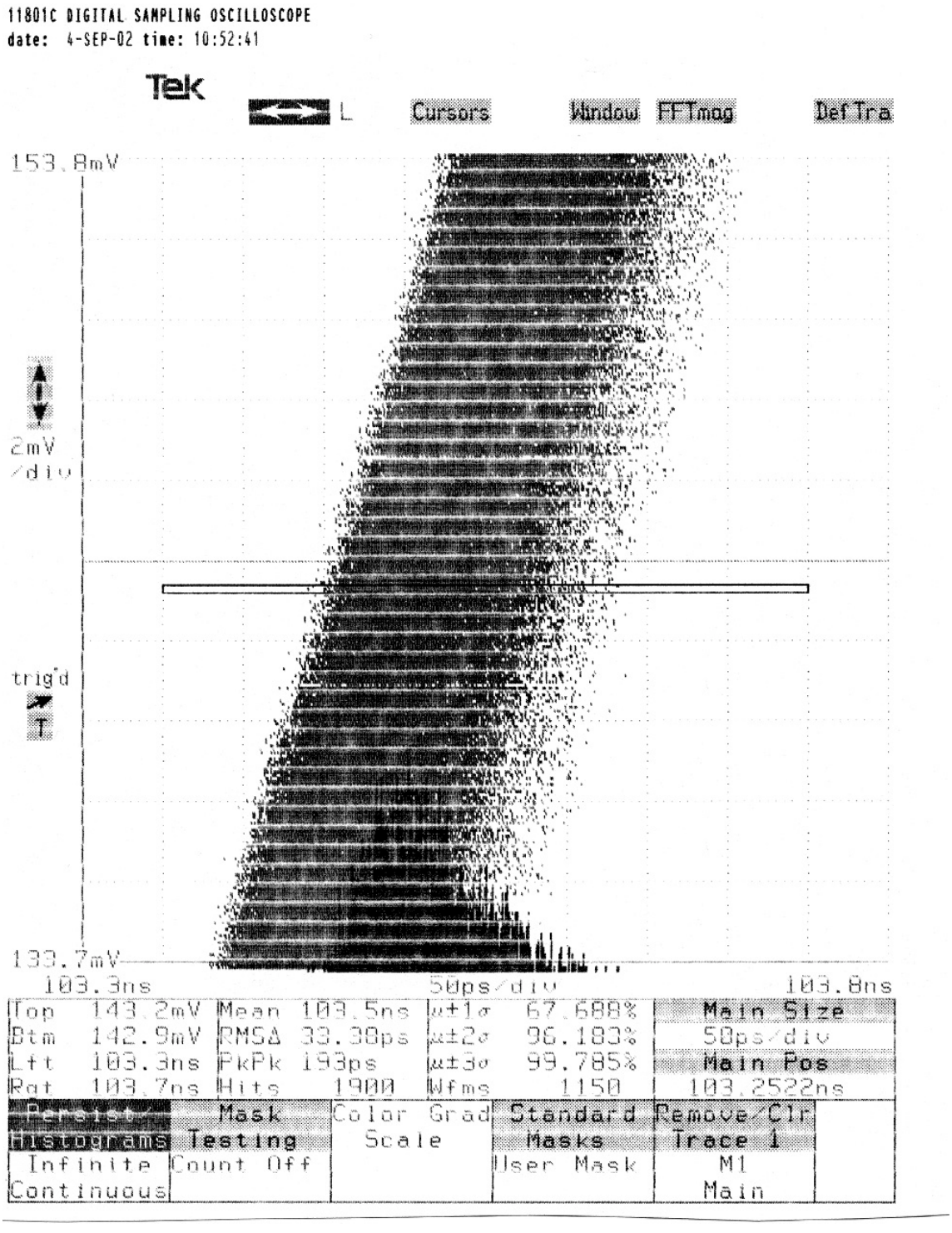

Figure 11: 77.76 MHz VCXO Output with the CPLD Output Programmed

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