Enhanced Qualification and Lot Acceptance Procedures

Introduction

Actel has recently implemented enhanced procedures for the qualification and lot acceptance of radiation-tolerant RTSX-SU and RTAX-S antifuse FPGAs for space-flight applications. This document describes the enhanced procedures and presents results of the additional qualification and lot acceptance tests performed in conformance with the new procedures.

Enhanced Antifuse Qualification (EAQ)

All Actel radiation-tolerant FPGAs are qualified in accordance with the MIL-STD-883 Class B specification prevailing at the time of qualification. The procedures described in this document are in addition to the procedures performed in compliance with MIL-STD-883 Class B.

High Stress Test Designs

The test designs employed for enhanced antifuse qualification are specifically designed to isolate antifuse failure mechanisms. They accomplish this by achieving an extremely high utilization factor for logic modules and by implementing a variety of test structures, which thoroughly exercise all of the various antifuse deployments. The test designs are extremely sensitive to small changes in net propagation delay, which could be caused by a change in the impedance of an antifuse. Such an impedance change could indicate damage in that antifuse. Note that Actel may modify the high stress test designs without notice in order to achieve higher levels of antifuse coverage or better resolution or perception of timing changes.

EAQ Test Method

As a supplement to the MIL-STD-883 Class B qualification procedures for each space-flight FPGA family, a sample of units is programmed with the high stress design, and subjected to a dynamic high temperature operating life (HTOL) test for a minimum of 1,000 hours. The units may be sampled from multiple wafer lots. Additionally, multiple part types within the device family being qualified may be sampled.

The EAQ test is not a pass/fail test. It is used to gather information on the long-term reliability of the antifuses used in Actel's space-flight FPGAs and to perform reliability testing beyond the requirements of MIL-STD-883 Class B. Table 1 and Table 2 on page 2 list the test conditions and results for the EAQ tests performed since inception of the procedure. In some cases, testing was sponsored by independent organizations.

Table 1: **EAQ HTOL Results for RTSX-SU and RTAX-S Space-Flight FPGAs**

Device	Units Started Testing	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTSX32SU	150	1,000	150,000	0	T_J = 153ºC, V_{CCA} = 2.75 V
RTSX32SU	149	250	37,250	0	T_J = 155ºC, V_{CCA} = 3.00 V
RTSX32SU	150	1,000	150,000	0	T_J = 153ºC, V_{CCA} = 2.75 V
RTSX32SU	150	1,000	150,000	0	T_J = 150ºC, V_{CCA} = 2.50 V
RTSX72SU	75	500	37,500	0	T_J = 150ºC, V_{CCA} = 2.50 V
RTAX1000S	291	1,000	291,000	0	T_J = 132ºC, V_{CCA} = 1.60 V

Table 2: **EAQ LTOL Results for RTSX-SU and RTAX-S Space-Flight FPGAs**

Device	Units Started Testing	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTSX32SU	150	250	37,500	1	T_J = –27ºC, V_{CCA}= 2.75 V
RTSX32SU	150	250	37,500	0	T_J = –27ºC, V_{CCA}= 2.75 V
RTSX32SU	150	500	75,000	0	T_J = –29ºC, V_{CCA}= 2.50 V
RTSX72SU	75	1,000	75,000	0	T_J = –29ºC, V_{CCA}= 2.50 V
RTAX1000S	292	250	73,000	0	T_J = –54ºC, V_{CCA}= 1.60 V

One antifuse failure occurred on RTSX32SU during Low Temperature Operating Life (LTOL) testing, manifesting itself as a marginal increase in propagation delay. This failure was due to an S-antifuse on a net with only one antifuse (this is known as a "single S-antifuse net"). An update to the routing software in release 6.2-SP1 was developed to mitigate this failure mechanism by significantly reducing operating current stress in single S-antifuse nets.

Enhanced Lot Acceptance (ELA)

In addition to enhanced qualification procedures, Actel has also implemented supplementary testing performed on a per-wafer-lot basis, in order to ensure that no process-dependent antifuse failure mechanisms are present. The enhanced lot acceptance tests are supplementary, and are performed in addition to the lot acceptance tests and screens that are already in place.

There are two types of enhanced lot acceptance screening:

- Cross-section analysis of samples from each wafer
- High-temperature operating life (HTOL) test of units sampled from each wafer lot

ELA Cross Section Analysis

In order to ensure that there are no construction issues which may lead to reliability problems, two dice are sampled from each wafer of incoming RTSX-SU and RTAX-S FPGAs. The dice are cross sectioned and a sample of electron micrographs are inspected by technology experts in Actel's Technology Development (TD) group. Any construction issues observed by the TD team will result in the wafer in question being quarantined until its reliability can be assured by more detailed testing.

ELA HTOL Test

A high temperature operating life test is performed on a sample from each wafer lot of RTSX-SU and RTAX-S FPGAs.

ELA HTOL Test Design

The design used during ELA testing will, in most cases, be identical to the high stress design used for EAQ. The objective of the design is to exercise as many different antifuses of as many different types as possible and to observe timing changes with resolution as fine as possible. In order to optimize resolution and coverage, Actel may change or update the ELA test design without notice.

ELA HTOL Test Method

The enhanced lot acceptance testing requires that a sample of packaged units be removed from the first assembly lot from each wafer lot of RTSX-SU and RTAX-S space-flight FPGAs. The sample size is determined by the product type. RTSX32SU and RTSX72SU are sampled at a minimum of 100 units per wafer lot. The larger RTAX-S parts are sampled at a lower rate, since there are fewer parts per wafer lot. The sampled units are subjected to HTOL testing for a minimum of 168 hours. RTSX-SU FPGAs are operated at junction temperature of 145ºC, and RTAX-S FPGAs are operated at a junction temperature of 125ºC. After the HTOL, a full electrical test is performed on the sampled units at room temperature. This testing will be performed in parallel with the production screening process for the flight units, and must be completed prior to shipment of flight units from the wafer lot. Any failures detected during the electrical test will be subjected to a full failure analysis. The lot will be put on hold pending resolution of the failure analysis. During this time, no customer shipments will be made from the lot.

ELA HTOL Results

Table 3 presents the results from the enhanced lot acceptance testing performed on the RTSX-SU and RTAX-S product families since inception of the enhanced procedure.

Table 3: **ELA Results for RTSX-SU and RTAX-S Space-Flight FPGAs**

Product	Wafer Lot	Quantity of Units	Failure Quantity	Number of Hours	Unit hours	Type of Test	Wafer Lot Status
RTSX32SU	D19S61	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1AYJ1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1AYJ1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1JW21	100	0	168	16,800	HTOL	PASS
RTSX32SU	D122H1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1N8F1	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1HLH4	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1HLJ1	79	0	1,000	79,000	HTOL	PASS
RTSX72SU	D1HLJ1	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1MM81	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1N8A1	100	0	168	16,800	HTOL	PASS
RTAX2000S	D1GAG1	14	0	168	2,352	HTOL	PASS
RTAX2000S	D1N9H1	14	0	168	2,352	HTOL	PASS

Conclusions

Actel has recently implemented enhanced procedures for the qualification and lot acceptance of radiation-tolerant antifuse FPGAs for space-flight applications. Results obtained from the testing required by these enhanced procedures demonstrates the high reliability of Actel's RTSX-SU and RTAX-S space-flight FPGAs. This report will be updated with the results of tests on additional wafer lots as they become available.

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