



Developing Embedded Applications
with ARM[®] Cortex[™]-M1
Processors in Actel IGLOO and
Fusion FPGAs
White Paper

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Introduction

Until recently, the embedded market has been primarily the domain of 8-bit microcontrollers. While embedded applications existed for 32-bit processors, they were limited to a few high-performance areas. The level of processing required for many embedded applications is increasing dramatically due to the convergence of communication and consumer applications and the delivery of higher levels of content, including video and high-end audio. This is driving the wider usage of 32-bit processors in system-on-chip (SoC) applications. [Figure 1](#) shows the percentage of ASIC designs that have incorporated a processor in recent years.

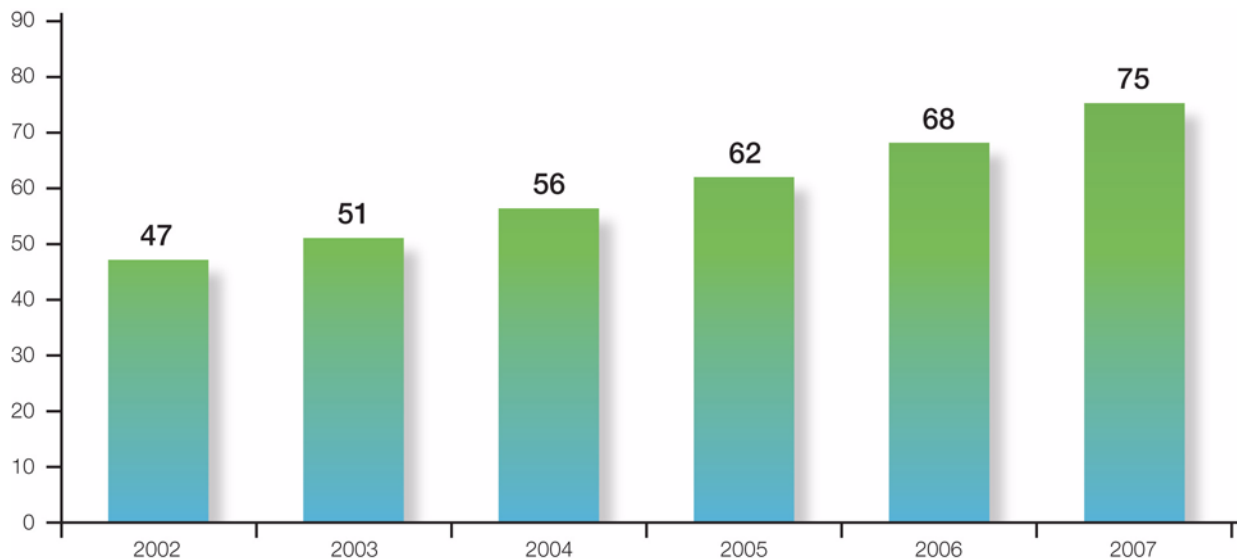


Figure 1: Percentage of ASIC Designs Using Microprocessors

At the same time, a transition is occurring in SoC implementation. Designs in markets from communications to consumer and automotive are moving from ASICs to FPGAs due to increasing mask and silicon costs. As ASIC development costs increase, the break-even volume required to justify the expense is also increasing, pushing a larger number of designs into programmable devices.

The same market and process dynamics that are causing ASIC costs to increase are also reducing the cost per gate of FPGAs. This boosts the level of integration, leading to larger devices that can support complex system-level applications. Just a few years ago, such applications could only be implemented in ASICs. When coupled with the fast time-to-market that FPGAs offer, this implementation shift will continue, presenting programmable logic vendors with a huge market opportunity.

Even with these trends, there has been, until now, a challenge: a majority of portable designers have implemented their devices using a microcontroller in conjunction with a programmable logic device. They have used the microcontroller to implement the necessary processing, and have programmed the FPGA with additional application-specific features and functions not supported by the microcontroller.

That issue is rapidly fading. Smaller cores, better IP and development environments, and the double-time march of technology has created a situation in which processor and controller cores can now be part and parcel of FPGAs. The combination of the ARM Cortex-M1 processor with low-power Actel IGLOO[®] and Fusion[®] mixed-signal FPGAs provides a single-chip solution that reduces cost, power, board space, and design complexity. It also broadens a designer's application reach and time-to-market.

It is commonplace now for FPGA vendors to include processor or MCU cores for their customers, but there are two distinct camps playing this game. In the first camp, the IP provided for the FPGA is proprietary. These cores are tightly controlled, optimized, and vetted by the FPGA vendor. The challenge associated with proprietary architectures is making them efficient in targeted applications and putting tools in place to support them. Experienced engineers know that there is a learning curve when using anything new; it takes time to climb the learning curve and gain the experience to deal with the product's unique characteristics. This is in direct conflict with ever-shortening development schedules, and it increases design risk. For these reasons, designers tend to reuse what they are familiar with. Over time, this causes a few architectures to become widely used industry standards, while most are used only in narrow, vertical niches. Remember that once there were plenty of companies that rolled their own microcontrollers, until open architectures and tools made that financially unfeasible.

Standard Benefits

With processor-enhanced FPGAs, an industry-standard architecture offers significant benefits over a proprietary architecture. Industry-standard processors have the several advantages:

- A broad selection of development tools
- A significant volume of available program code
- A large following of design engineers who have knowledge and experience using them

These benefits enable users to get their designs developed faster and to market sooner while reducing risk, and as a result, offer customers a better solution and increased value.

For Actel, choosing an industry-standard core came down to the best and broadest; the processor with the best legacy in embedded design, broadest application reach, and most established design and support ecosystem: ARM. But a straight port of an existing ARM processor into Actel FPGAs would not serve system designers well; they would see that for what it is: an adornment with little behind it.

Flexible, Extensible, and Free

To address this need, Actel and ARM developed the 32-bit Cortex-M1 processor ([Figure 2 on page 5](#)), the first ARM core designed specifically for FPGA implementation. When combined with Actel nonvolatile M1-enabled IGLOO low-power FPGAs and Fusion mixed-signal FPGAs, the small, fast, and highly configurable ARM Cortex-M1 processor offers a number of benefits.

- The combination of a low-cost FPGA with the Cortex-M1 processor extends the ARM architecture to lower-volume applications.
- It provides a lower-cost entry into SoC design, and shortens time-to-market for ARM users.
- The ARM Cortex-M1 processor enables economical reuse of tools, code, and knowledge, which reduces risk and gets products to market sooner.
- For designs that scale to ultra-high volumes, the ARM Cortex-M1 processor runs the Thumb[®]-2 instruction set and is upward-compatible with the ARM Cortex-M3 processor, providing an easy migration path to ASIC implementation.
- It is free. Removing the license, royalty fees, and contracts typically associated with licensing models for industry-leading processor cores, Actel's delivery of the ARM Cortex-M1 processor gives embedded designers access to programmable flexibility and system-on-chip integration with the ARM architecture, enabling the development of low-cost, high-performance systems.

Features and Functionality

Derived from the ARM 3-stage Cortex-M3 processor pipeline, the highly configurable Cortex-M1 processor balances size and speed for embedded applications. The core in its smallest configuration is 4,435 tiles and fits into a 250,000-gate M1AGL250 device with room left for a selection of peripherals or user logic. It runs at over 62 MHz in Actel M1-enabled IGLOO and Fusion devices.

The ARM Cortex-M1 processor has a separate memory interface from the external Advanced Microcontroller Bus Architecture (AMBA) peripheral bus interface. This is similar to the high-performance ARM9™ architecture but different from that of ARM7™, which has a combined memory and peripheral bus. The separate memory interface on the ARM Cortex-M1 processor is actually implemented as two interfaces, giving separate access to instruction and data tightly coupled memory spaces (ITCM and DTCM). This increases the performance of the processor, because it can fetch an instruction from the ITCM on every clock cycle (right side of Figure 2), and it is never stalled due to data memory accesses, or reads and writes to the peripherals on the AMBA bus.

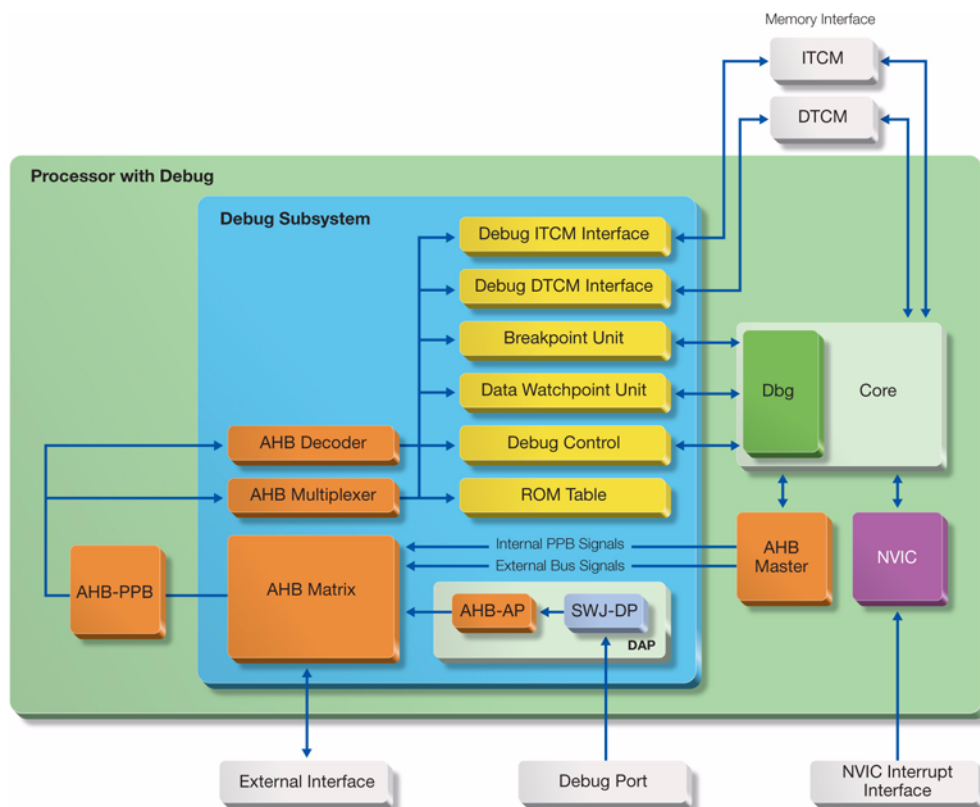


Figure 2: Processor with Debug Block Diagram

The processor runs a subset of the new Thumb-2 instruction set and features support for tightly coupled memory and a sophisticated low latency interrupt controller to improve embedded performance and capabilities.

Thumbs Up

That subset is the ARMv6-M, which is a full subset of the Thumb-2 (ARMv7) instruction set used across the rest of the Cortex family. ARM recognizes the benefit of having a large volume of legacy code available for customers to use, so engineers made the Cortex family upward-compatible with Thumb code written for their legacy cores (ARM7, ARM9, and ARM11™).

Existing Thumb code can be run without change on ARM's Cortex-family processors, including Cortex-M1 devices. This is a big advantage for designers. Most of the important processing on legacy ARM processors was done in subroutines written in Thumb code, so designers can take advantage of their existing code for ARM processors.

For performance-optimized code, Thumb-2 technology uses 31 percent less memory to reduce system cost, while providing up to 38 percent higher performance than existing high-density code, which can be used to prolong battery life or to enrich the product feature set.

One of the other benefits of Thumb-2 over previous ARM instruction set architectures is that 16- and 32-bit instructions are executed in the same mode. In older ARM architectures, Thumb instructions were primarily used in subroutines with the 32-bit ARM instructions used to service interrupts. This often resulted in long latency between the time an interrupt was received and the time it was serviced. In Thumb-2, ARM merged the 16- and 32-bit operating modes so that interrupts could be serviced without the need to switch from 16-bit mode. It is a big advantage to be able to freely mix 16- and 32-bit instructions. This greatly simplifies the programming task and eliminates the need to profile the code to minimize code size and maximize throughput. It also results in increased performance, because the instructions can be optimally mixed without having to cluster them in 16- and 32-bit groupings.

Implementation in Actel M1-Enabled FPGAs

FPGA usage is growing in part because of the flexibility that these devices offer. Engineers can tailor the function of a device exactly to their application by adding or removing soft IP. This is similar to what can be done with an ASIC. With FPGAs, however, a design can be developed and running in the application within a few hours, whereas ASICs require many months and large up-front, non-recurring engineering (NRE) charges.

When developing Cortex-M1, ARM and Actel made the processor highly configurable. The tightly coupled memory size, the size and speed of the multiplier, the number of external interrupts, the endianness, and whether the debug circuitry and OS extensions are included are all selectable by the user. This gives designers the control to select the minimum processor configuration that best meets their application requirements.

Because ARM Cortex-M1 is being implemented in an FPGA, designers can quickly configure the core and program it into an M1-enabled, flash-based device and test it in their application. If a change is required, it can be modified and reprogrammed into the device within minutes. In this way, engineers can modify and test their design many times within a few hours to find the optimal implementation for their product.

Using ARM's Cortex-M1 Processor in IGLOO FPGAs

The biggest growth segment of electronics design today is low power, but until recently, low power came at a price, which often included designing out performance or functionality. The Actel IGLOO family brings the low-power benefits of flash-based FPGAs to bear in applications previously reserved just for ASICs.

Attractive for portable applications with as low as 2 μ W static power, IGLOO FPGAs consume more than 200 times less static power than competitive FPGA offerings and deliver more than 10 times the battery life of the leading programmable logic devices in portable applications. In an IGLOO FPGA, the ARM Cortex-

M1 core features very low operating current and static power, consuming only 24 μA in static mode and 3 μA in sleep mode. The innovative IGLOO Flash*Freeze mode, which enables easy entry and exit from ultra-low power modes while retaining SRAM and register data, reduces quiescent current to 20 μA . The Flash*Freeze feature also allows instant on/off cycling of the ARM Cortex-M1 core for maximum performance and minimum power consumption.

Using ARM’s Cortex-M1 Processor in Fusion FPGAs

Fusion mixed-signal FPGAs provide a unique solution, combining programmable logic, RAM, flash, and analog in a single chip. They range in density from 90,000 to 1,500,000 system gates and are popular in applications such as TCA system management. M1-enabled Fusion devices offer all the benefits of Actel nonvolatile, flash-based families: single chip, reprogrammable, live at power-up, secure, firm-error immune, and low power. The first M1-enabled device offered by Actel was the M1AFS600, a member of the world's first mixed-signal Fusion FPGA family.

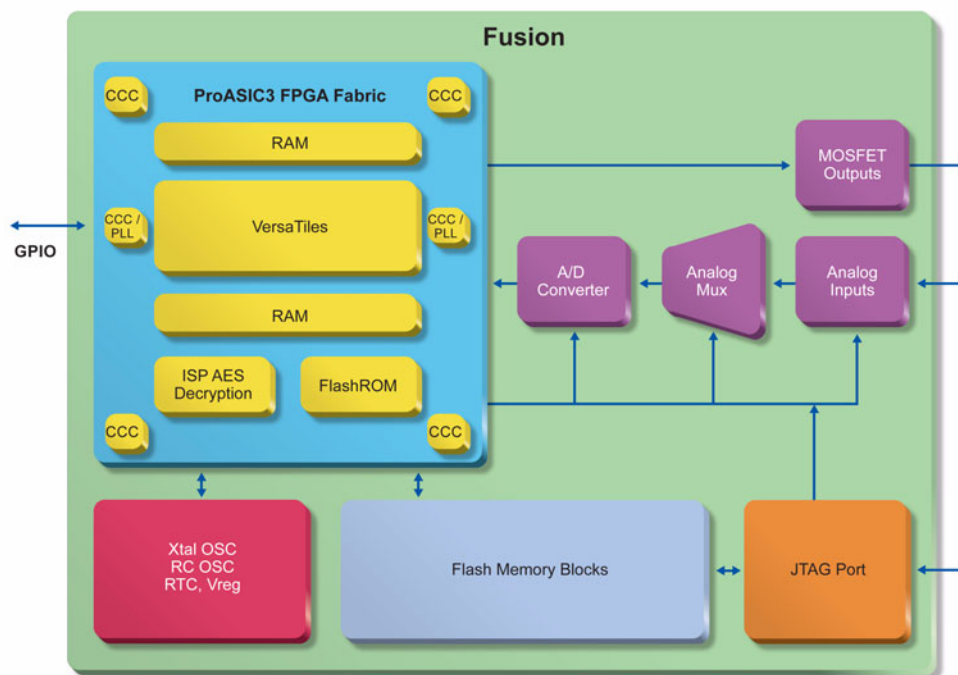


Figure 3: Fusion Mixed-Signal FPGA Architecture

The 600,000-system-gate M1AFS600 integrates a 12-bit analog-to-digital converter (ADC), as many as 40 analog I/Os, up to 8 Mbits of flash memory, and FPGA fabric—all in a single device. The ARM Cortex-M1 processor can be implemented in as few as 4,435 VersaTiles, less than 30 percent of the FPGA logic in an M1AFS600 device.

Since that introduction, the M1AFS250 (250,000 system gates) and the M1AFS1500 (1,500,000 system gates) have come to market, each with Cortex-M1-enabled device options.

Conclusion

The movement from ASICs to FPGAs is driving the usage of 32-bit processors in FPGAs as embedded applications transition to programmable logic. Working together, Actel and ARM have developed an efficient FPGA-optimized 32-bit industry-standard processor, giving designers a powerful new solution for their embedded applications. The features of the ARM Cortex-M1 processor—balanced three-stage pipeline, sophisticated interrupt controller, and tightly coupled memories—are targeted to give users maximum embedded performance while minimizing size and cost. Because it is based on an industry-standard architecture, users can exploit the huge volume of existing code, extensive industry knowledge and support, and a vast ecosystem of tools. The free delivery of the ARM Cortex-M1 processor for use in Actel flash-based, low-power IGLOO and mixed-signal Fusion FPGAs provides all designers with a flexible and cost-effective platform for the development of low-cost, high-performance embedded applications.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com.



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