Actel
POWER MATTERS

Using DirectCore in Libero® IDE

v8.4

July 2008

Table of Contents

Actel produces Intellectual Property (IP) functional cores, called DirectCores, which are designed and optimized for use with Actel devices. The Actel Libero IDE tool offers simple implementation of these DirectCores into a design. The goal of this document is to explain how to generate DirectCores in Libero IDE v8.4, and instantiate them into a design. The terms "DirectCore" and "Cores" are used interchangeably in this document.

DirectCore License Types

DirectCores are licensed in three ways: Evaluation, Obfuscated, or RTL. The license type for each core is specified in your license.dat file. The license settings control the flow and functionality for the DirectCore.

Evaluation

Precompiled simulation libraries are provided, enabling the core to be instantiated and simulated within the Actel Libero Integrated Design Environment (IDE). Using the Evaluation version of the core it is possible to create and simulate the complete design in which the core is being included. The design is not synthesizable (RTL code is not provided). No license feature in the license.dat file is needed to run the DirectCore in evaluation mode.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with Libero IDE. Simulation, Synthesis, and place-and-route can be performed with the Actel Libero IDE. The RTL code for the core is obfuscated. Some of the testbench source files are not provided; they are pre-compiled into the compiled simulation library instead. A license feature in the license.dat file may be needed to use obfuscated DirectCores.

RTL

Complete RTL source code and testbenches are available for the DirectCores. A full RTL license is needed to run DirectCores in RTL mode.

The Catalog in the Project Manager displays the DirectCores available for your product family. DirectCores have an icon next to their name to indicate the license type available for your design.

- Green key indicates RTL or Obfuscated license types.
- Yellow key indicates limited evaluation license only.
- Yellow key with red slash indicates license is protected and not available for use.

Please note that Libero IDE Platinum users have Obfuscated IP licenses for most DirectCores. However, some DirectCores require separate obfuscated license that must be purchased separately. Also, most RTL licenses require separate purchase. Please see http://www.actel.com/products/software/coreconsole/IPcores.aspx for details.

Generating DirectCores Using the Libero IDE

To generate a DirectCore:

- Open the core from the Project Manager Catalog OR
- Drag-and-drop the DirectCore from the Catalog onto the SmartDesign Canvas

You must know which interface the core uses in order to generate and configure it. Different interfaces are responsible for handling communications with the processor, AMBA interface (APB, AHB or both), SFR

(Special Function Register) interface, or other special interfaces (local bus interface in CoreSDR and CoreDDR).

You can generate DirectCores with non-AMBA interfaces using the Project Manager Catalog. You can also use SmartDesign to configure and generate as few as one DirectCore.

DirectCores with AMBA interfaces can also be generated from the Catalog, but peripheral DirectCores using the AMBA bus interface are normally required to connect to the AMBA bus along with the various processor cores (such as Cortex-M1, CoreMP7, and Core8051s). These connections can be done easily using the SmartDesign Canvas in the Project Manager.

Open the Core from the Project Manager Catalog

The Libero Project Manager Catalog lists DirectCores available for easy implementation into your HDL design. To generate the DirectCore using the Catalog:

1. Go to the Catalog window in the Project Manager. Select a category (such as Peripherals), expand it, and select the desired DirectCore IP. Please note that the list is filtered based on your project family settings. DirectCores have a key icon next to their name to represent the license type.
2. Double-click the core name and the new file dialog box appears.
3. Enter a component name and click OK. The Configuring window appears.
4. Modify the core configuration as needed. Please refer to the DirectCore's respective handbooks for details on core configuration.
5. Check the license settings. You may have multiple options if you have both obfuscated and RTL license.
6. Click OK to generate the HDL for the DirectCore.

The Project Manager imports all the required files from the DirectCore package to the project directory and creates a top level wrapper using your settings.

Drag-and-drop the DirectCore from the Catalog onto the SmartDesign Canvas

The SmartDesign tool inside the Libero IDE Project Manager enables you to configure the DirectCore IPs and modify I/O ports as needed before you generate the core. To generate a DirectCore using SmartDesign:

In Libero IDE Project Manager, click the SmartDesign button and enter a design name to open a new SmartDesign. SmartDesign opens and displays the Canvas.

1. Drag and drop a DirectCore from the Catalog onto canvas. The Configuration window appears.
2. Modify the core configuration as needed. Please refer to the DirectCore's respective handbooks for details on core configuration.
3. Check the license settings. You may have multiple options if you have both obfuscated and RTL license.

4. Click OK to instantiate the DirectCore IP on the Canvas. Instantiated IP is indicated by the IP icon under your SmartDesign in the Project Manager Design Explorer. It indicates that the IP was instantiated in your design but the HDL files have not been generated (see Figure 1).

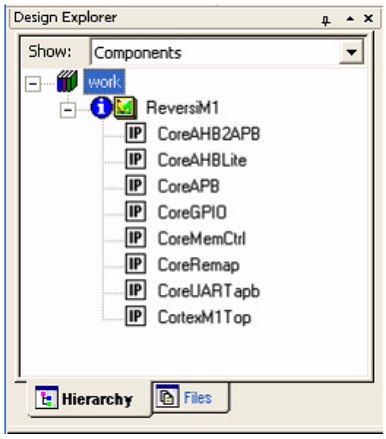

Figure 1: **Instantiated IP in a SmartDesign Before Generating HDL**

5. Select the I/Os required for your design, right click the pin(s), and choose Promote to Top Level or use the Canvas to connect pins to other blocks on the Canvas.
6. From the File menu, choose Save <filename> to save the design on your Canvas.
7. From the SmartDesign menu, choose Generate Design.

During HDL generation, the Project Manager imports all the required files from the DirectCore package to the project directory and creates a top level wrapper using customer settings. For example, if you are configuring CoreUART using a component name "my_uart", then the top level wrapper is called "my_uart" and it instantiates CoreUART inside the top level wrapper HDL file.

Note that either method above generates the same RTL files. The difference between the two methods is that opening the DirectCore from the Catalog creates a wrapper with all the I/Os (required and optional) promoted to top level. If you do not want to use some of the optional I/Os, you must manually modify the top-level wrapper to remove them.

Dragging-and-dropping the DirectCore onto your Canvas enables you to choose which I/Os you want to promote to top level before you generate. Please note that the required I/Os must be promoted to top level. In addition, dragging the core onto your Canvas enables you to connect the interface signal to other blocks or macros before you generate.

Accessing the Handbook and Release Notes

You can open the DirectCore handbook and release notes from the Catalog in the Project Manager. To do so:

1. Select the DirectCore in the Catalog.
2. Right-click the core and choose Open documentation.

3. Select the handbook (*_HB.pdf) or release notes (*_RN.pdf).

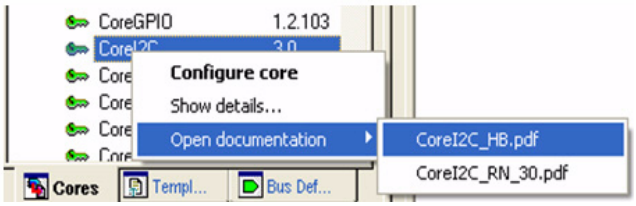

Figure 2: **Accessing DirectCore Documentation from the Catalog**

Installing New Versions of DirectCores

The Libero IDE Project Manager checks for availability of new or updated DirectCores that can be added to your Vault. When the cores are available for download, the Project Manager explains how to update the Vault.

1. There may be some special cases where you need to manually update the Vault with a *.ccz file. To do so:
2. In the Project Manager Catalog click Add Core > From File. The Import Files dialog box opens.
3. Browse to the file and click Import to add it. The Project Manager adds the new file and updates the Vault.

Updating an Existing Design with a New Version of a DirectCore

You may need to update a DirectCore in a design when a new version becomes available. Updating the version of the DirectCore for an existing design depends on which method you used to generate the IP.

If you opened the core from the Project Manager Catalog: Generate the new source files for the core using a separate Libero IDE project and then manually update the files in the existing project.

If you drag-and-dropped the DirectCore from the Catalog onto the SmartDesign Canvas:

1. Open the SmartDesign that includes the DirectCore.
2. Right-click the DirectCore IP and choose Replace components for this instance.
3. Select the new version from Replace Instance version dialog box and click OK.
4. Check the core configuration and the I/O connections to make sure it has been updated and regenerate the SmartDesign component.

Simulating DirectCores

Most of the DirectCores support two types of testbench: full verification environment and simple user testbench. Make sure to select the required testbench during the configuration, before you generate the core. Libero IDE installs appropriate testbench files when you generate,.

To run the testbenches, set the design root to the CoreName instantiation in the Project Manager File Manager. Figure 1 on page 7 shows an example where the core is generated directly from the Catalog. You must change the Design Explorer view from Components to Modules to see the core instantiation and then select DirectCore instantiation.

EQ 2 on page 7 shows the core generated by dragging the DirectCore onto a SmartDesign Canvas. Select the instantiated core and click the Simulation icon in the Project Manager. This invokes ModelSim® and automatically runs the simulation.

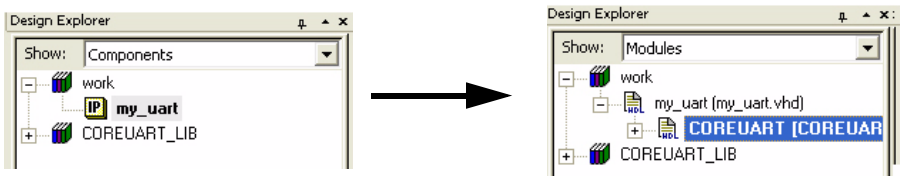

Figure 1: **Set Core as Root in Design Explorer - Core Opened Directly from Catalog**

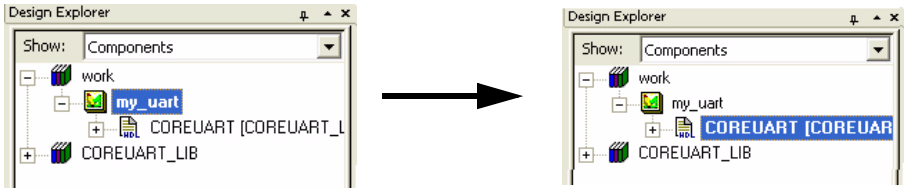

Figure 2: **Set Core as Root in Design Explorer - Core Added in SmartDesign**

Synthesizing DirectCores

To run Synthesis on a core with user parameters, set the design root to the top of the project (For example: my_uart in Figure 1 on page 7 and Figure 2 on page 7). This is a wrapper around the core that sets all the generics correctly. Make sure the required timing constraints files are associated with the synthesis tool. Click the Synthesis icon in the Project Manager. The synthesis window appears and displays Synplicity® project. To run Synthesis, click the Run icon.

Place-and-Route DirectCores

After you set the design route and run Synthesis, click the Place&Route icon in the Project Manager to invoke Designer. Make sure the required timing constraints and physical design constraints are applied during Layout.

For more information, visit our website at **www.actel.com**

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655
USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwatery
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
http://jp.actel.com

Actel Hong Kong
Room 2107, China Resources Building
26 Harbour Road
Wanchai, Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

55900085-0/07.08