

TOTAL IONIZING DOSE TEST REPORT

No. 06T-RTSX32SU-D1P8W1

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 60 krad (Si) per 25-mA spec for 10-year extrapolation. Post 100 krad (Si) and after 15 days room temperature annealing: average $I_{CCA} = 96.7$ mA, and average $I_{CCI} = 49$ mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in <http://www.klabs.org/> and <http://www.actel.com>) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. In this test, the threshold of most of the available inputs is measured.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 86598 and 86618 are irradiated to 60 krad; DUT 86482, 86520 and 86537 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μ m CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D1P8W1
Quantity Tested	8
Serial Number	60 krad: 86598, 86618 100 krad: 86482, 86520, 86537, 1848, 1899, 2105
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	3 krad (Si)/min ($\pm 5\%$)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

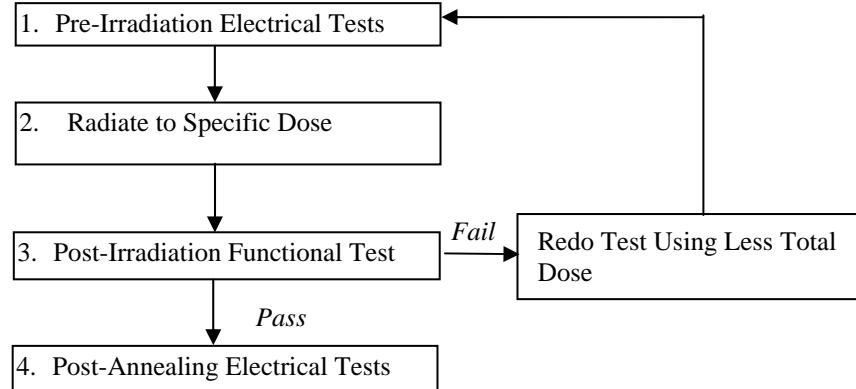


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs in both the 60-krad group and 100-krad group are bias-annealed for 15 days after the irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TH}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCCTR/Y00, ENCCTRH/Y00H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC} -plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is probably due to the state changes during irradiation. However, this transition does not affect the functionality since each DUT passed the gross functionality test right after the irradiation.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
86482	100 krad	310	96	220	52
86520	100 krad	287	82	191	37
86537	100 krad	391	112	264	58
86598	60 krad	45	18	19	15
86618	60 krad	46	20	20	16

The 60 krad group pass the 25 mA spec if annealing is extrapolated for 10-year typical mission time.

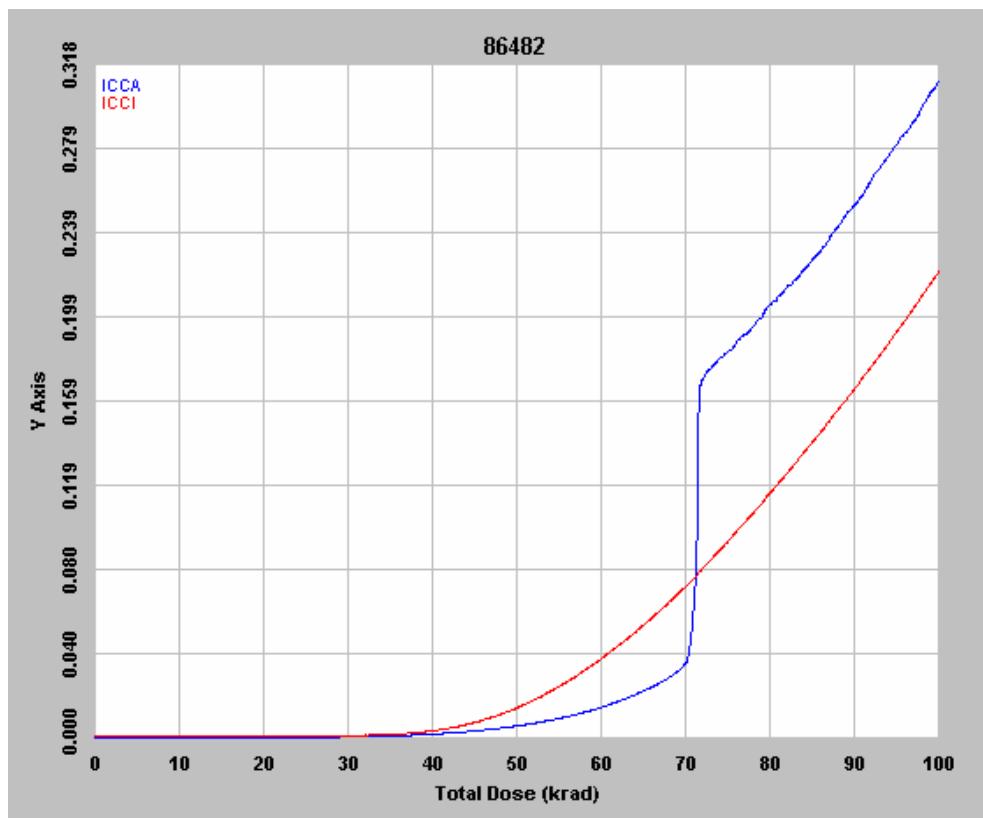


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 86482, 100 krad total dose

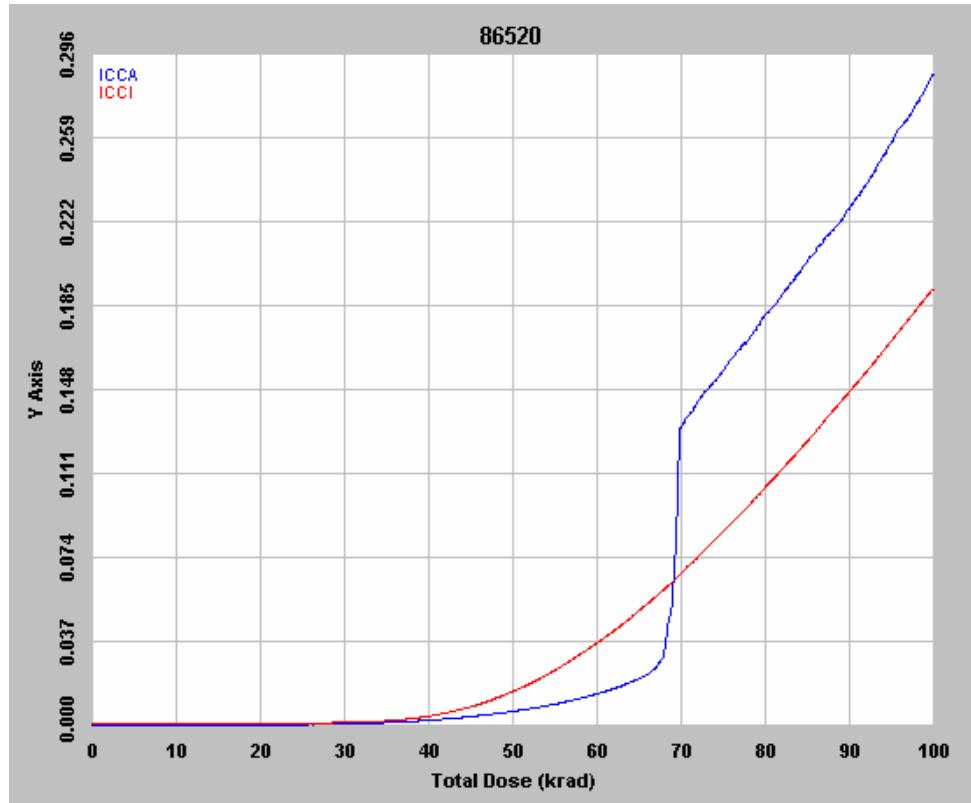


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 86520, 100 krad total dose

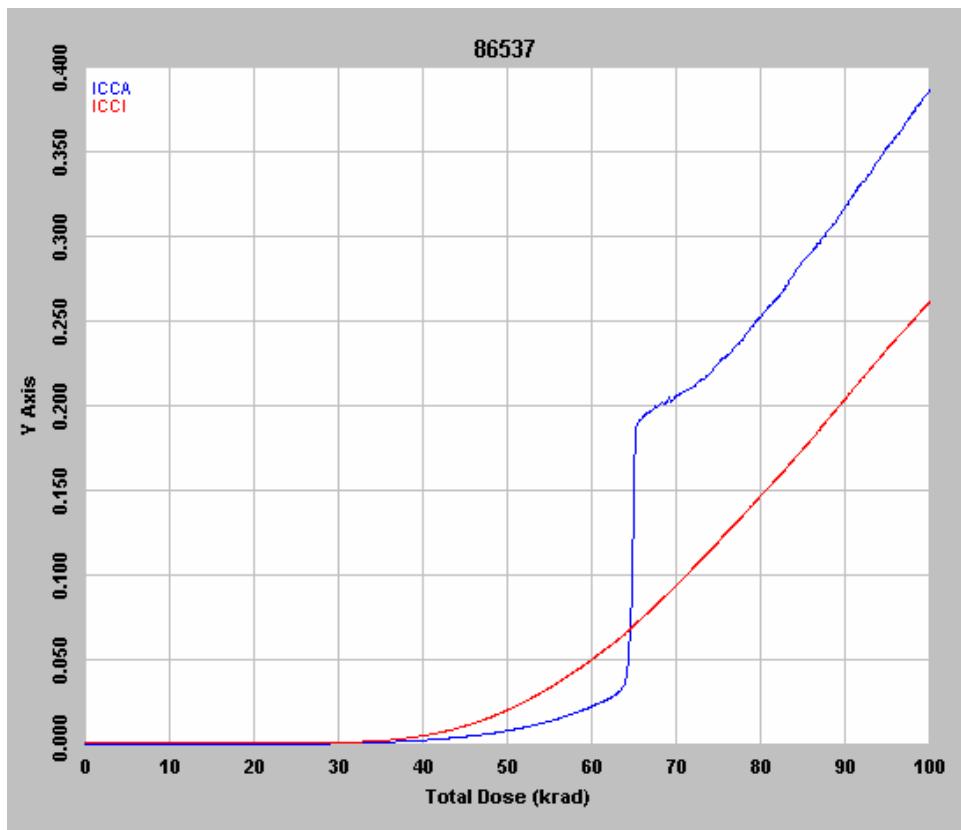


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 86537, 100 krad total dose

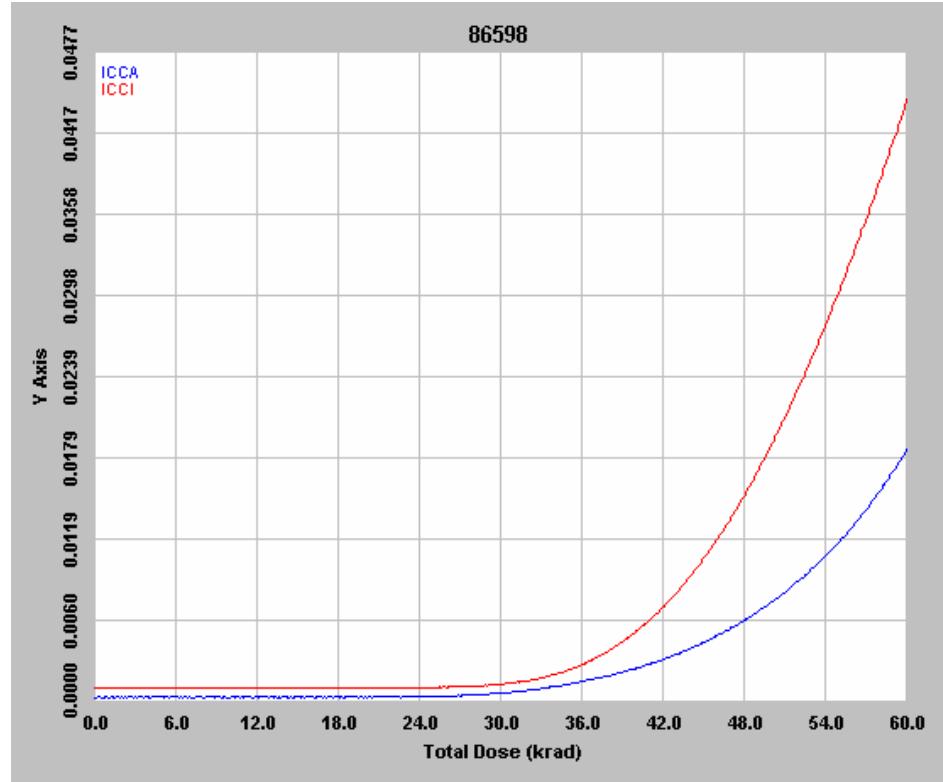


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 86598, 60 krad total dose

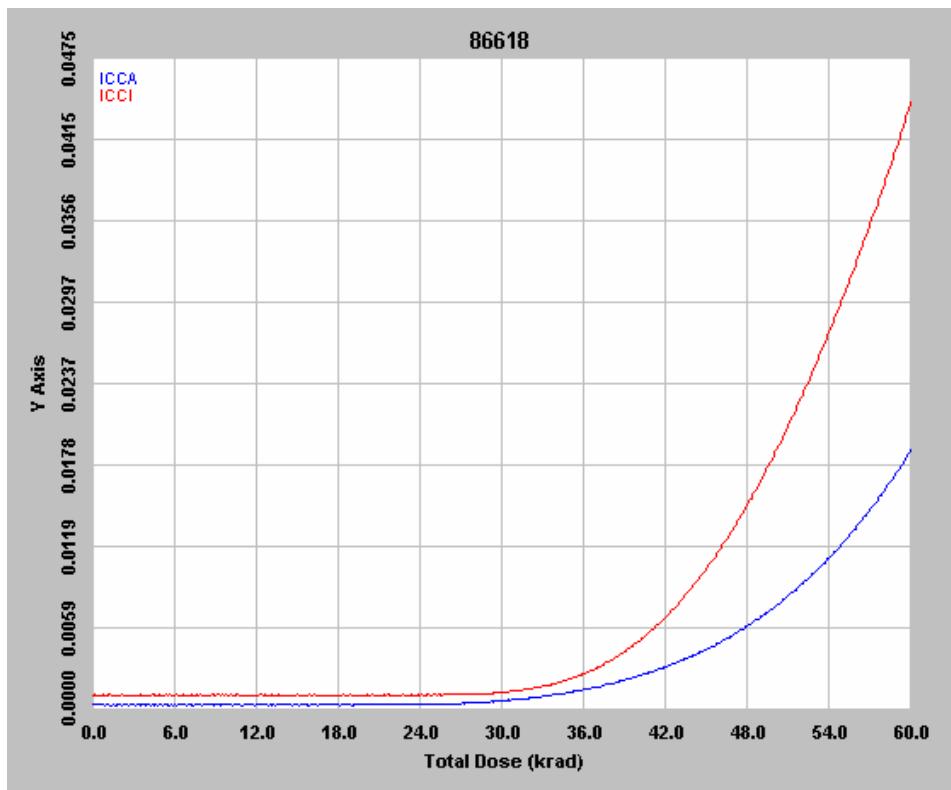


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 86618, 60 krad total dose

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input threshold. The radiation effects are insignificant.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA / QA0				DAH / QA0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)						
86482	100 krad	1.02	1.35	1.57	1.27	1.35	1.27	1.42	1.33
86520	100 krad	1.03	1.36	1.58	1.49	1.35	1.25	1.43	1.33
86537	100 krad	1.02	0.95	1.56	1.43	1.34	1.24	1.41	1.30
86598	60 krad	1.02	1.38	1.57	1.31	1.35	1.29	1.42	1.36
86618	60 krad	1.01	1.38	1.56	1.31	1.35	1.28	1.42	1.34

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR / YO0				ENCNTRH / YO0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
86482	100 krad	0.76	0.81	1.98	1.92	1.23	1.19	1.58	1.54
86520	100 krad	0.75	0.81	1.98	1.92	1.22	1.20	1.60	1.56
86537	100 krad	0.74	0.93	1.94	1.89	1.14	1.22	1.57	1.53
86598	60 krad	0.75	0.80	1.96	1.91	1.21	1.14	1.58	1.56
86618	60 krad	0.76	0.81	1.96	1.94	1.31	1.21	1.59	1.56

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0 / IDIO0				IDII1 / IDIO1			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
86482	100 krad	1.40	1.43	1.42	1.40	1.42	1.42	1.41	1.39
86520	100 krad	1.40	1.41	1.39	1.38	1.41	1.41	1.39	1.41
86537	100 krad	1.40	1.42	1.41	1.40	1.35	1.41	1.38	1.41
86598	60 krad	1.40	1.42	1.42	1.40	1.35	1.41	1.39	1.43
86618	60 krad	1.43	1.43	1.42	1.41	1.41	1.40	1.39	1.40

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2 / IDIO2				IDII3 / IDIO3			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
86482	100 krad	1.39	1.38	1.43	1.42	1.26	1.26	1.48	1.48
86520	100 krad	1.40	1.39	1.43	1.42	1.28	1.28	1.48	1.49
86537	100 krad	1.38	1.39	1.41	1.40	1.26	1.20	1.47	1.50
86598	60 krad	1.39	1.39	1.42	1.42	1.26	1.24	1.47	1.47
86618	60 krad	1.38	1.38	1.42	1.40	1.26	1.24	1.47	1.48

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4 / IDIO4				IDII5 / IDIOS			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V _{IL} (V)	V _{IH} (V)						
86482	100 krad	1.42	1.42	1.40	1.40	1.45	1.45	1.39	1.39
86520	100 krad	1.43	1.42	1.40	1.40	1.45	1.43	1.39	1.39
86537	100 krad	1.38	1.41	1.39	1.37	1.43	1.42	1.39	1.38
86598	60 krad	1.39	1.40	1.39	1.39	1.43	1.43	1.39	1.39
86618	60 krad	1.42	1.41	1.39	1.39	1.44	1.43	1.39	1.39

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6 / IDIO6				IDII7 / IDIO7			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V _{IL} (V)	V _{IH} (V)						
86482	100 krad	1.42	1.20	1.43	1.39	1.45	1.36	1.39	1.40
86520	100 krad	1.31	1.20	1.42	1.40	1.45	1.45	1.40	1.40
86537	100 krad	1.32	1.19	1.39	1.40	1.44	1.41	1.39	1.40
86598	60 krad	1.29	1.33	1.41	1.40	1.46	1.41	1.40	1.40
86618	60 krad	1.31	1.20	1.38	1.48	1.44	1.35	1.39	1.40

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an								
86482	100 krad	0.146	0.146	0.225	0.224	0.283	0.283	0.505	0.504	0.964	0.961
86520	100 krad	0.145	0.145	0.224	0.223	0.282	0.281	0.503	0.502	0.960	0.956
86537	100 krad	0.147	0.146	0.226	0.226	0.285	0.284	0.508	0.507	0.971	0.969
86598	60 krad	0.146	0.145	0.225	0.225	0.283	0.282	0.506	0.504	0.967	0.962
86618	60 krad	0.146	0.145	0.226	0.225	0.284	0.283	0.508	0.505	0.970	0.963

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an								
86482	100 krad	4.82	4.81	4.74	4.73	4.59	4.58	4.04	4.02	2.74	2.67
86520	100 krad	4.82	4.82	4.74	4.74	4.59	4.58	4.04	4.02	2.74	2.67
86537	100 krad	4.82	4.81	4.74	4.73	4.59	4.58	4.03	4.01	2.71	2.63
86598	60 krad	4.82	4.82	4.74	4.74	4.59	4.59	4.03	4.02	2.72	2.68
86618	60 krad	4.82	4.82	4.74	4.73	4.59	4.59	4.03	4.02	2.72	2.69

E. Propagation Delay

Due handling error, the propagation delay had to be retested. Table 7 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage for three extra DUT. In every case the DUT passes the 10% degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (ns)	Post-Annealing (ns)	Degradation
1848	100 krad	569.115	600.030	5.43%
1899	100 krad	583.895	611.950	4.80%
2105	100 krad	582.550	611.810	5.02%

F. Transition Time

The transition characteristics also needed to be measured on those three extra DUT. Figures 7 to 12 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

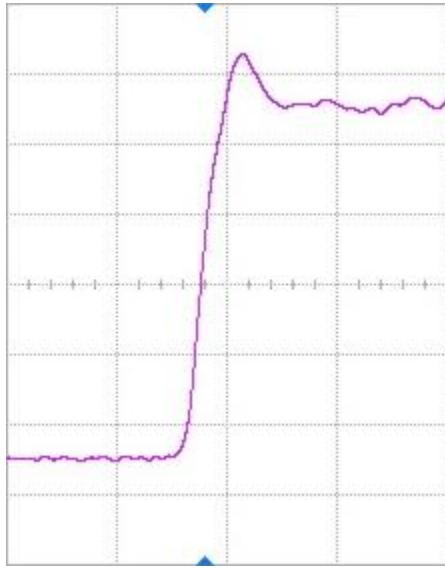


Figure 7(a) DUT 1848 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

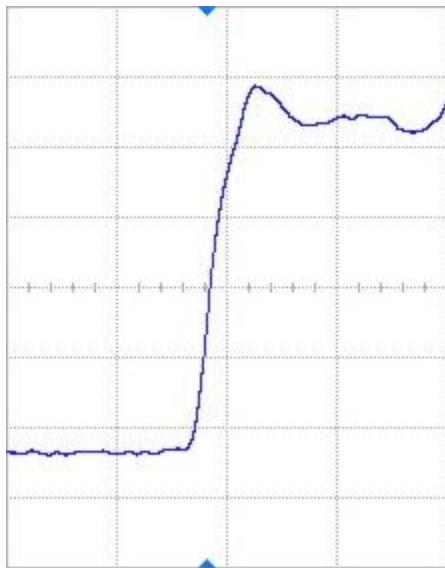


Figure 7(b) DUT 1848 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

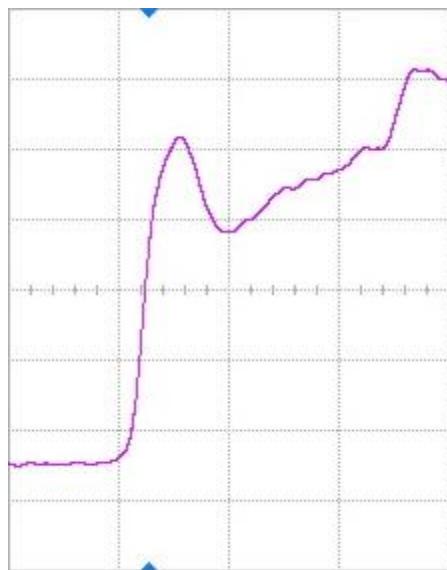


Figure 8(a) DUT 1899 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

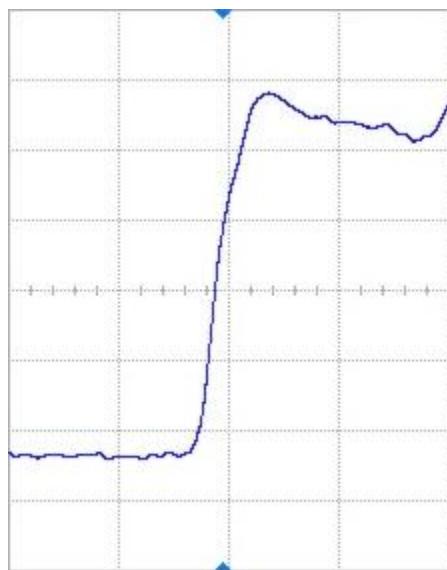


Figure 8(b) DUT 1899 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

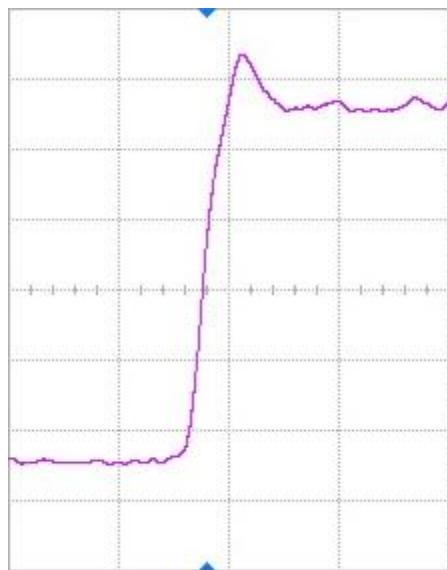


Figure 9(a) DUT 2105 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

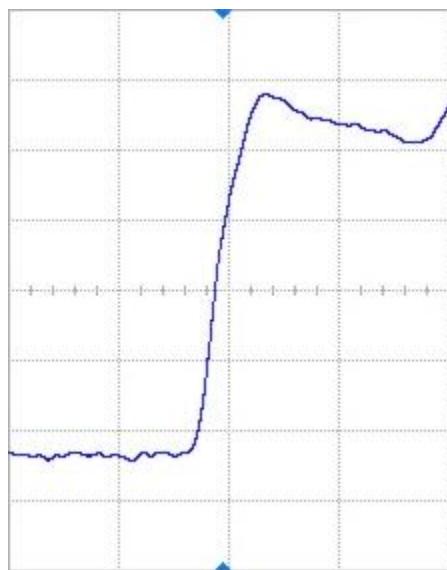


Figure 9(b) DUT 2105 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.



Figure 10(a) DUT 1848 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

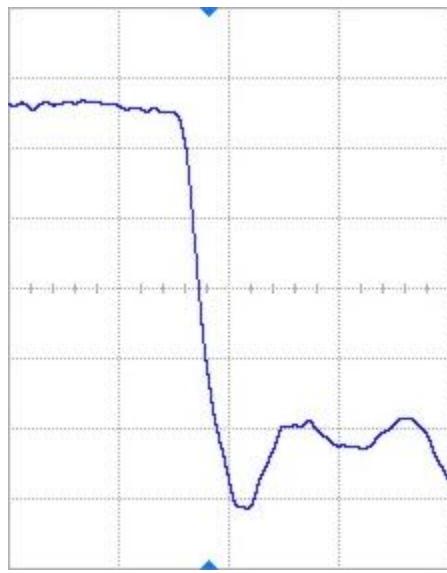


Figure 10(b) DUT 1848 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

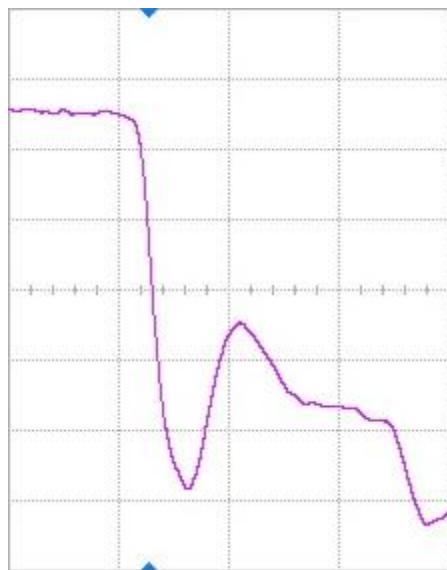


Figure 11(a) DUT 1899 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

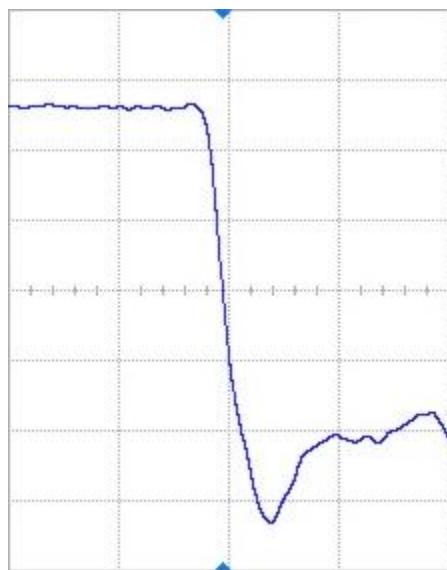


Figure 11(b) DUT 1899 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

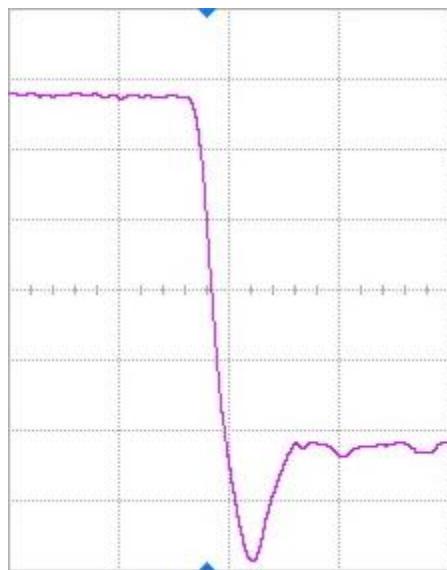


Figure 12(a) DUT 2105 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

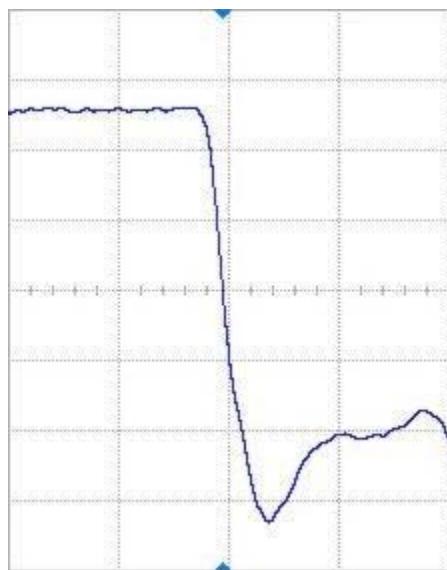
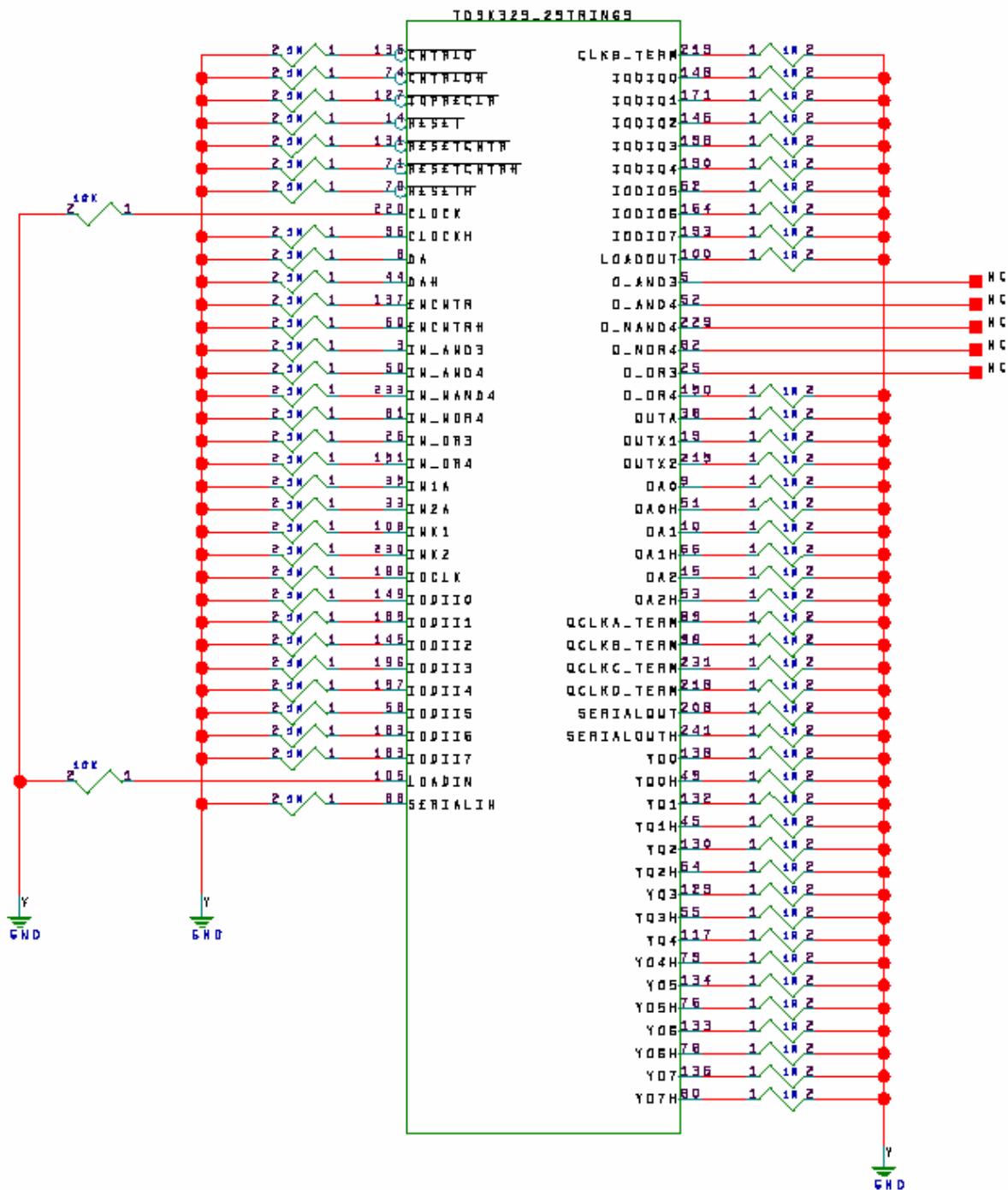
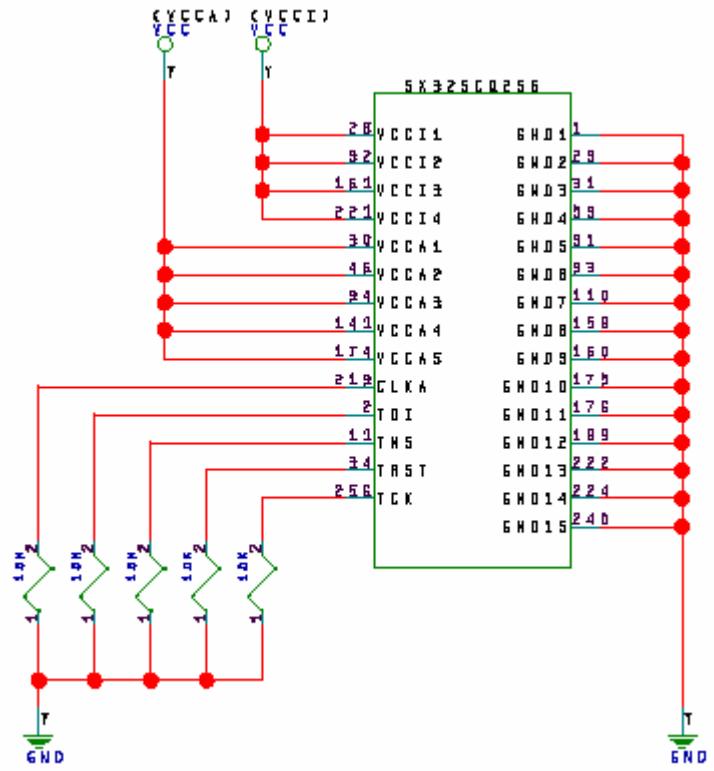


Figure 12(b) DUT 2105 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 5 ns/div.

Appendix A DUT Bias





APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

