TOTAL IONIZING DOSE TEST REPORT

No. 01T-RT1020-1980166
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I. Summary Table

Parameters	Tolerance
1. Gross Functional	> 120 krad(Si) static-biased irradiation
2. $I_{DDSTDBY}$	Passed 120 krad(Si)
3. V_{IL}/V_{IH}	Passed 120 krad(Si)
4. V_{OL}/V_{OH}	Passed 120 krad(Si)
5. Propagation Delays	Passed 120 krad(Si)
6. Rising/Falling Edge Transient	Passed 120 krad(Si)
7. Power-up Transient Current	Passed 120 krad(Si)

Note: This test was performed in NASA/Goddard radiation facility following their radiation guidelines.

II. Total Ionizing Dose (TID) Testing

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT1020
Package	CQFP84
Foundry	BAE-MANASSAS
Technology	0.8 µm CMOS
Die Lot Number	1980166
Quantity Tested	4
Serial Numbers	LAN5401, LAN5402, LAN5403, LAN5404

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	24 krad(Si)/day (+/-10%)
Data Mode	Static
Temperature	Room
Bias	5.0 V

C. Test Method

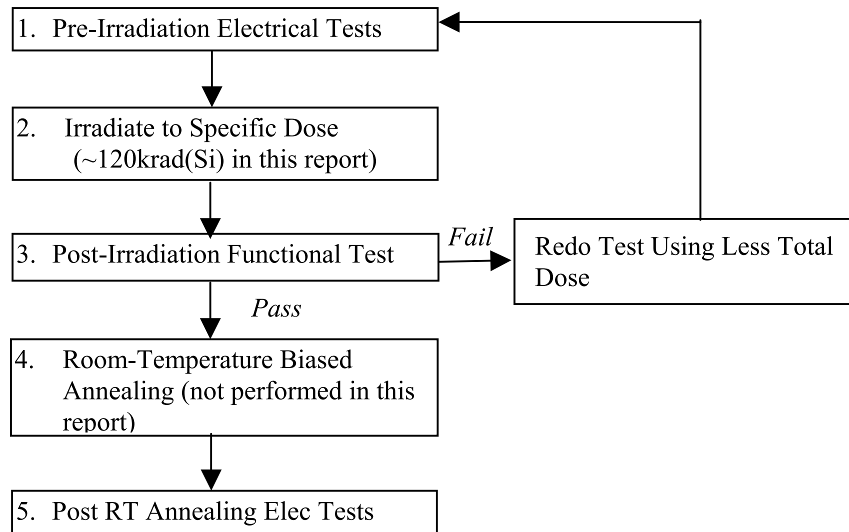


Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs. Because the product, RT1020 is relatively radiation tolerant, we had forgone this test in this report.

Method two performs irradiation and parametric test. It is in compliance with TM1019.5. Figure 1 shows the testing process flow. Rebound annealing at 100 °C is omitted because Actel antifuse FPGA, fabricated by CMOS technologies, have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, this bench setup has much less noise. It only samples selected pins for threshold voltage and switching transient measurements. However, these parameters usually have very small changes after being irradiated with a total dose lower than the tolerance for functionality. I_{CC} usually limits the tolerance for the “parametric radiation testing”. Thus, sampling few pins is sufficient enough to prove that the radiation effects causes no concerns on the measured parameters. Other advantages for the bench setup are the in-flux measurement of I_{CC} and functionality, and the measurement of the power-up transient current. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. I_{CC}	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. TEST RESULTS

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post-irradiation test (step 5). The DUT used for this test are LAN5401, LAN5402, LAN5403 and LAN5404.

A. Functional Test

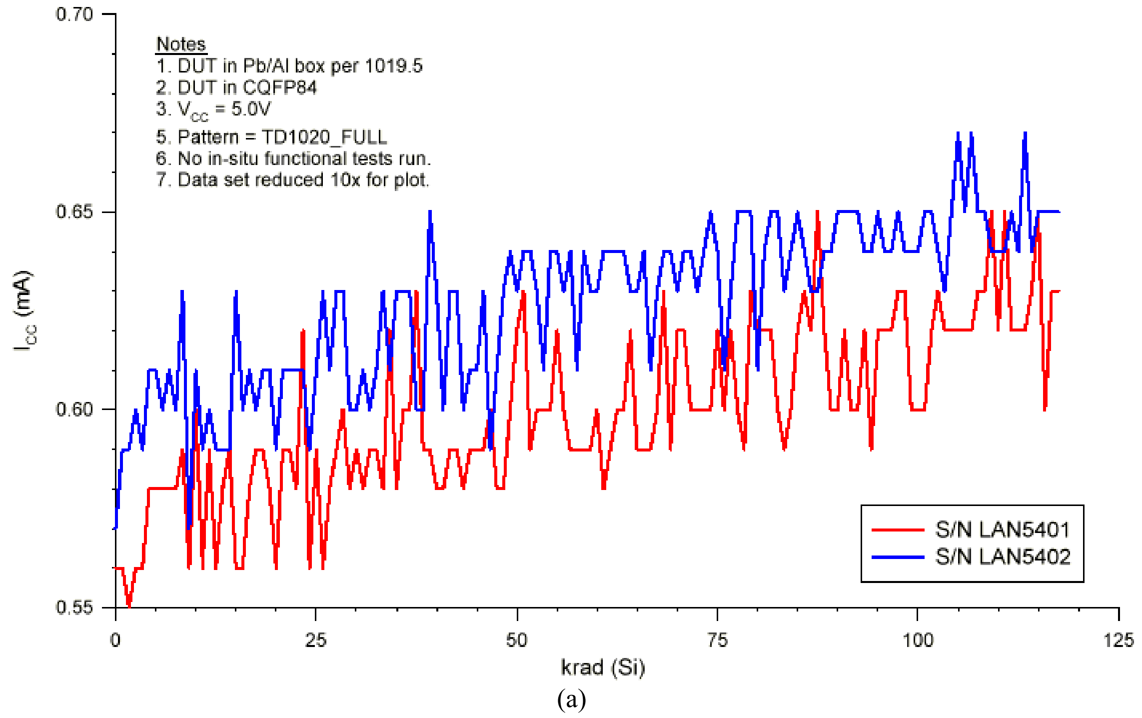
Table 4 lists the results of the functional test.

Table 4. Functional Test Results

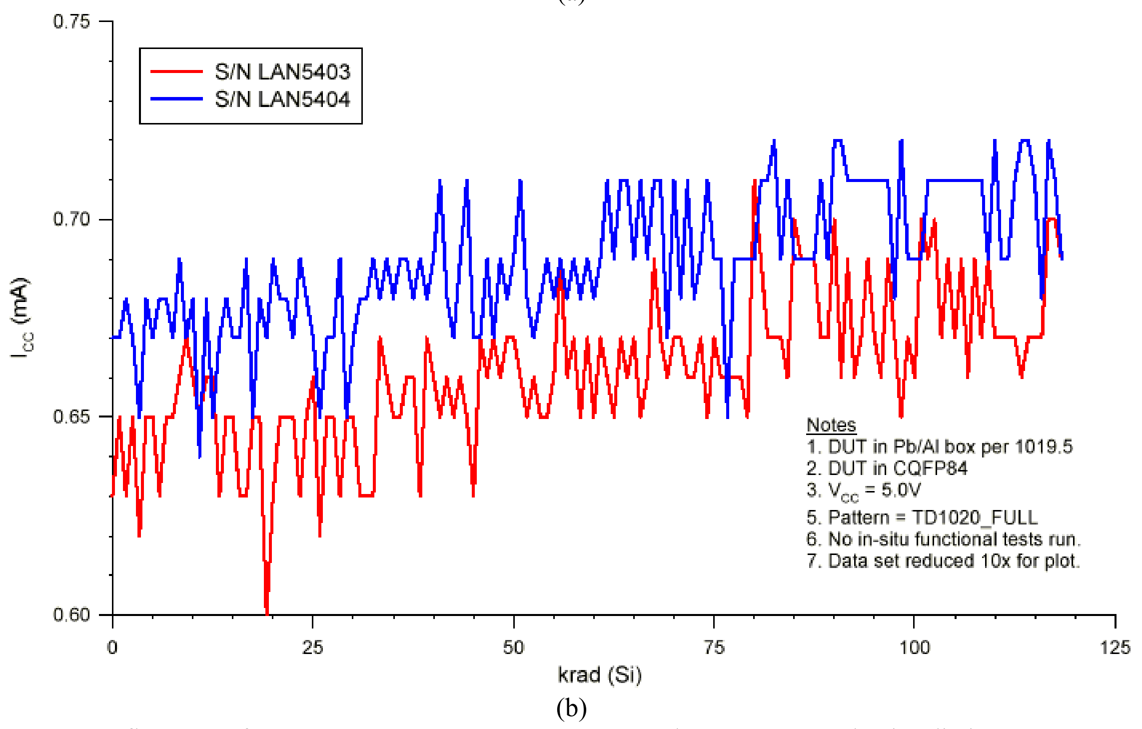
	Pre-Irradiation	Post-Irradiation
LAN5401	passed	passed
LAN5402	passed	passed
LAN5403	passed	passed
LAN5404	passed	passed

B. I_{CC}

Figure 2a and 2b show the in-flux I_{CC} of DUT LAN5401, LAN5402, LAN5403, and LAN5404. The irradiation was done in two batches. LAN5401 and LAN5402 were the first batch, and LAN5403 and LAN5404 were the second batch. Both radiation were stopped at 120 krad(Si) when all the DUT were functional. The radiation-induced I_{CC} in every DUT is negligible.



(a)



(b)

Figure 2. In-flux I_{CC} of LAN5401, LAN5402, LAN5403 and LAN5404. The irradiation were stopped at 120 krad(Si). The radiation-induced I_{CC} is barely visible in each DUT.

C. Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-irradiation. The radiation effect on this parameter is negligible in every DUT.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Irradiation
LAN5401	1.73	1.70
LAN5402	1.76	1.74
LAN5403	1.77	1.75
LAN5404	1.77	1.76

D. Output Characteristic

Figure 3a and 3b show the V_{OL} characteristic curves for the pre-irradiated and post-irradiated DUT. All measured V_{OL} are within the spec, and the radiation effect on V_{OL} is negligible for every DUT. The spec is that when I_{OL} = 6 mA, V_{OL} cannot exceed 0.4 V.

Figure 4a and 4b show the V_{OH} characteristic curves for the pre-irradiated and post-irradiated DUT. All measured V_{OL} are within the spec, and the radiation effect on VOL is negligible for every DUT. The spec is that when I_{OH} = 4 mA, V_{OH} cannot be lower than 3.7 V.

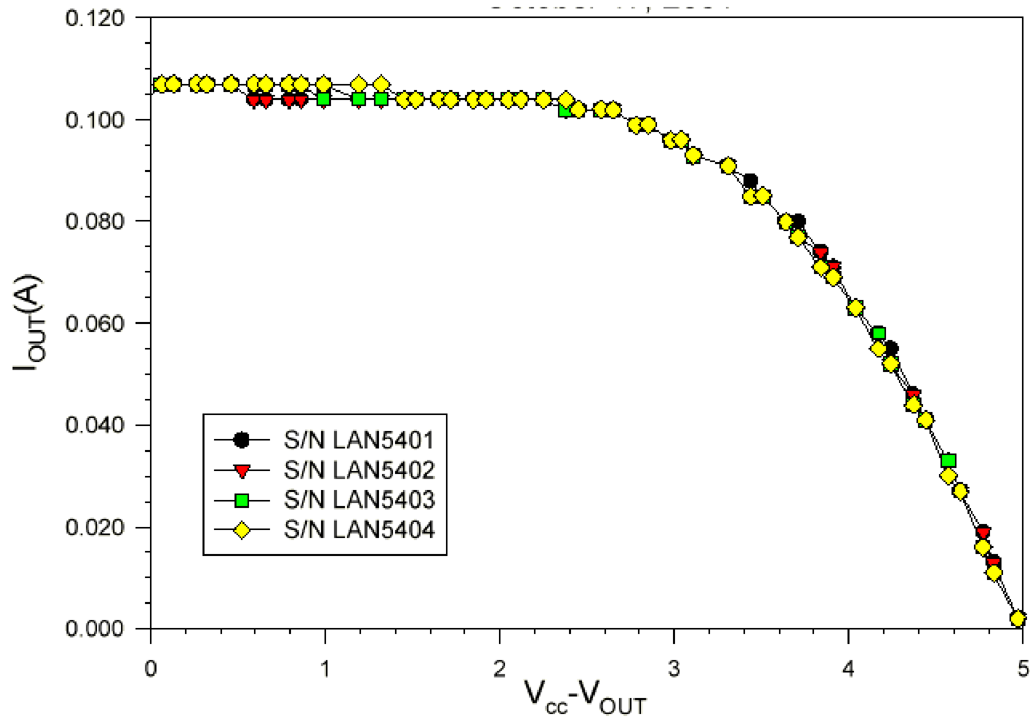


Figure 3a. Pre-irradiation V_{OL} characteristic curves.

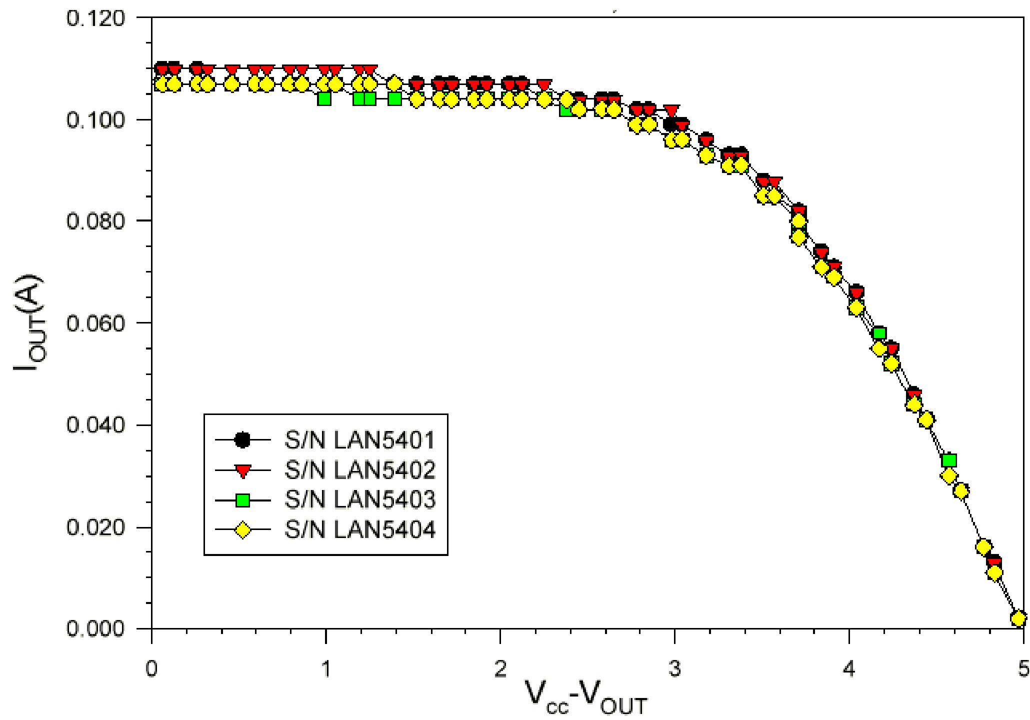


Figure 3b. Post-irradiation V_{OL} characteristic curves.

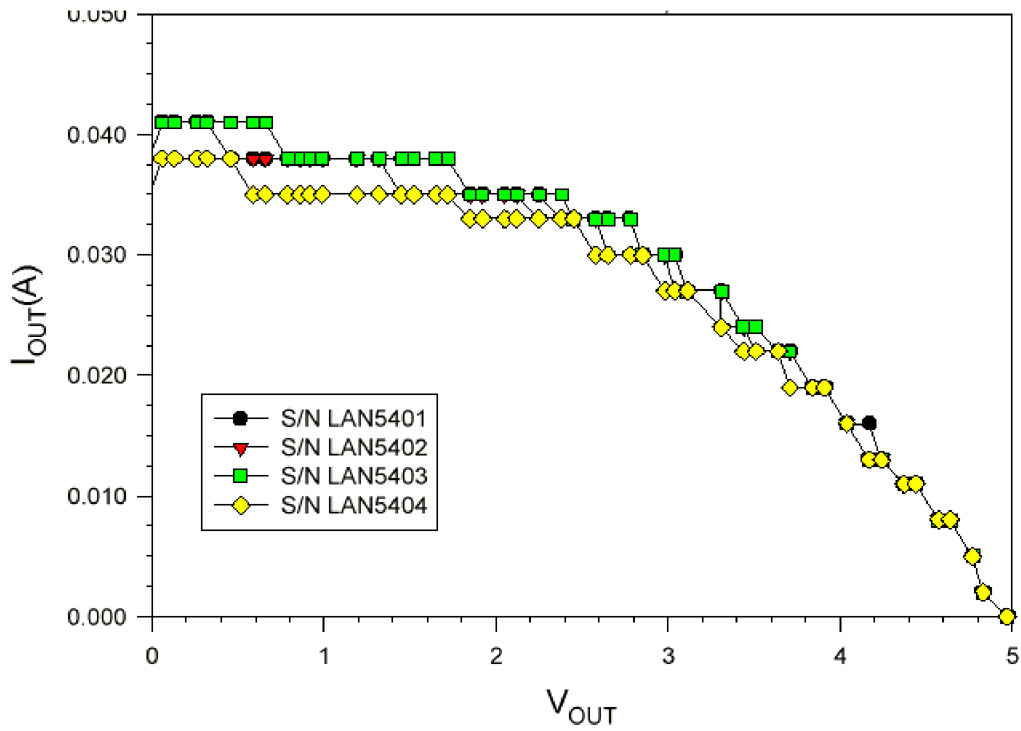


Figure 4a. Pre-irradiation V_{OH} characteristic curves.

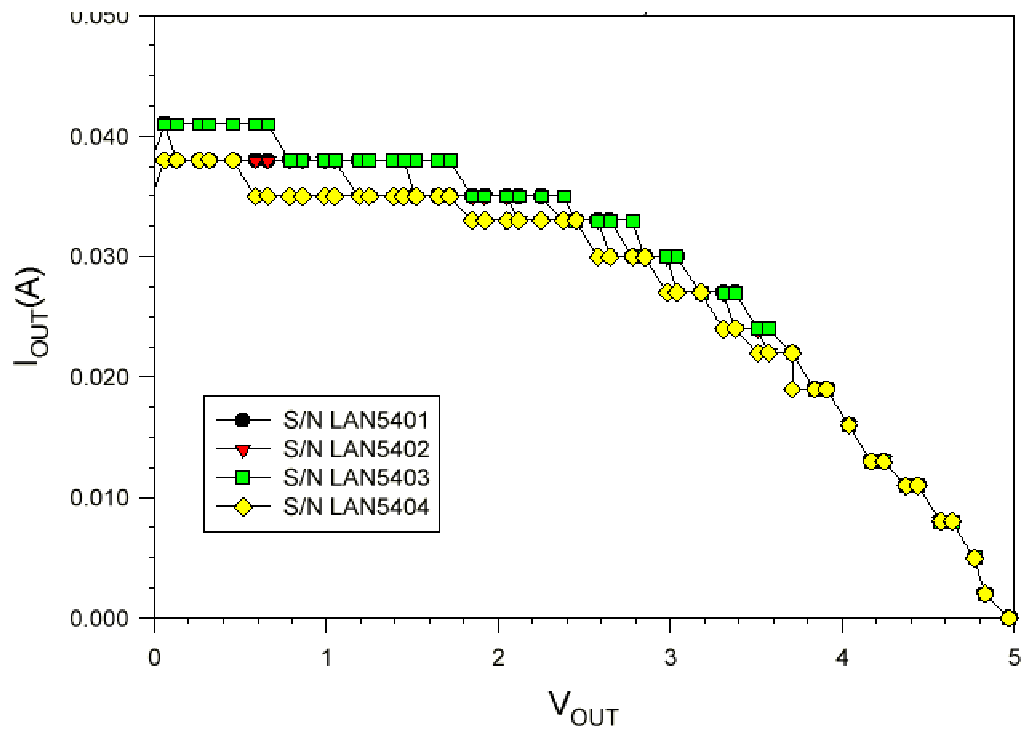


Figure 4b. Post-irradiation V_{OH} characteristic curves.

E. Propagation Delays

The propagation delays, both the rising and falling edges, were measured on a combinatorial logic path. This combinatorial logic is a worst-case-design for radiation-induced degradation on propagation delays. Table 6 lists the results. Data show no measurable radiation-induced degradation, since the post-irradiation delay in every case, is smaller than the pre-irradiation delay.

Table 6. Propagation Delays of Combinatorial Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN5401	506	503	479	477
LAN5402	498	495	472	470
LAN5403	504	500	478	474
LAN5404	506	501	484	484

F. Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-irradiation. Figures 5-8 show the rising edge transient. Figures 9-12 show the falling edge transient. The radiation effect in every case is practically negligible.

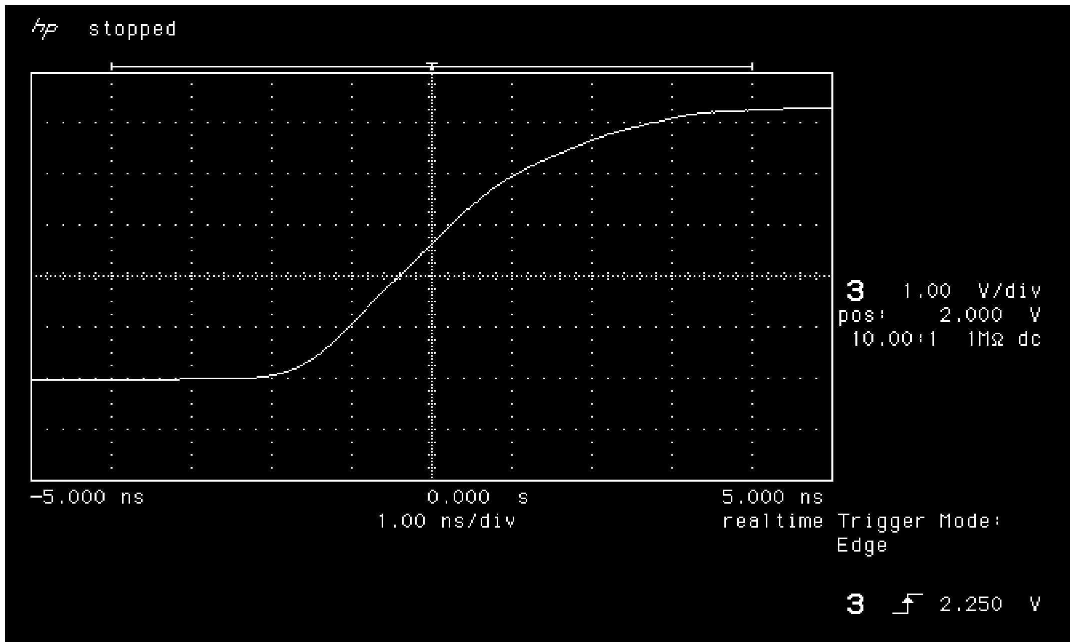


Figure 5a. Rising edge of LAN5401 pre-irradiation.

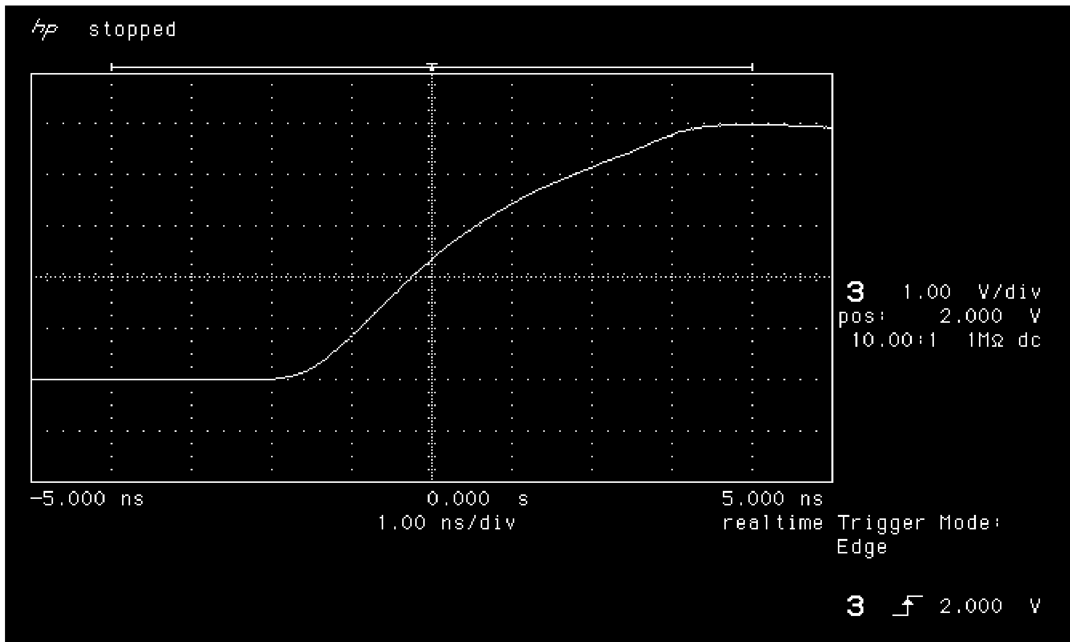


Figure 5b. Rising edge of LAN5401 post-irradiation.

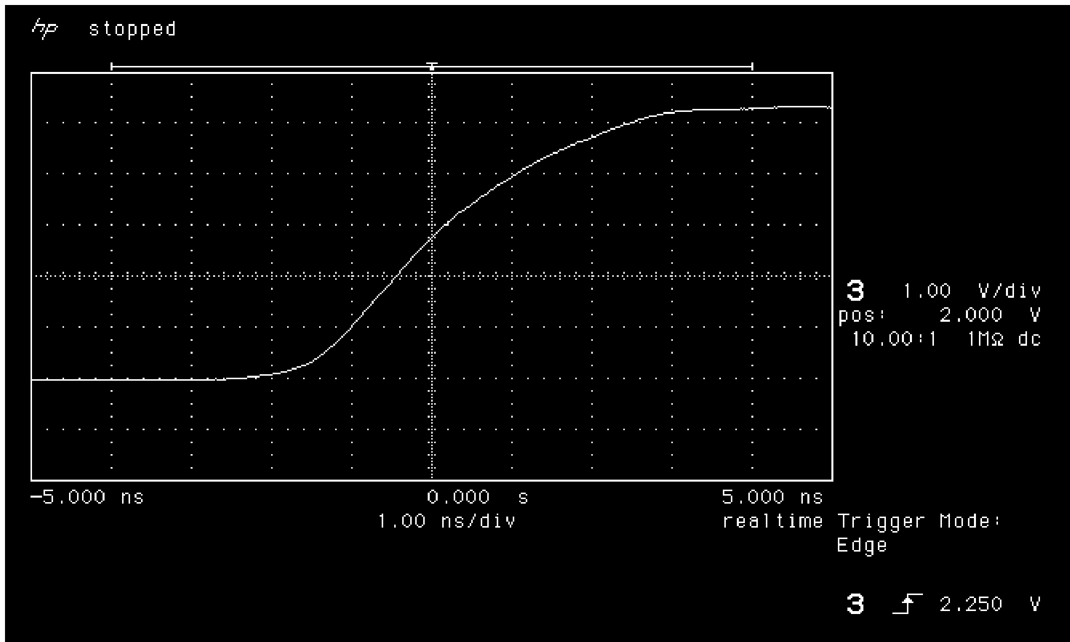


Figure 6a. Rising edge of LAN5402 pre-irradiation.

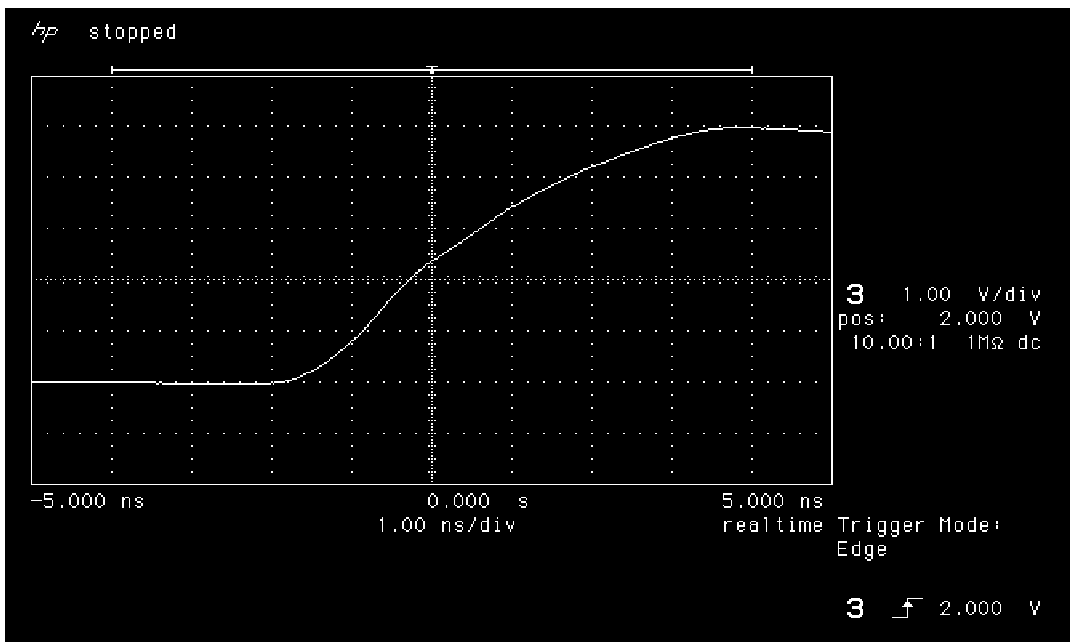


Figure 6b. Rising edge of LAN5402 post-irradiation.

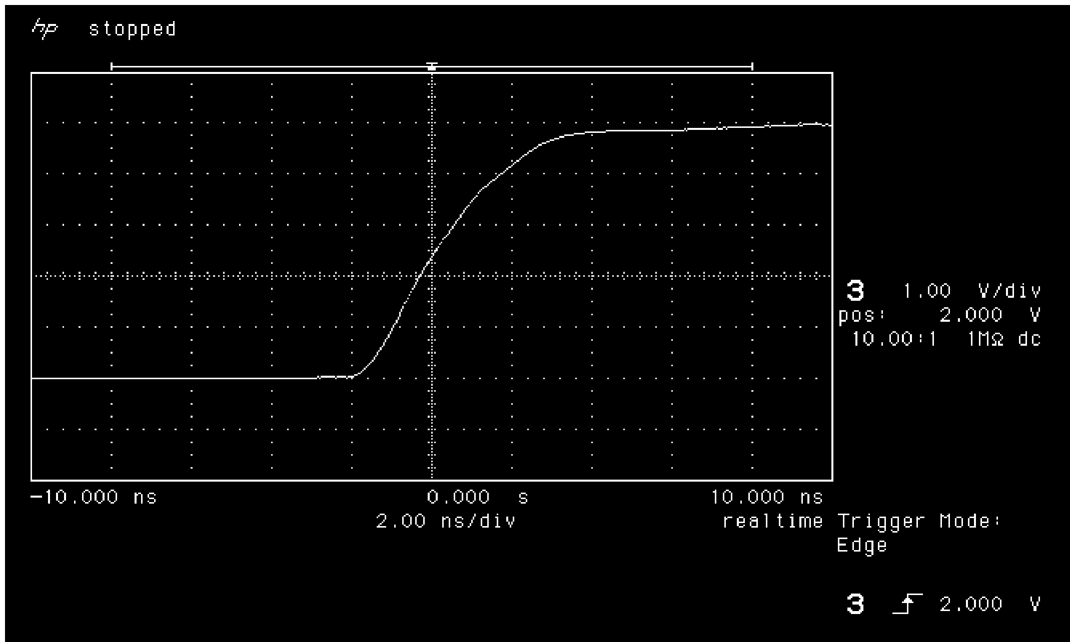


Figure 7a. Rising edge of LAN5403 pre-irradiation.

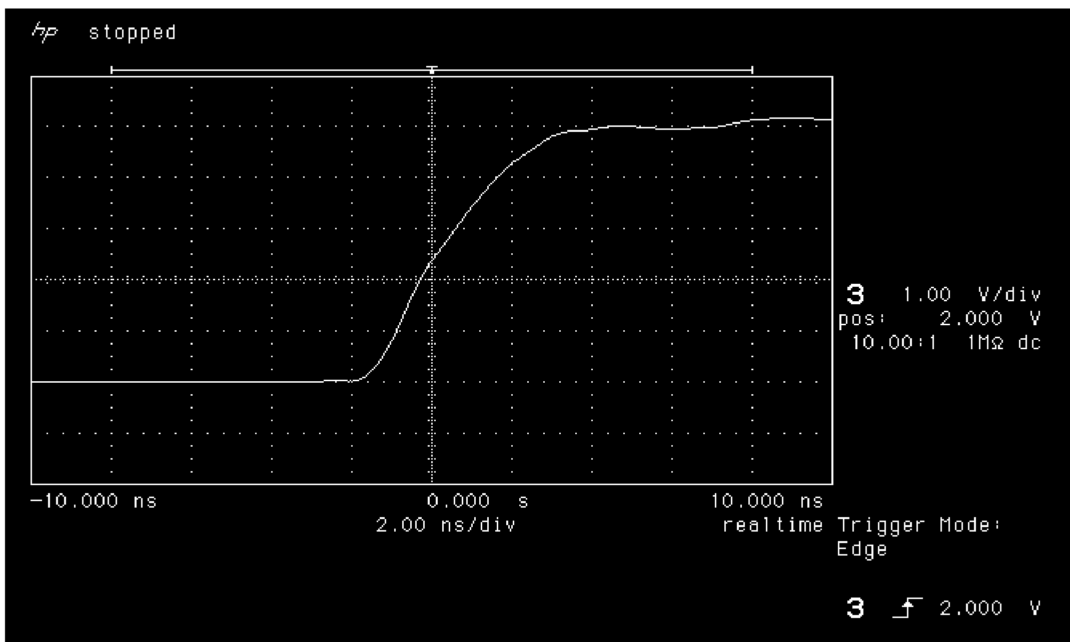


Figure 7b. Rising edge of LAN5403 post-irradiation.

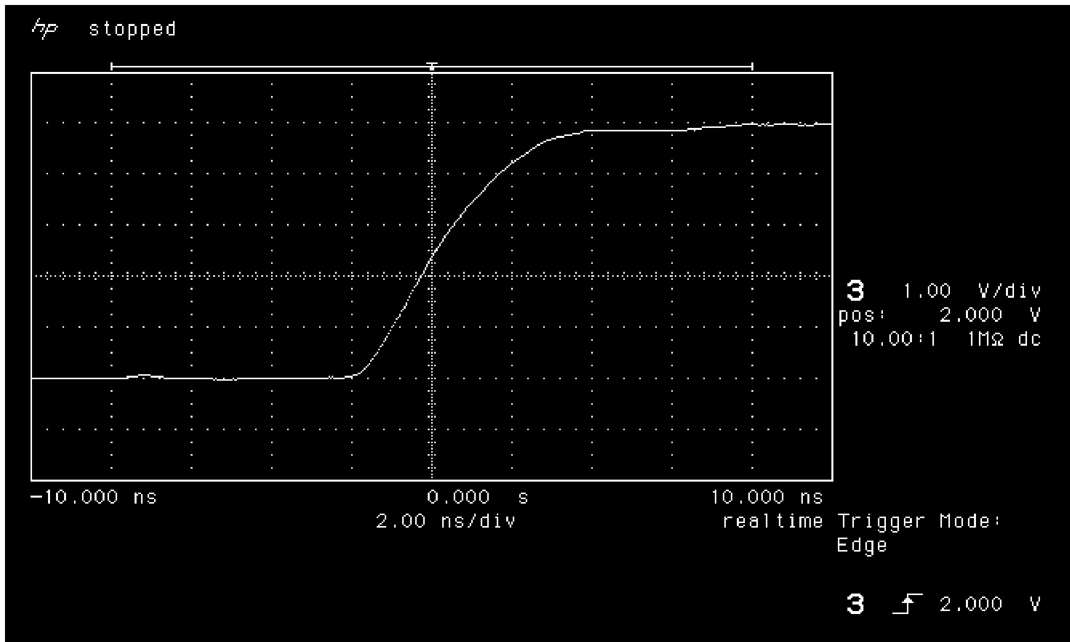


Figure 8a. Rising edge of LAN5404 pre-irradiation.

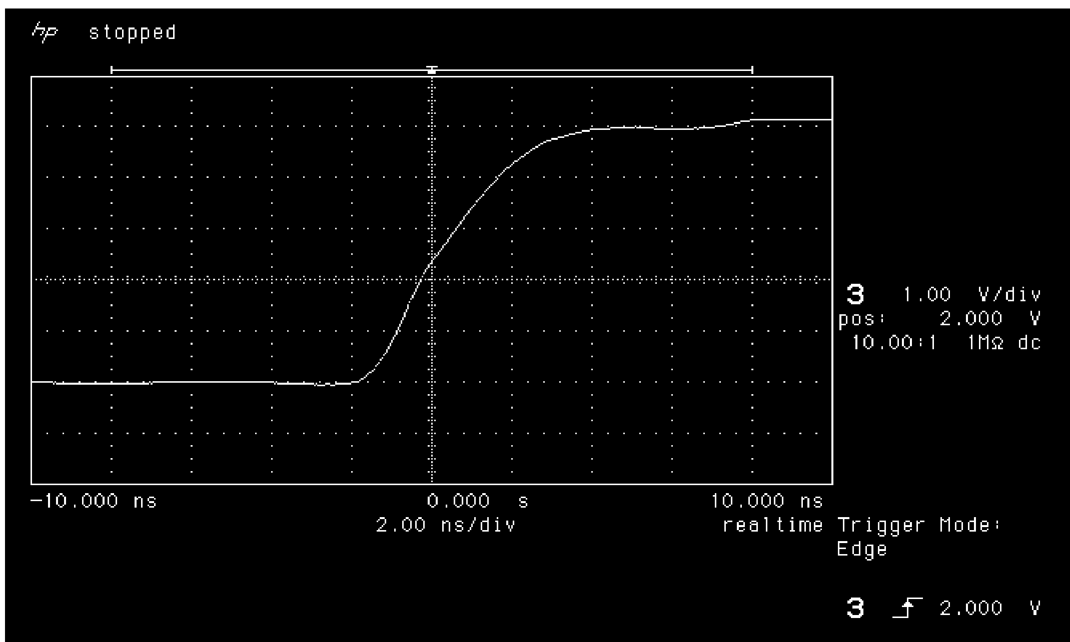


Figure 8b. Rising edge of LAN5404 post-irradiation

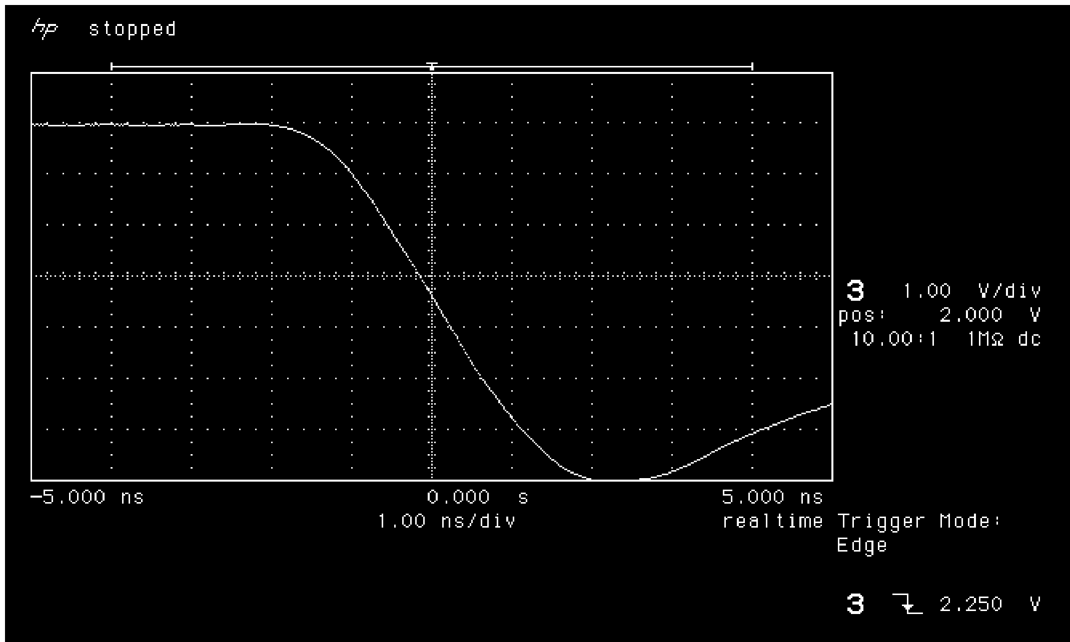


Figure 9a. Falling edge of LAN5401 pre-irradiation

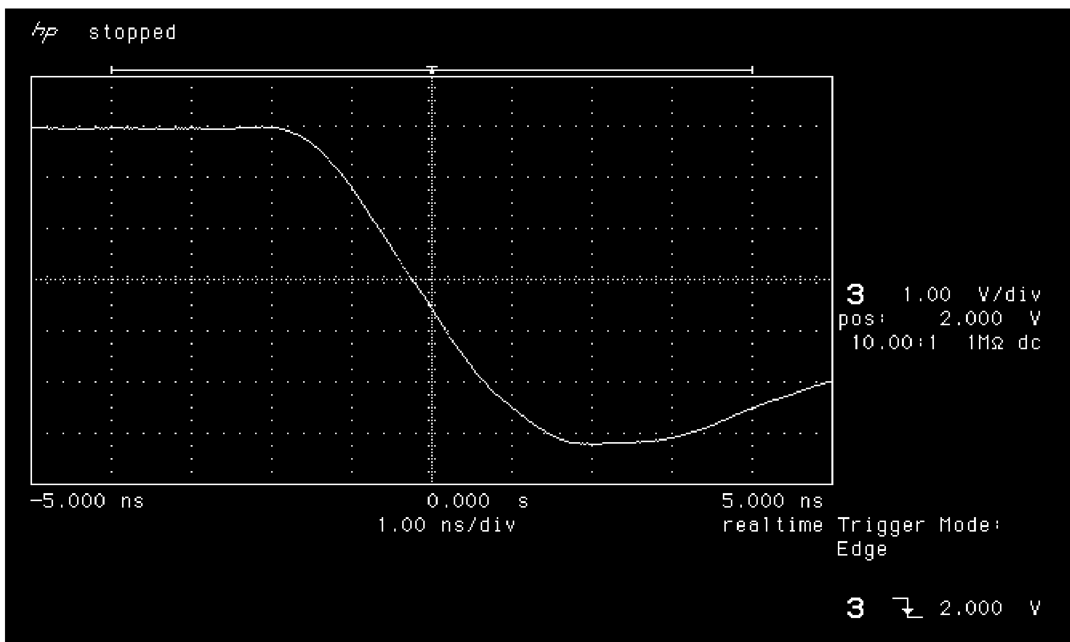


Figure 9b. Falling edge of LAN5401 post-irradiation.

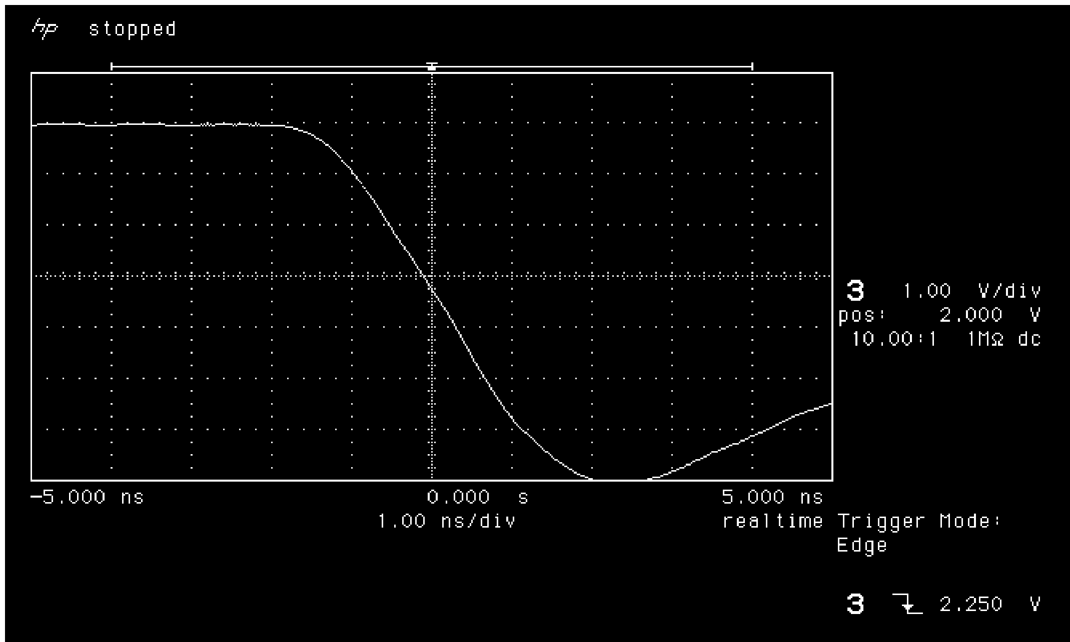


Figure 10a. Falling edge of LAN5402 pre-irradiation.

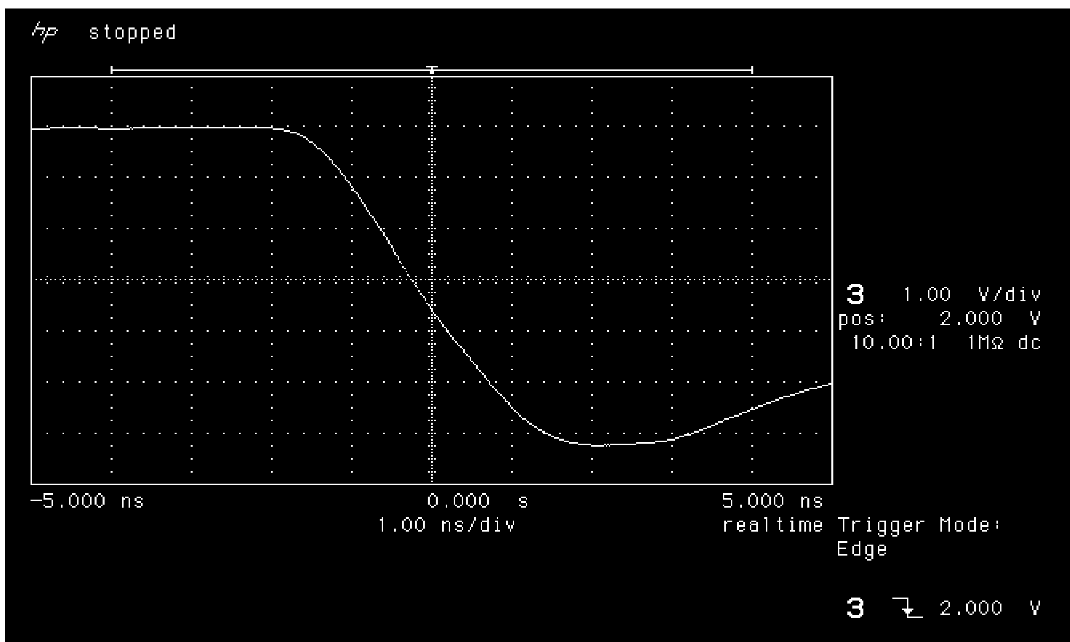


Figure 10b. Falling edge of LAN5402 post-irradiation.

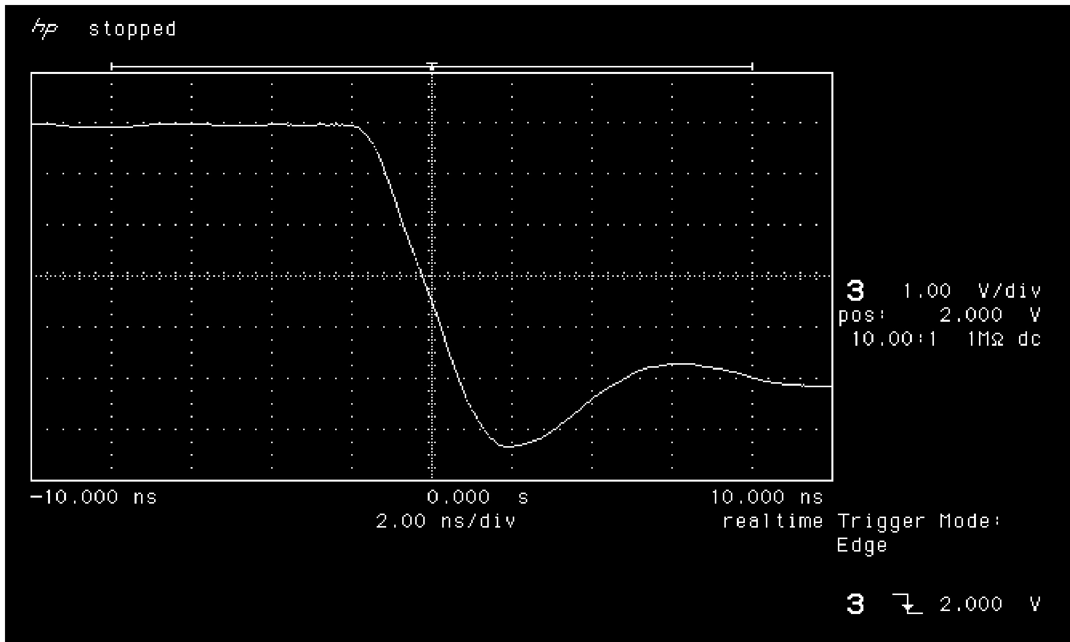


Figure 11a. Falling edge of LAN5403 pre-irradiation.

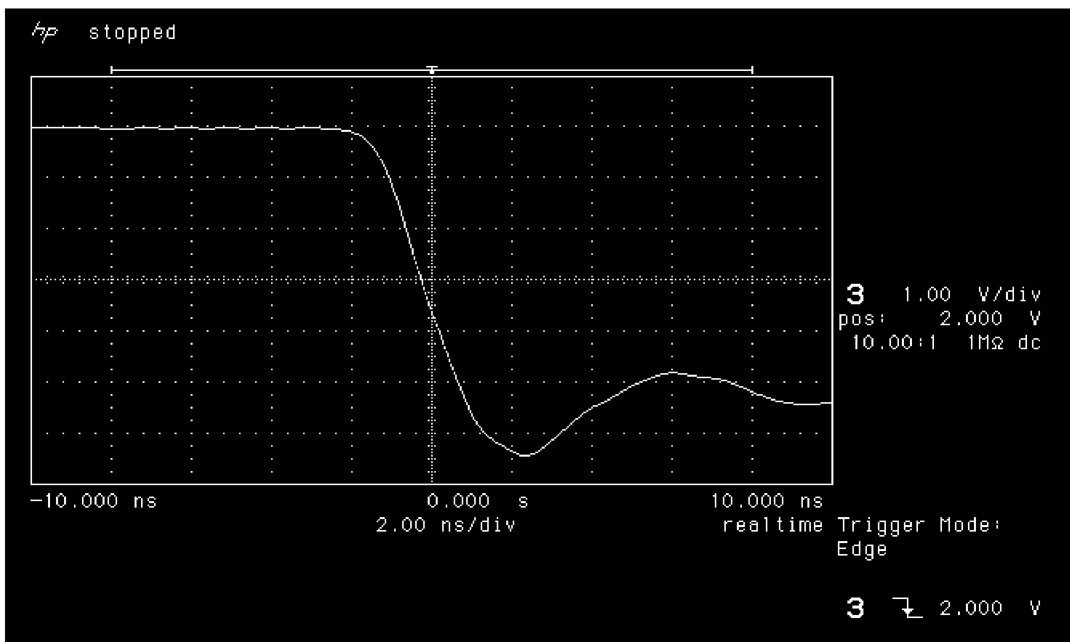


Figure 11b. Falling edge of LAN5403 post-irradiation.

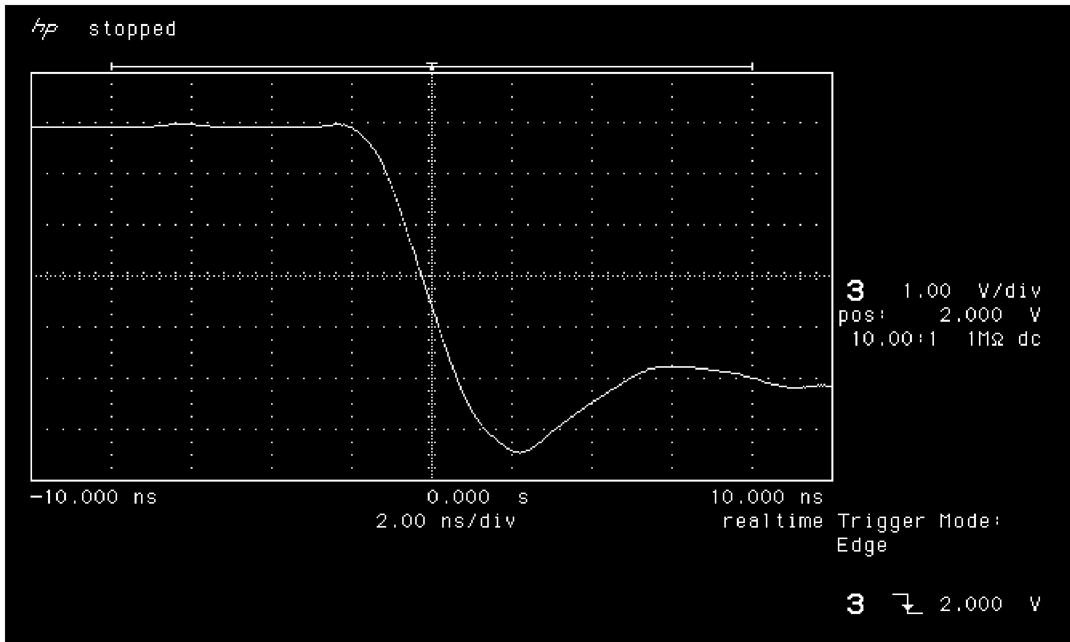


Figure 12a. Falling edge of LAN5404 pre-irradiation

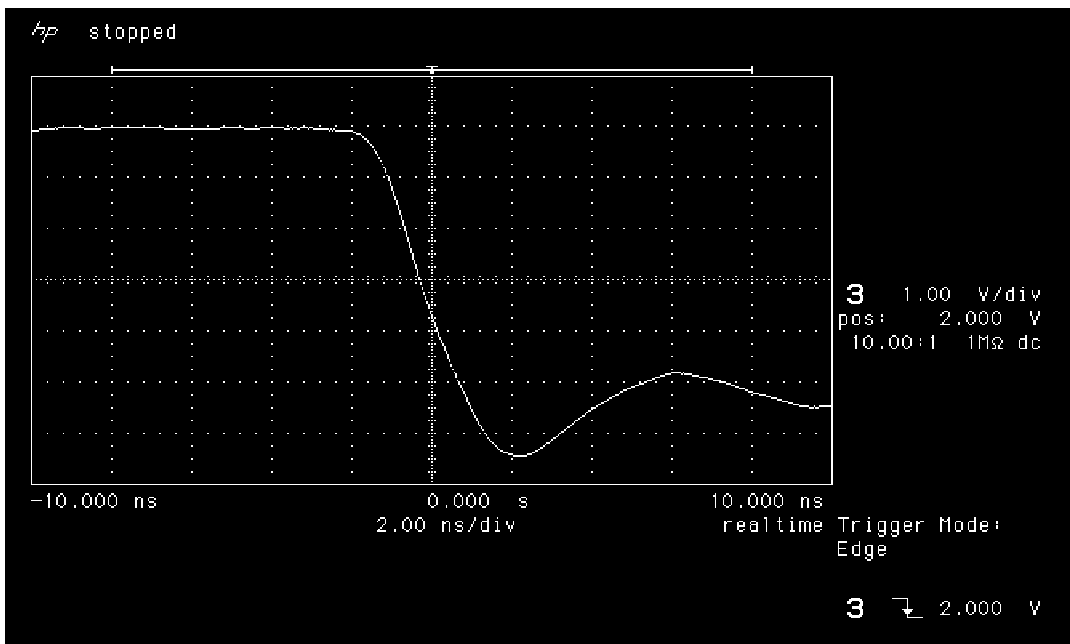


Figure 12b. Falling edge of LAN5404 post-irradiation

7) Power-Up Transient

In each measurement, the rise time of the power supply voltage (V_{CC}) was 1.2 ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 13-16 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 5.0 V, and another curve showing I_{CC}. The scale is 1 V per division for V_{CC} and 100 mA per division for I_{CC}. Every post-irradiation DUT shows negligible radiation-induced transient current during power up. Readers interested in the details of power up transient should consult the paper, "Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA" (by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278).

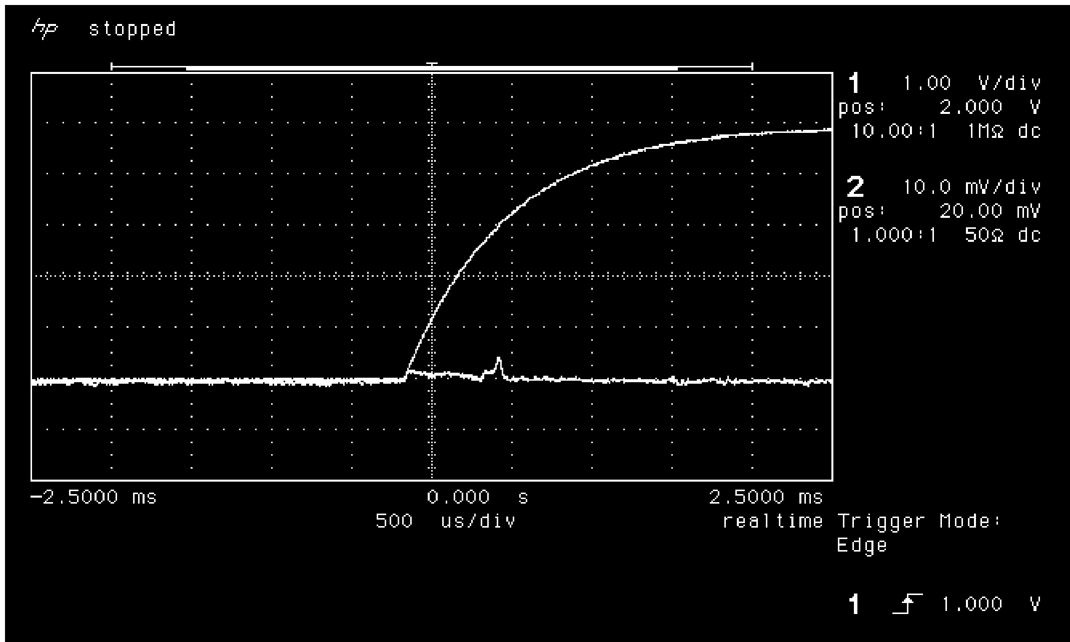


Figure 13a. Power-up transient of LAN5401 pre-irradiation.

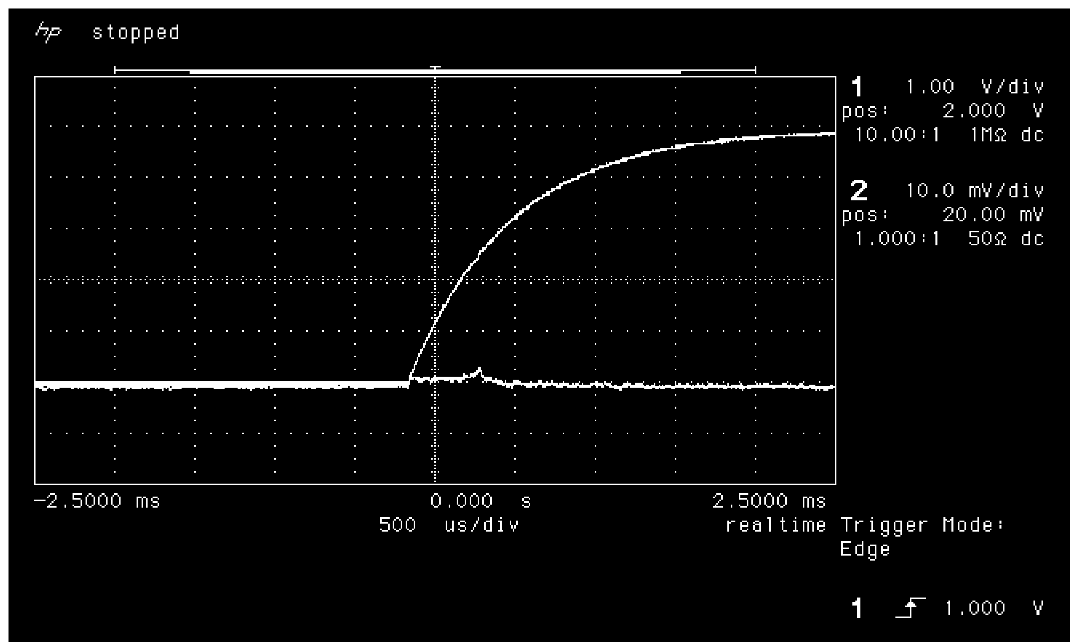


Figure 13b. Power-up transient of LAN5401 post-irradiation.

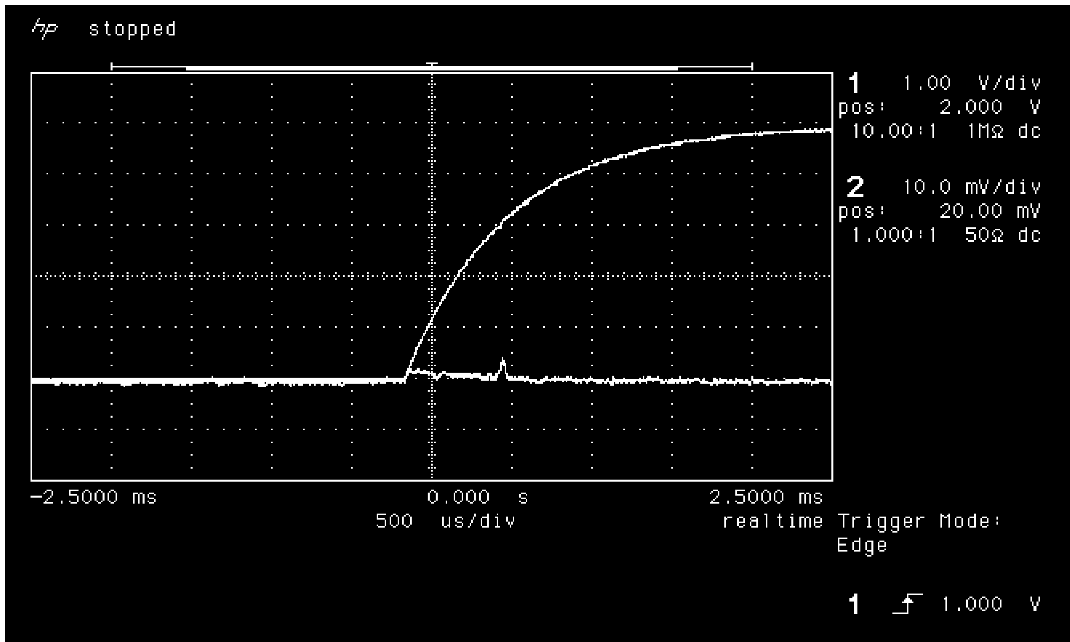


Figure 14a. Power-up transient of LAN5402 pre-irradiation.

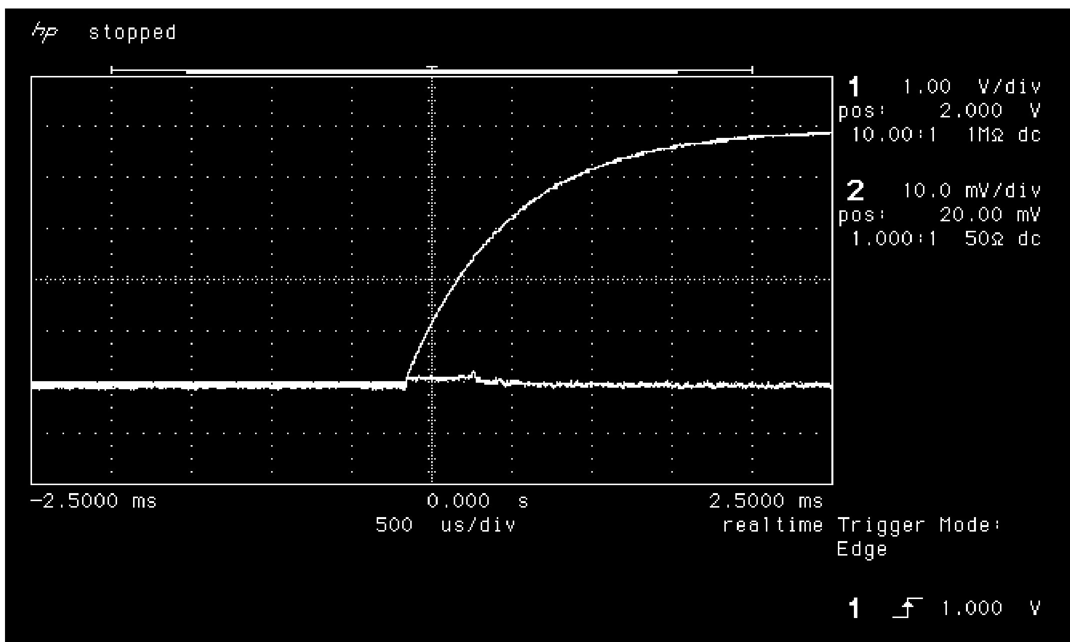


Figure 14b. Power-up transient of LAN5402 post-irradiation.

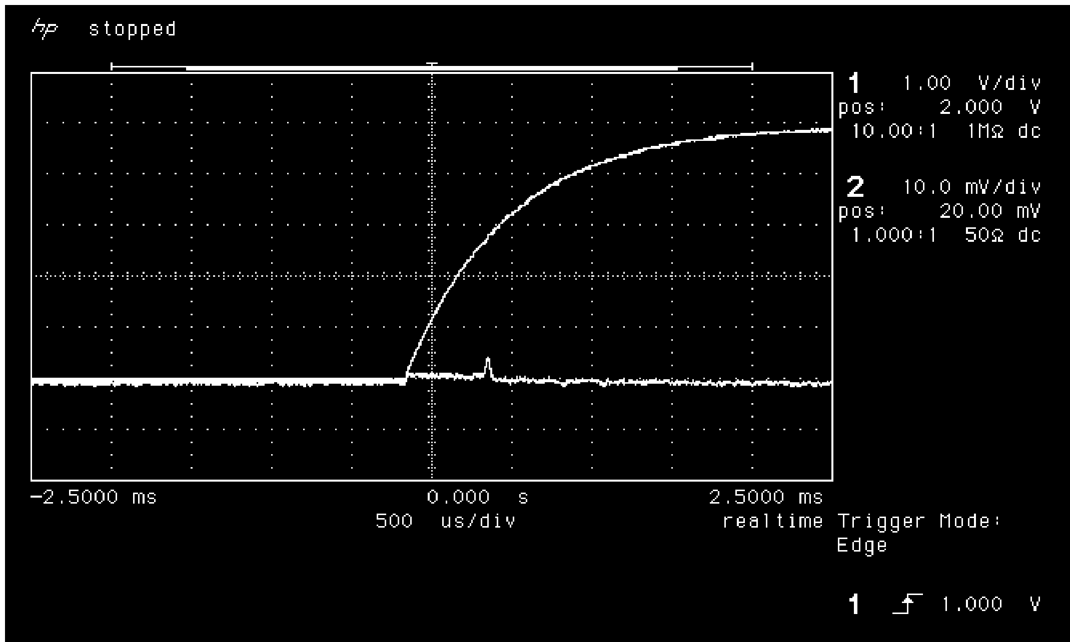


Figure 15a. Power-up transient of LAN5403 pre-irradiation.

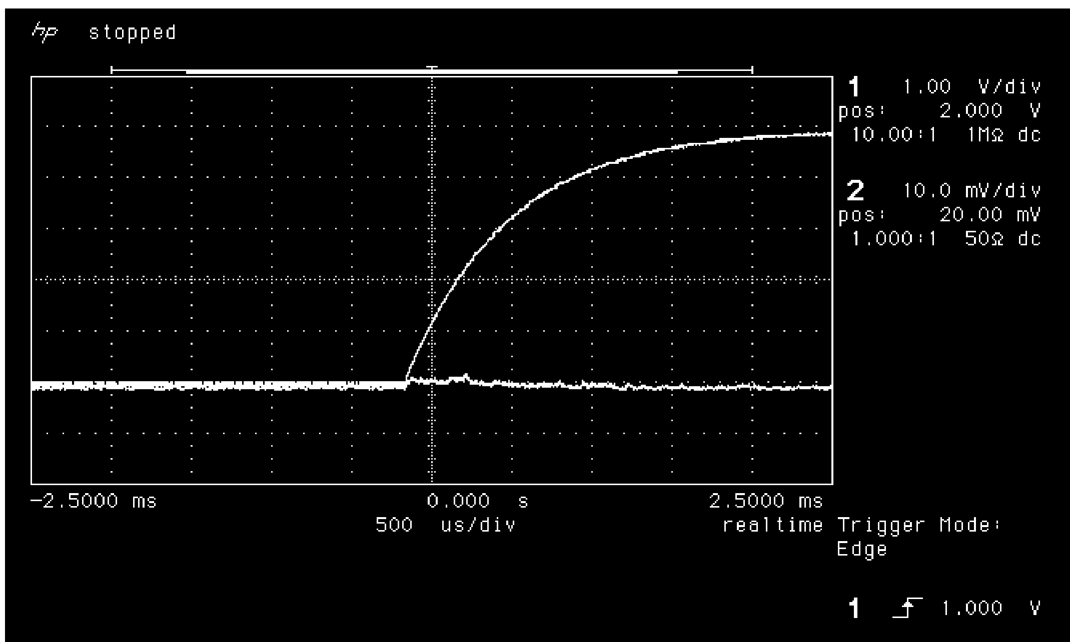


Figure 15b. Power-up transient of LAN5403 post-irradiation.

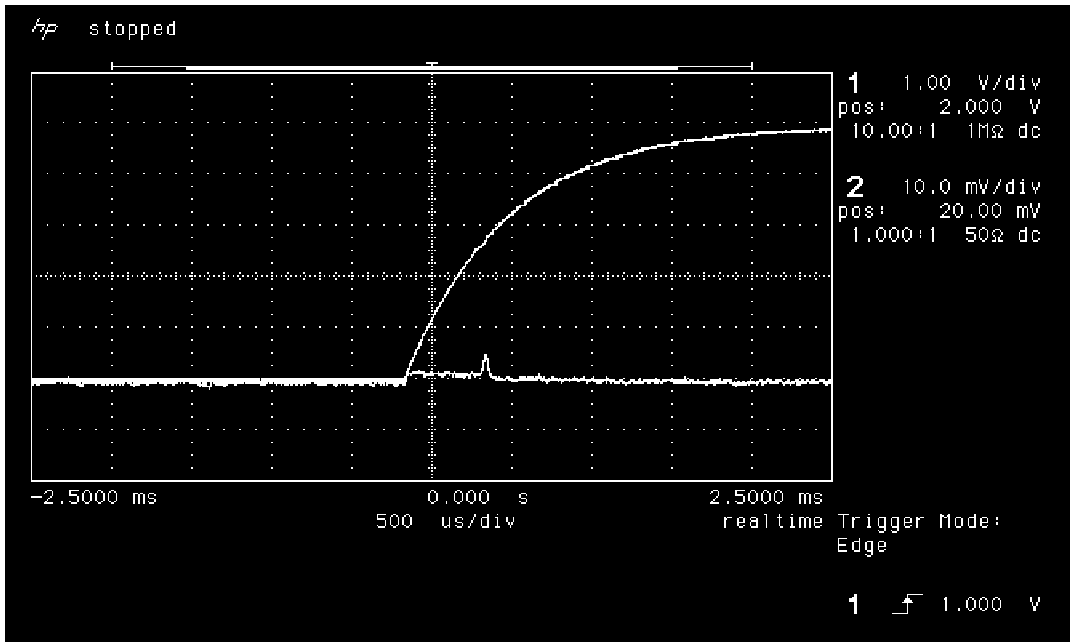


Figure 16a. Power-up transient of LAN5404 pre-irradiation

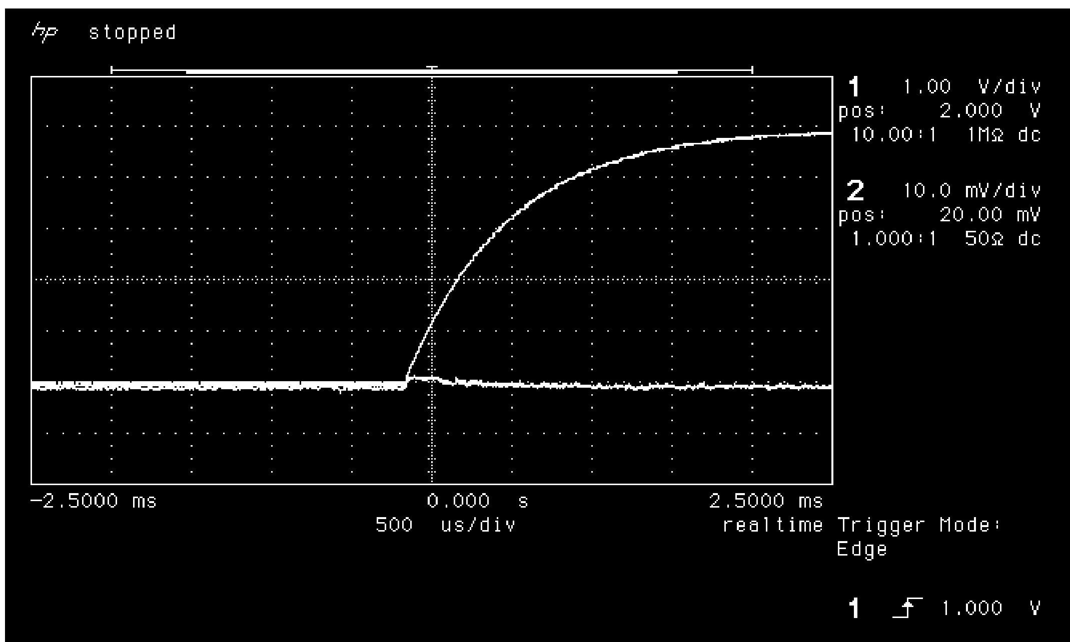


Figure 16b. Power-up transient of LAN5404 post-irradiation