June 24, 1999

TOTAL IONIZATION DOSE TEST REPORT

No. 99T-RT1020-159
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1.0 SUMMARY TABLE

RT1020 Parameters/Characteristics	Results
1. Functionality	>> 100 krad(Si)
2. $I_{DDSTDBY}$	Passed 100 krad(Si) (see Figure 2)
3. V_{IL}/V_{IH}	Passed 100 krad(Si) (see Table 5)
4. V_{OL}/V_{OH}	Passed 100 krad(Si) (see Figures 3-8)
5. Propagation Delays	Passed 100 krad(Si) (see Table 6,7)
6. Rising/Falling Edge Transient	Passed 100 krad(Si) (see Figures 9-18)
7. Power-on Transient Current	Passed 100 krad(Si) (see Figures 19-22)

2.0 TID TEST

This section describes the device under test (DUT), the irradiation parameters, and the testing method.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1

Part Number	RT1020
Package	CQ84
Foundry	LMSEC
Technology	0.8 µm CMOS
Die Lot Number	970159
Date Code	9839
Quantity Tested	5
Serial Numbers	Control (LAN1705), LAN1701, LAN1702, LAN1703, LAN1704

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2

Facility	NASA
Radiation Source	Co-60
Dose Rate	12.95 krad(Si)/min (+-10%)
Final Total Dose for DC/AC Parameter Measurement	100 krad(Si)
Temperature	Room
Bias	5.0 V

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2.3 TESTING METHOD

The testing method is following the spirit of TM1019.5 and targets for the low-dose-rate space applications. Figure 1 shows the flow. Room temperature annealing and post annealing tests were omitted in this testing because the DUTs showed no radiation effects after 100 krad(Si) (e.g. I_{DDSTDY} in Figure 2 was constant throughout the irradiation). Rebound annealing is also omitted because there are enough data showing Actel antifuse FPGA not having any adverse rebound effects.

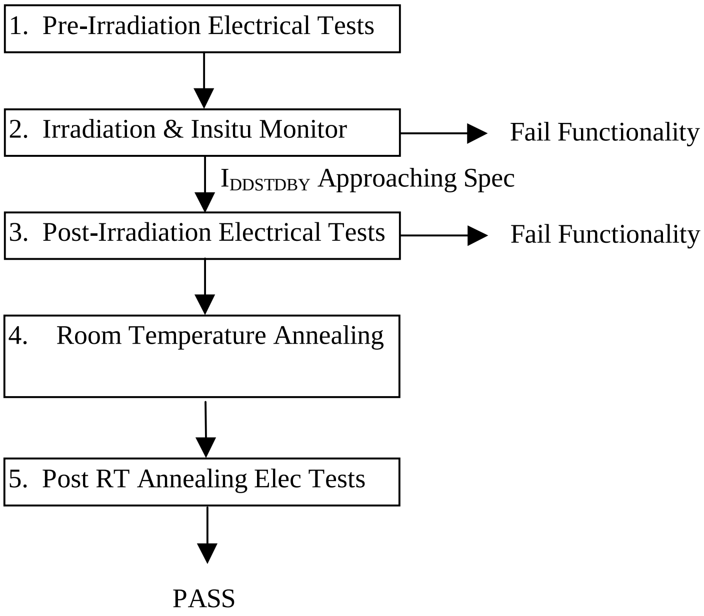


Figure 1. Test method flow-chart

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on bench with relative low noise. The corresponding logic design circuits are listed in Table 3.

Table 3

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power line
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	Output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-on Transient	DUT power line

3.0 TEST RESULTS

This section presents all the parameters/characteristics results for pre-irradiation (step 1 in Figure 1), post-irradiation (step 3).

3.1 FUNCTIONAL TEST

Two types of functionality tests were performed. Samples were irradiated until functional failure occurred to determine the functionality tolerance in the summary table. The second type is including in the testing flow (Figure 1). Each test step (step 1, 3) has a functional test by default. Table 4 lists the second testing results of all five DUTs.

Table 4. Functionality Test

	Pre-Irradiation	Post-100krad (Si) Irradiation
Cntl (LAN1705)	passed	passed
LAN1701	passed	passed
LAN1702	passed	passed
LAN1703	passed	passed
LAN1704	passed	passed

3.2 IDDSTANDBY

$I_{DDstandby}$ and functionality of four pins were monitored during the irradiation period. Because the board had a measurable leakage, only the delta $I_{DDstandby}$ due to radiation was recorded. Using delta $I_{DDdstandby}$, won't create any significant extraneous error since the pre-irradiation value of $I_{DDstandby}$ is under 1 mA. The increment of $I_{DDstandby}$ by irradiation determines the tolerance. Although only two DUTs are shown in Figure 2, all the irradiated DUTs showed no increase in standby current throughout the irradiation.

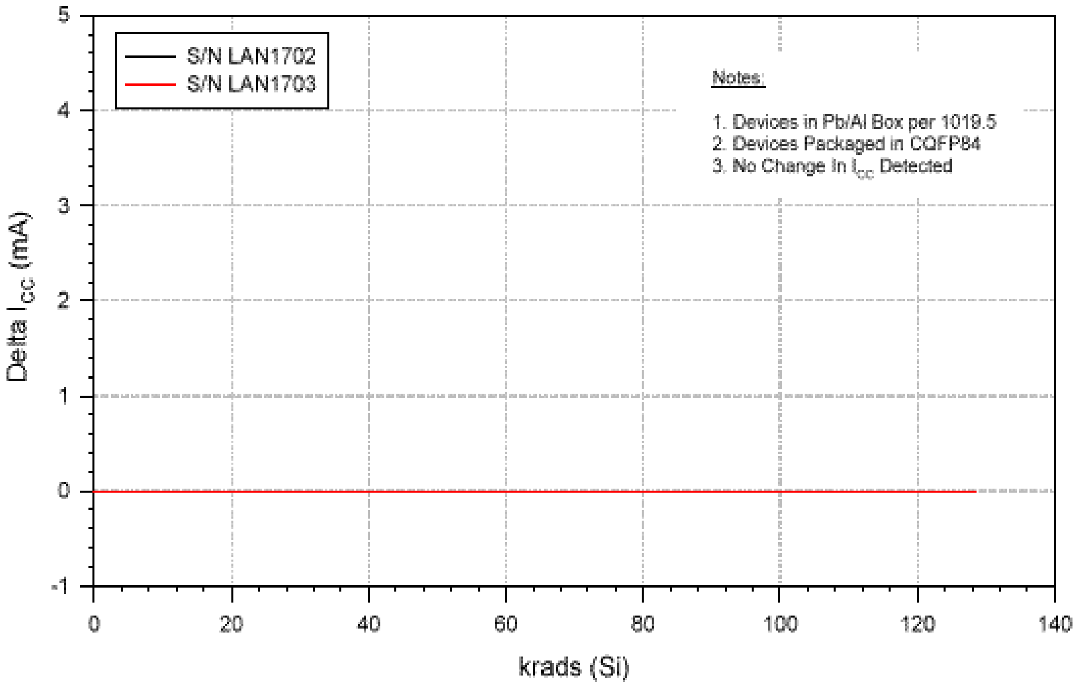


Figure 2. Delta $I_{DDstandby}$ versus total cumulative dose

3.3 INPUT LOGIC THRESHOLD

The testing result of the input logic threshold (V_{IL}/V_{IH}) is listed in Table 5.

Table 5. Input Logic (V_{IL}/V_{IH}) Threshold (Volts)

	Pre-Irradiation	Post-100krad(Si) Irradiation
Cntl (LAN1705)	1.71	1.74
LAN1701	1.72	1.72
LAN1702	1.71	1.71
LAN1703	1.72	1.64
LAN1704	1.72	1.64

3.4 OUTPUT I-V CHARACTERISTICS

Figures 3 and 4 display the radiation effects on output (V_{OL}/ V_{OH}) characteristics (I-V curves). Only the post 100 krad(Si) data are shown with the control data. There are no radiation effects on these characteristics.

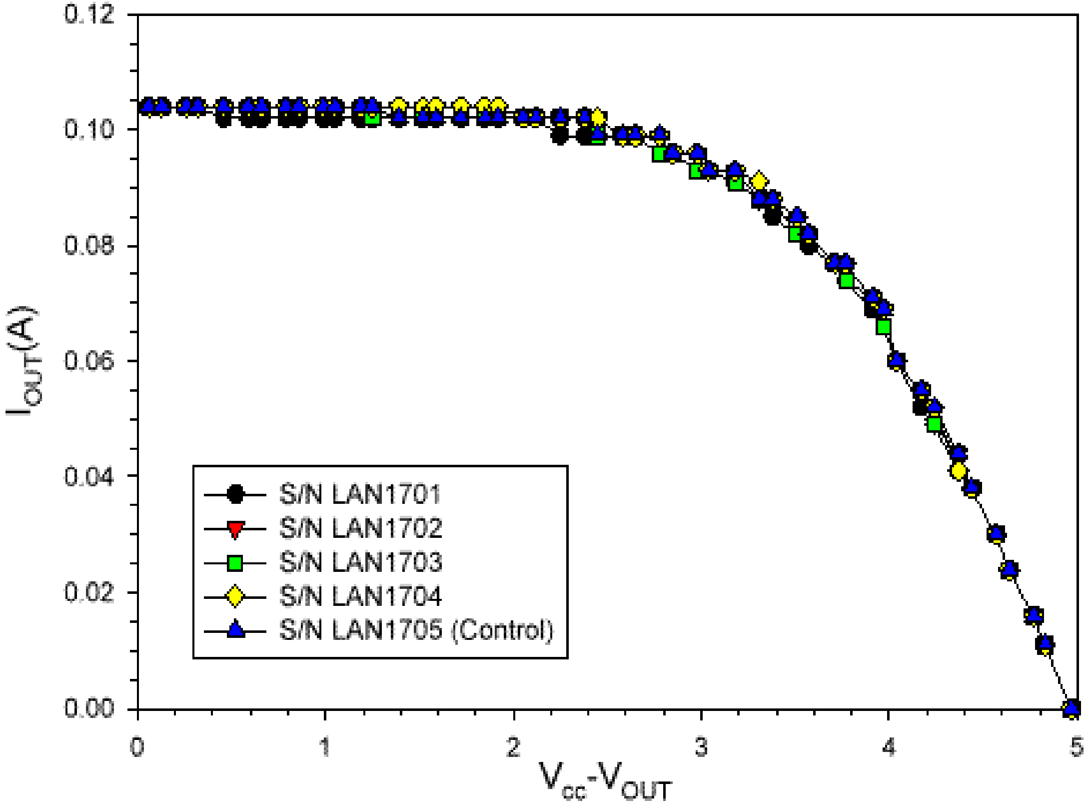


Figure 3. Post 100 krad(Si) irradiation V_{OL} I-V

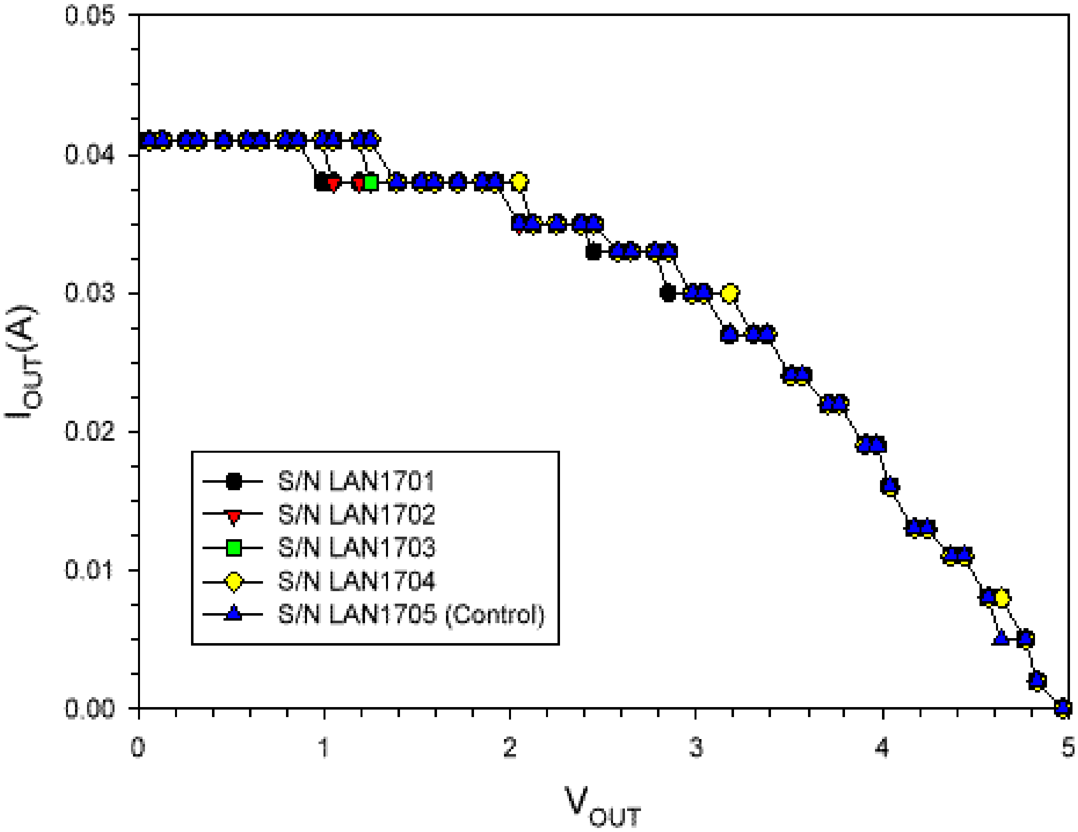


Figure 4. Post-100 krad(Si) irradiation V_{OH} I-V

3.5 PROPAGATION DELAYS

Rising and falling edge delays are shown in Table 6 and 7 respectively.

Table 6. Rising Edge Propagation Delays (ns)

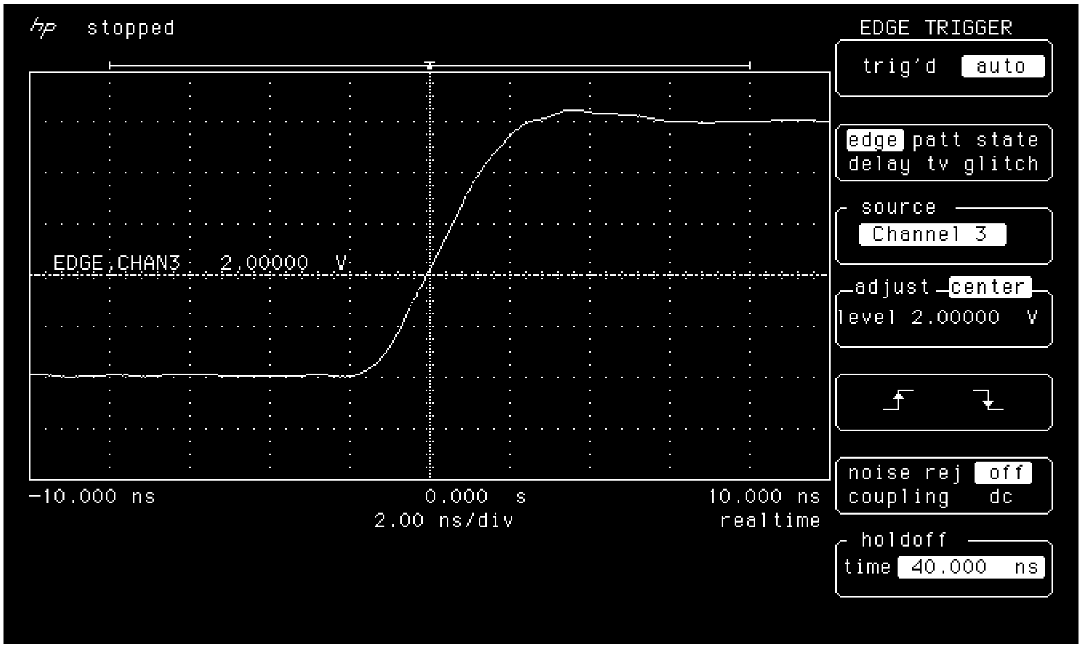
	Pre-Irradiation	Post-100krad(Si) Irradiation
Cntl (LAN1705)	260	259
LAN1701	269	265
LAN1702	261	259
LAN1703	264	262
LAN1704	261	259

Table 7. Falling Edge Propagation Delays (ns)

	Pre-Irradiation	Post-100krad(Si) Irradiation
Cntl (LAN1705)	232	232
LAN1701	235	241
LAN1702	231	238
LAN1703	230	236
LAN1704	229	235

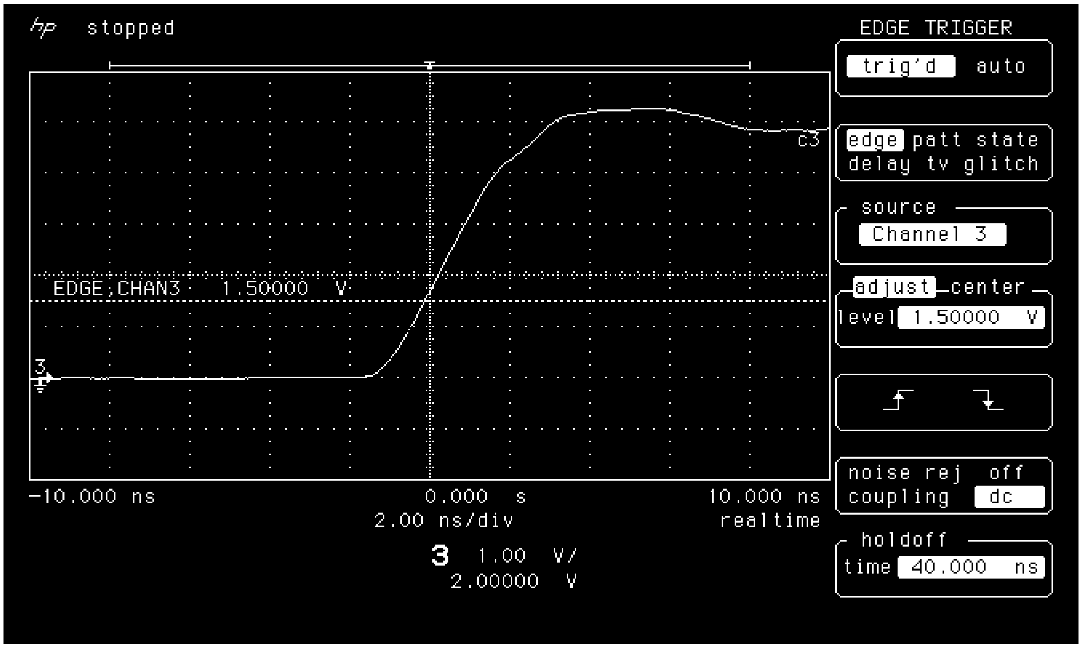
3.6 RISING/FALLING EDGE TRANSIENT

The 100 krad(Si) total dose effects on the rising and falling edge transient characteristics were measured on a D flip-flop. Figures 5-8 show the rising edge of the DUTs. Figures 9-12 show the falling edge. No significant radiation effects can be detected in any case.



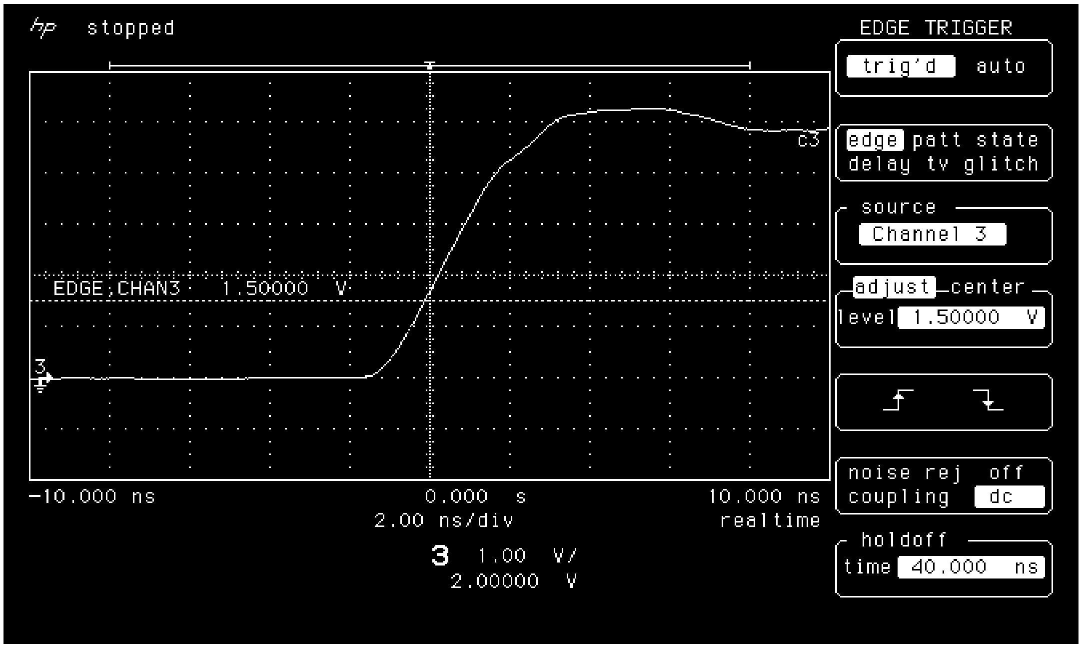
trig'd auto
source Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff time 40.000 ns

Figure 5a. Rising edge of LAN1701 pre-irradiation



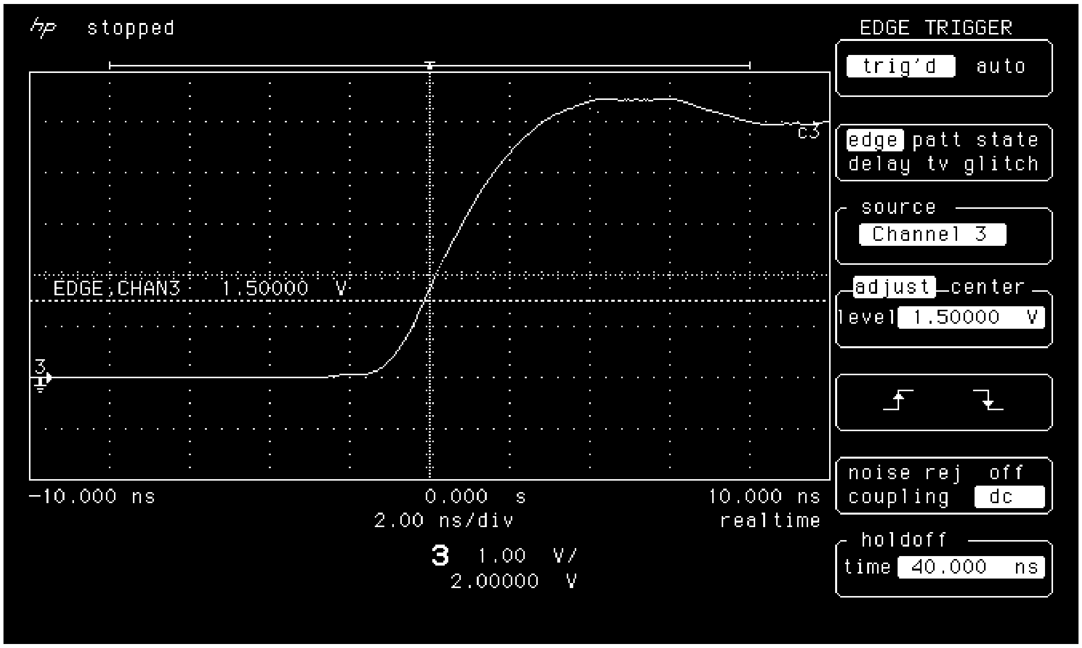
3 1.00 V/
2.00000 V
trig'd auto
source Channel 3
adjust center
level 1.50000 V
noise rej off
coupling dc
holdoff time 40.000 ns

Figure 5b. Rising edge of LAN1701 post-100 krad(Si) irradiation



source Channel 3
EDGE;CHAN3 1.50000 V
level 1.50000 V
noise rej off
coupling dc
holdoff time 40.000 ns
-10.000 ns 0.000 s 10.000 ns
2.00 ns/div realtime
3 1.00 V/
2.00000 V

Figure 6a. Rising edge of LAN1702 pre-irradiation



source Channel 3
EDGE;CHAN3 1.50000 V
level 1.50000 V
noise rej off
coupling dc
holdoff time 40.000 ns
-10.000 ns 0.000 s 10.000 ns
2.00 ns/div realtime
3 1.00 V/
2.00000 V

Figure 6b. Rising edge of LAN1702 post 100 krad(Si) irradiation

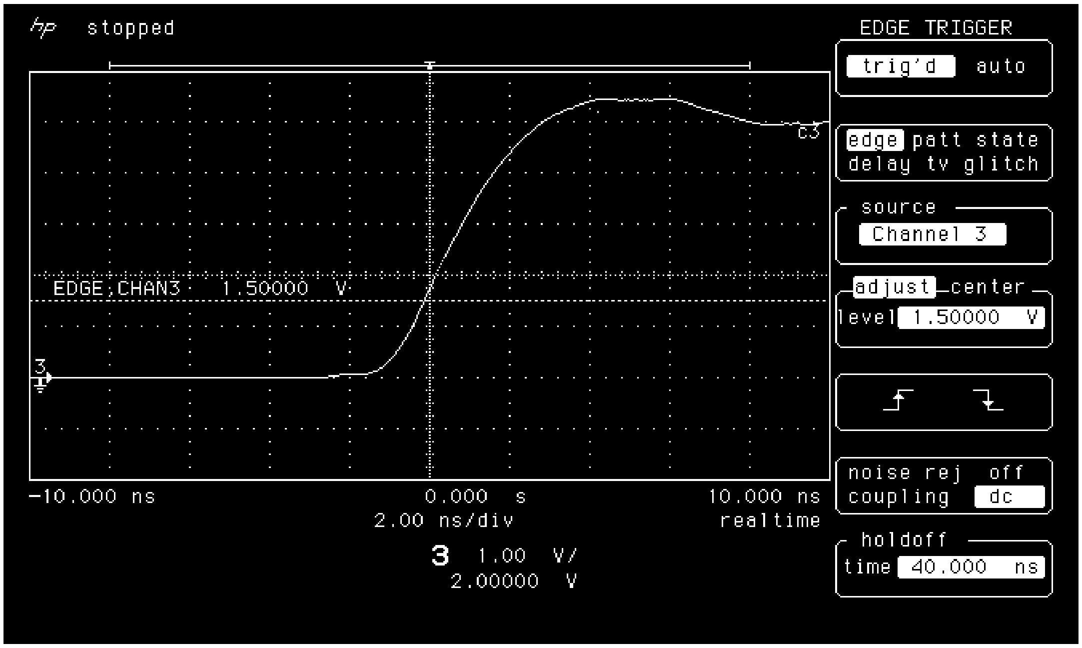

hp stopped
EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source
Channel 3
adjust center
level 1.50000 V
noise rej off
coupling dc
holdoff
time 40.000 ns
EDGE;CHAN3: 1.50000 V
-10.000 ns
0.000 s
10.000 ns
2.00 ns/div
realtime
3 1.00 V/
2.00000 V

Figure 7a. Rising edge of LAN1703 pre-irradiation

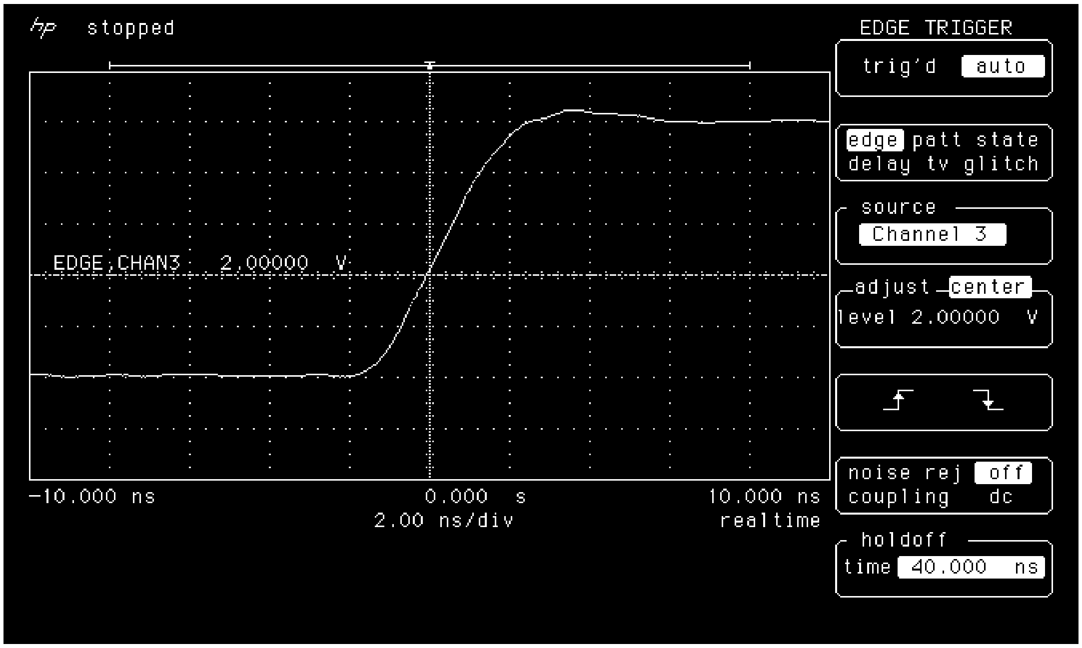
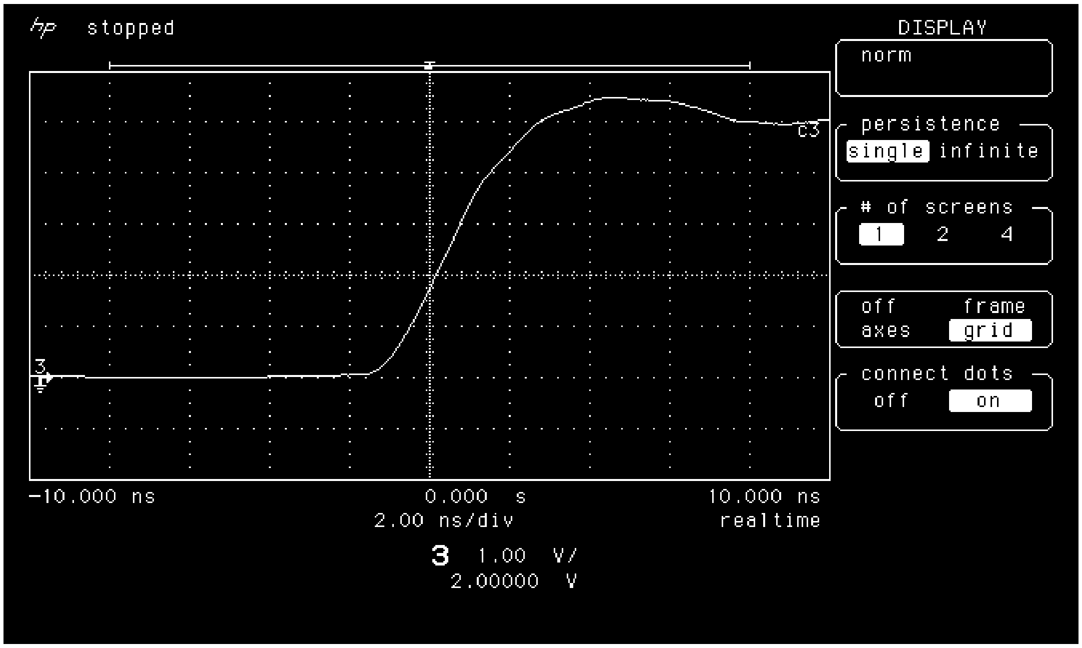
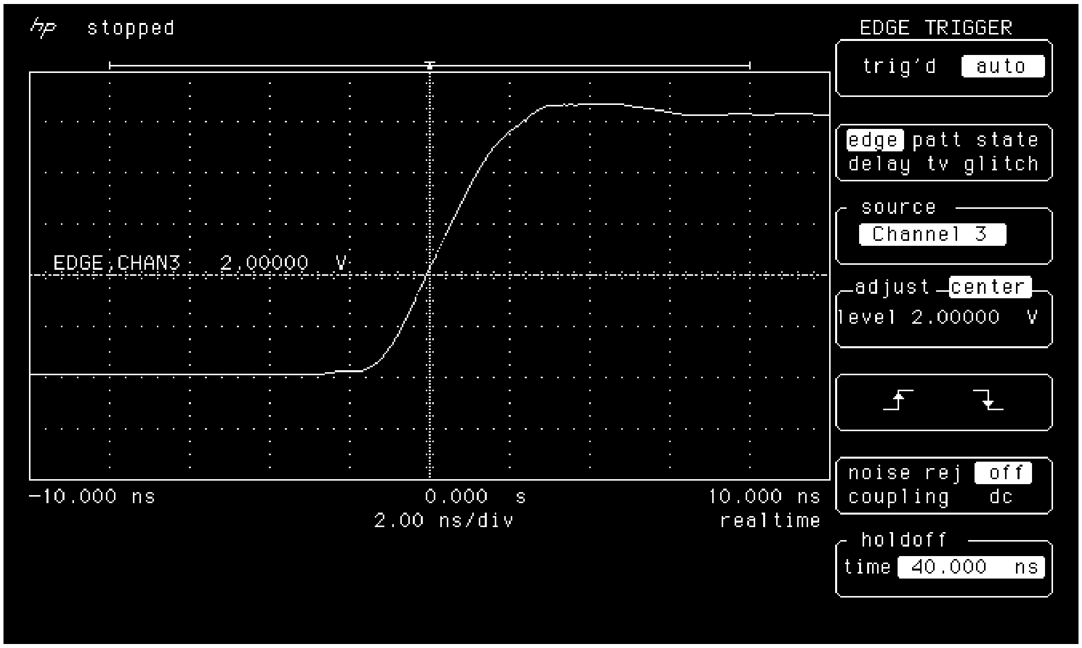

hp stopped
EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source
Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns
EDGE;CHAN3: 2.00000 V
-10.000 ns
0.000 s
10.000 ns
2.00 ns/div
realtime

Figure 7b. Rising edge of LAN1703 post 100 krad(Si) irradiation



DISPLAY
norm
persistence single infinite
# of screens 1 2 4
off frame
axes grid
connect dots off on

Figure 8a. Rising edge of LAN1704 pre-irradiation



EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns

Figure 8b. Rising edge of LAN1704 post-100 krad(Si) irradiation

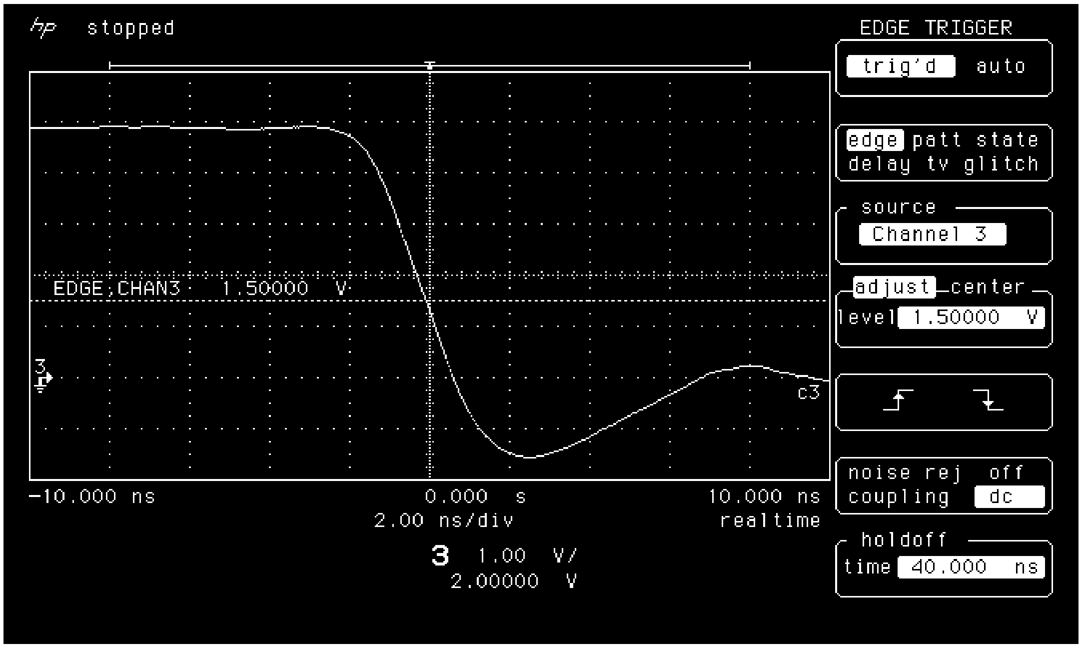


Figure 9a. Falling edge of LAN1701 pre-irradiation

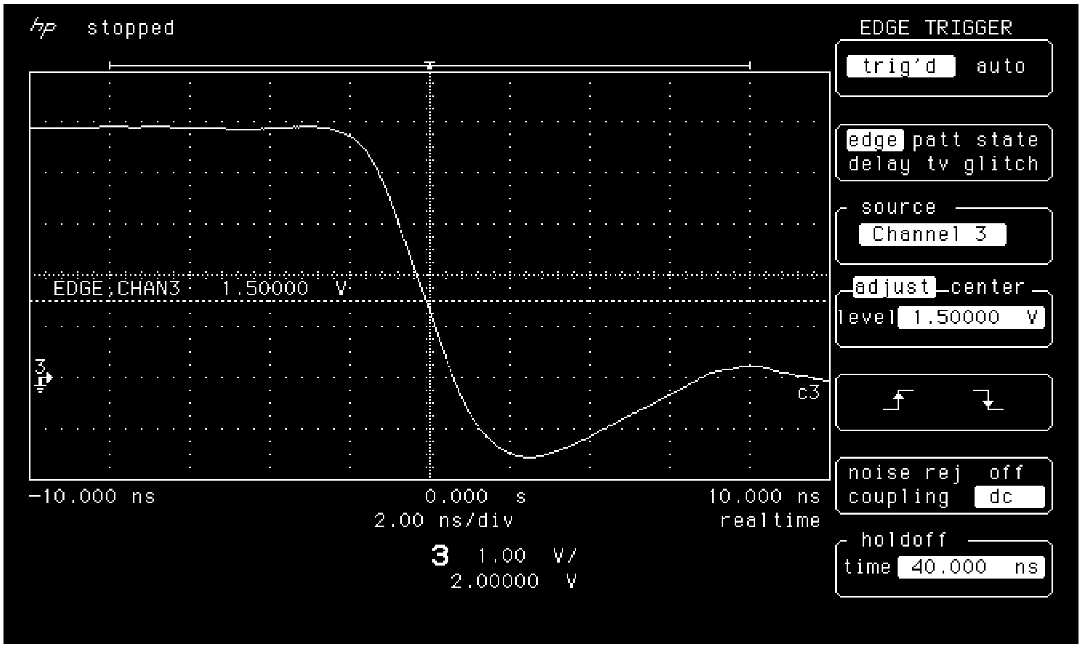
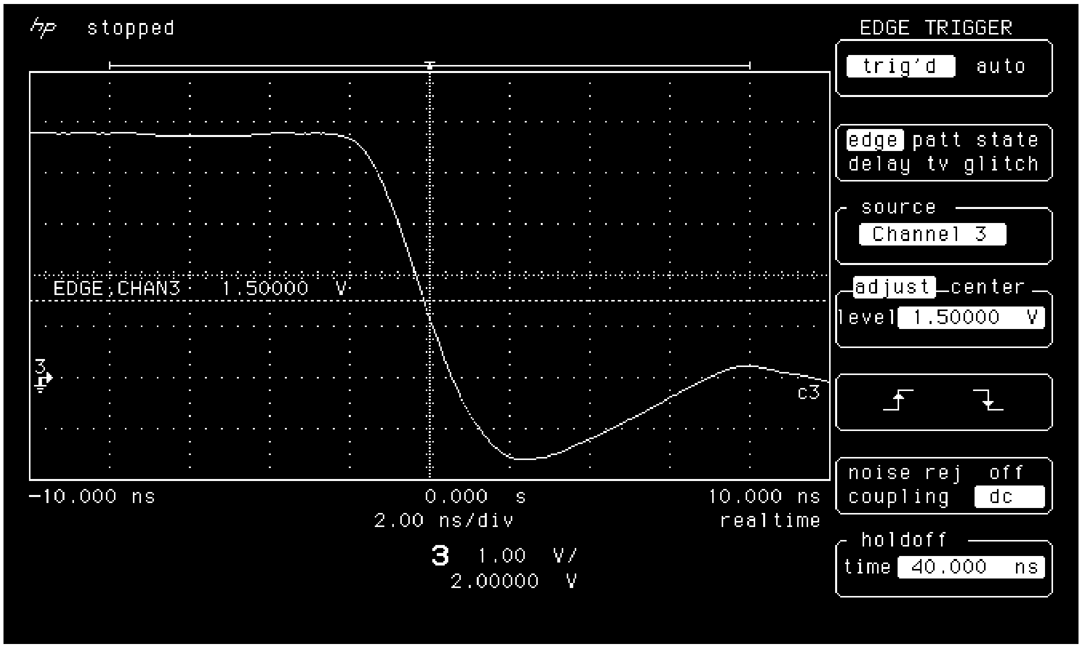


Figure 9b. Falling edge of LAN1701 post-100 krad(Si) irradiation



source Channel 3

level 1.50000 V

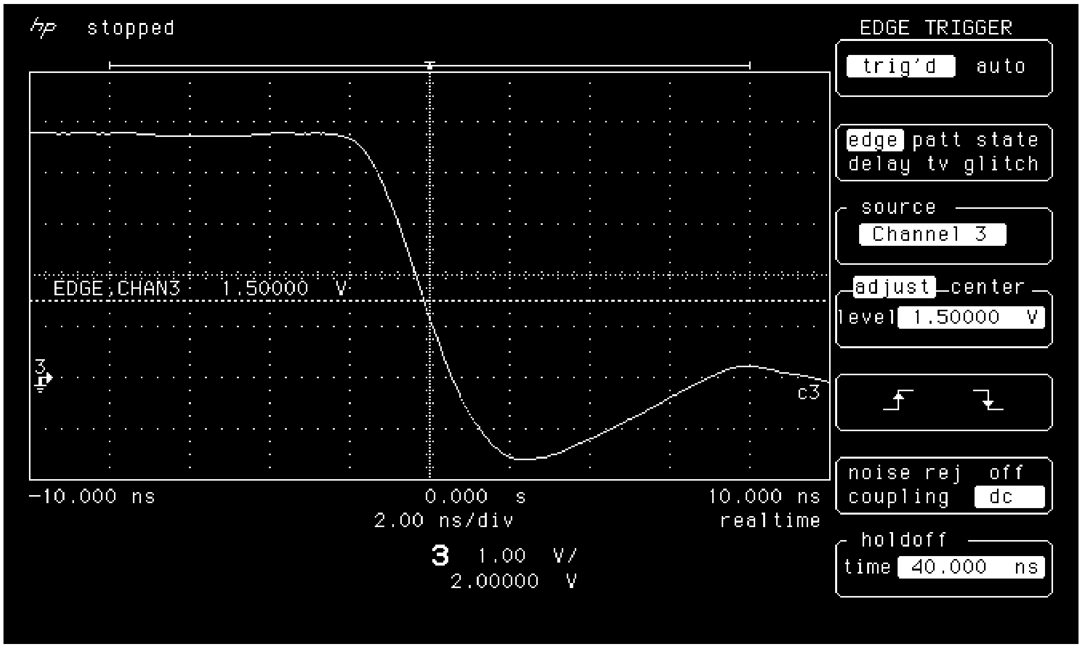
coupling dc

holdoff time 40.000 ns

2.00 ns/div

3 1.00 V/
2.00000 V

Figure 10a. Falling edge of LAN1702 pre-irradiation



source Channel 3

level 1.50000 V

coupling dc

holdoff time 40.000 ns

2.00 ns/div

3 1.00 V/
2.00000 V

Figure 10b. Falling edge of LAN1702 post-100 krad(Si) irradiation

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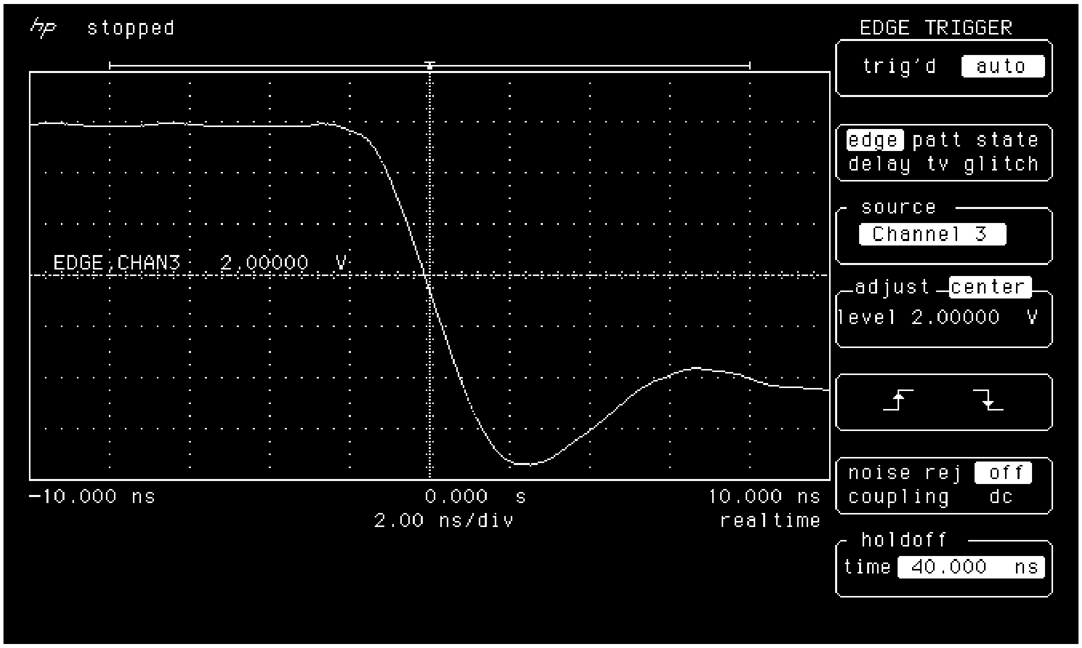

stopped
EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns
EDGE,CHAN3: 2.00000 V
-10.000 ns
0.000 s
10.000 ns
2.00 ns/div
realtime

Figure 11a. Falling edge of LAN1703 pre-irradiation

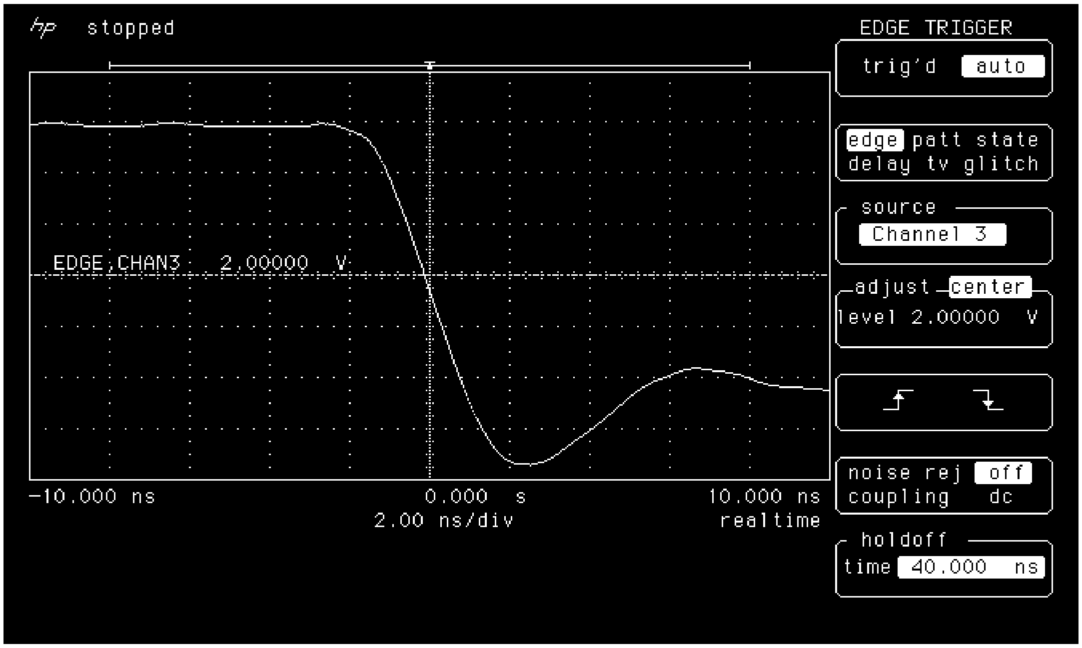
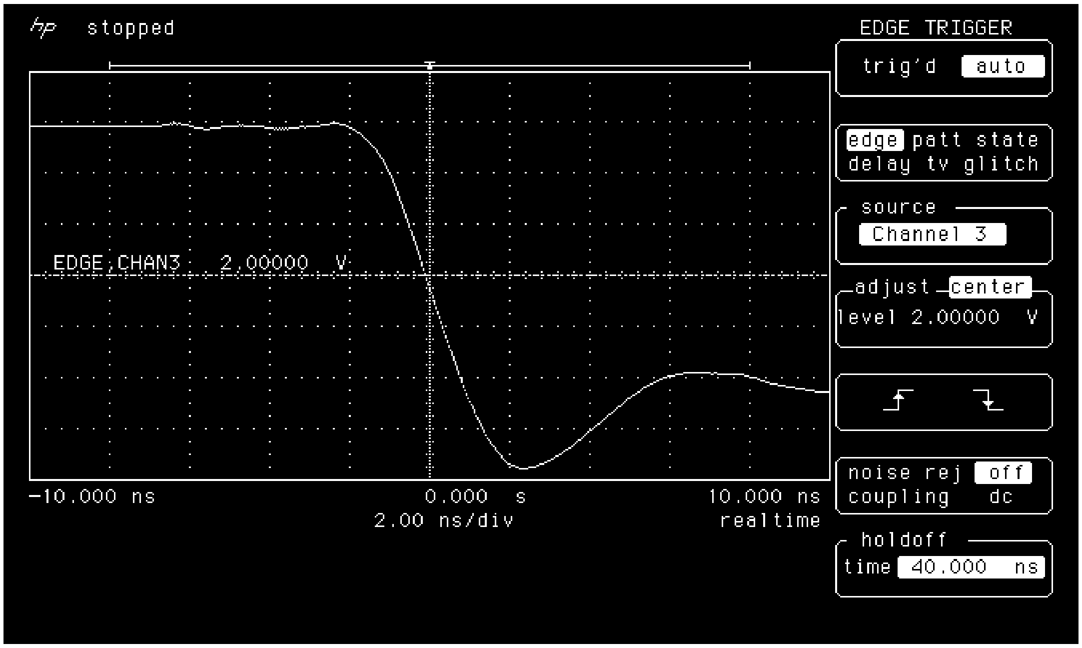

stopped
EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns
EDGE,CHAN3: 2.00000 V
-10.000 ns
0.000 s
10.000 ns
2.00 ns/div
realtime

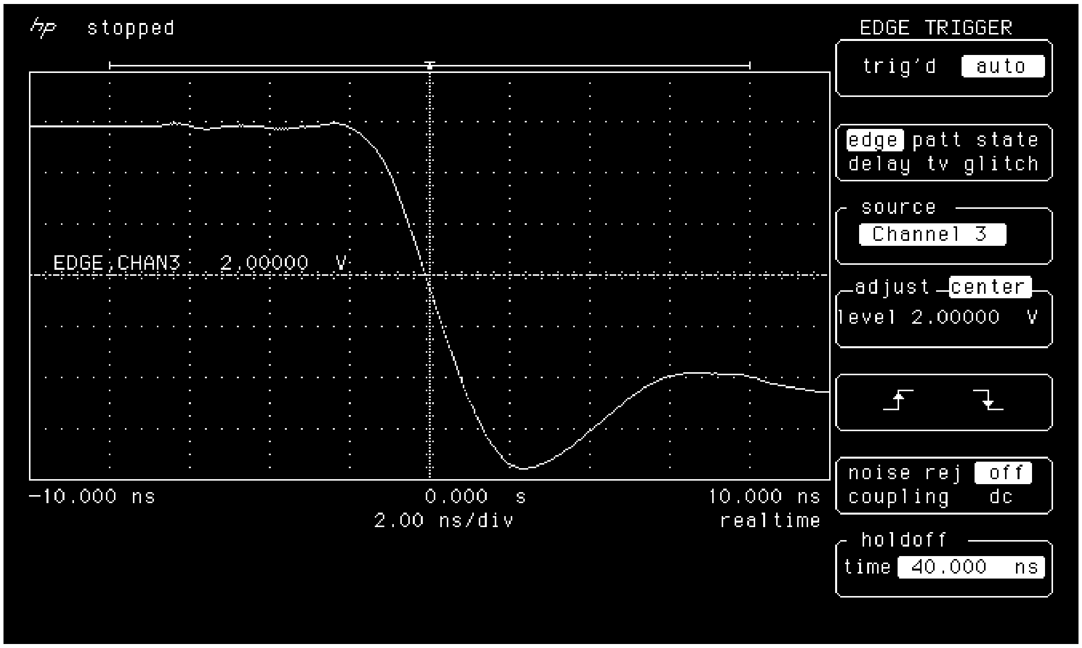
Figure 11b. Falling edge of LAN1703 post-100 krad(Si) irradiation



stopped

EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source
Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns

Figure 12a. Falling edge of LAN1704 pre-irradiation.



stopped

EDGE TRIGGER
trig'd auto
edge patt state
delay tv glitch
source
Channel 3
adjust center
level 2.00000 V
noise rej off
coupling dc
holdoff
time 40.000 ns

Figure 12b. Falling edge of LAN1704 post-100 krad(Si) irradiation

3.7 POWER-ON TRANSIENT CURRENT

The power-on transient characteristics with respect to final total irradiation dose were measured. Figures 13-16 show the oscilloscope captures of power-on voltage and the current of pre-, post-100 krad(Si) irradiation of the DUTs. Note that in these Figures, C1 is the voltage, and C2 the current. The scale for current (C2) is always 100 mA/division. The results show that 100 krad(Si) irradiation at the dose rate of 12.95 krad(Si)/min didn't induce significant transient current in any case.

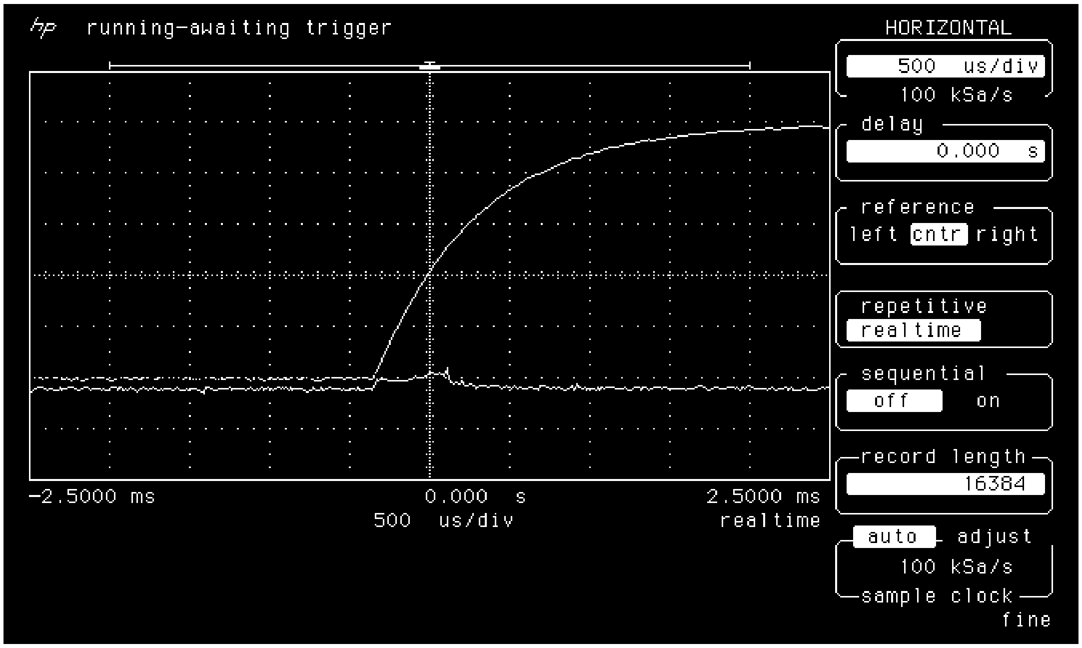


Figure 13a. Power-on transient current of LAN1701 pre-irradiation

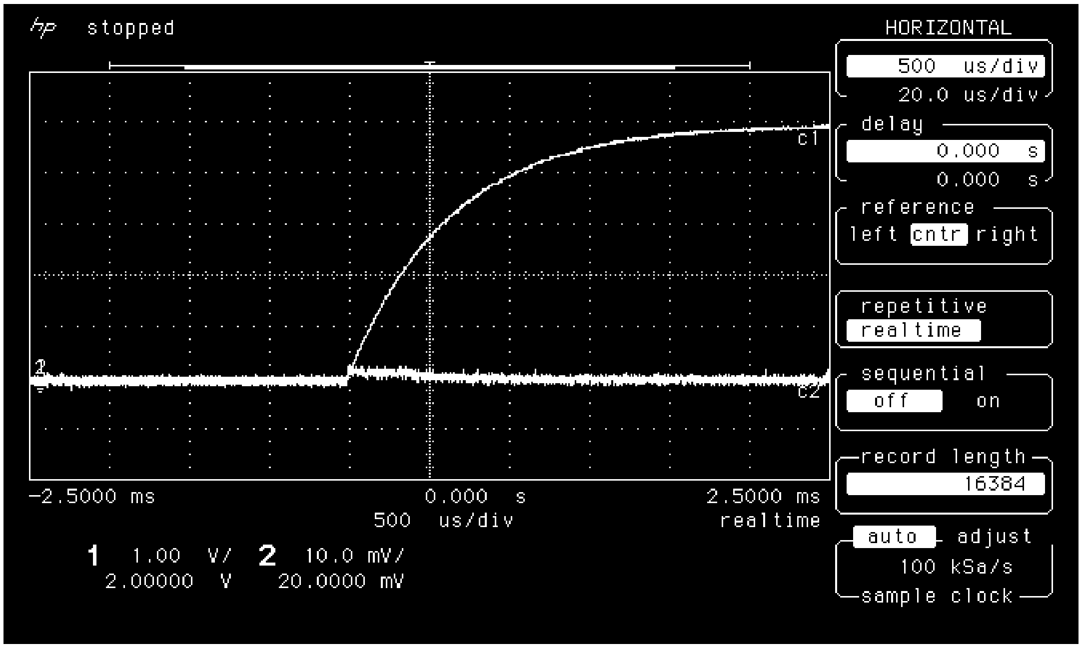
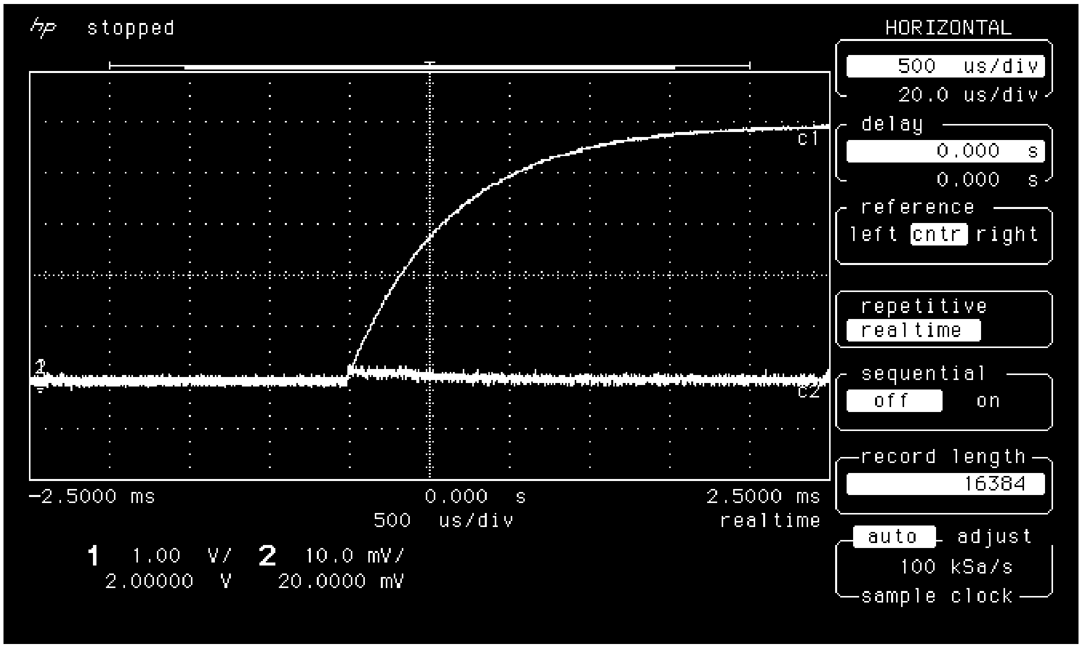


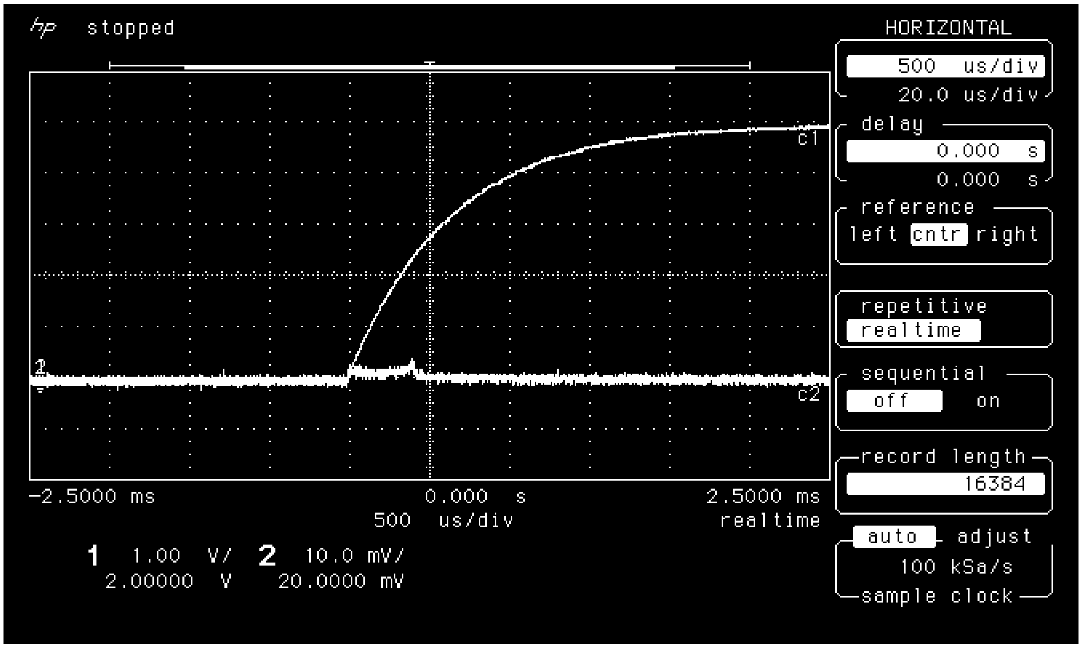
Figure 13b. Power-on transient current of LAN1701 post-100 krad(Si) irradiation


stopped

HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock

-2.5000 ms
0.000 s
500 us/div
2.5000 ms
realtime
1 1.00 V/ 2 10.0 mV/
2.00000 V 20.0000 mV

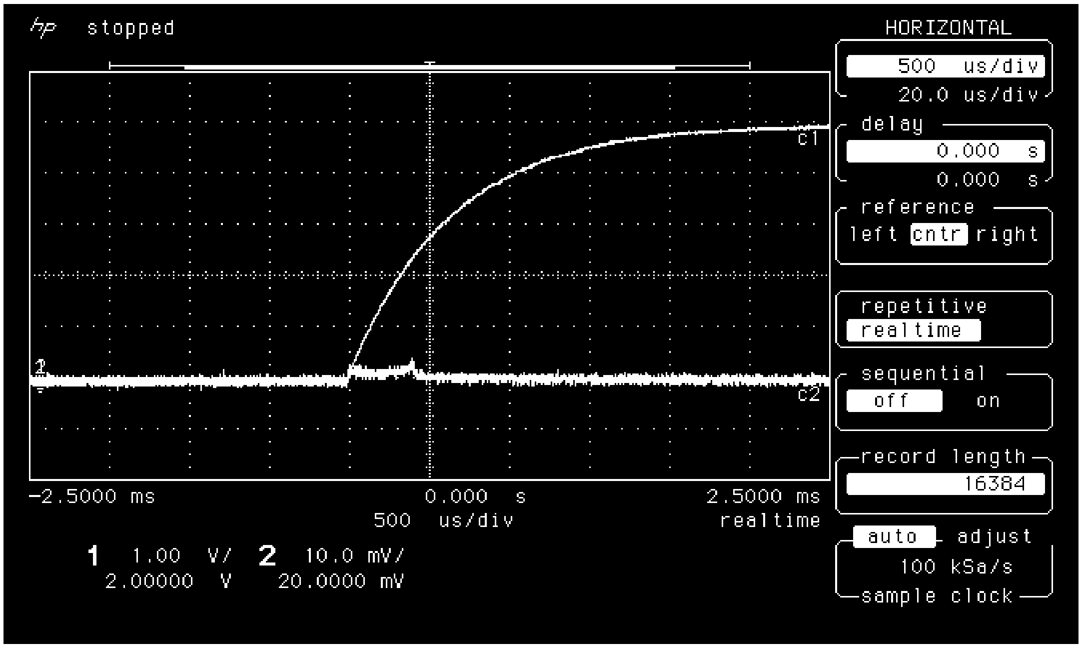
Figure 14a. Power-on transient current of LAN1702 pre-irradiation


stopped

HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock

-2.5000 ms
0.000 s
500 us/div
2.5000 ms
realtime
1 1.00 V/ 2 10.0 mV/
2.00000 V 20.0000 mV

Figure 14b. Power-on transient current of LAN1702 post-100 krad(Si) irradiation

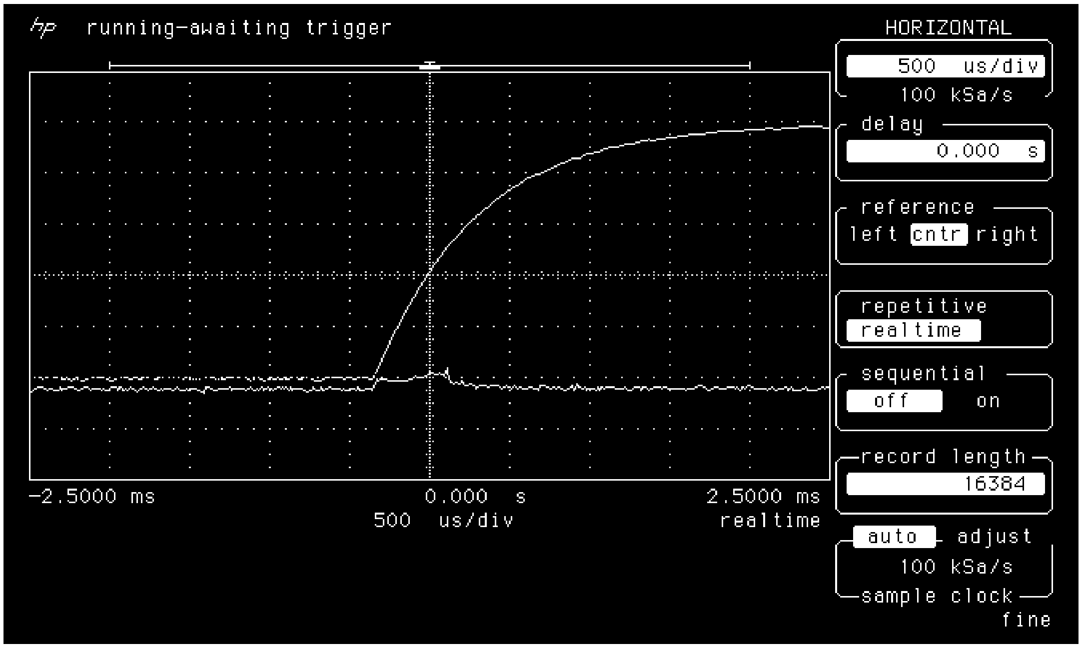

stopped

HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock

-2.5000 ms
0.000 s
500 us/div
2.5000 ms
realtime

1 1.00 V/ 2 10.0 mV/
2.00000 V 20.0000 mV

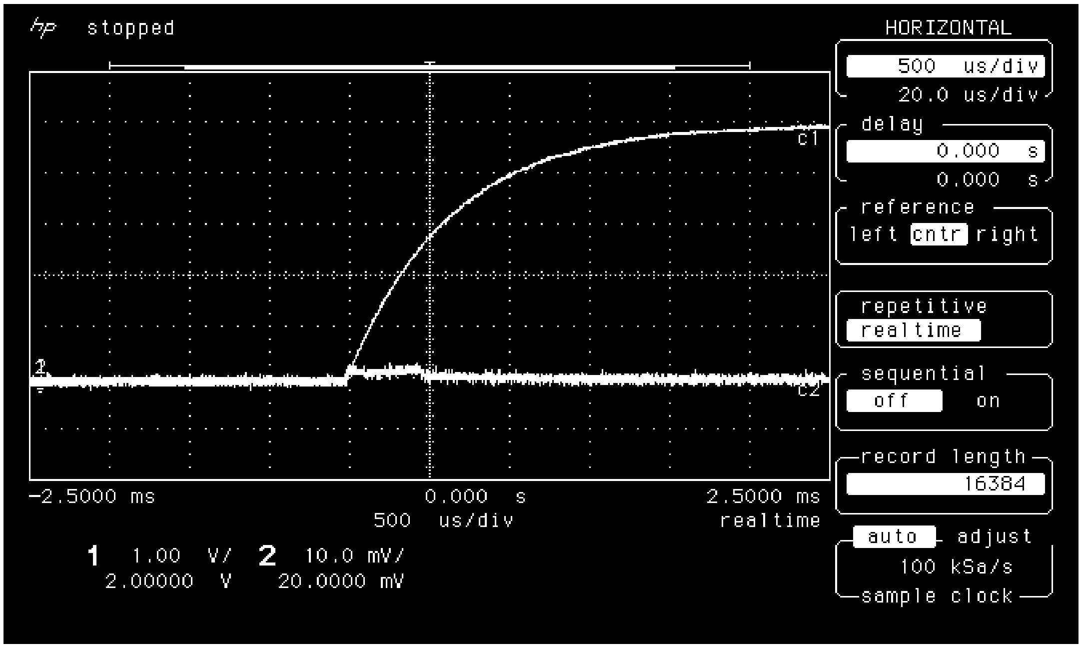
Figure 15a. Power-on transient current of LAN1703 pre-irradiation


running-awaiting trigger

HORIZONTAL
500 us/div
100 kSa/s
delay 0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock
fine

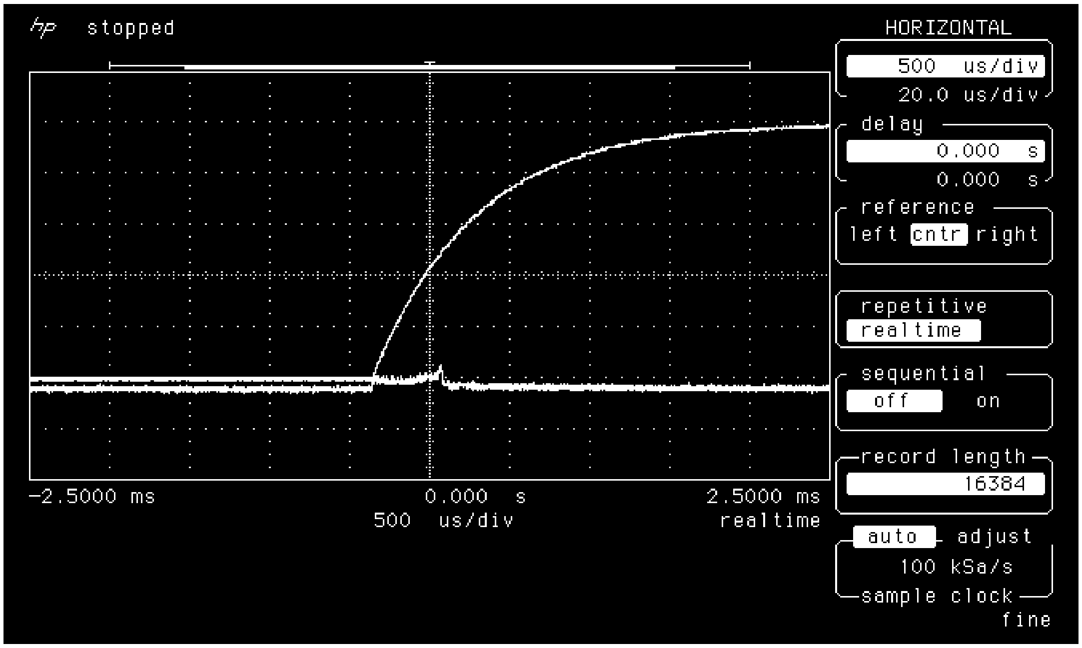
-2.5000 ms
0.000 s
500 us/div
2.5000 ms
realtime

Figure 15b. Power-on transient current of LAN1703 post-100 krad(Si) irradiation



HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock
1 1.00 V/ 2 10.0 mV/
2.00000 V 20.0000 mV

Figure 16a. Power-on transient current of LAN1704 pre-irradiation



HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 16384
auto adjust
100 kSa/s
sample clock
fine

Figure 16b. Power-on transient current of LAN1704 post-100 krad(Si) irradiation