June 8, 1999

TOTAL IONIZATION DOSE TEST REPORT

No. 99T-RT54SX16-P05
J. J. Wang
(408)522-4576
jih-jong.wang@actel.com

1.0 SUMMARY TABLE

RT54SX16A Parameters/Characteristics	Results
1. Functionality	Passed 100 krad(Si)
2. $I_{DDSTDBY}$	Passed 75 krad(Si) (< 6 mA) (see Figure 2)
3. V_{IL}/V_{IH}	Passed 75 krad(Si) (see Table 5)
4. V_{OL}/V_{OH}	Passed 75 krad(Si) (see Figures 3-8)
5. Propagation Delays	Passed 75 krad(Si) (see Table 6,7)
6. Rising/Falling Edge Transient	Passed 75 krad(Si) (see Figures 9-18)
7. Power-on Transient Current	Passed 75 krad(Si) (see Figures 19-22)

2.0 TID TEST

This section describes the device under test (DUT), the irradiation parameters, and the testing method.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1

Part Number	RT54SX16
Package	PQ208
Foundry	MEC
Technology	0.5 µm CMOS
Die Lot Number	P05
Date Code	9849
Quantity Tested	6
Serial Numbers	Control, LAN1221, LAN1222, LAN1231, LAN1232, LAN1233

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2

Facility	NASA
Radiation Source	Co-60
Dose Rate	18.65 krad(Si)/day (+-10%)
Final Total Dose for DC/AC Parameter Measurement	75 krad(Si)
Temperature	Room
Bias	3.3 V/5.0 V

2.3 TESTING METHOD

The testing method is following the spirit of TM1019 and targets for the low-dose-rate space applications. Figure 1 shows the flow.

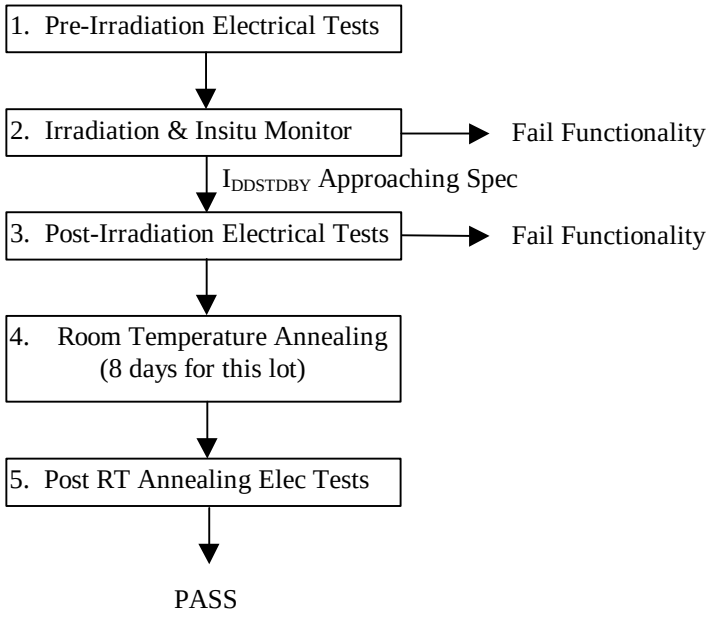

Figure 1. Test method flow-chart

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on bench with relative low noise. The corresponding logic design circuits are listed in Table 3.

Table 3

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power line
3. V_{IL}/V_{IH}	EI_1, EL_1
4. V_{OL}/V_{OH}	EI_1, EL_1
5. Propagation Delays	E25_1, E1, E12, E16, E12, E17
6. Rising/Falling Edge	E1
7. Power-on Transient	DUT power line

3.0 TEST RESULTS

This section presents all the parameters/characteristics testing results for pre-irradiation (step 1 in Figure 1), post-irradiation (step 3), and post room temperature annealing tests (step 5).

3.1 FUNCTIONAL TEST

Two types of functionality tests were performed. Samples (two in this lot) were irradiated until functional failure occurred to determine the functionality tolerance in the summary table. The second type is including in the

testing flow (Figure 1). Each test step (step 1, 3, 5) has a functional test by default. Table 4 lists the second testing results of all six DUTs.

Table 4. Functionality Test

	Pre-Irradiation	Post-Irradiation	RT Anneal
Control	passed	passed	passed
LAN1221	passed	passed	passed
LAN1222	passed	passed	passed
LAN1231	passed	passed	passed
LAN1232	passed	passed	passed
LAN1233	passed	passed	passed

3.2 IDDSTANDBY

$I_{DDstandby}$ and functionality of four pins were monitored during the irradiation period. Because the board had a measurable leakage, only the delta $I_{DDstandby}$ due to radiation was recorded. Using delta $I_{DDdstandby}$, won't create any significant extraneous error since the pre-irradiation value of $I_{DDstandby}$ is under 1 mA. The increment of $I_{DDstandby}$ by irradiation determines the tolerance.

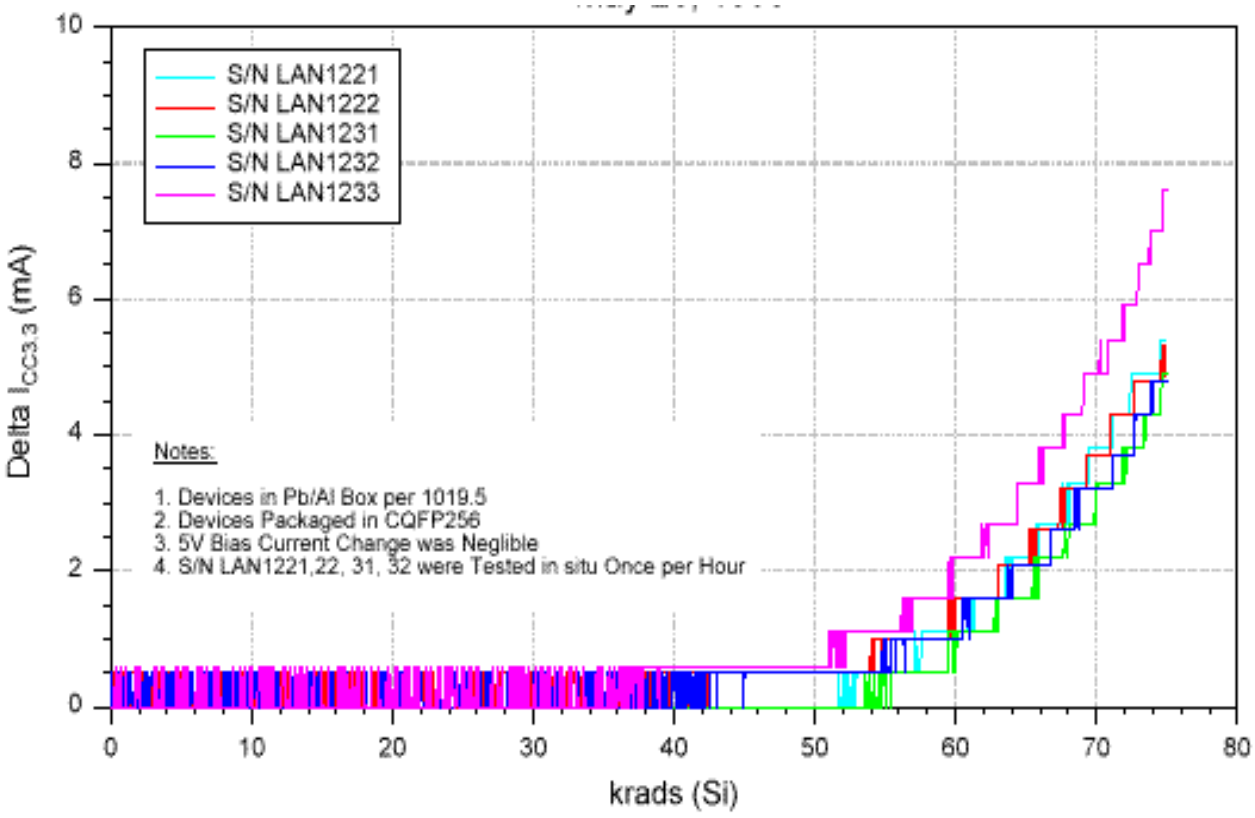

Figure 2. Delta $I_{DDstandby}$ versus total cumulative dose

3.3 INPUT LOGIC THRESHOLD

The testing result of the input logic threshold (V_{IL}/V_{IH}) is listed in Table 5.

Table 5 Input Logic (V_{IL}/V_{IH}) Threshold (Volts)

	Pre-Irradiation	Post-Irradiation	RT Anneal
Control	1.45	1.40	NA
LAN1221	1.42	1.40	1.36
LAN1222	1.40	1.40	1.33
LAN1231	1.39	1.35	1.36
LAN1232	1.39	1.35	1.37
LAN1233	1.40	1.37	1.37

3.4 OUTPUT I-V CHARACTERISTICS

Figures 3-8 display the radiation effects on output (V_{OL}/ V_{OH}) characteristics (I-V curves).

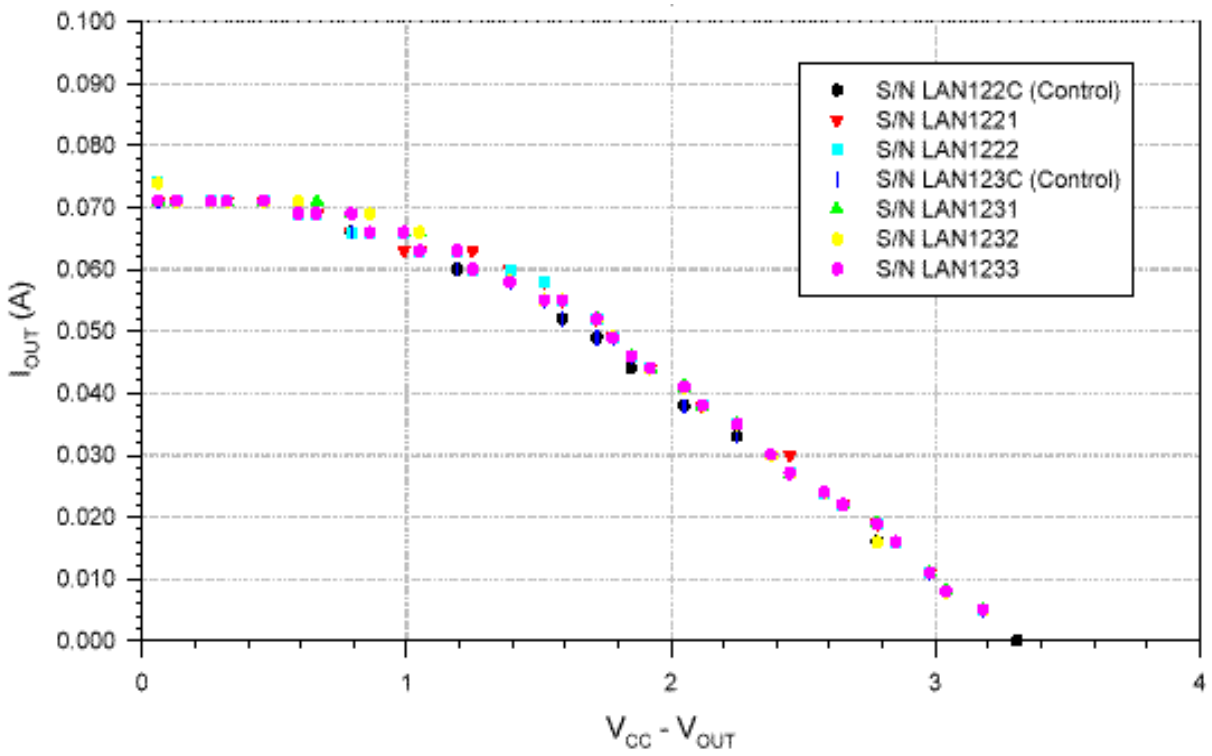

Figure 3 Pre-irradiation V_{OL} I-V

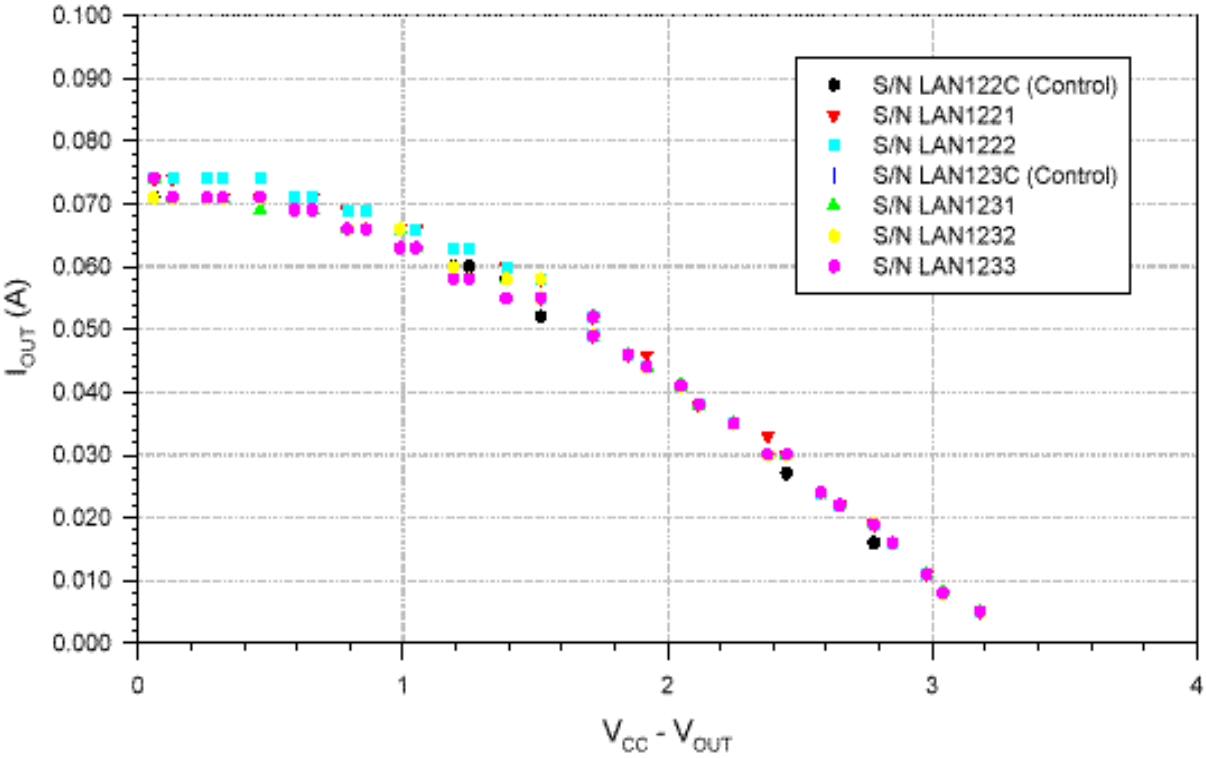

Figure 4 Post-75 krad(Si) irradiation V_{OL} I-V

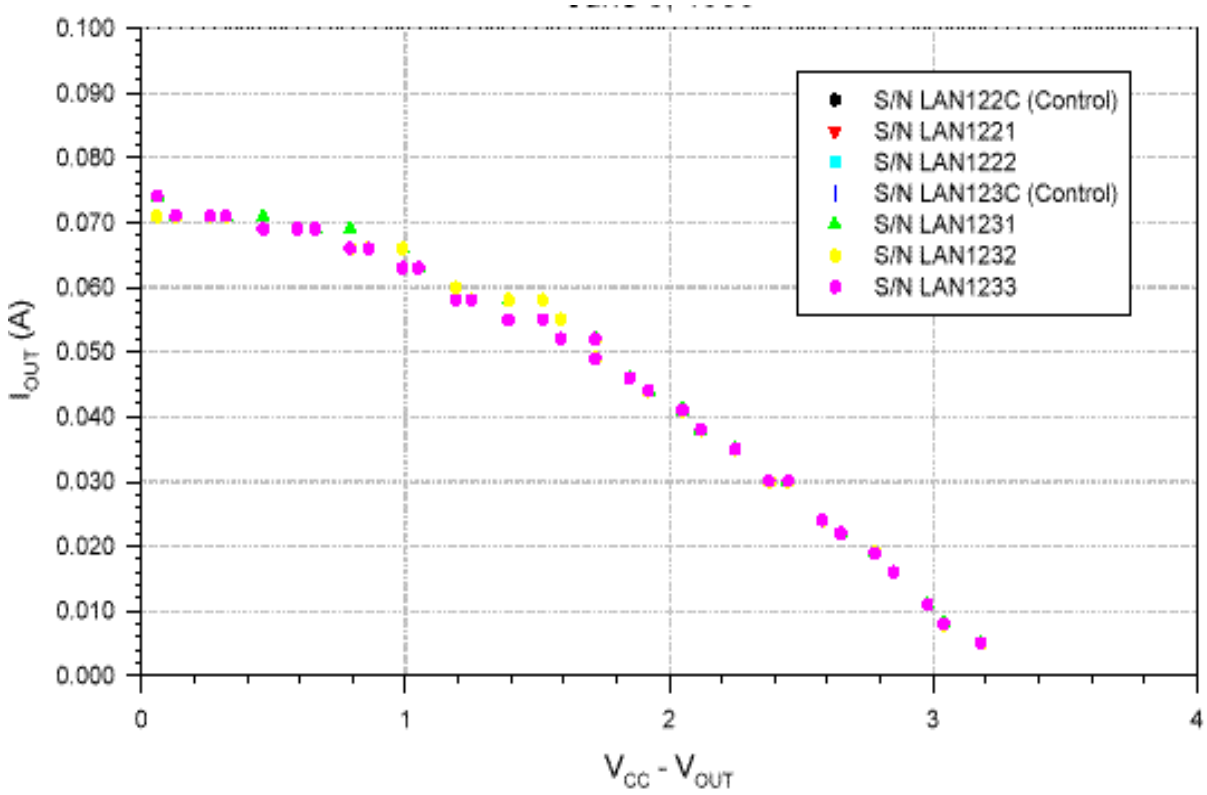

Figure 5 Post-room-temperature annealing V_{OL} I-V

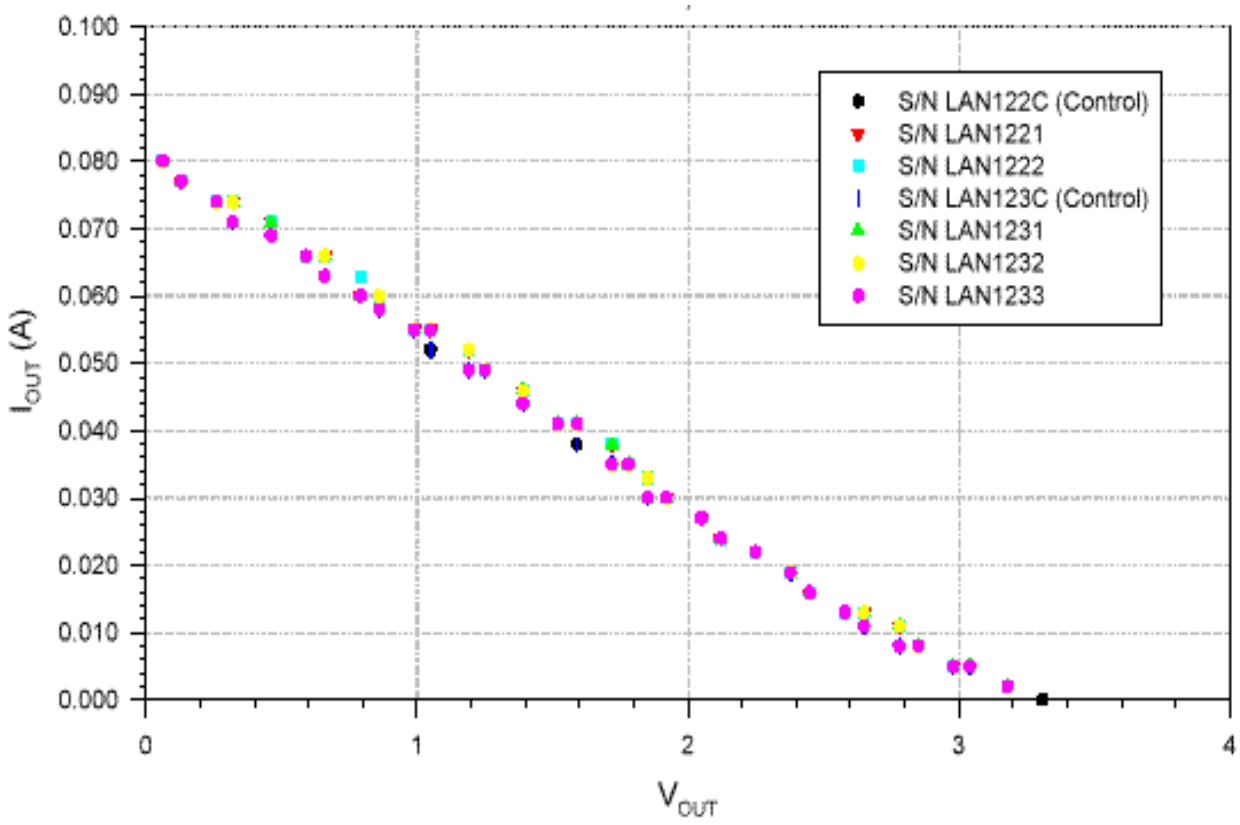

Figure 6 Pre-irradiation V_{OH} I-V

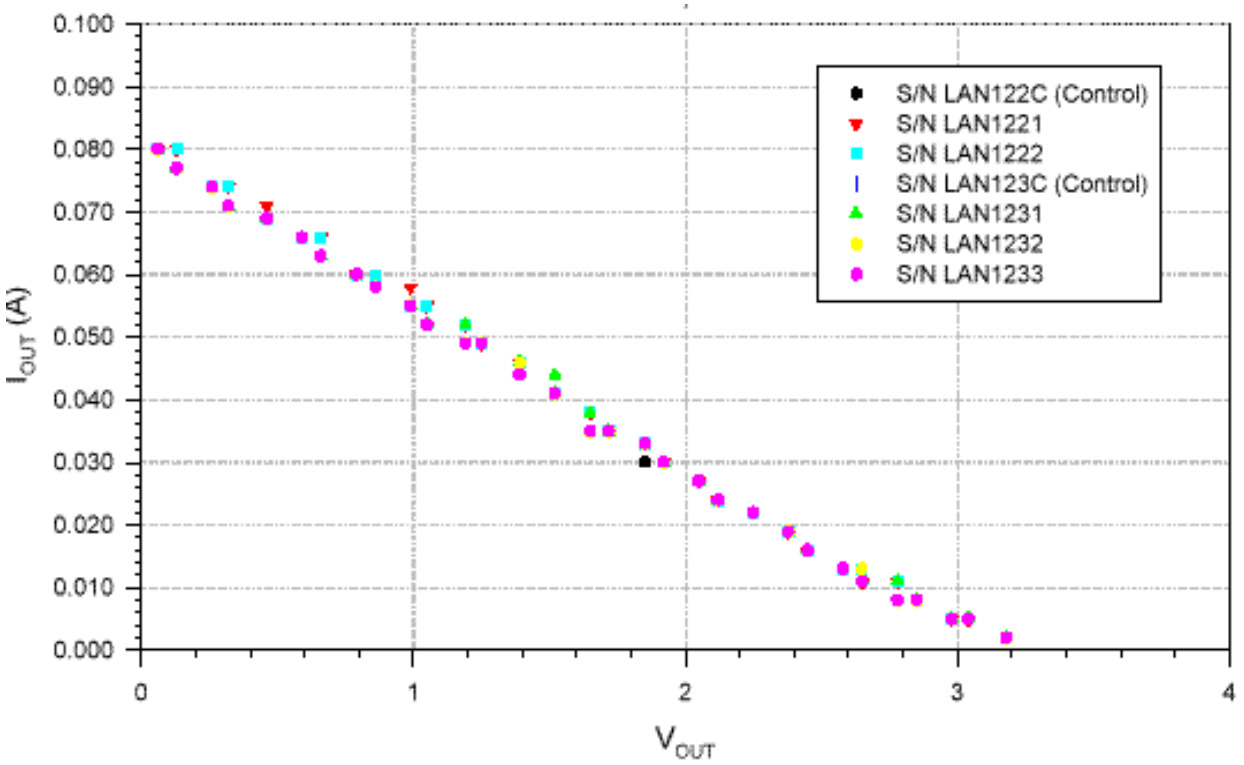

Figure 7 Post-75 krad(Si) irradiation V_{OH} I-V

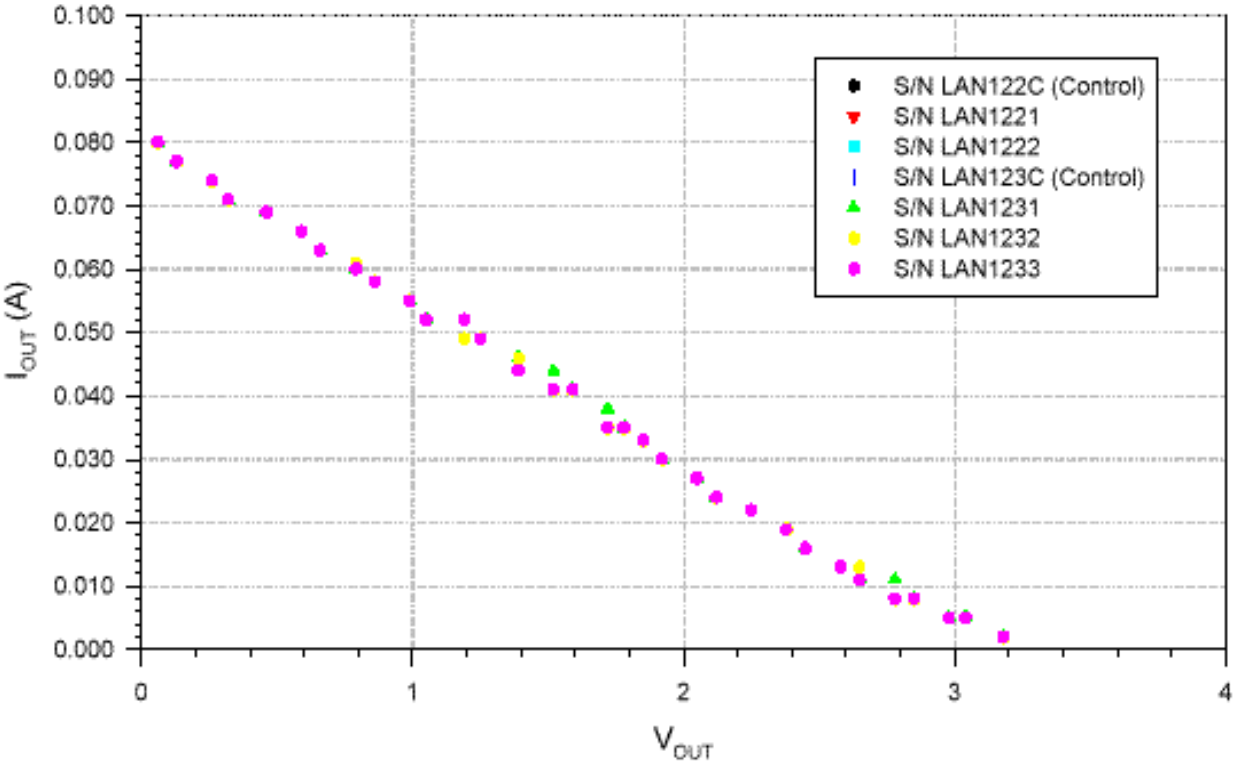

Figure 8 Post-room-temperature annealing V_{OH} I-V

3.5 PROPAGATION DELAYS

Rising and falling edge delays are shown in Table 6 and 7 respectively.

Table 6. Rising Edge Propagation Delays (μs)

	Pre-Irradiation	Post-Irradiation	RT Anneal
Control	667	665	NA
LAN1221	720	712	713
LAN1222	713	701	705
LAN1231	708	703	716
LAN1232	724	720	734
LAN1233	723	719	731

Table 7. Falling Edge Propagation Delays (μs)

	Pre-Irradiation	Post-Irradiation	RT Anneal
Control	663	661	NA
LAN1221	717	717	713
LAN1222	710	707	705
LAN1231	704	691	706
LAN1232	721	707	723
LAN1233	719	706	720

3.6 RISING/FALLING EDGE TRANSIENT

The 75 krad(Si) total dose effects on the rising and falling edge transient characteristics were measured on a D flip-flop. Figures 9-13 show the rising edge of the DUTs. Figures 14-18 show the falling edge. No significant radiation effects can be detected in any case.

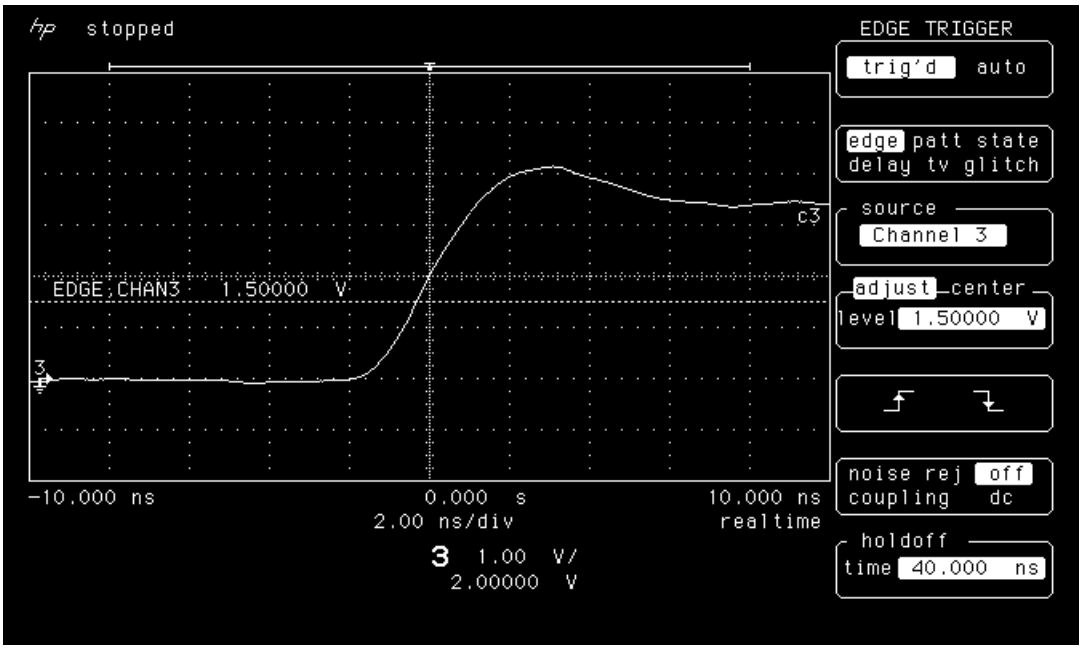

Figure 9a. Rising edge of LAN1221 pre-irradiation

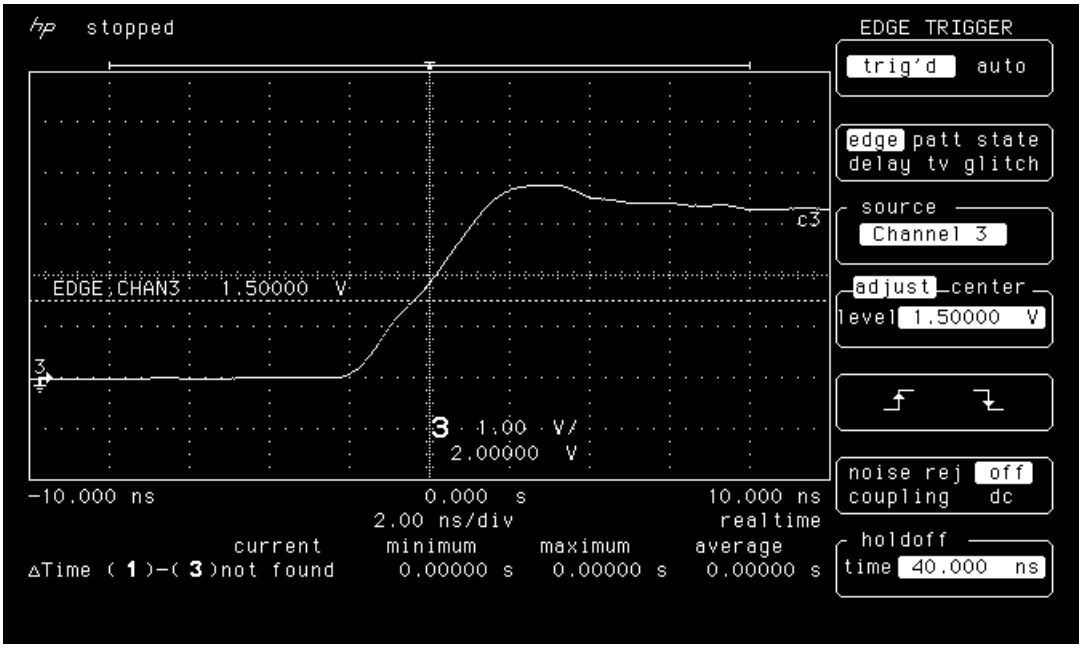

Figure 9b. Rising edge of LAN1221 post-75 krad(Si) irradiation

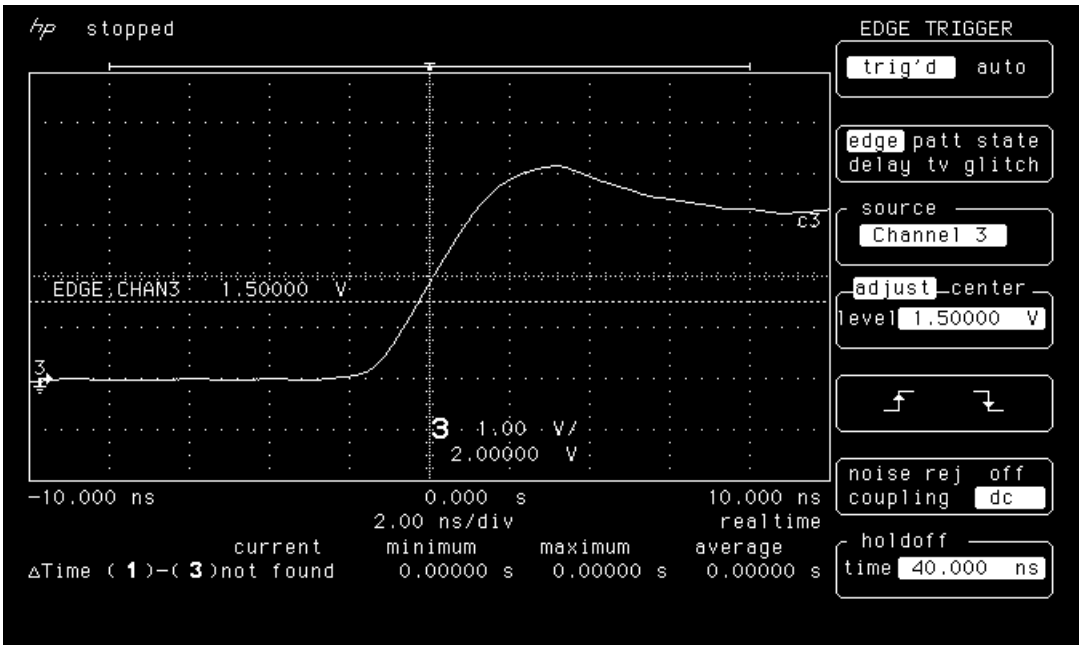

Figure 9c. Rising edge of LAN1221 post-room-temperature-annealing

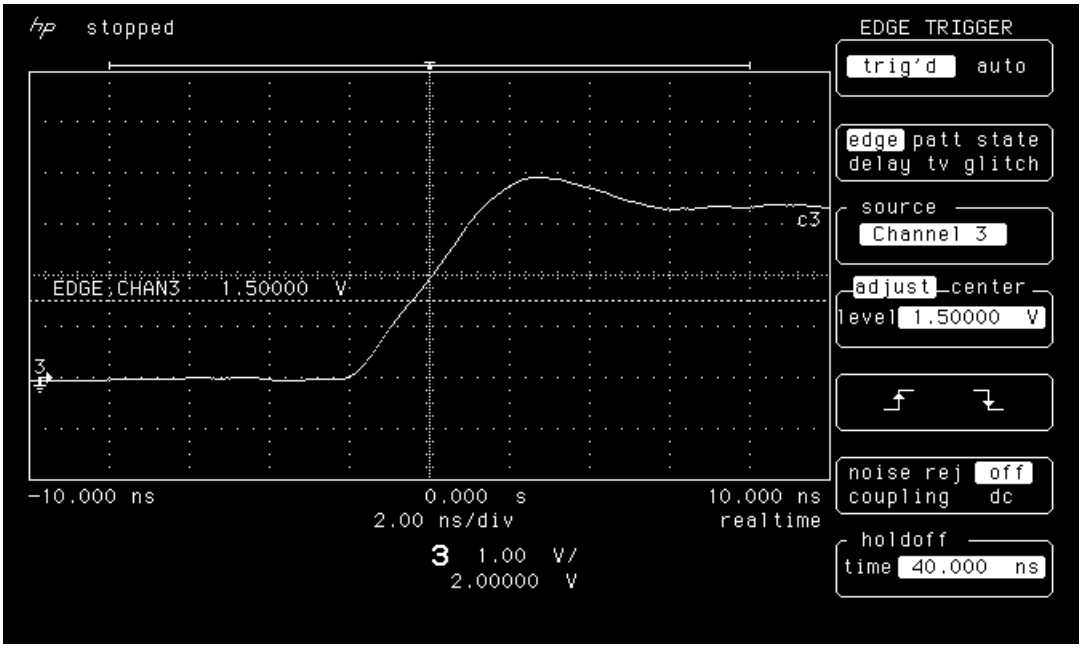

Figure 10a. Rising edge of LAN1222 pre-irradiation

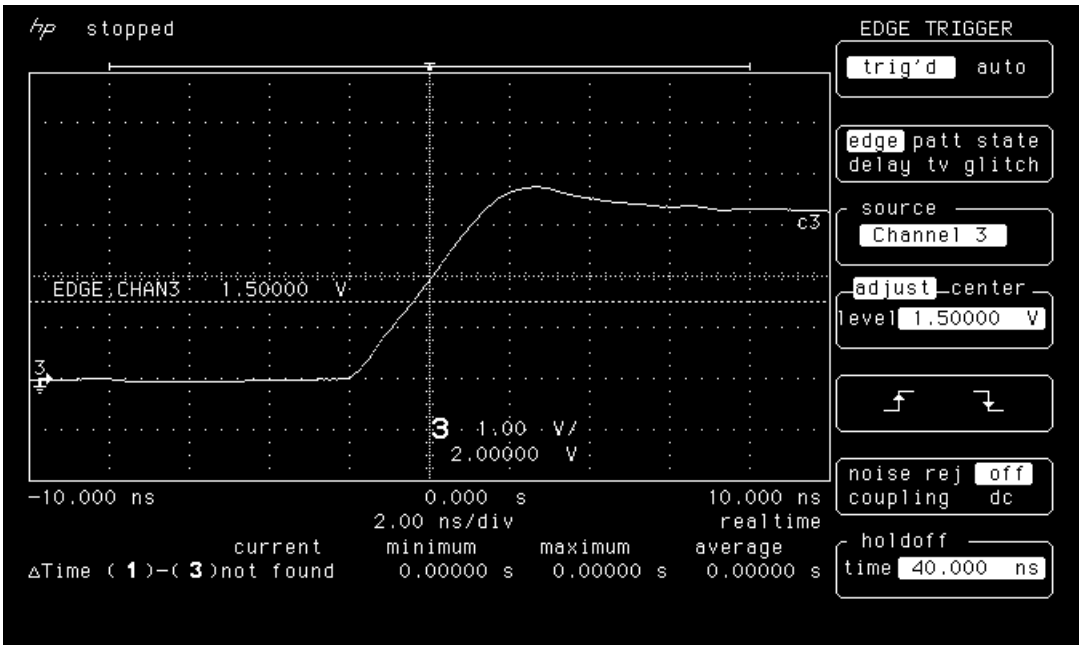

Figure 10b. Rising edge of LAN1222 post-75 krad(Si) irradiation

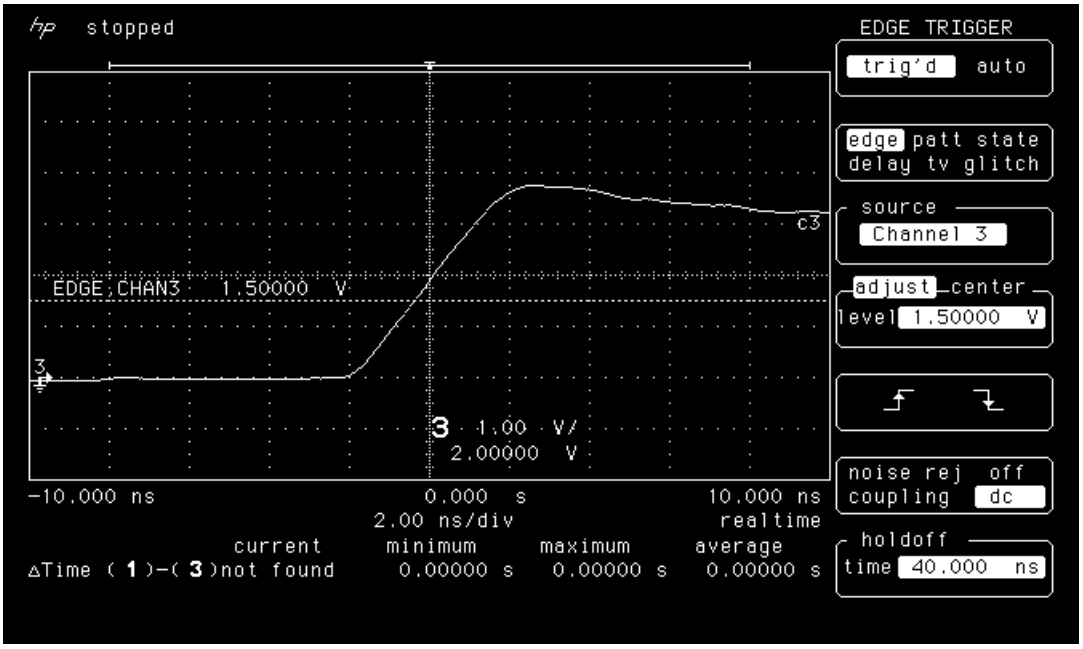

Figure 10c. Rising edge of LAN1222 post-room-temperature annealing

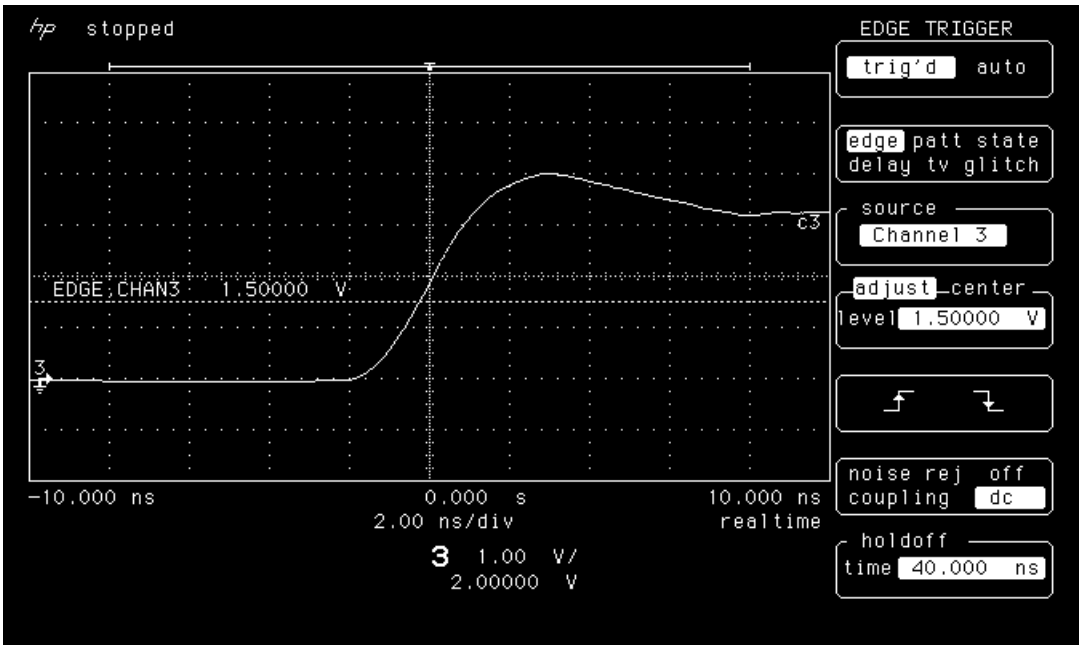

Figure 11a. Rising edge of LAN1231 pre-irradiation

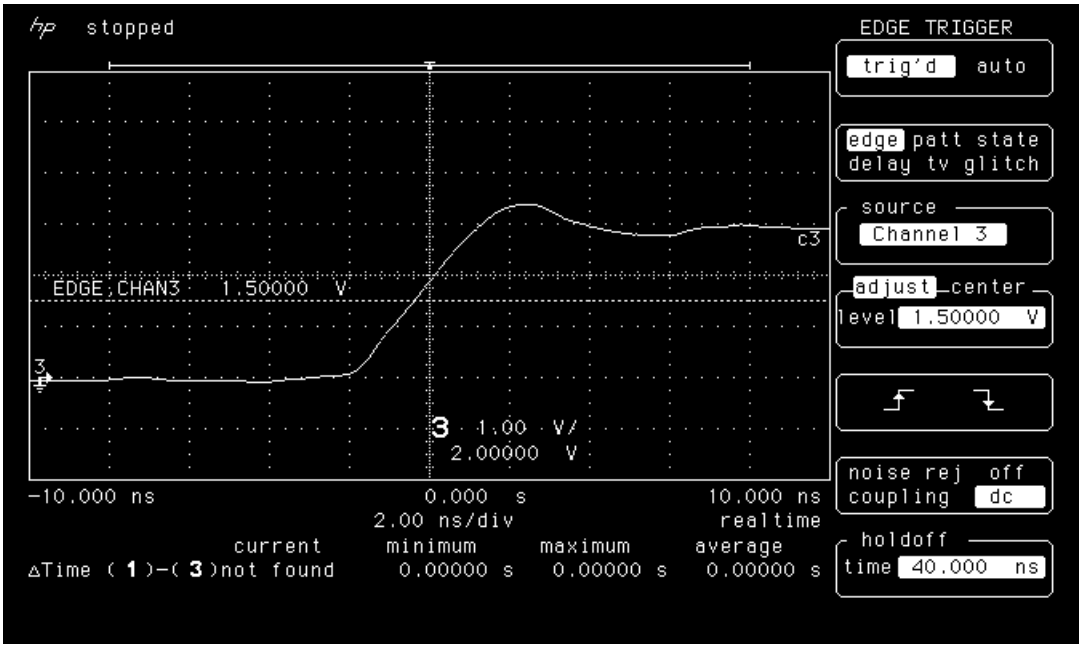

Figure 11b. Rising edge of LAN1231 post-75 krad(Si) irradiation

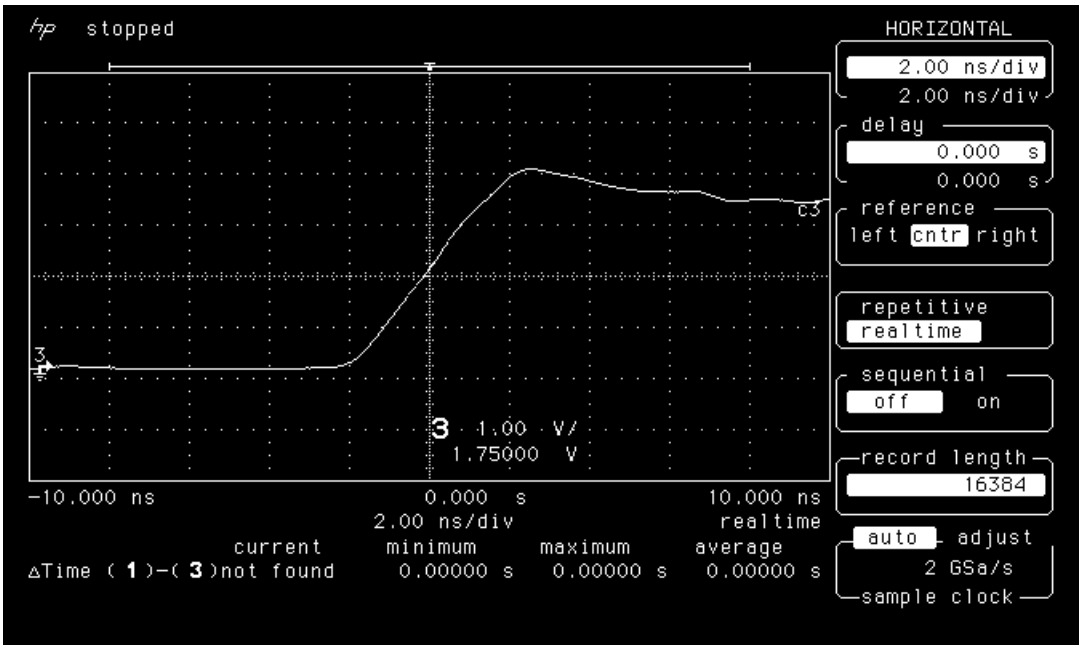

Figure 11c. Rising edge of LAN1231 post-room-temperature annealing

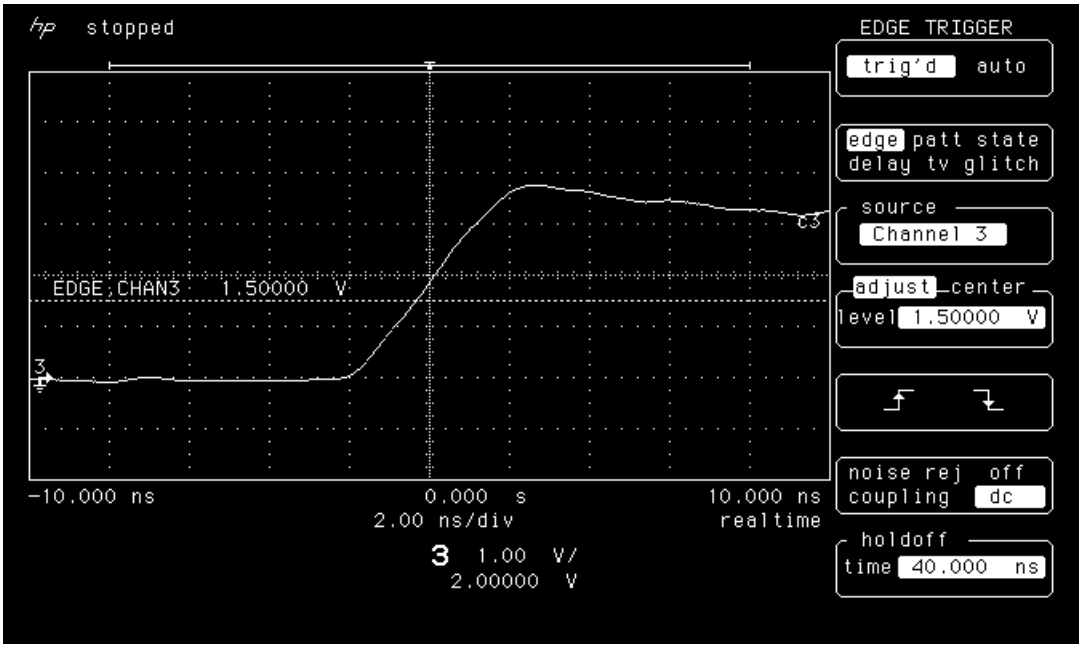

Figure 12a. Rising edge of LAN1232 pre-irradiation

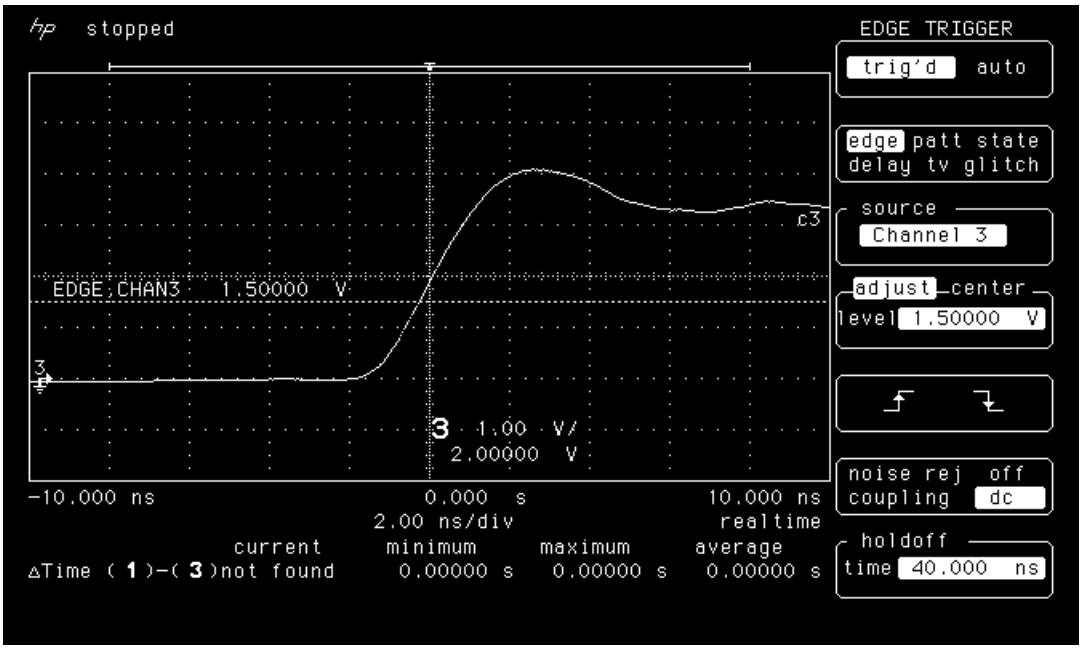

Figure 12b. Rising edge of LAN1232 post-75 krad(Si) irradiation

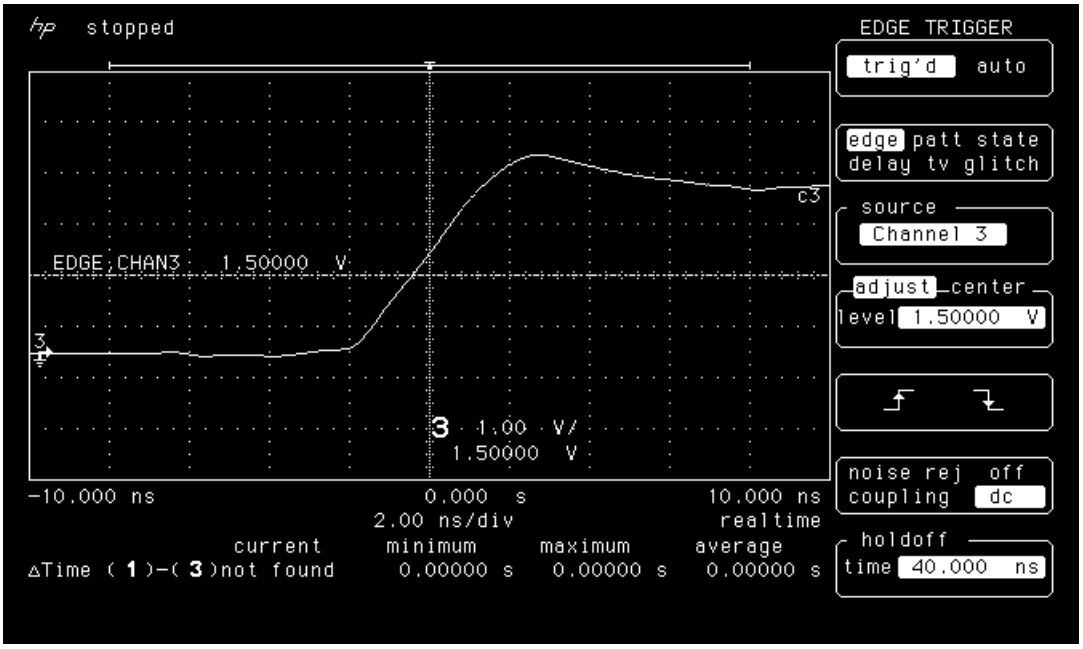

Figure 12c. Rising edge of LAN1232 post-room-temperature annealing

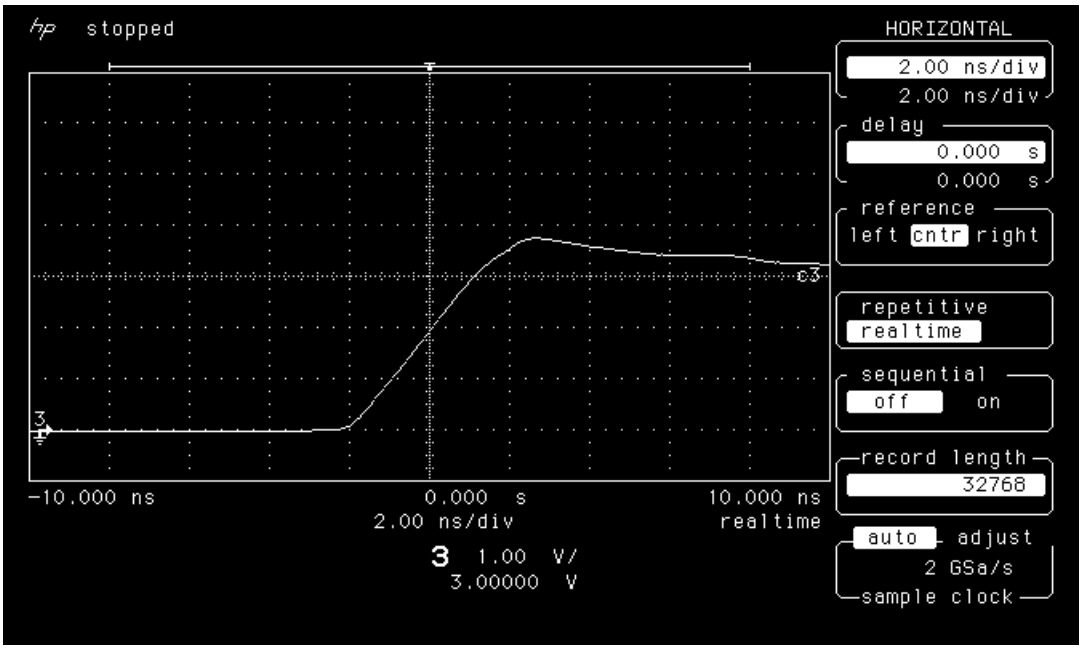

Figure 13a. Rising edge of LAN1233 pre-irradiation

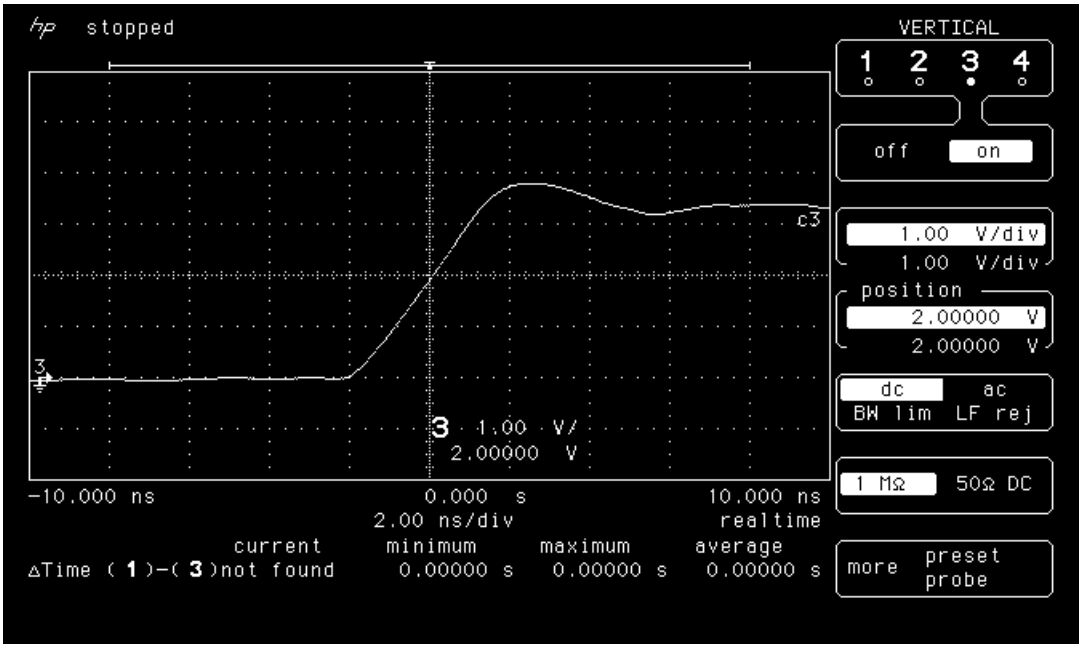

Figure 13b. Rising edge of LAN1233 post-75 krad(Si) irradiation

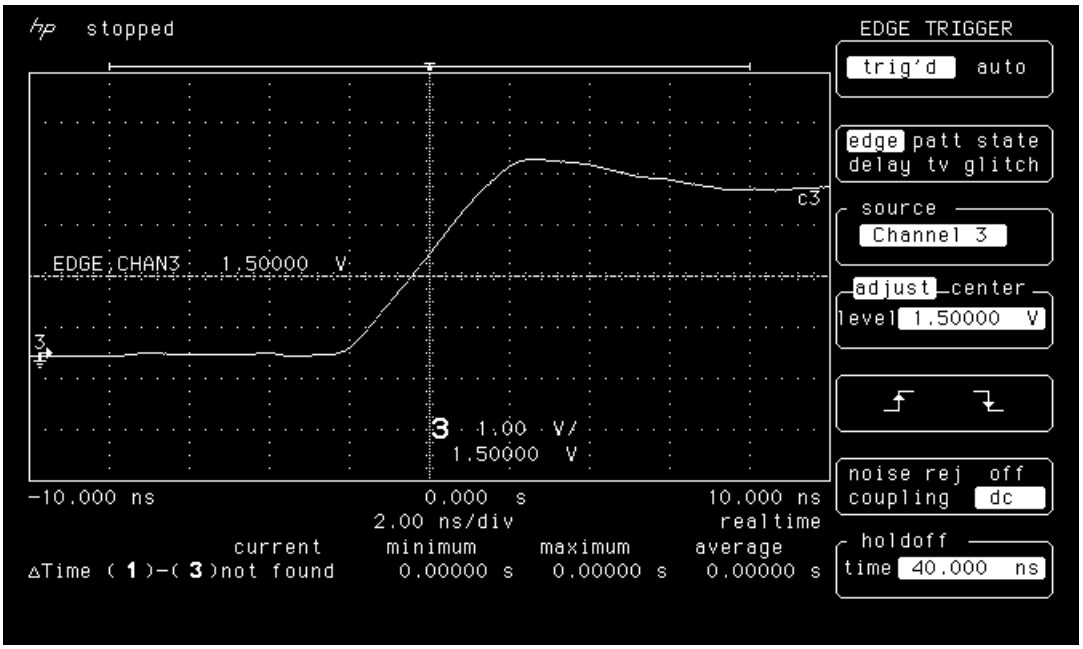

Figure 13c. Rising edge of LAN1233 post-room-temperature annealing

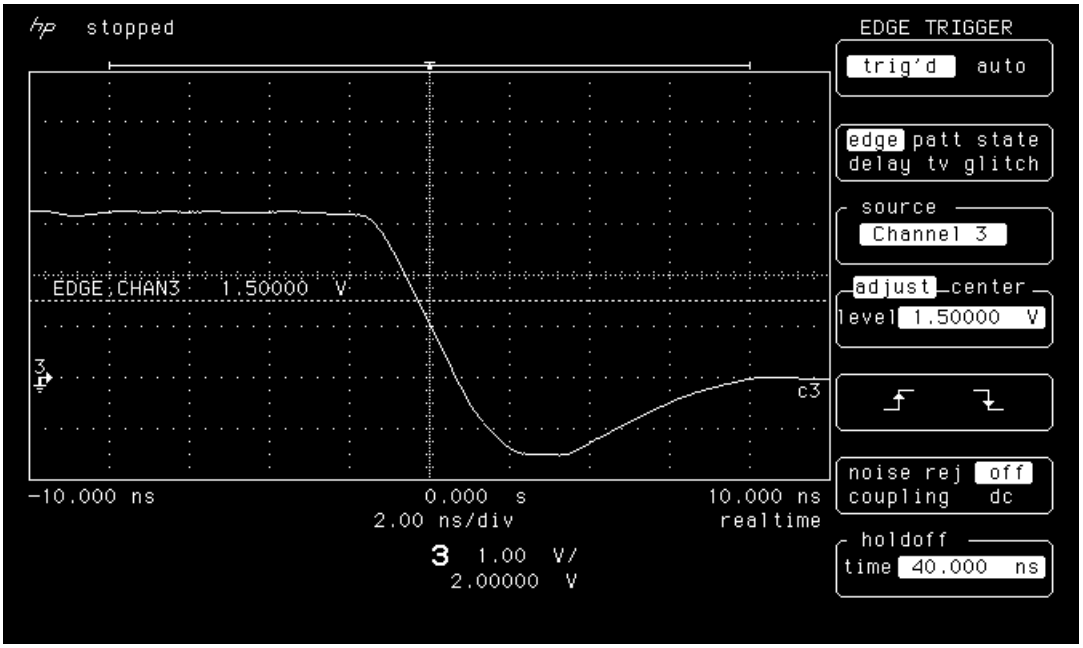

Figure 14a. Falling edge of LAN1221 pre-irradiation.

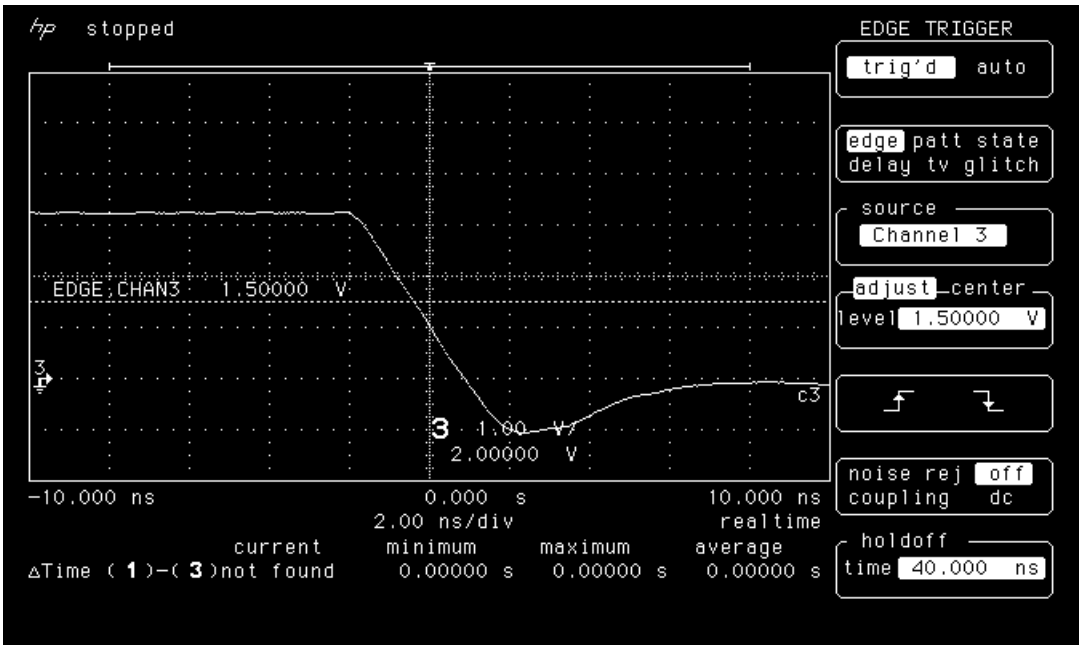

Figure 14b. Falling edge of LAN1221post-75 krad(Si) irradiation

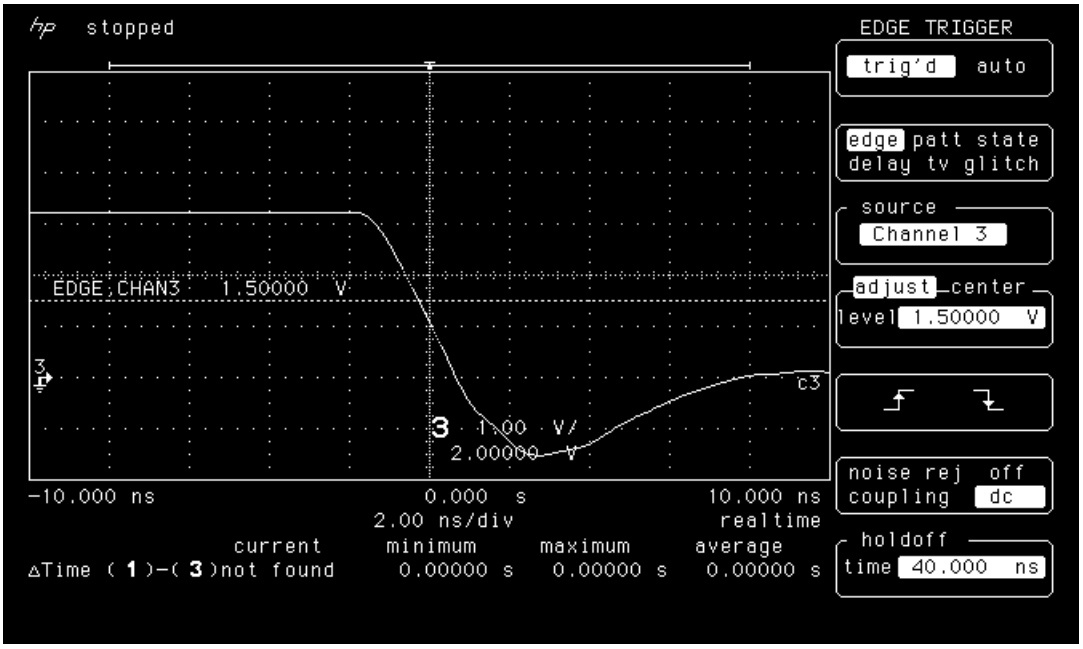

Figure 14c. Falling edge of LAN1221 post room temperature annealing

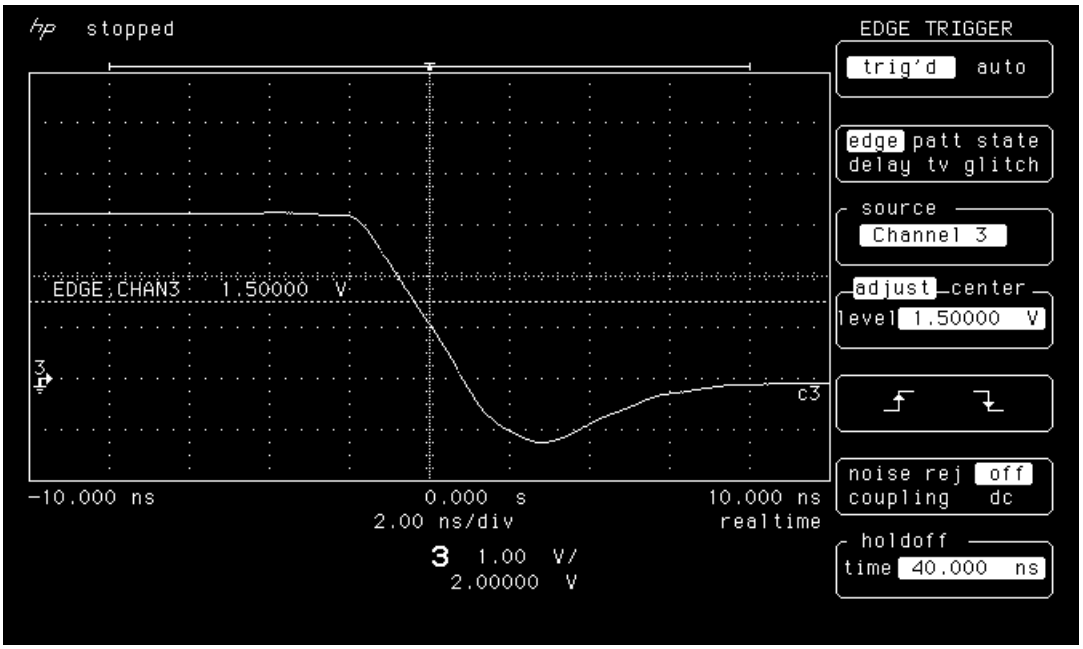

Figure 15a. Falling edge of LAN1222 pre-irradiation.

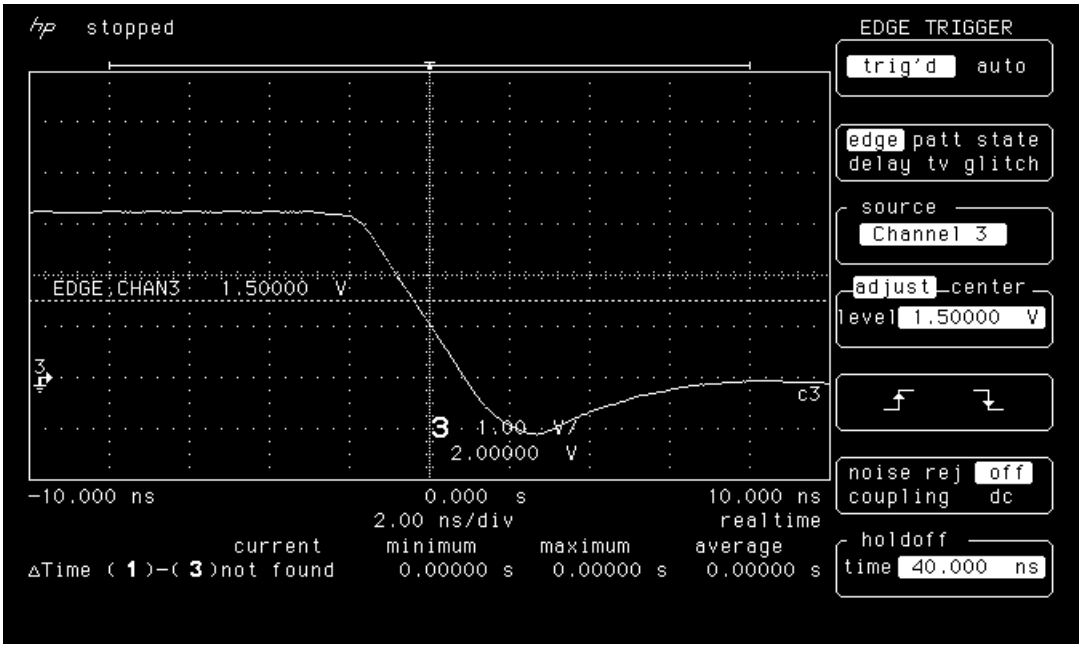

Figure 15b. Falling edge of LAN1222 post-75 krad(Si) irradiation

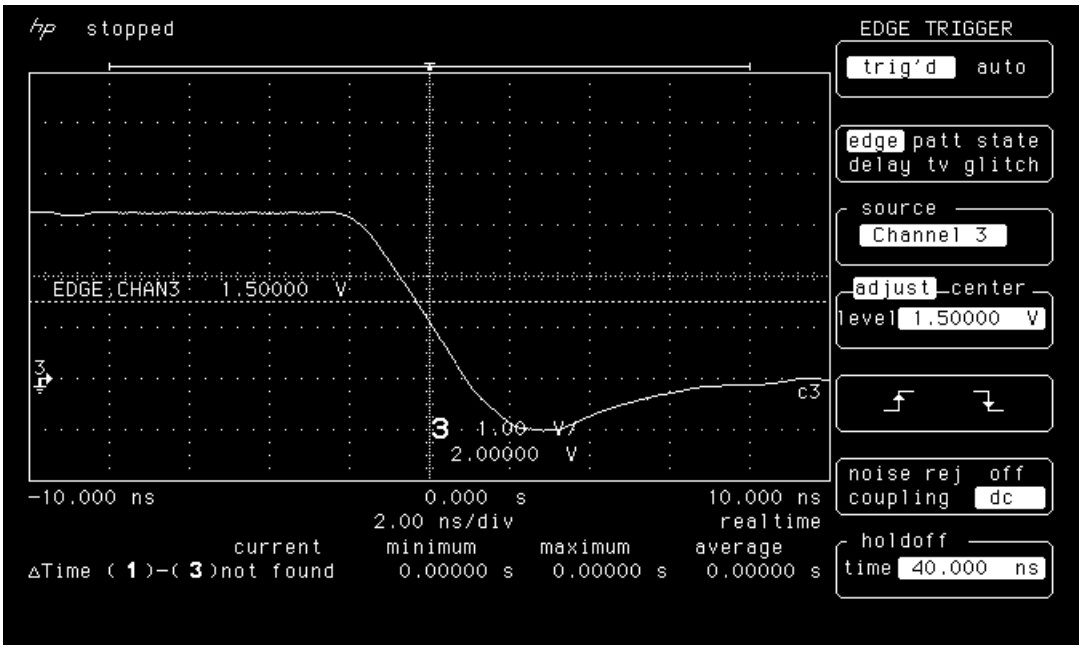

Figure 15c. Falling edge of LAN1222 post room temperature annealing

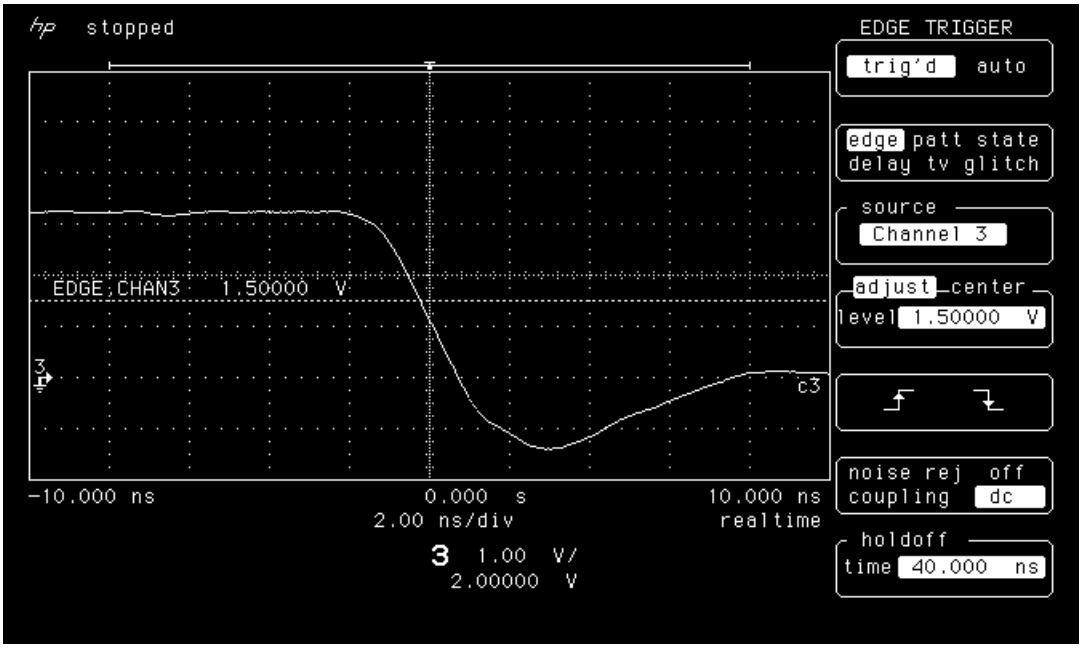

Figure 16a. Falling edge of LAN1231 pre-irradiation

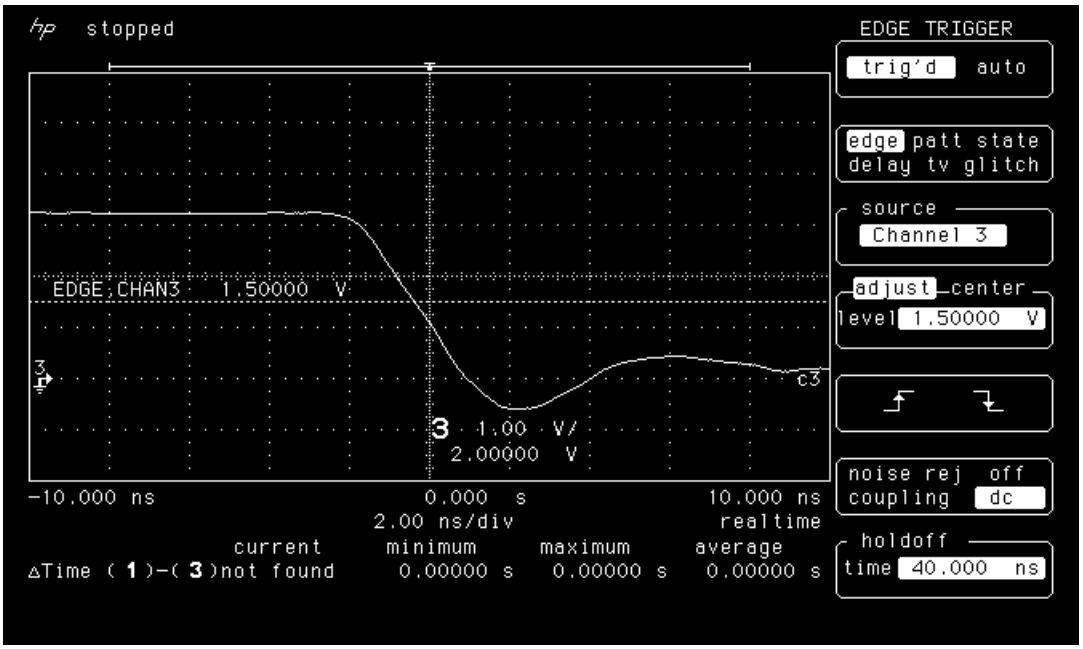

Figure 16b. Falling edge of LAN1231 post-75 krad(Si) irradiation

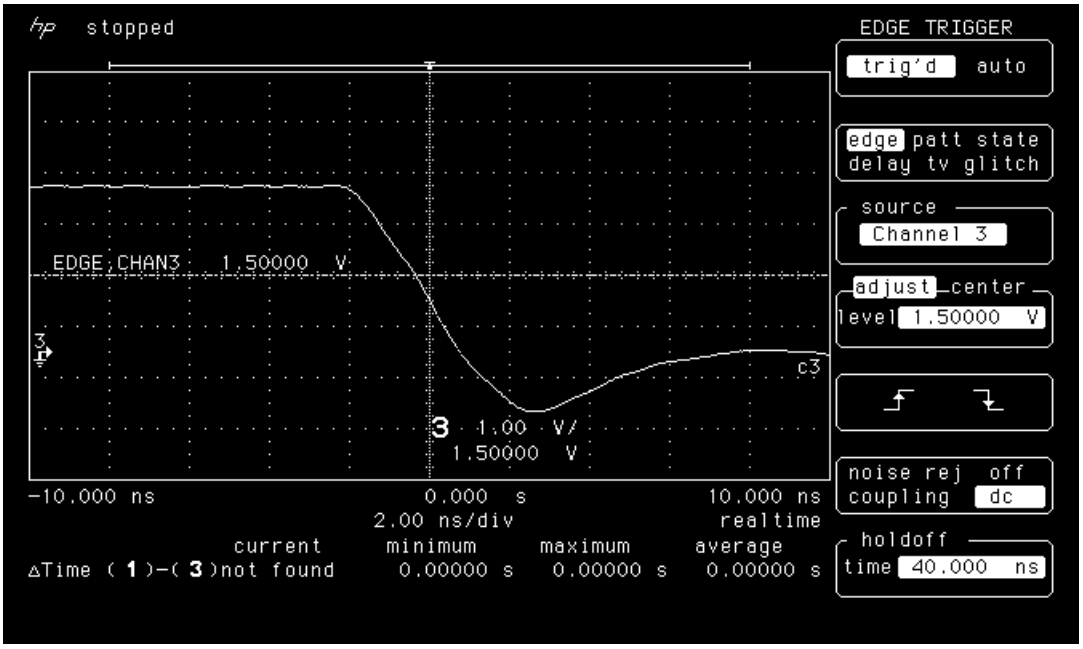

Figure 16c. Falling edge of LAN1231 post room temperature annealing

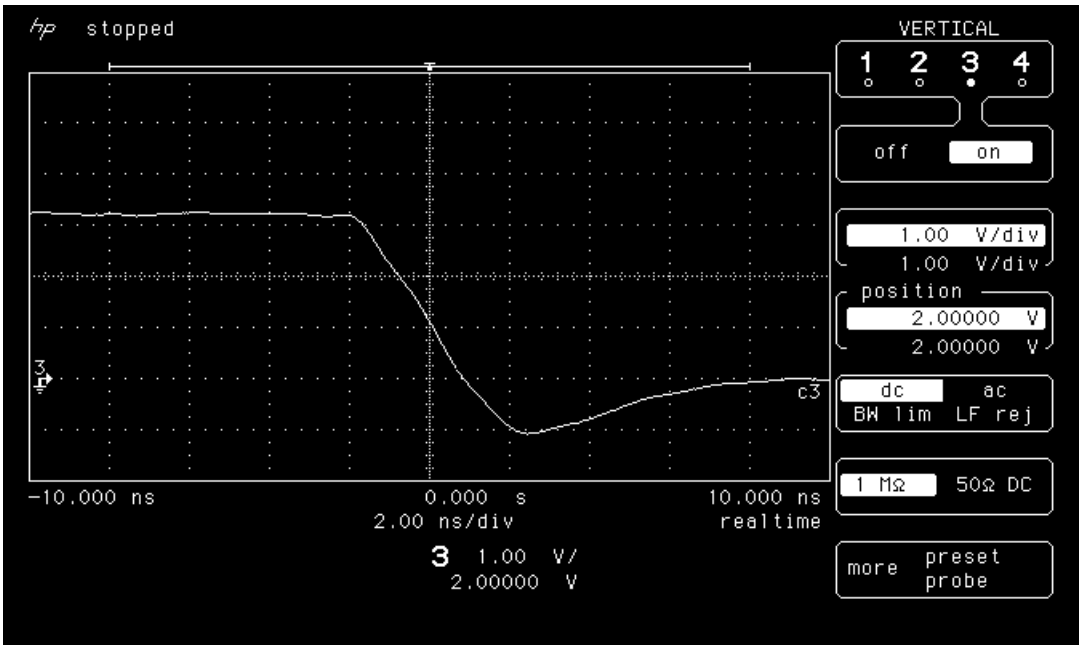

Figure 17a. Falling edge of LAN1232 pre-irradiation

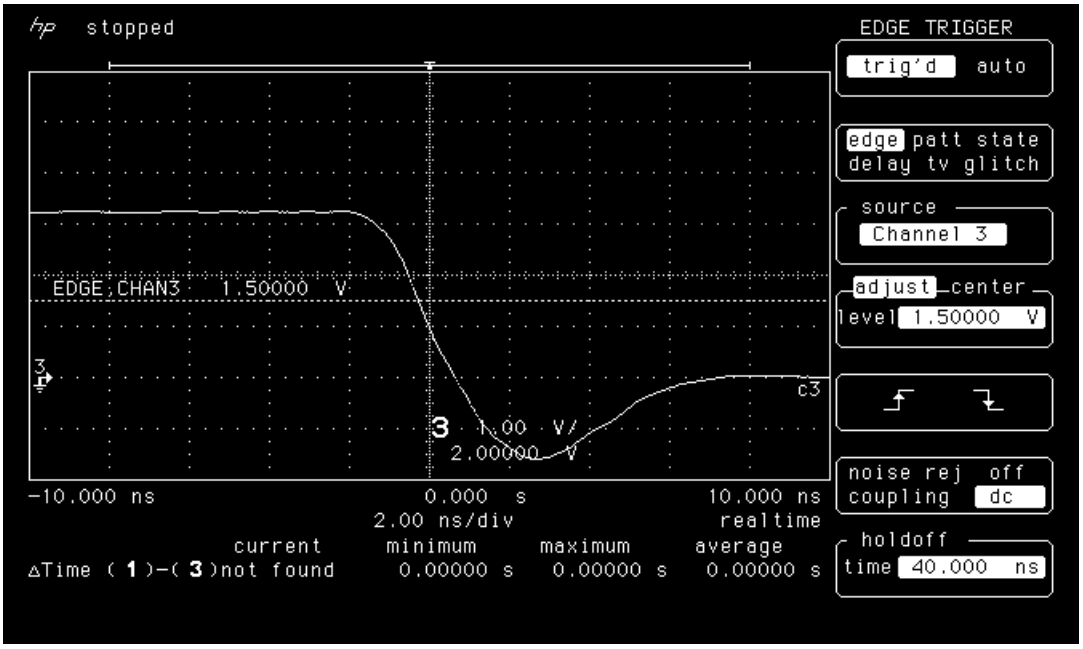

Figure 17b. Falling edge of LAN1232 post-75 krad(Si) irradiation

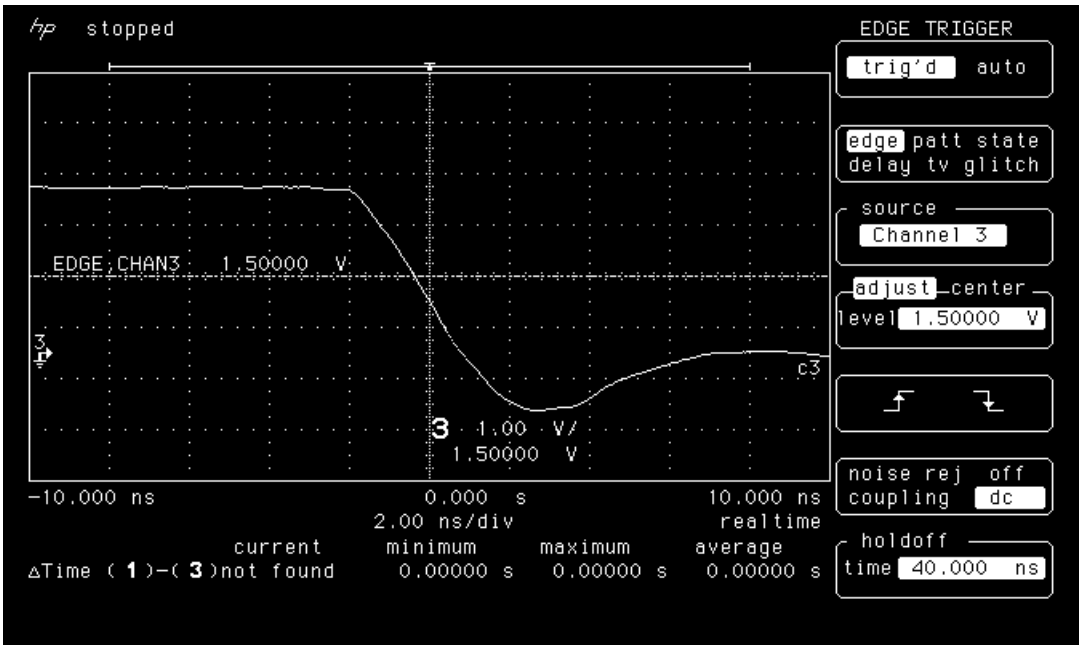

Figure 17c. Falling edge of LAN1232 post room temperature annealing

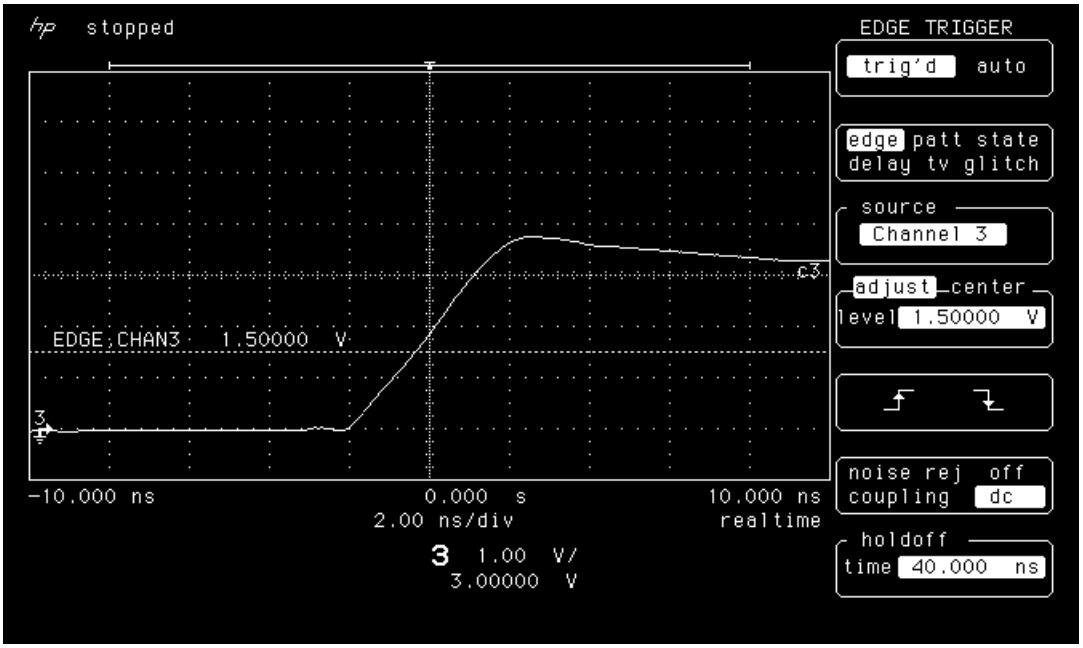

Figure 18a. Falling edge of LAN1233 pre-irradiation

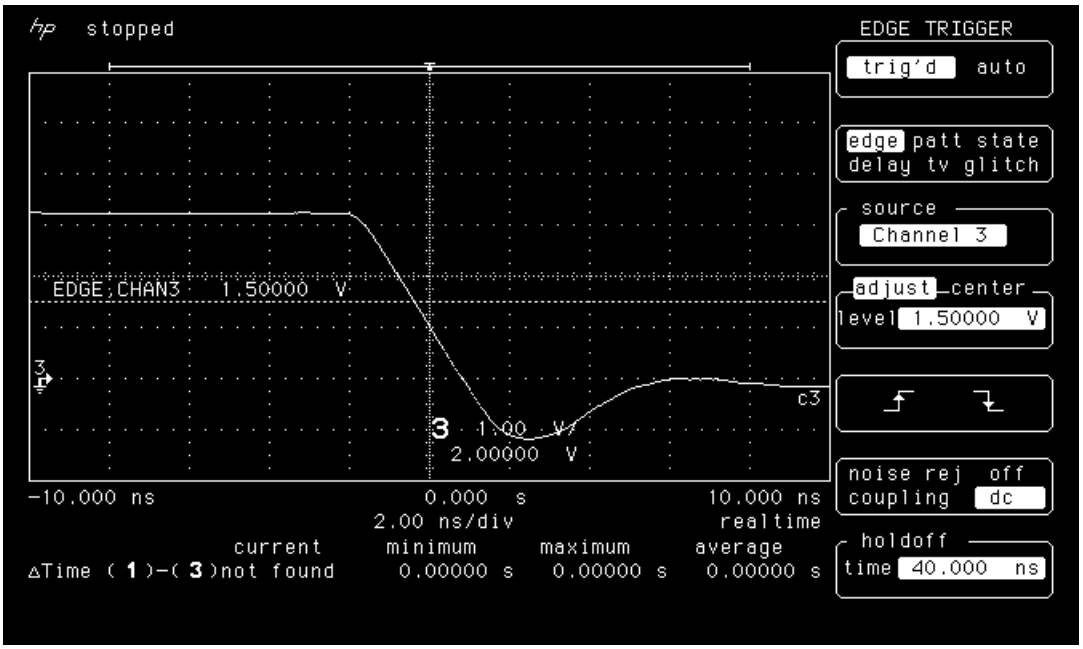

Figure 18b. Falling edge of LAN1233 post 75 krad(Si) irradiation

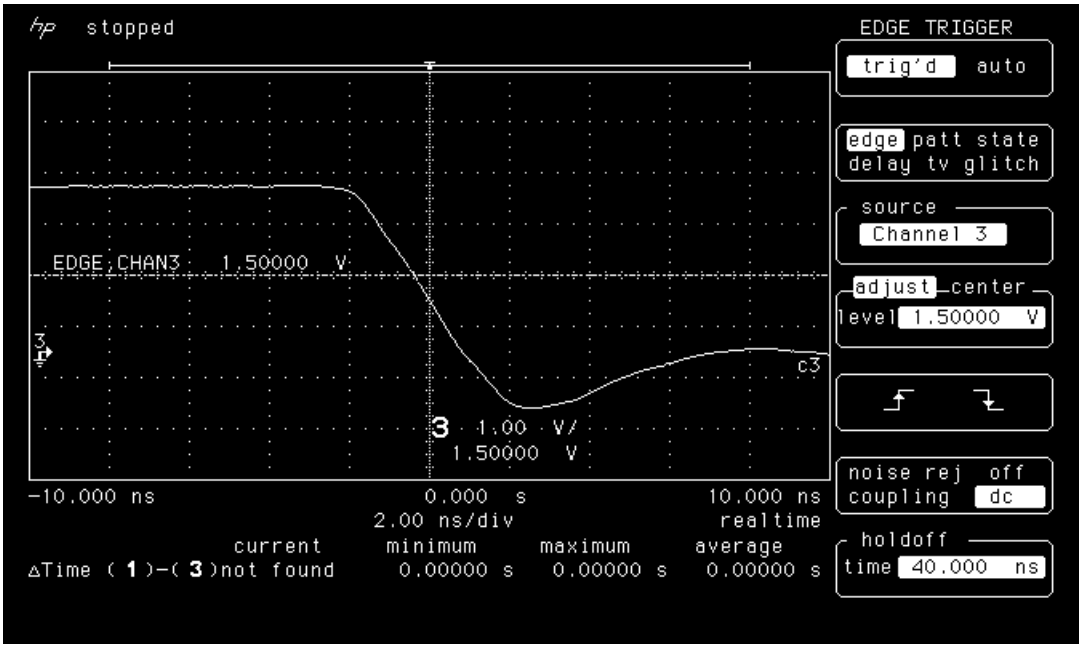

Figure 18c. Falling edge of LAN1233 post room temperature annealing

3.7 POWER-ON TRANSIENT CURRENT

The power-on transient characteristics with respect to irradiation dose, and post-irradiation annealing were measured. Figures 19-23 show the oscilloscope captures of power-on voltage and the current of pre-, post-irradiation and post-room-temperature annealing of the DUTs. Note that in these Figures, C1 is the voltage, and C2 the current. The scale for current (C2) is 100 mA/division.

The results show that 75 krad(Si) irradiation at the dose rate of 18.65 krad(Si)/day did induce a transient current peak during the power-on (comparing Figures 21b, 22b and 23b with 21a, 22a and 23a). The pulse has peak about 150 mA with FWHM about 1 μs. Notice that Figures 19b and 20b don't show this peak, because too slow a sample rate was used. The pulse is occurring at approximately 2.5 V. The energy consumption at the testing ramping rate by this pulse is approximately 0.375 μJ, which is believed a non-issue for power-on sequence in space applications. However, 8 days room-temperature-anneal didn't really alter this effect (see Figures 21d, 22d, and 23d). This behavior is believed due to the on-chip charge pump circuitry [see "Total dose and dose-rate effects on start-up current in antifuse FPGA", by J. J. Wang et al, accepted for publication at RADECS99]. The details are still under investigation.

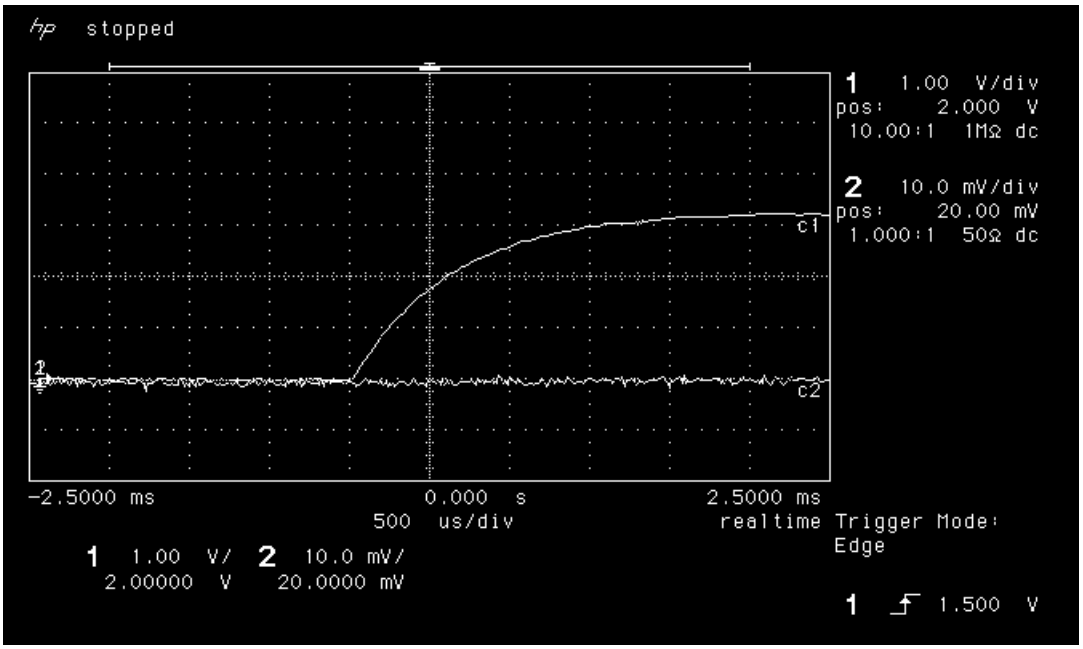

Figure 19a Power-on transient current of LAN1221 pre-irradiation

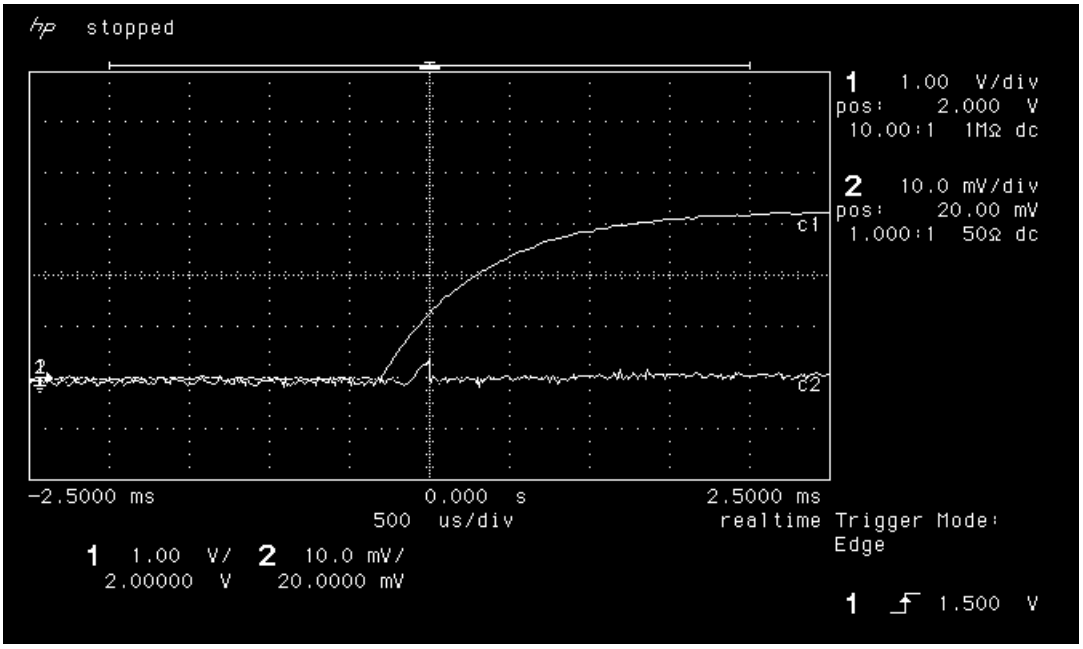

Figure 19b Power-on transient current of LAN1221 post 75krad(Si) irradiation

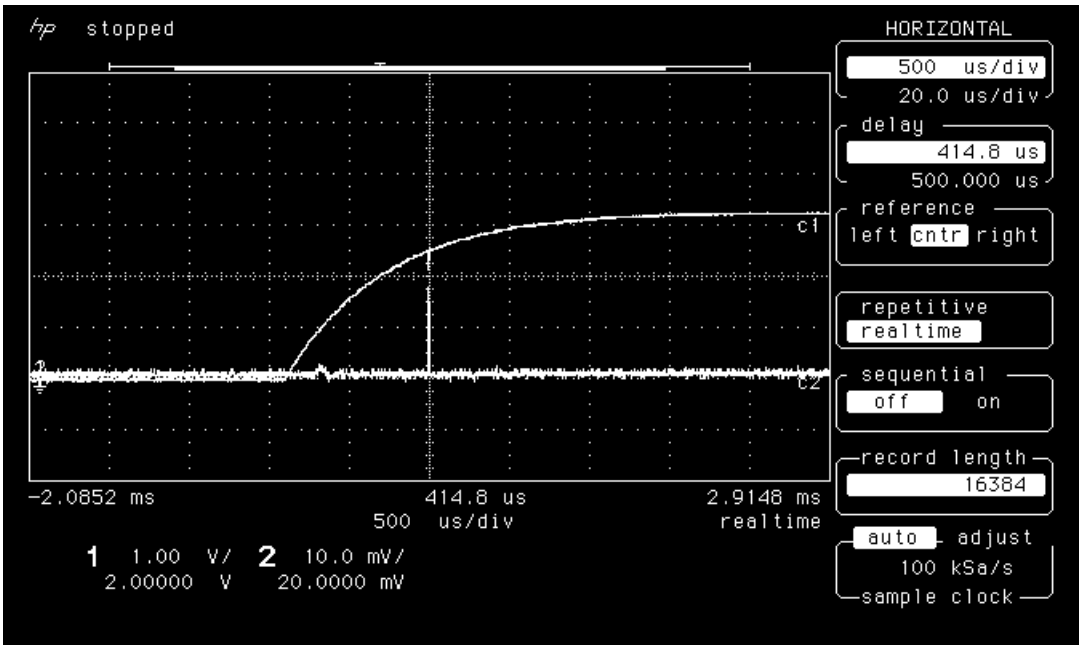

Figure 19c Power-on transient current of LAN1221 post-room-temperature annealing

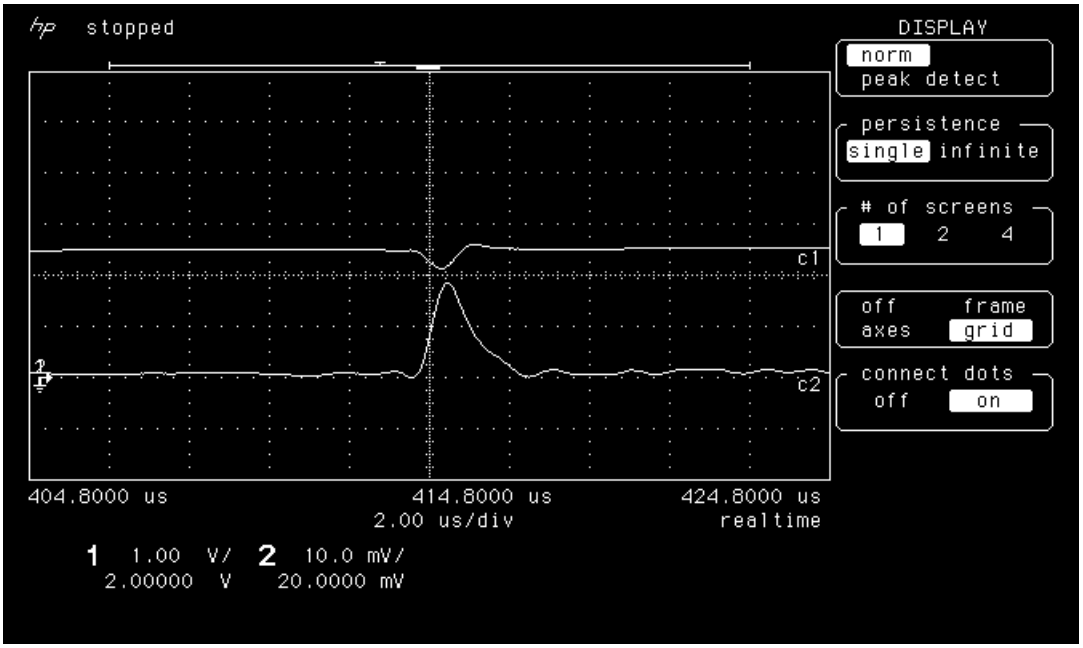

Figure 19d Close-up of 18c

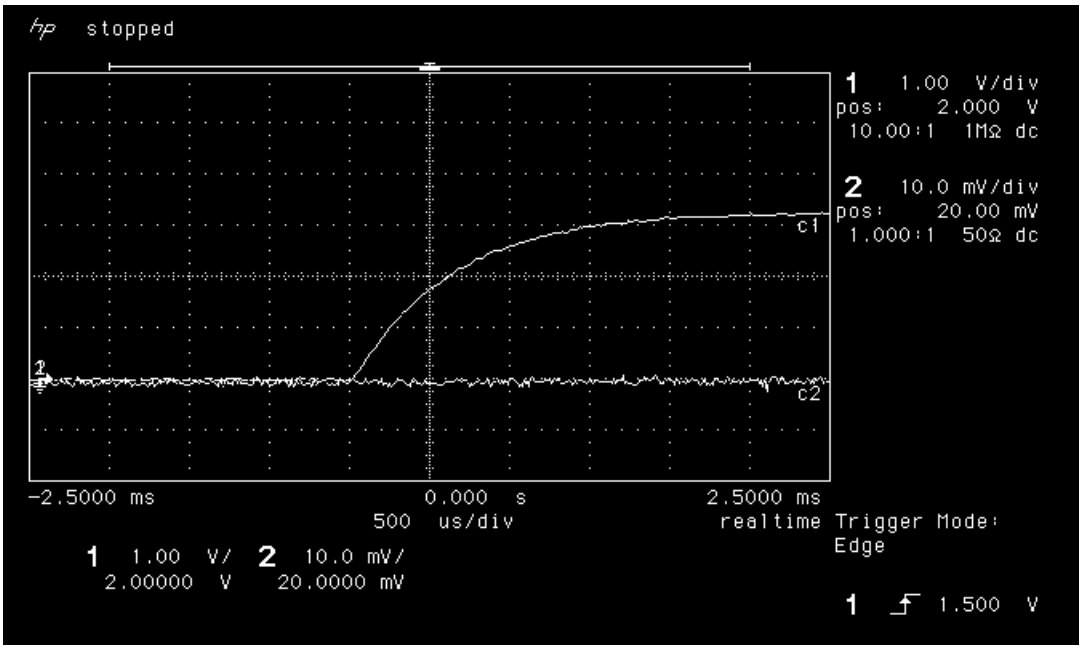

Figure 20a Power-on transient current of LAN1222 pre-irradiation

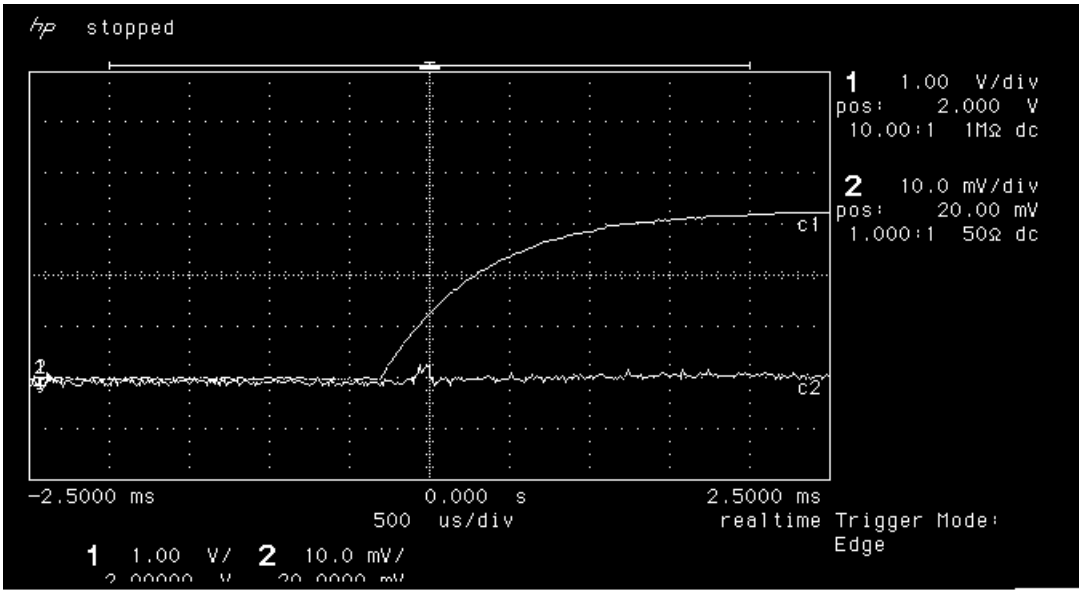

Figure 20b Power-on transient current of LAN1222 post 75 krad(Si) irradiation

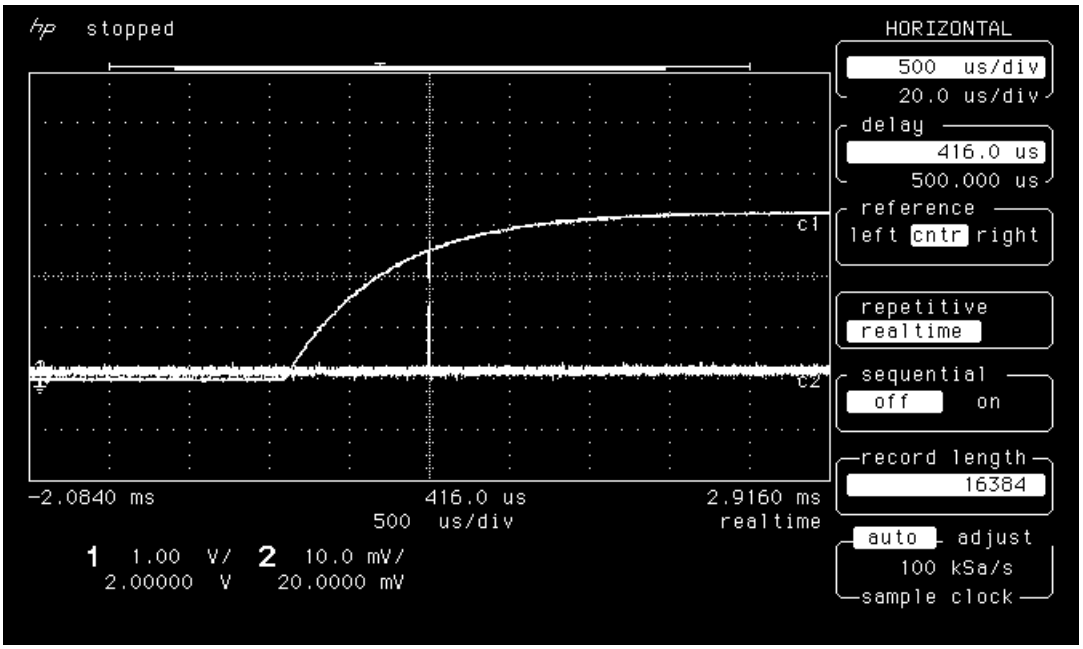

Figure 20c Power-on transient current of LAN1222 post-room-temperature annealing

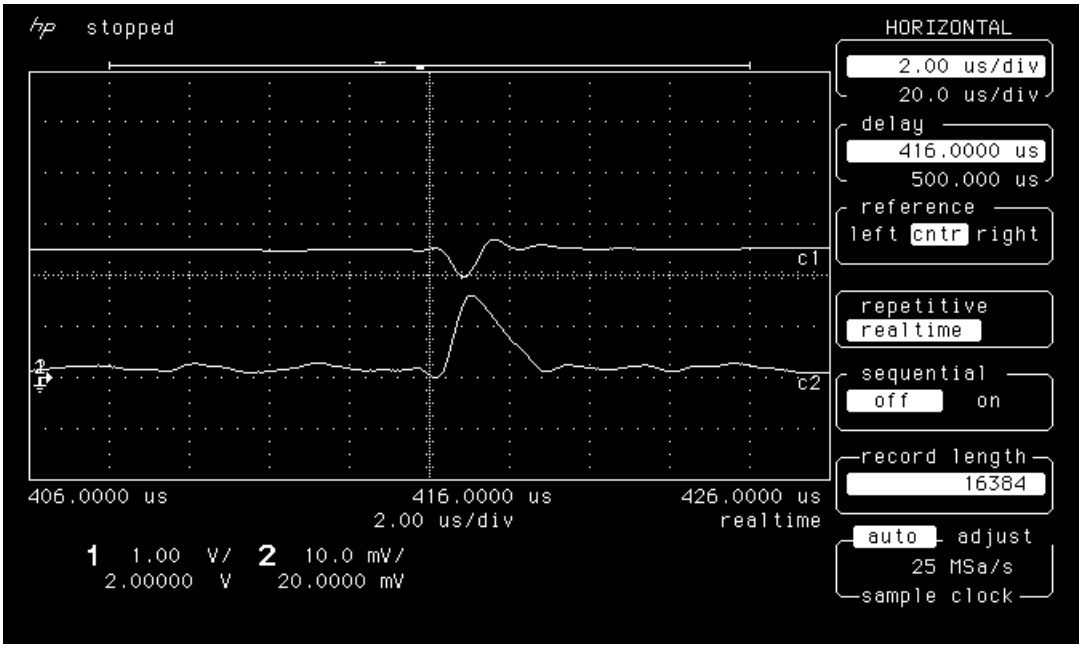

Figure 20d Close-up of 19c

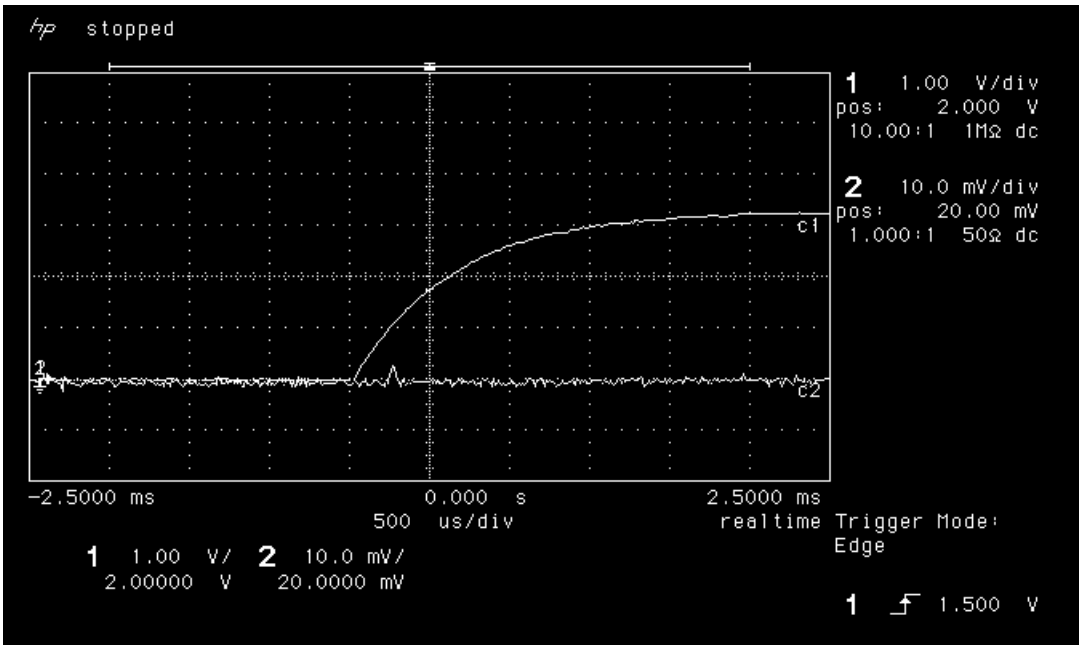

Figure 21a Power-on transient current of LAN1231 pre-irradiation

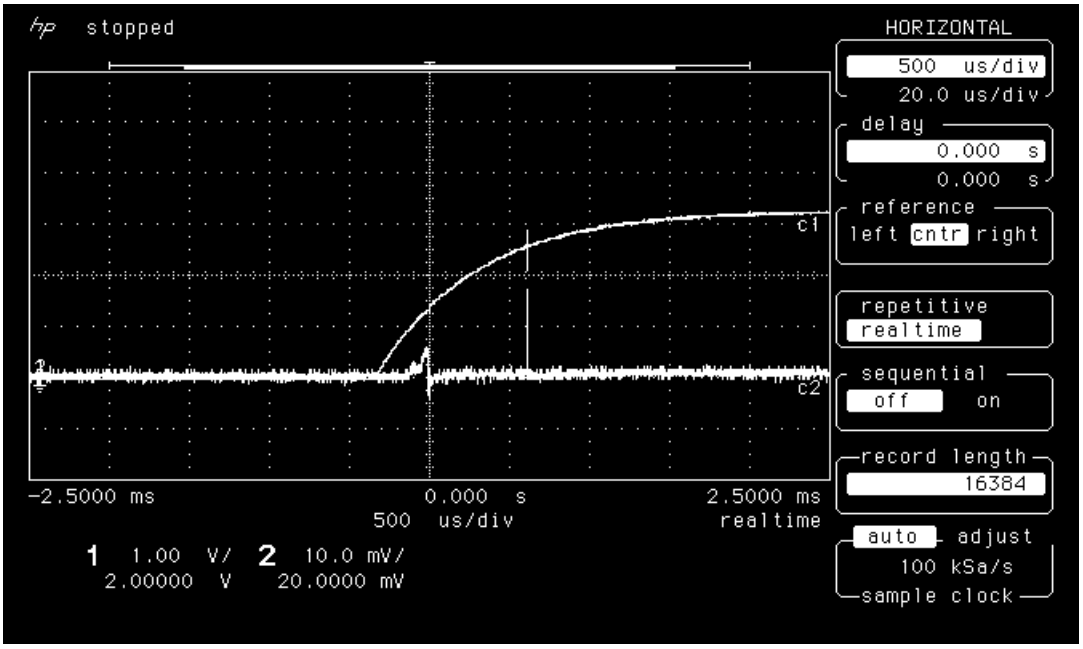

Figure 21b Power-on transient current of LAN1231 post 75 krad(Si) irradiation

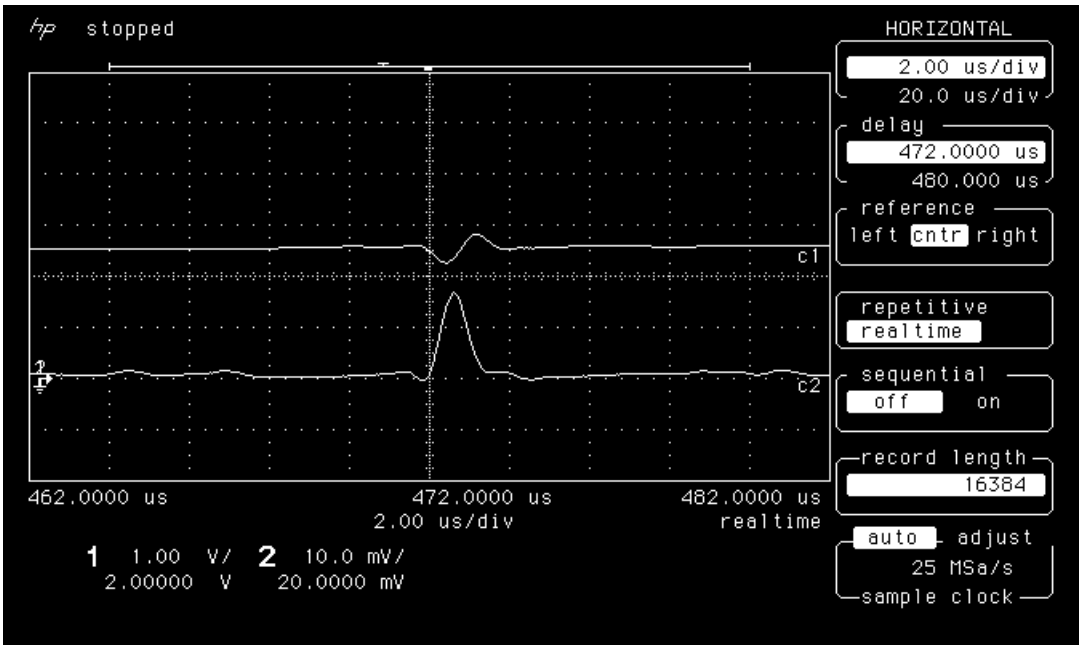

Figure 21c Close-up of 20b

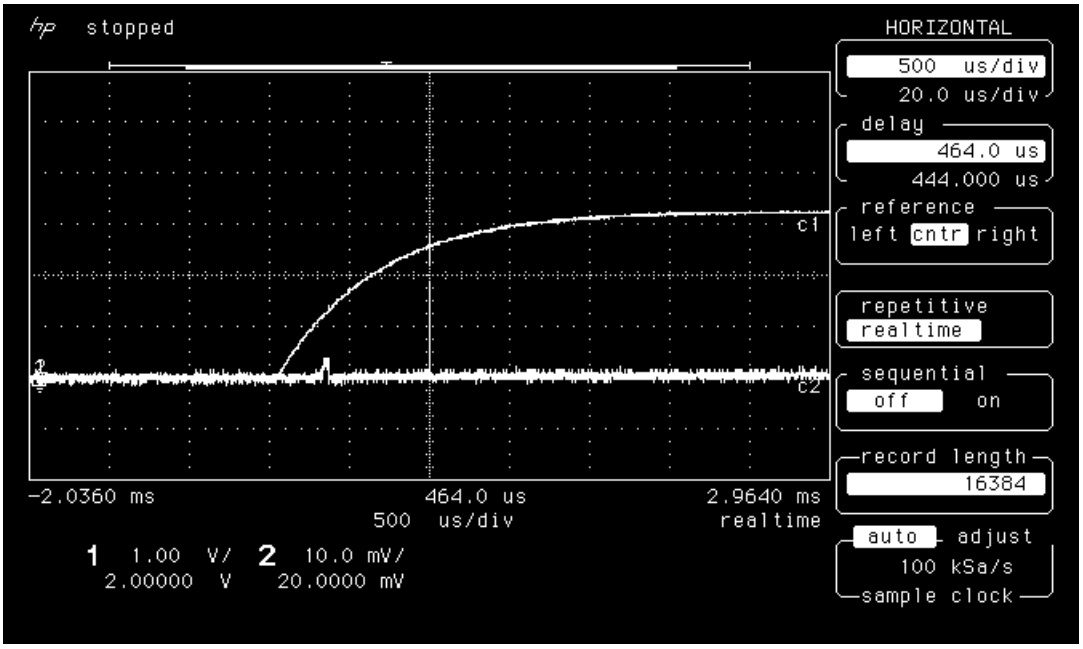

Figure 21d Power-on transient current of LAN1231 post-room-temperature annealing

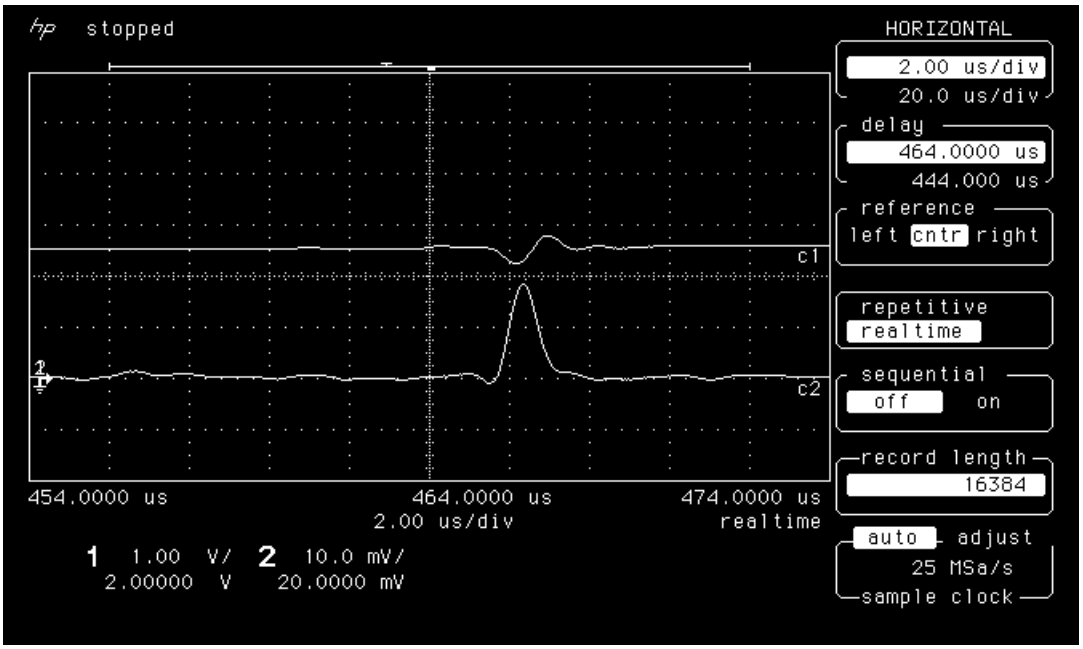

Figure 21e Close-up of 20d

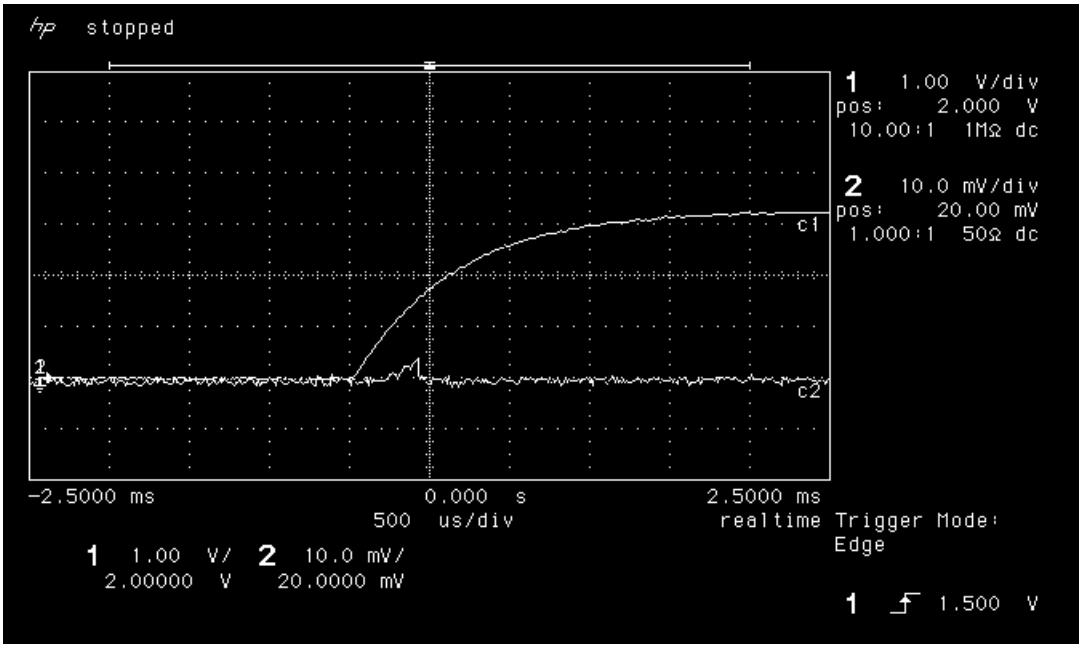

Figure 22a Power-on transient current of LAN1232 pre-irradiation

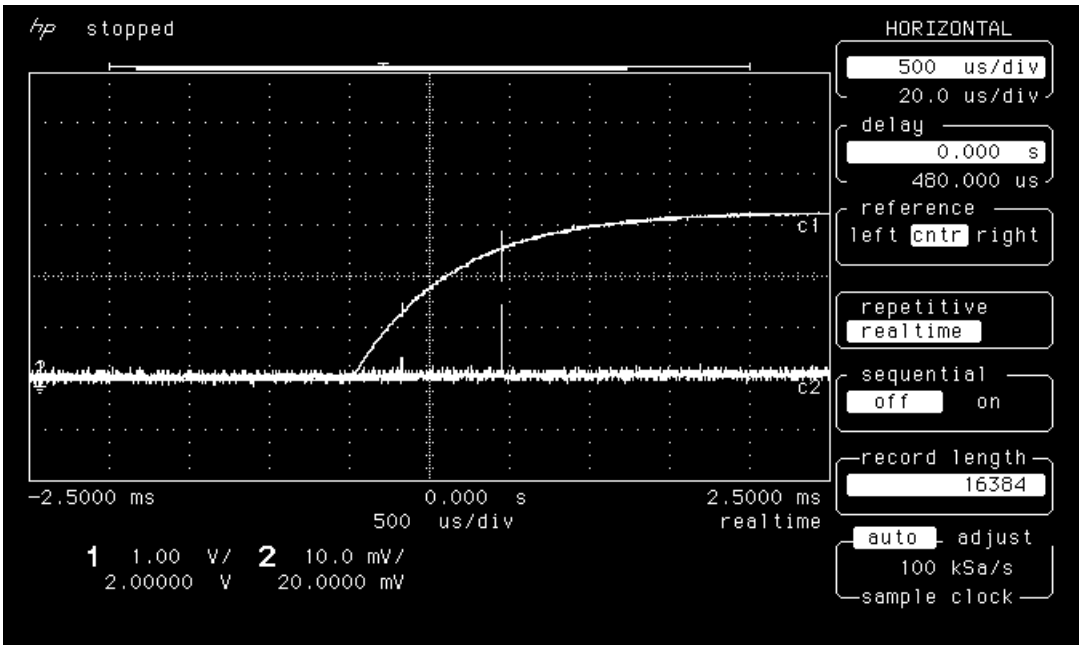

Figure 22b Power-on transient current of LAN1232 post 75 krad(Si) irradiation

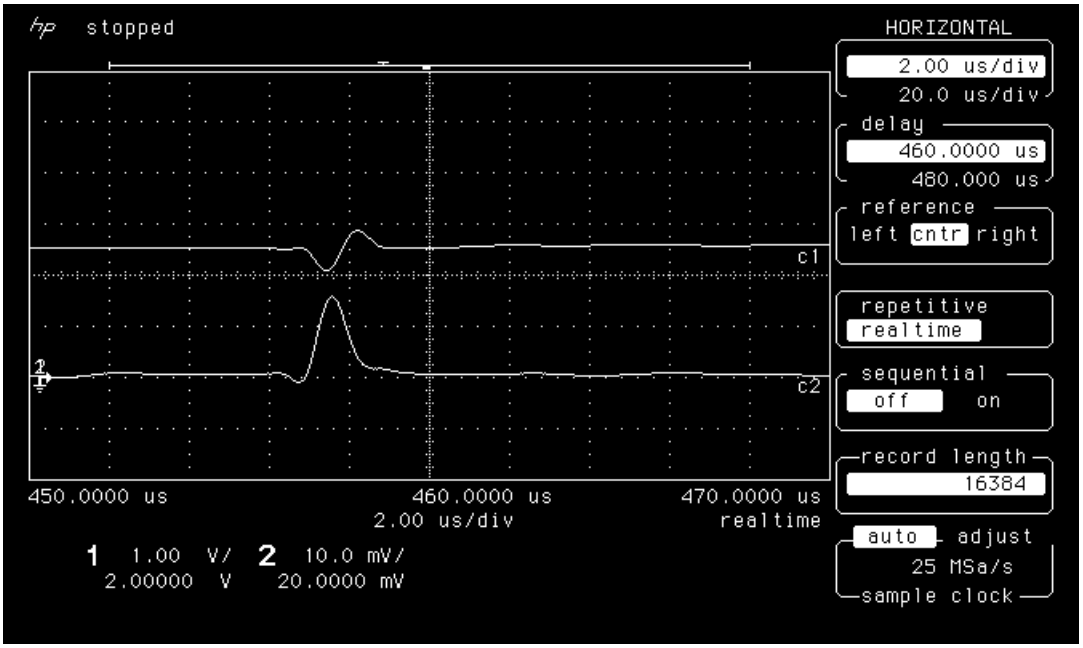

Figure 22c Close-up of 21b

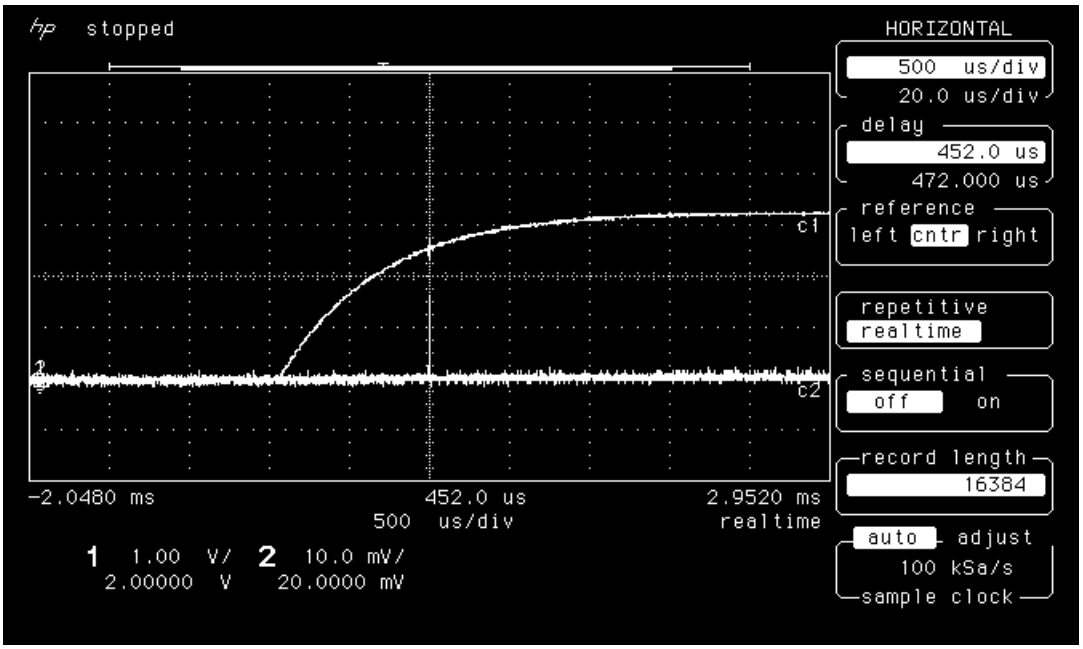

Figure 22d Power-on transient current of LAN1232 post-room-temperature annealing

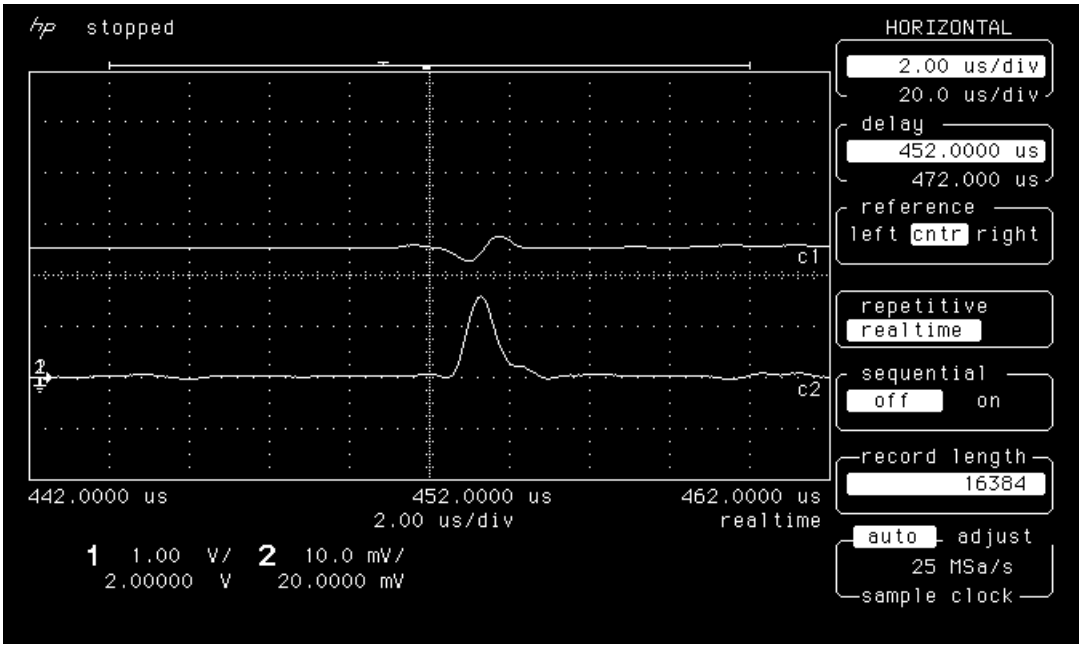

Figure 22e Close-up of 21d

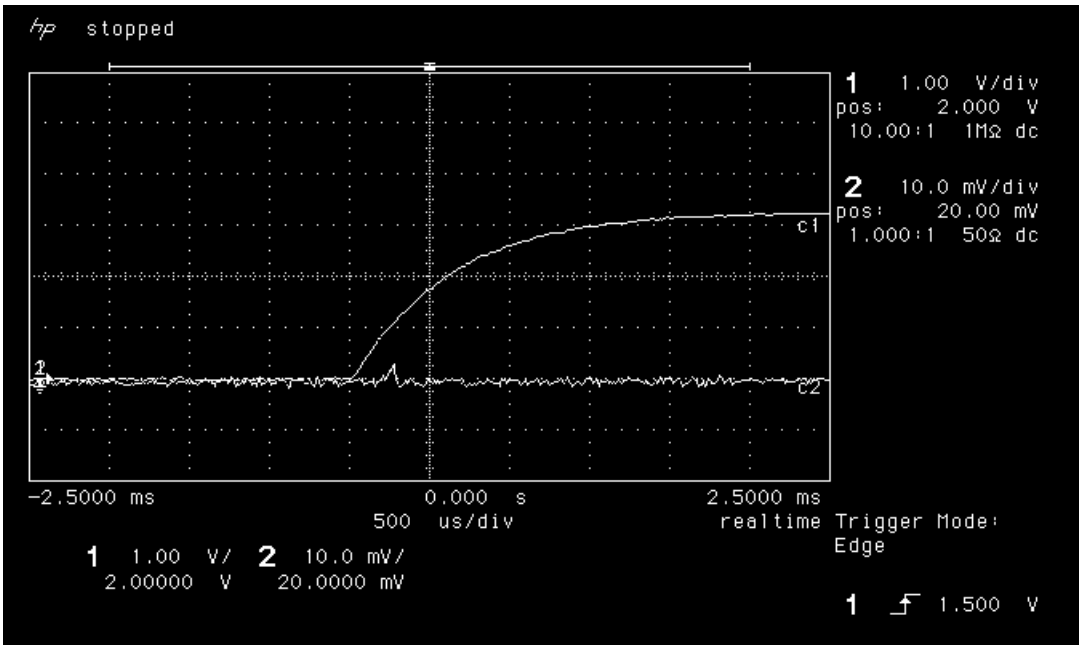

Figure 23a Power-on transient current of LAN1233 pre-irradiation

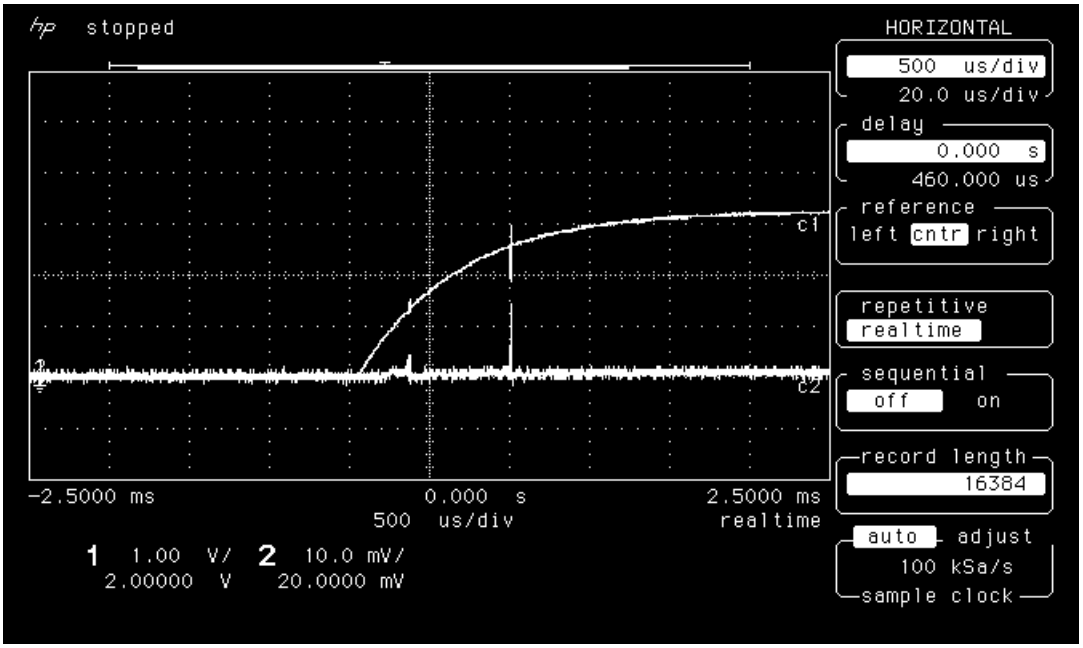

Figure 23b Power-on transient current of LAN1233 post 75 krad(Si) irradiation

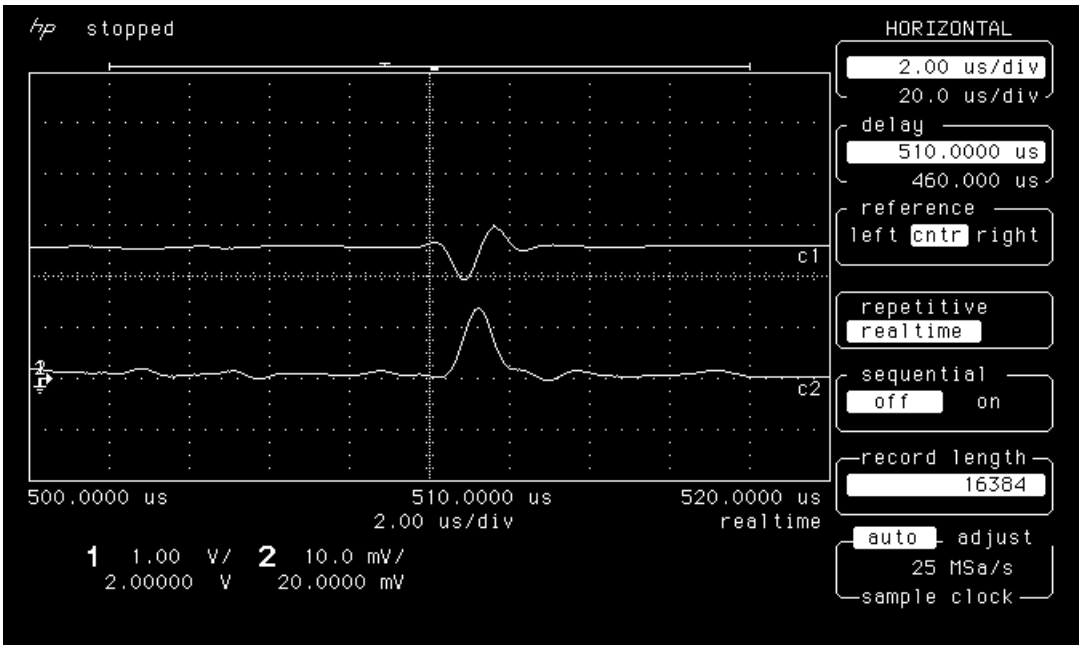

Figure 23c Close-up of 22b

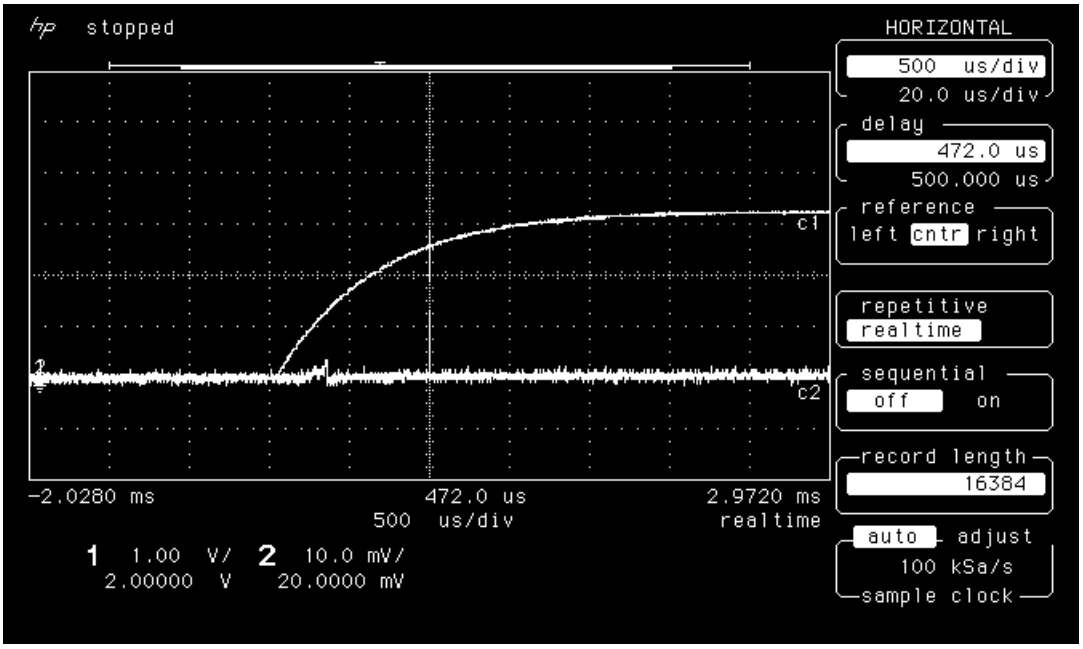

Figure 23d Power-on transient current of LAN1233 post-room-temperature annealing

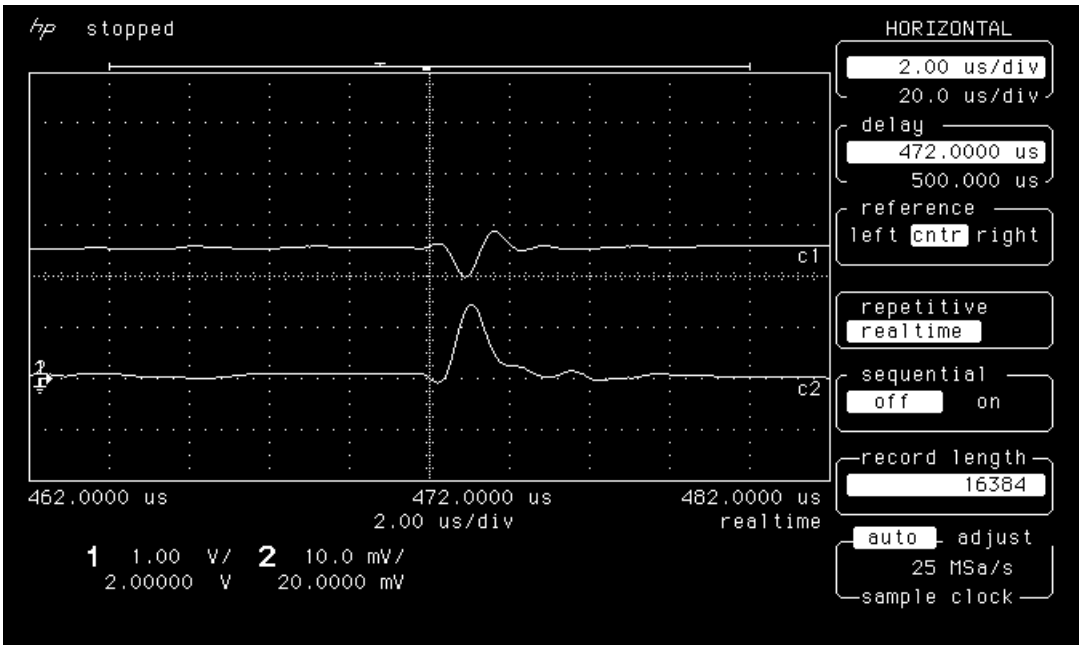

Figure 23e Close-up of 22d