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TOTAL IONIZATION DOSE TEST REPORT

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1.0 SUMMARY TABLE

A14100A Parametrics/Characteristics	Results
1. Functionality	Not tested to the limit, Passed 20krad(Si)
2. $I_{DDSTDBY}$	Passed 20krad(Si)
3. V_{IL}/V_{IH}	Passed 20krad(Si)
4. V_{OL}/V_{OH}	Passed 20krad(Si)
5. Propagation Delays	Passed 20krad(Si)
6. Rising/Falling Edge Transient	Passed 20krad(Si)
7. Startup Transient Current	Passed 20krad(Si)

2.0 TID TEST

This section describes the device under test (DUT), the irradiation parameters, and the testing method.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT14100A
Package	CQFP256
Foundry	MEC
Technology	0.8µm CMOS
Die Lot Number	UCL073
Quantity Tested	4
Serial Numbers	LAN2501, LAN2502, LAN2503, LAN2504

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA
Radiation Source	Co-60
Dose Rate	2krad(Si)/day (+-10%)
Final Total Dose	20krad(Si)
Temperature	Room
Bias	5V

2.3 TEST METHOD

The test method is in compliance with TM1019. It uses the biased room-temperature anneal to simulate the extremely slow-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous data showing ONO-based antifuse FPGAs fabricated in MEC foundry have no rebound effects (see, for example, the recent TID Report No. 98-T14100-2).

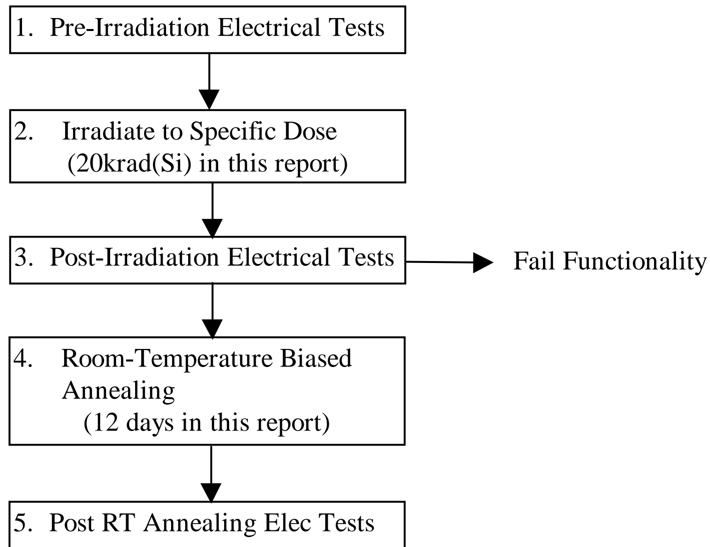

Figure 1. Test method flow chart.

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on the bench. Compared to an automatic tester, this bench setup has much lower noise. For AC/DC characteristic measurement, the automatic tester can measure every possible pin while the bench setup only samples few pins (due to logistics, not inability). However, since the total dose tolerance is always limited by the $I_{Ddstandby}$ (not by AC/DC characteristics), sampling pins for AC/DC characteristics should not affect the fidelity of the test. Also, $I_{DDstandby}$ is best measured by a bench setup. For example, the in-situ monitoring during irradiation in this report is logistically impossible for an automatic tester. An important but non-standard parameter, startup transient current, also can only be measured on the bench. The corresponding logic design circuit for each test parameter is listed in Table 3.

Table 3. Logic Design for each Measured Parameter/Characteristic

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Startup Transient Current	DUT power supply

3.0 TEST RESULTS

This section presents all the parameter/characteristic results for pre-irradiation (step 1 in Figure 1) and post room temperature anneal tests (step 5). The only post-irradiation (step 3) tests performed are the functionality test and output characteristics.

3.1 FUNCTIONAL TEST

Table 4 lists the functional test results.

Table 4. Functionality Test Results

	Pre-Irradiation	Post-Irradiation	Post-Anneal
LAN2501	passed	passed	passed
LAN2502	passed	passed	passed
LAN2503	passed	passed	passed
LAN2504	passed	passed	passed

3.2 IDDSTANDBY

$I_{DDstandby}$ (labeled I_{CC} in some Figures) was monitored during the irradiation and room-temperature annealing. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation/anneal effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. Thus the delta $I_{DDstandby}$ spec is approximately 25mA.

As shown in Figure 2, four DUTs, LAN2501, LAN2502, LAN2503 and LAN2504 were irradiation to just over 20krad(Si). The worst case is LAN2501, with final $I_{DDstandby}$ ~ 28mA. Since all DUTs passed post-irradiation functional test, per TM1019, room temperature and V_{CC} (5V) biased annealing can be performed to reduce the leakage current ($I_{DDstandby}$). Figure 3 shows the reduction of leakage with respect to annealing time. After 12 days anneal, all DUTs have $I_{DDstandby}$ less than 10mA.

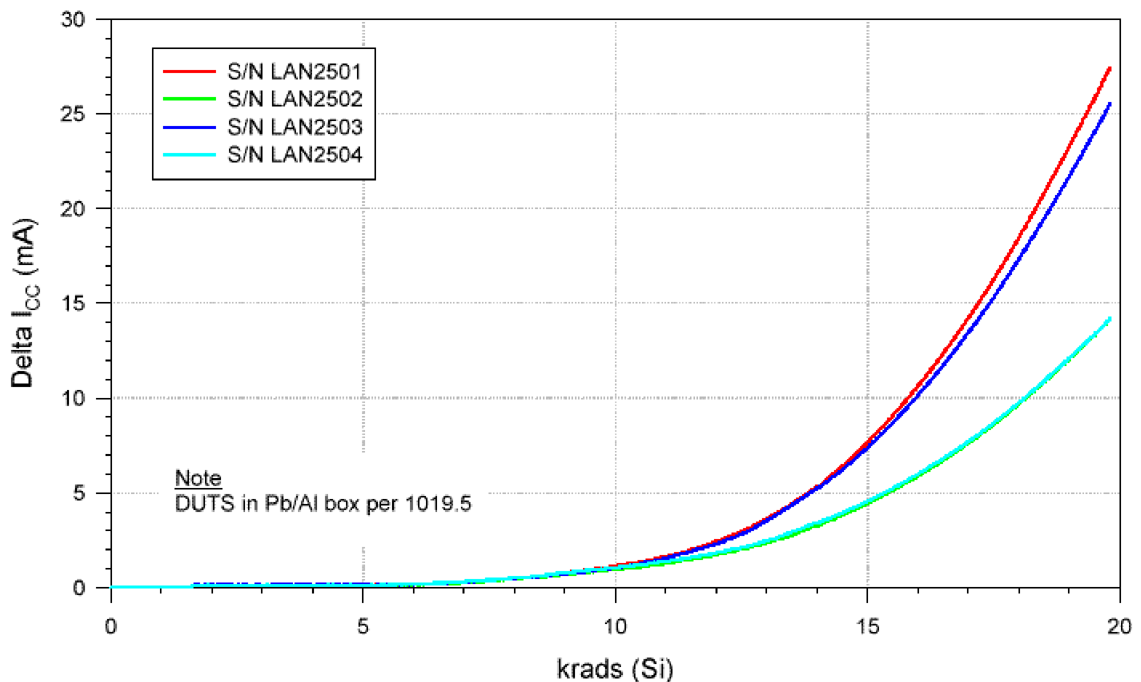

Figure 2. Delta $I_{DDstandby}$ versus total cumulative dose.

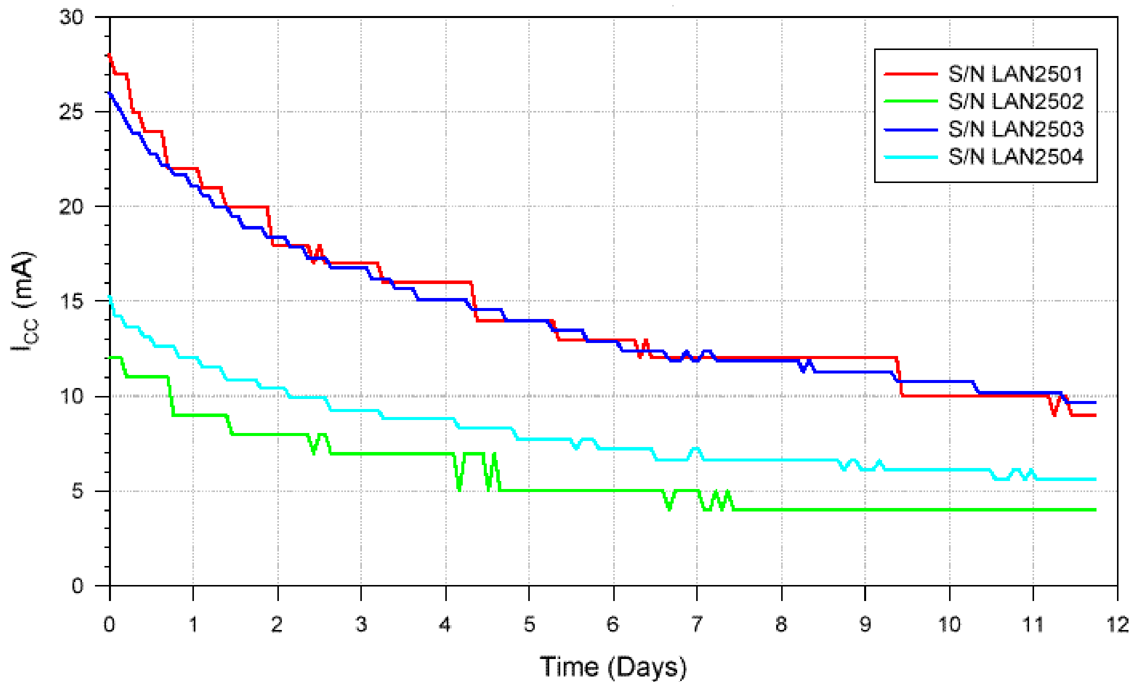

Figure 3. Showing the reduction of $I_{DDstanby}$ by room temperature annealing.

3.3 INPUT LOGIC THRESHOLD

Table 5 lists the input logic threshold of each DUT for pre-irradiation, and post room-temperature anneal.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results

	Pre-Irradiation	Post-Anneal
LAN2501	1.41V	1.41V
LAN2502	1.40V	1.40V
LAN2503	1.42V	1.41V
LAN2504	1.41V	1.43V

3.4 OUTPUT CHARACTERISTIC

Figure 4 shows the V_{OL} characteristic curve for the post-irradiation DUTs. All DUTs passed the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 6mA, V_{OL} cannot exceed 0.4V.

Figure 5 shows the V_{OH} characteristic curve for the post-irradiation DUTs. All DUTs passed the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 4mA, V_{OH} cannot be lower than 3.7V.

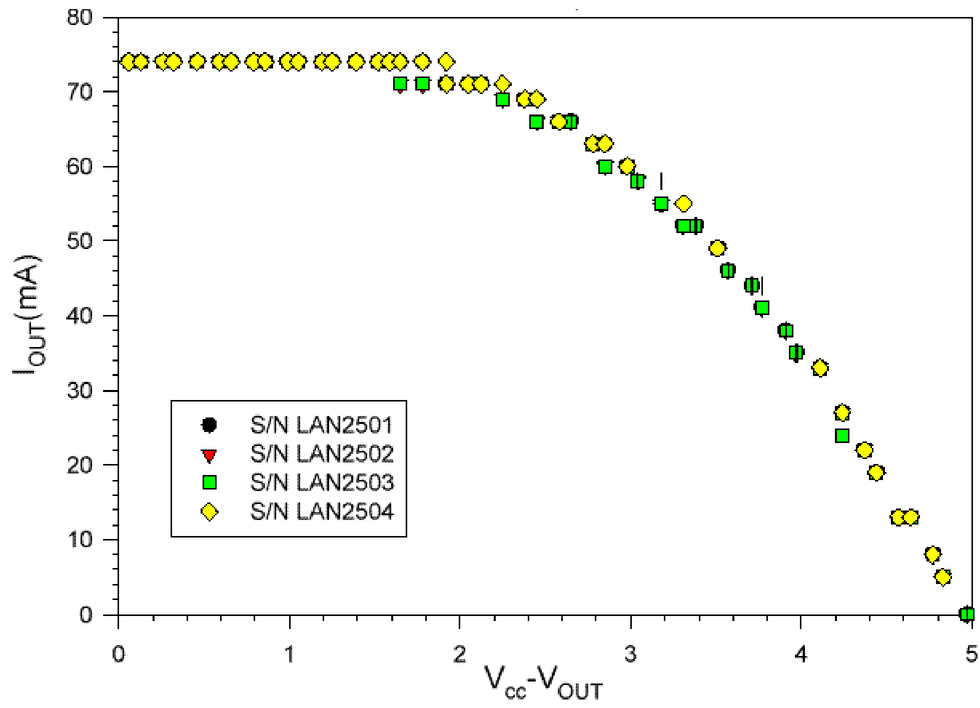

Figure 4 Post-irradiation V_{OL} characteristic curve.

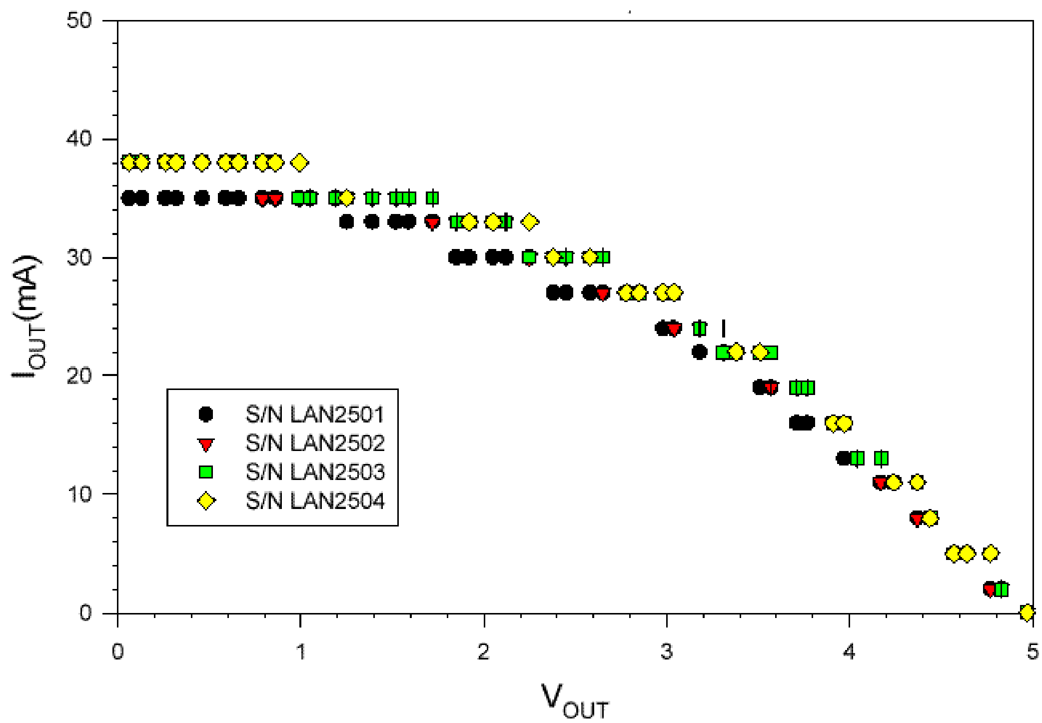

Figure 5 Post-irradiation V_{OH} characteristic curve

3.5 PROPAGATION DELAYS

Four types of propagation delays were measured, a combinational logic, the global clock to Q delay of a shift register, the hard-wired array clock (HCLK) to Q of a shift register, and I/O clock to Q of a shift register. The rising edge and falling edge were measured separately. Table 6, 7, 8, and 9 list the results. The variation due to irradiation/annealing effect is always well within 10%.

Table 6. Propagation Delay of Combinational Logic (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Anneal	Pre-Irradiation	Post-Anneal
LAN2501	428	437	430	441
LAN2502	434	442	437	447
LAN2503	439	448	441	453
LAN2504	429	442	432	438

Table 7. Global Clock to Q Delay (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Anneal	Pre-Irradiation	Post-Anneal
LAN2501	10.8	11.1	10.2	10.3
LAN2502	11.0	11.3	10.3	10.4
LAN2503	11.0	11.3	10.4	10.5
LAN2504	11.0	11.4	10.3	10.6

Table 8. H-Clock to Q Delay (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Anneal	Pre-Irradiation	Post-Anneal
LAN2501	9.7	9.8	8.9	9.1
LAN2502	9.7	9.8	8.8	9.0
LAN2503	9.4	9.8	8.7	9.3
LAN2504	9.6	9.6	8.7	9.1

Table 9. I/O Clock to Q Delay (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Anneal	Pre-Irradiation	Post-Anneal
LAN2501	9.7	9.8	8.9	9.1
LAN2502	9.7	9.8	8.8	9.0
LAN2503	9.4	9.8	8.7	9.3
LAN2504	9.6	9.6	8.7	9.1

3.6 RISING/FALLING EDGE TRANSIENT

The rising and falling edge transient of the output of a D flip-flop in the DUT were measured pre-irradiation and post-anneal. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The irradiation/annealing effect is basically negligible.

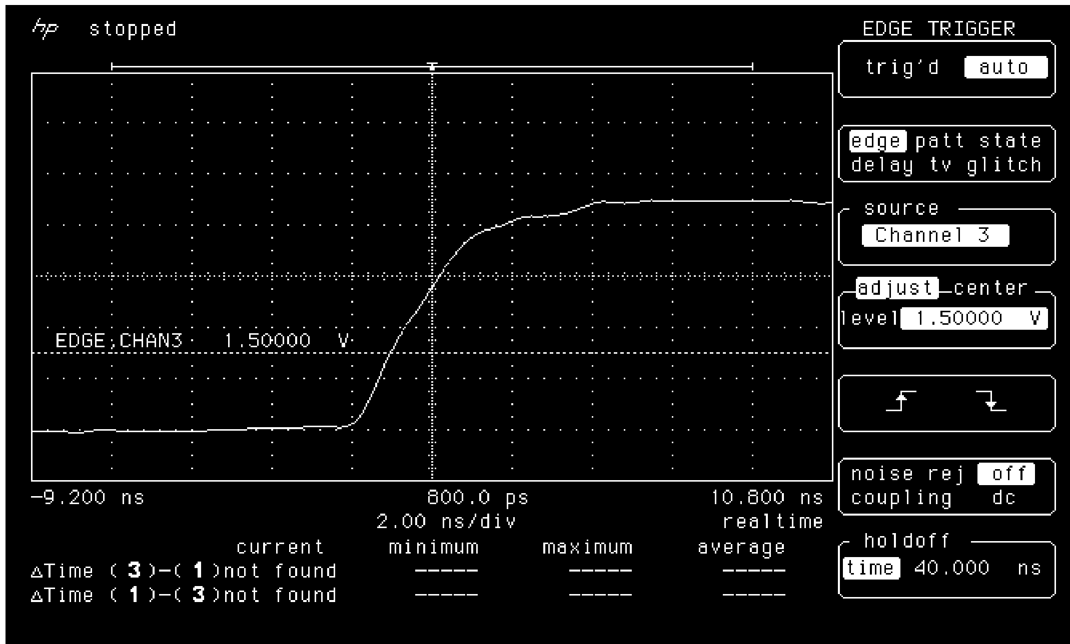

Figure 6a. Rising edge of LAN2501 pre-irradiation.

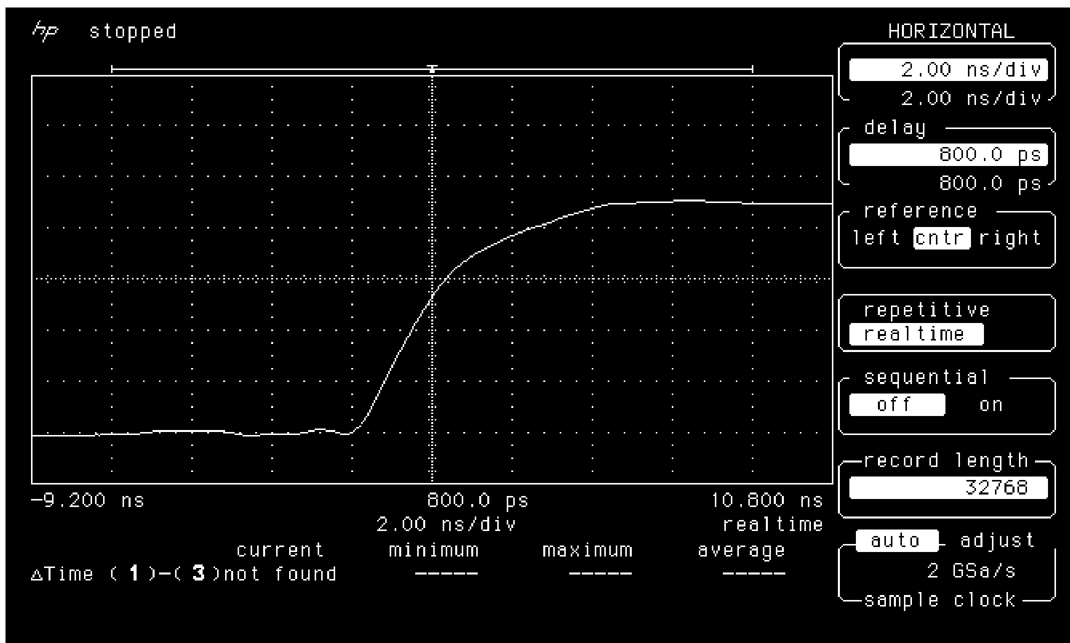

Figure 6b. Rising edge of LAN2501 post-anneal.

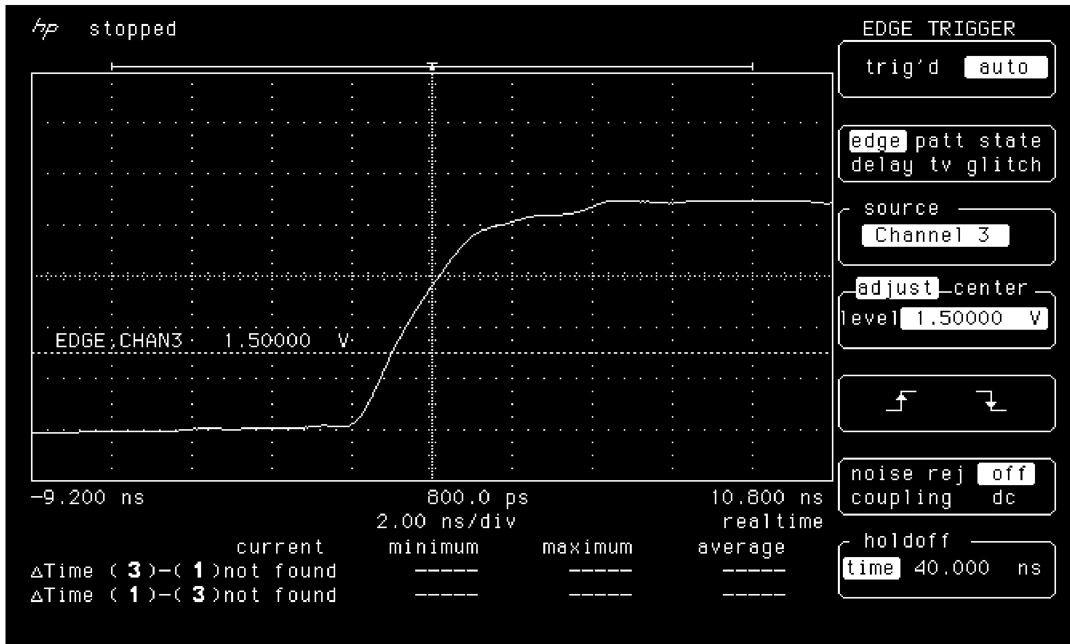

Figure 7a. Rising edge of LAN2502 pre-irradiation.

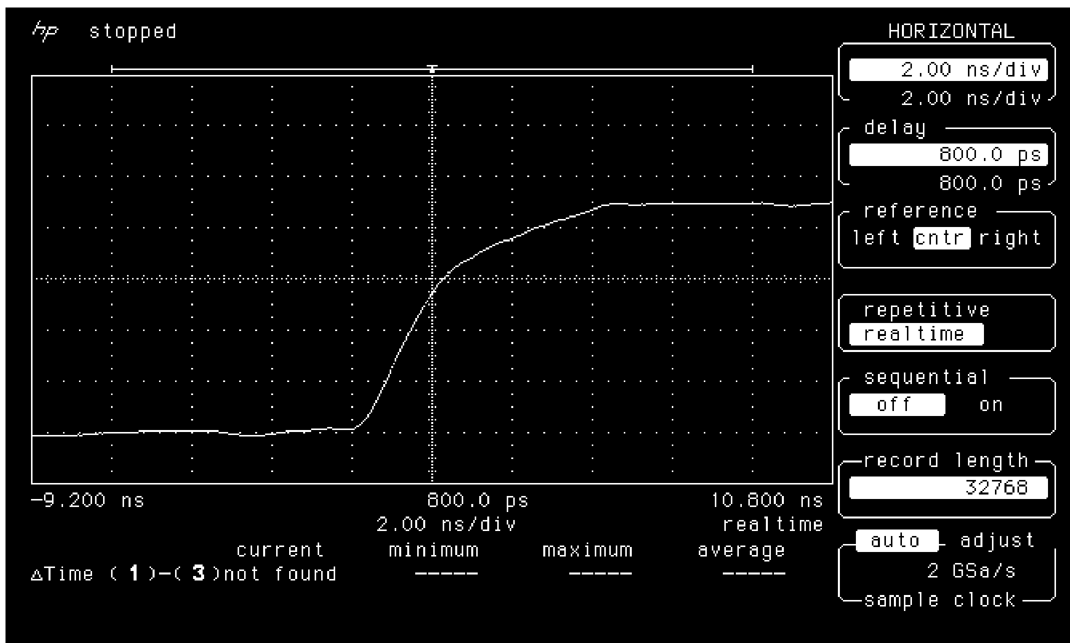

Figure 7b. Rising edge of LAN2502 post-anneal.

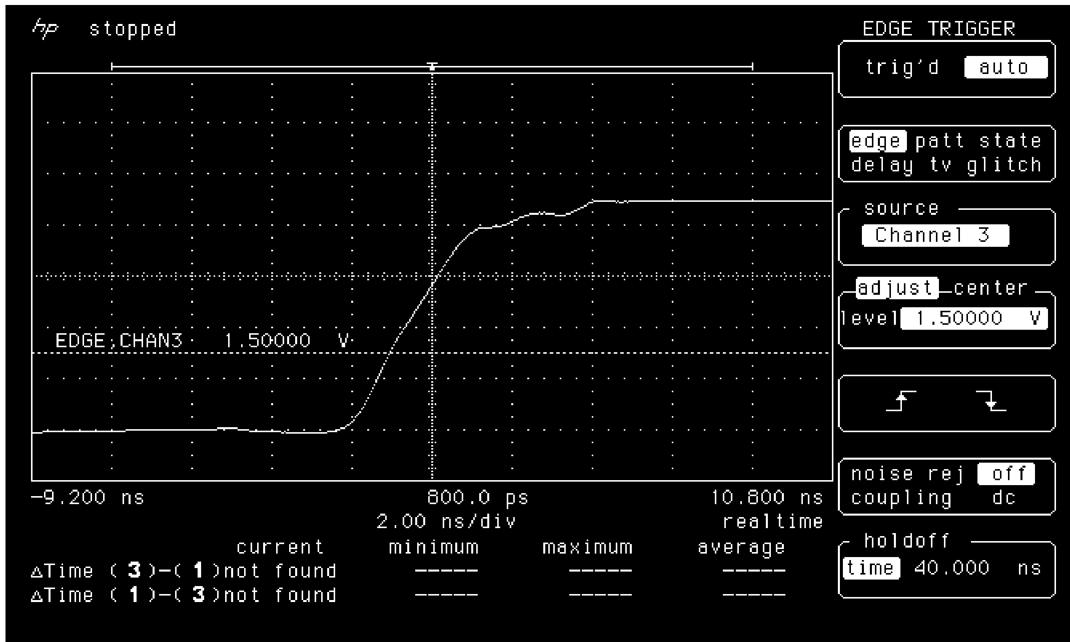

Figure 8a. Rising edge of LAN2503 pre-irradiation.

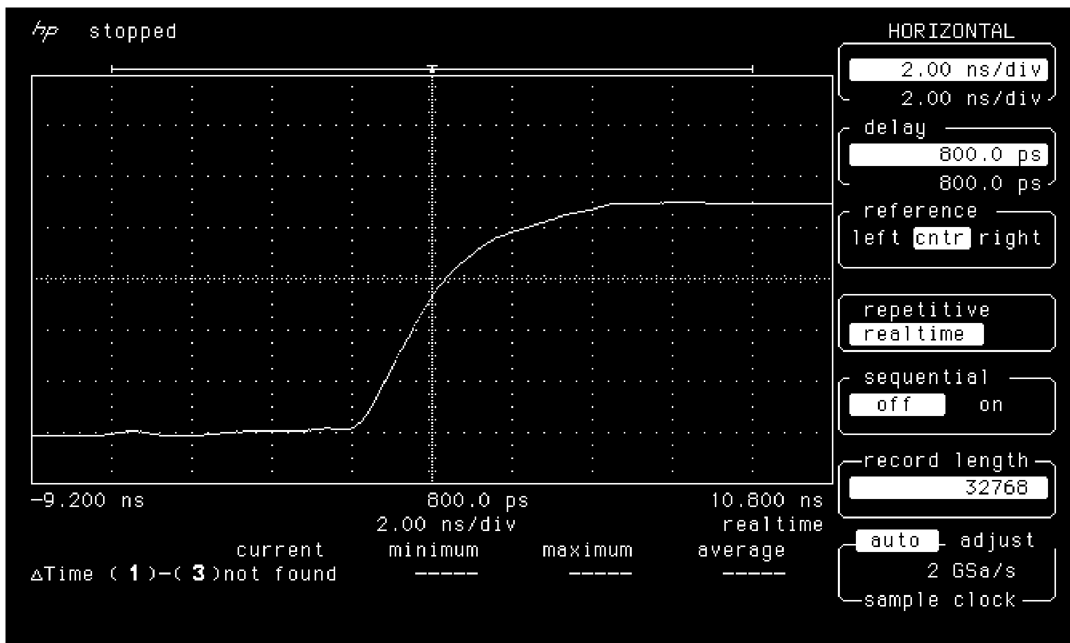

Figure 8b. Rising edge of LAN2503 post-anneal.

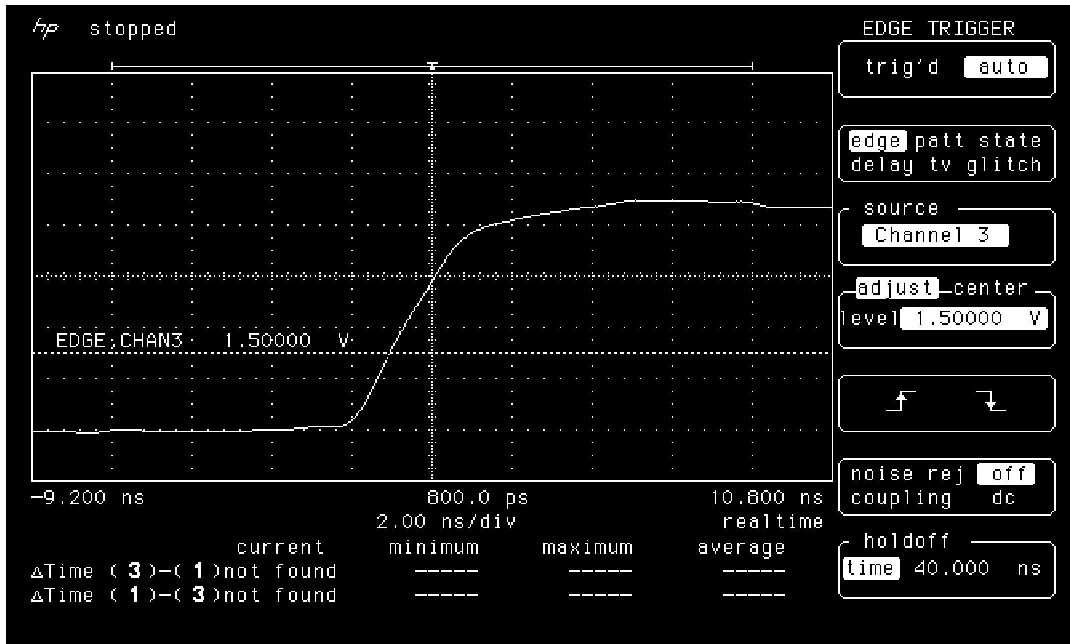

Figure 9a. Rising edge of LAN2504 pre-irradiation.

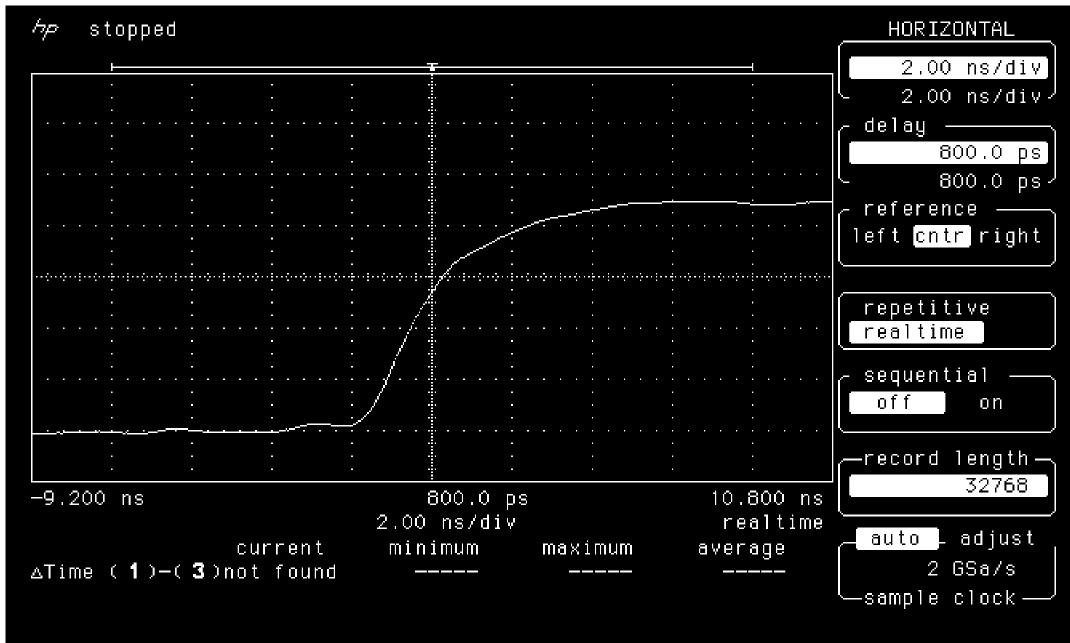

Figure 9b. Rising edge of LAN2504 post-anneal.

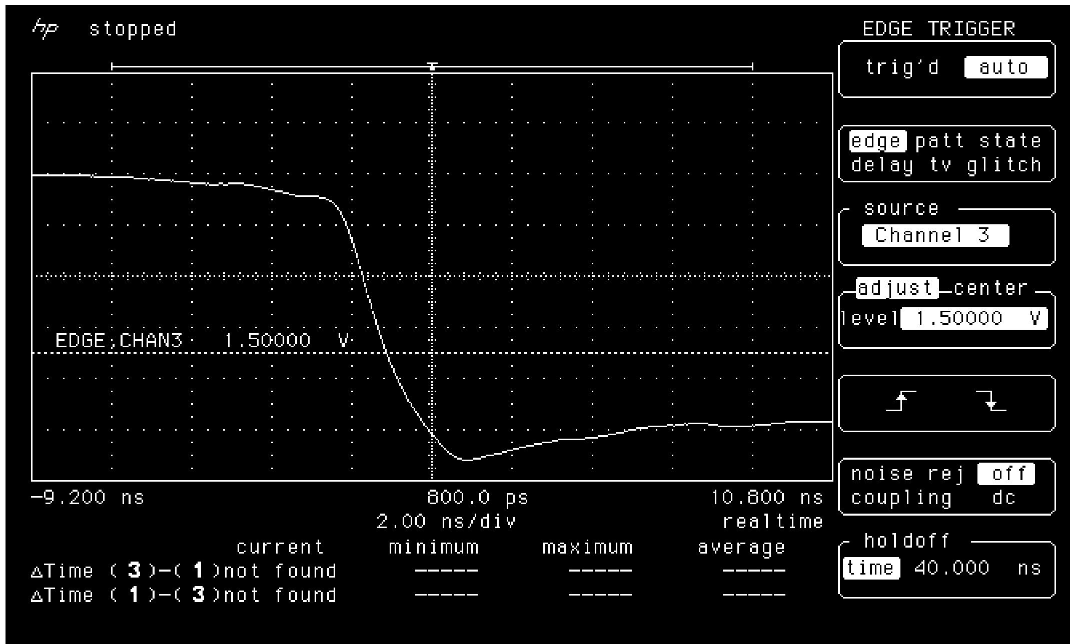

Figure 10a. Falling edge of LAN2501 pre-irradiation.

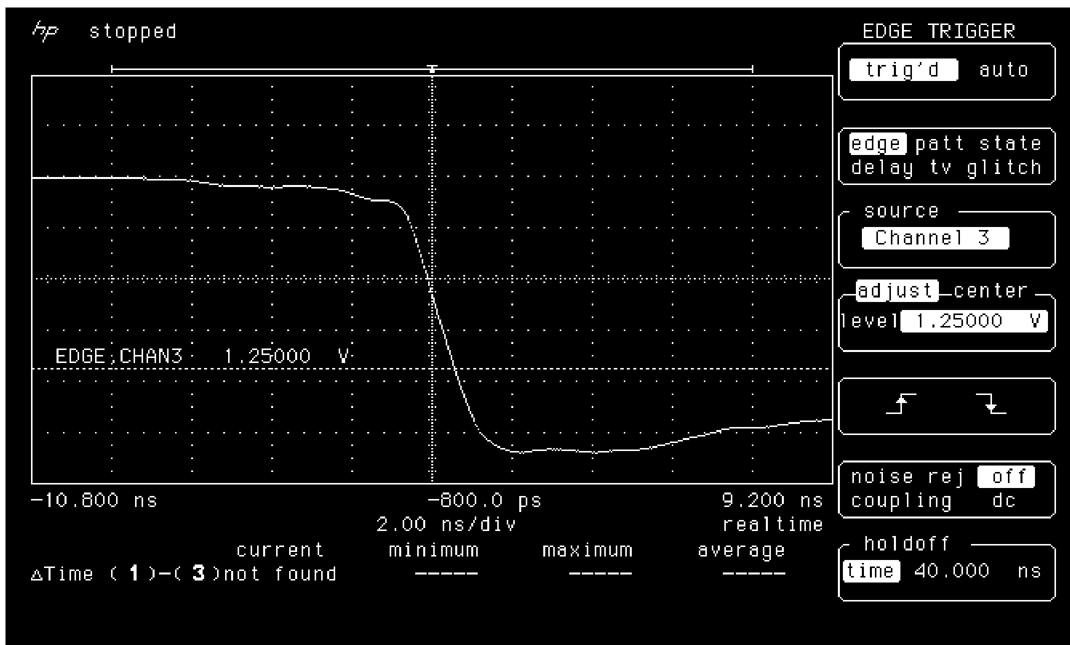

Figure 10b. Falling edge of LAN2501 post-anneal.

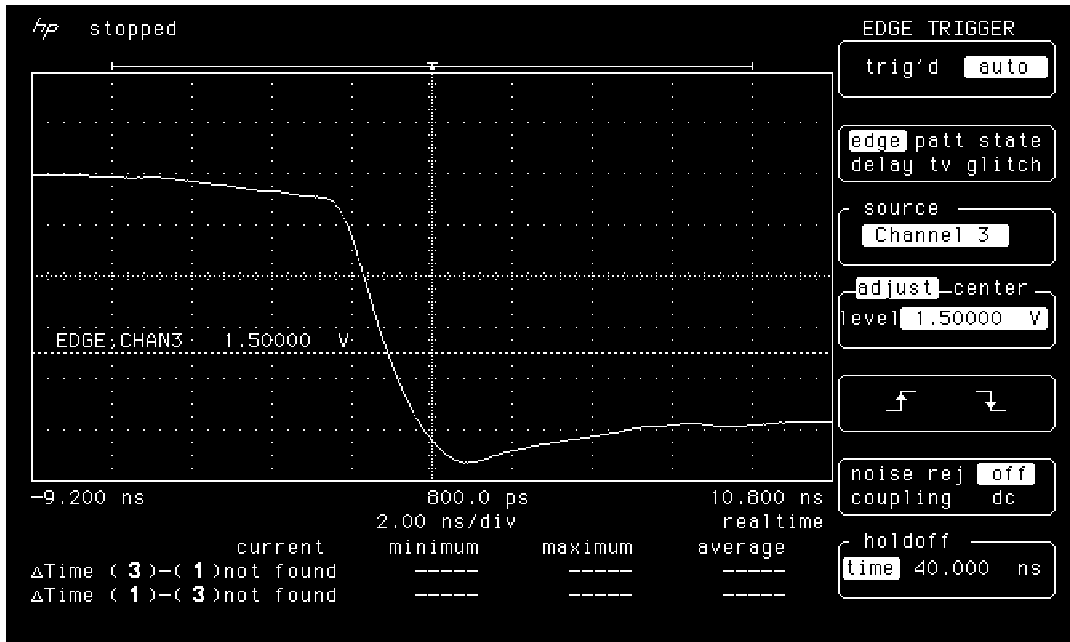

Figure 11a. Falling edge of LAN2502 pre-irradiation

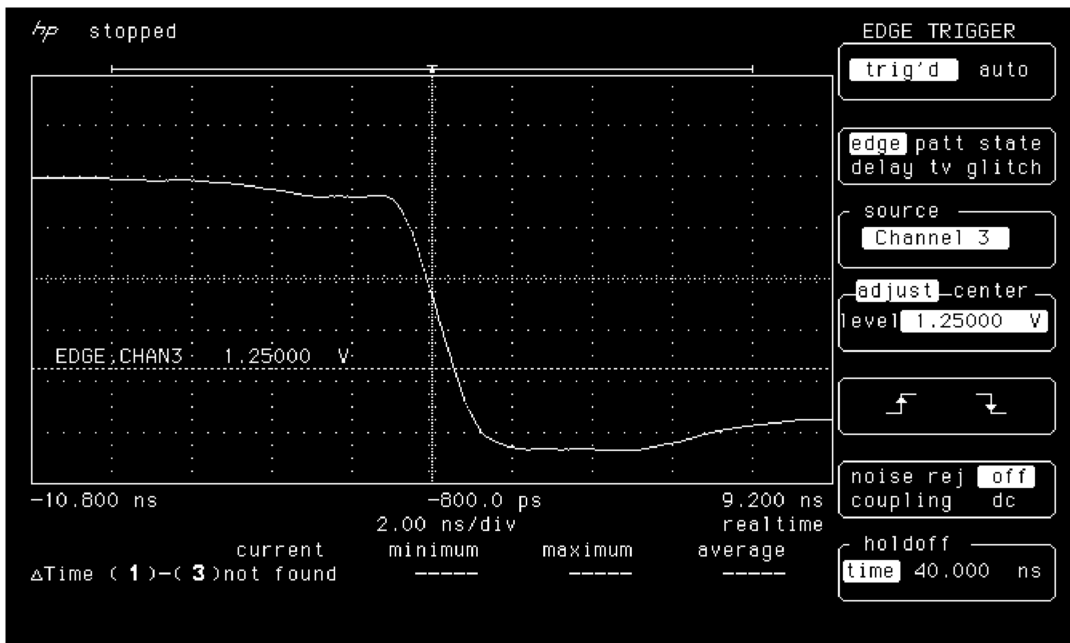

Figure 11b. Falling edge of LAN2502 post-anneal.

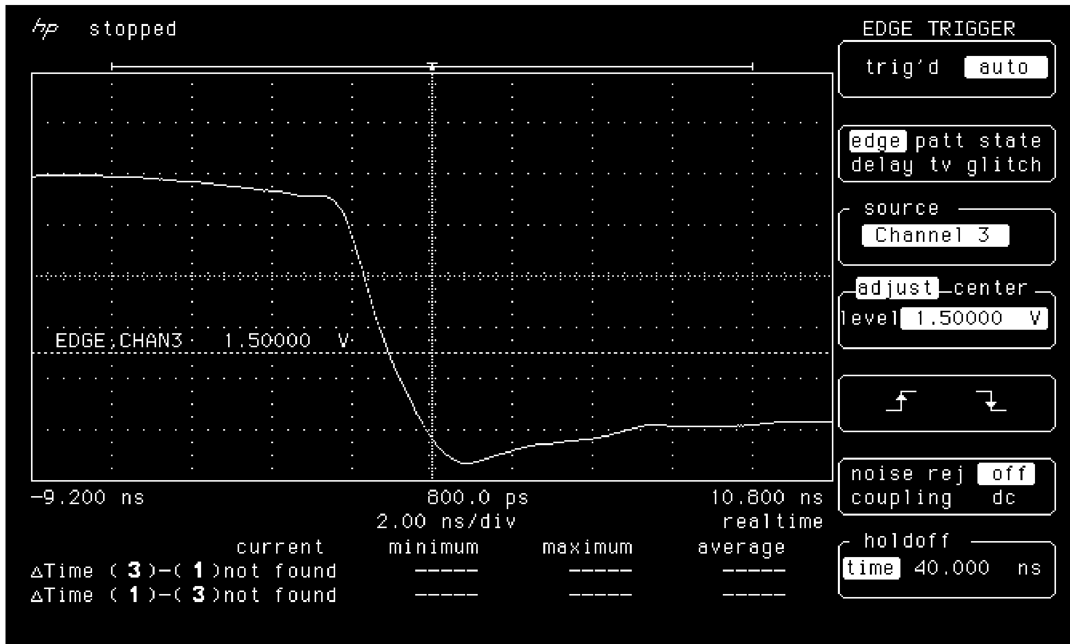

Figure 12a. Falling edge of LAN2503 pre-irradiation.

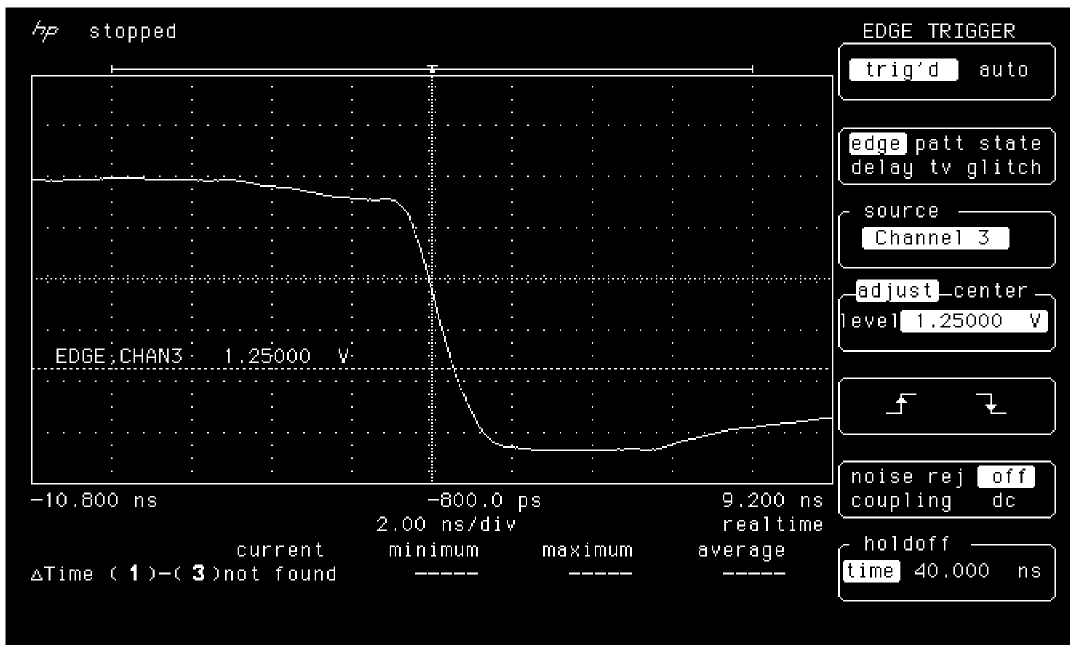

Figure 12b. Falling edge of LAN2503 post-anneal.

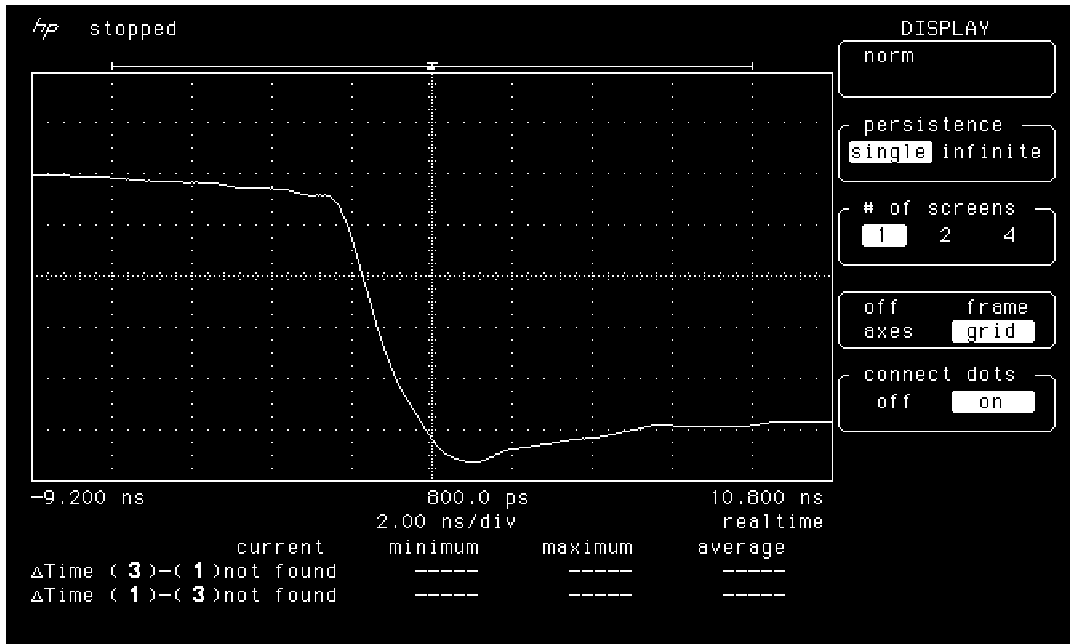

Figure 13a. Falling edge of LAN2504 pre-irradiation.

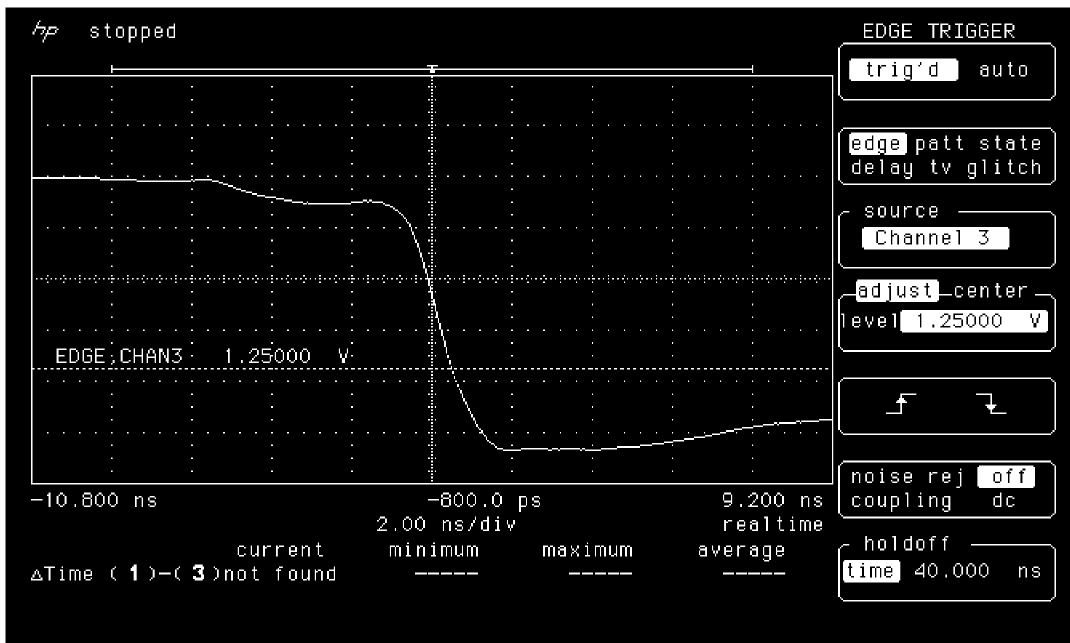

Figure 13b. Falling edge of LAN2504 post-anneal.

3.7 STARTUP TRANSIENT

In each measurement, the power supply (V_{CC}) rising time was set at 1.2ms. The board housing the DUT has minimum capacitance so that the transient current is all coming from the DUT. Figure 14-17 shows the oscilloscope picture of the startup transient of the DUTs. In each picture, there is a curve showing V_{CC} ramping from GND to 5V, and another curve showing I_{CC} which has a transient pulse at V_{CC} close to 3V. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. The transient pulse of I_{CC} is approximately 100mA peak pre-irradiation, 150mA post-anneal. The width is always less than 100µs. The irradiation/annealing (within 20krad(Si) total dose) does not significantly increase the transient pulse. Actually further annealing, although not necessary, will further reduce this startup transient.

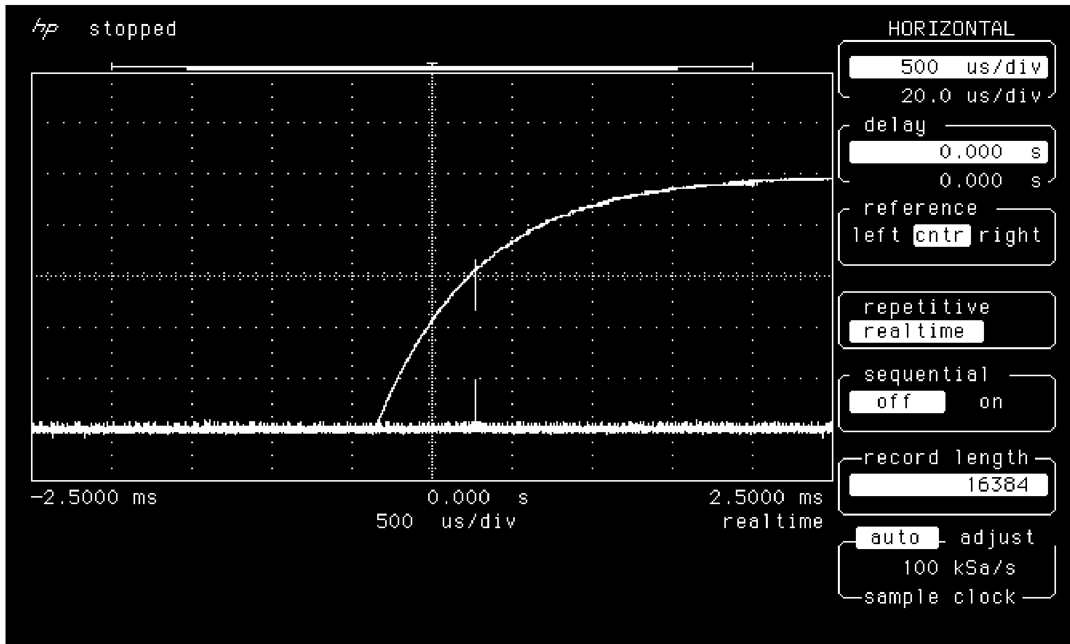

Figure 14a. Startup transient of LAN2501 pre-irradiation.

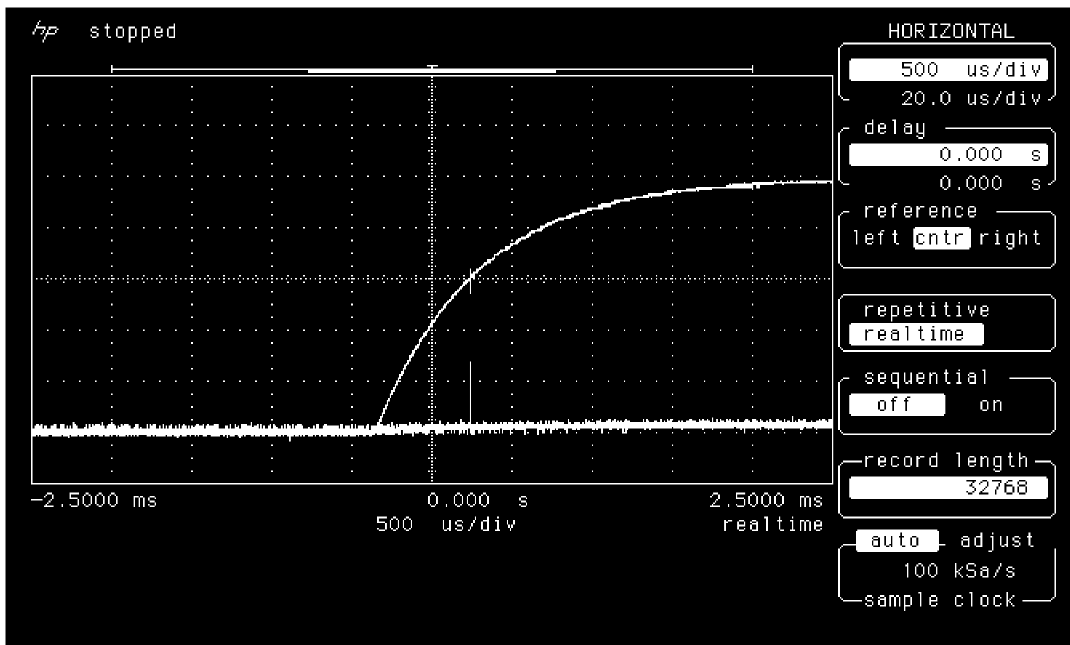

Figure 14b. Startup transient of LAN2501 post-anneal.

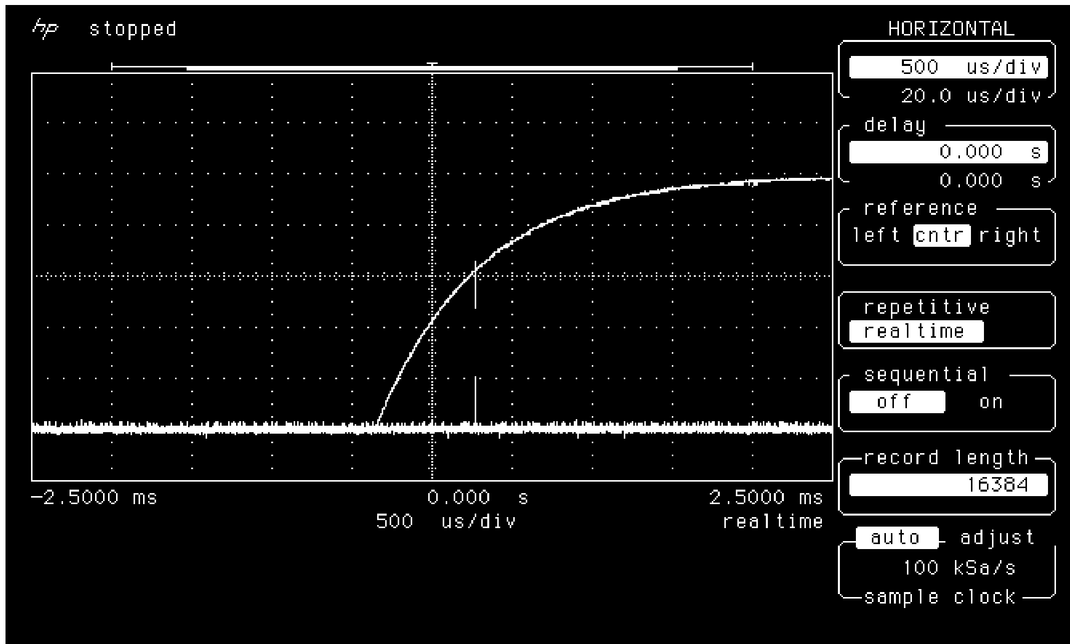

Figure 15a. Startup transient of LAN2502 pre-irradiation.

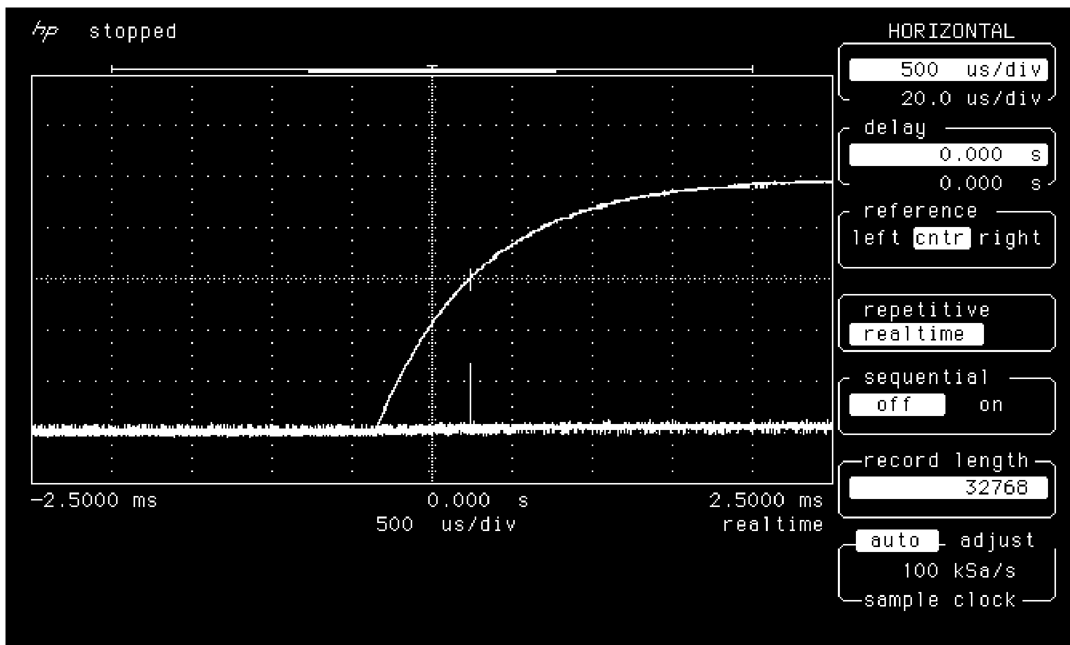

Figure 15b. Startup transient of LAN2502 post-anneal.

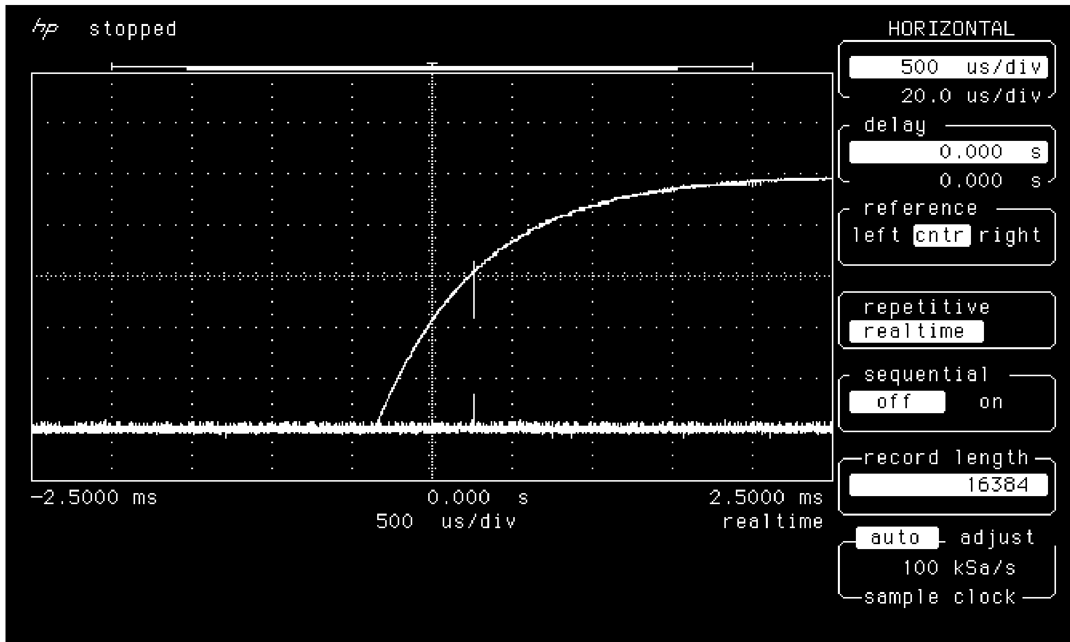

Figure 16a. Startup transient of LAN2503 pre-irradiation.

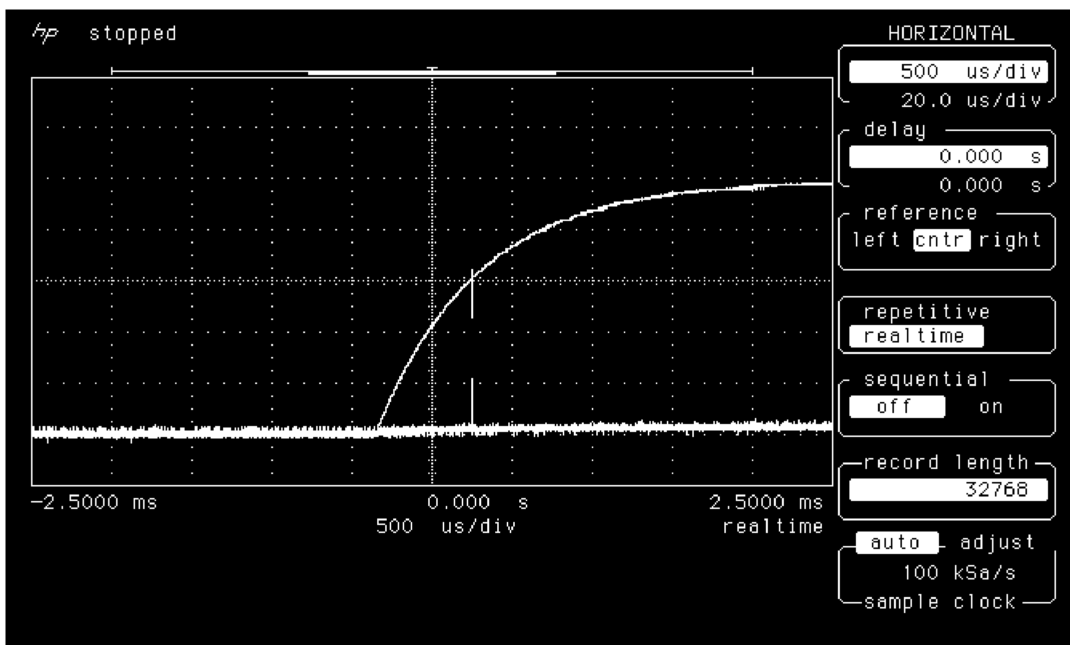

Figure 16b. Startup transient of LAN2503 post-anneal.

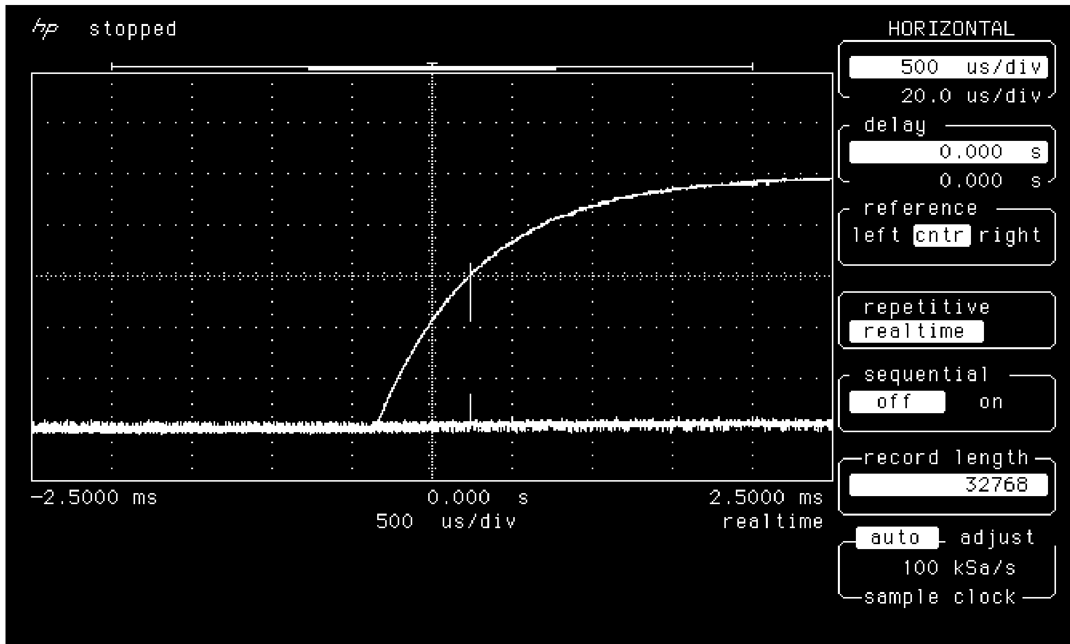

Figure 17a. Startup transient of LAN2504 pre-irradiation.

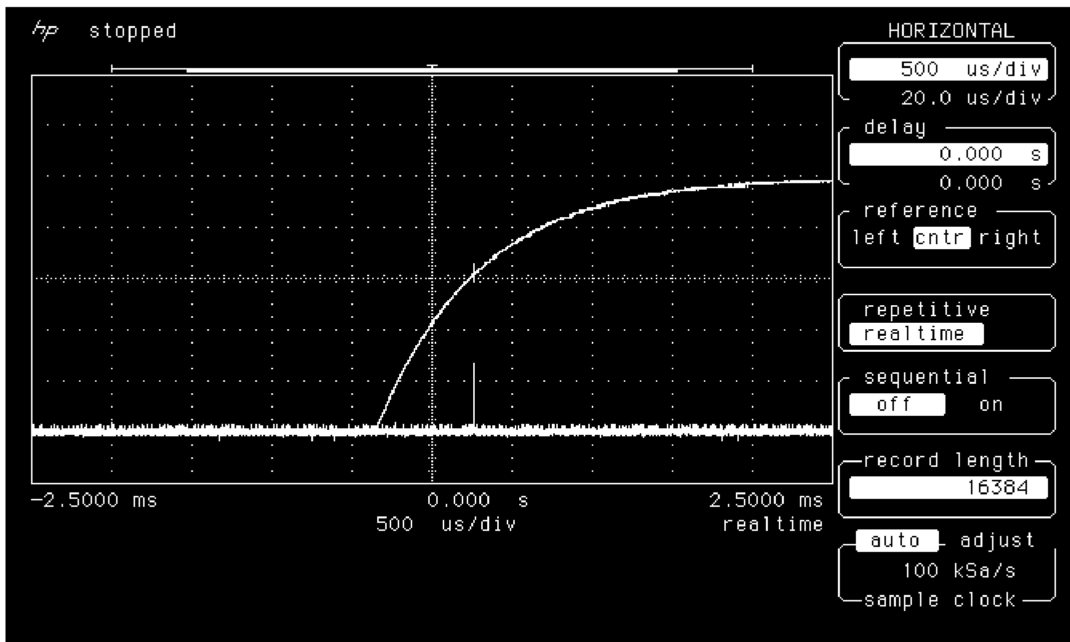

Figure 17b. Startup transient of LAN2504 post-anneal.