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TOTAL IONIZATION DOSE TEST REPORT

No. 98-RT1460-4
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1.0 SUMMARY TABLE

Parametrics/Characteristics	Results
1. Functionality	Functional up to 23 krad(Si) (Figure 2)
2. $I_{DDSTDBY}$	~ 20 mA after ~13 krad(Si) (Figure 2), < 5 mA after 12 krad(Si) + 280 hrs room temp anneal (Figure 3, 4)
3. V_{IL}/V_{IH}	Negligible change for 12 krad(Si) (Table x)
4. V_{OL}/V_{OH}	Not Available
5. Propagation Delays	Negligible change for 12 krad(Si) (Table x)
6. Start-up Transient	Negligible change for 12 krad(Si) (Figures x)
7. Rising/Falling Edge Transient	Negligible change for 12 krad(Si) (Figures x)

2.0 TID TEST

This section describes the device under test (DUT), the testing method, and the irradiation parameters.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1

Part Number	A1460A
Package	PGA
Foundry	MEC
Technology	0.8 um CMOS
Die Lot Number	UCK062
Date Code	9826
Quantity Tested	6
Serial Numbers	LAN 300, LAN301 (Control), LAN302, LAN303, LAN304, LAN305

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2

Facility	NASA
Radiation Source	Co-60
Dose Rate	6 krad(Si)/day (+-10%)
Final Total Dose for DC/AC Parameter Measurement	12 krad(Si)
Temperature	Room
Bias	5 V

2.3 TEST METHOD

The test method is basically a modified TM1019 suitable for space applications. Figure 1 shows its flow. Rebound annealing is omitted in this test flow. However, that doesn't affect the integrity of the test because there are enough data showing that Actel's FPGA had no rebound effect (see, for example, the most recent TID Report No. 98-T14100-2). One DUT (LAN300) was irradiated to find the boundary functional failure (Figure 2). After 23 krad(Si) of total cumulative dose, the irradiation was aborted because we felt the I_{DDSTDY} (marked I_{CC} on curve) was already too high.

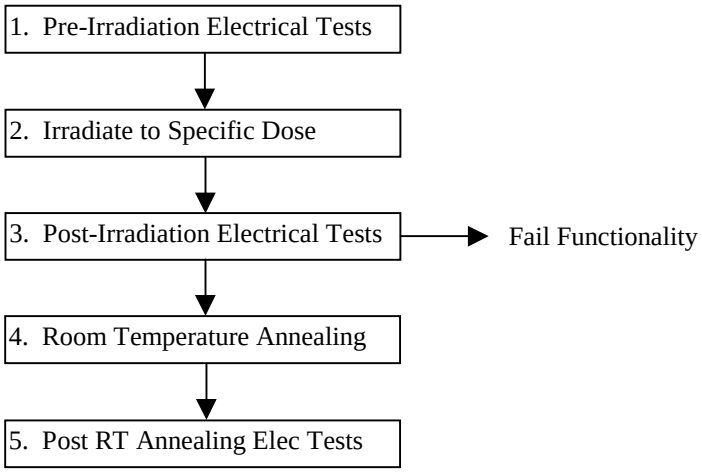

Figure 1. Test Method Flow Chart

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on bench with relative low noise. The corresponding logic design circuits (referring to Appendix) are listed in Table 3.

Table 3

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power line
3. V_{IL}/V_{IH}	IOPRECLR, monitored on IODIO19
4. V_{OL}/V_{OH} (Output I-V)	OUTX1
5. Propagation Delays	Input = INX1, Output = OUTX1
6. Start-up Transient	DUT power line
7. Rising/Falling Edge	QA0 (D flip-flop output)

3.0 TEST RESULTS

This section presents all the results of post irradiation tests (step 3 in Figure 1) and post room temperature annealing tests (step 5).

3.1 FUNCTIONAL TEST

Table 4 shows the test results matrix.

Table 4. Functionality Test

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN301	passed	passed	passed
LAN302	passed	passed	passed
LAN303	passed	passed	passed
LAN304	passed	passed	passed
LAN305	passed	passed	passed

3.2 IDDSTANDBY

$I_{DDstandby}$ was monitored during the irradiation and annealing period. Because the board had a measurable leakage, only the delta I_{DD} due to radiation and/or annealing was recorded. Using delta I_{DD} is quite appropriate since the pre-irradiation value of $I_{DDstandby}$ is only approximately 0.5 mA.

Figure 3 shows the delta $I_{DDstandby}$ curves versus total cumulative dose up to 12 krad(Si). At total dose of 12 krad(Si), the delta $I_{DDstandby}$ of every DUT is below 14 mA. Based on previous experiences, this is a save point to perform all the electrical tests with low risk of failure.

Although room-temperature annealing to reduce delta $I_{DDstandby}$ is not necessary from the qualification point of view, it was done for the sake of low-power design. Figure 4 shows the room temperature annealing characteristics in which delta $I_{DDstandby}$ dropped to less than 5 mA after approximately 280 hours of annealing.

3.3 INPUT LOGIC THRESHOLD

The input logic threshold (V_{IH}/V_{IL}) is tabulated in Table 5. The equipment limited the resolution to be only 0.1 V, which rendered the difference between V_{IH} and V_{IL} within the noise.

Table 5. Input Logic Threshold Voltage (V)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN301	1.45	1.44	1.44
LAN302	1.48	1.45	1.43
LAN303	1.48	1.44	1.43
LAN304	1.47	1.44	1.42
LAN305	1.44	1.42	1.42

3.4 OUTPUT I-V CHARACTERISTICS

The output characteristics were not measured in this lot because the operator forgot to do so.

3.5 PROPAGATION DELAYS

Rising and falling edge delays are shown in Table 6 and 7 respectively.

Table 6. Rising Edge Propagation Delays (ns)

	Pre-Irradiation	Post-Irradiation	RT Anneal

LAN301	619.8	617.8	619.6
LAN302	608.4	622.5	623.5
LAN303	599.6	613.0	615.0
LAN304	615.0	629.3	633.0
LAN305	617.8	634.5	636.2

Table 7. Falling Edge Propagation Delays (ns)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN301	617.7	616.0	617.6
LAN302	607.2	623.7	623.3
LAN303	598.0	614.6	615.2
LAN304	613.4	629.0	631.5
LAN305	616.5	636.0	636.4

3.6 STARTUP CURRENT TRANSIENT

The TID effect on startup current transient in Actel's FPGA was sometimes considered as a potential problem for spacecraft designers ["Total Dose Responses of Actel 1020B and 1280A Field Programmable Gate Arrays" by R. Katz et al, RADECS 95, p.412-p.419]. The recent study by NASA/GSFC and Actel showed strong dose rate dependence on this effect. Using dose rate much higher than space may draw an over-conservative conclusion about this particular characteristic. The recommendation is that if this is the limiting characteristic for the total dose tolerance, the post radiation room temperature annealing characteristic should be measured carefully. Since it's impractical to use the same dose rate as the real space environment, room temperature annealing after irradiation is always necessary.

The oscilloscope plots of startup current transient are shown in Figure 5 to 14. All the pictures in each Figure are the same measurement for the same part and arranged in the order of, from top, pre-irradiation, post-irradiation, and post room temperature annealing. C1 is the voltage with the scale of 1 volt/division and C2 the current with 100 mA/division. The overviews using time scale of 500 us/division show voltage and current glitches at about C1 = 3 V. The close-ups using time scale of 1 us/division show the details of the glitches. No significant radiation effect can be detected in any case for total dose of 12 krad(Si).

3.7 RISING/FALLING EDGE TRANSIENT

The TID effects on the rising and falling edge transient characteristics were also measured on a D flip-flop (QA0 in page 2 of Appendix). Figure 15 to 19 show oscilloscope pictures of the rising edge, and Figure 20 to 24 show the falling edge. The arrangement of pictures is the same as those in the last section. No significant radiation effects can be detected in any case for total dose of 12 krad(Si).

APPENDIX A: TEST PATTERN SCHEMATICS