Total Ionizing Dose Test Report

No. 12T-RTAX2000S-CQ256-D66PG1

December 20, 2012

Table of Contents

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 300 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Charateristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGA in http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded through a jumper; during annealing each input or output is tied to the ground or VCCI with a resistor. Appendix A contains the schematics of the irradiation-bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	EAQ_RTAX2000S_rev1
Die Lot Number	D66PG1
Quantity Tested	5
Serial Number	300 krad(SiO_2): 8371, 8377, 8378 200 krad(SiO_2): 8381, 8383
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

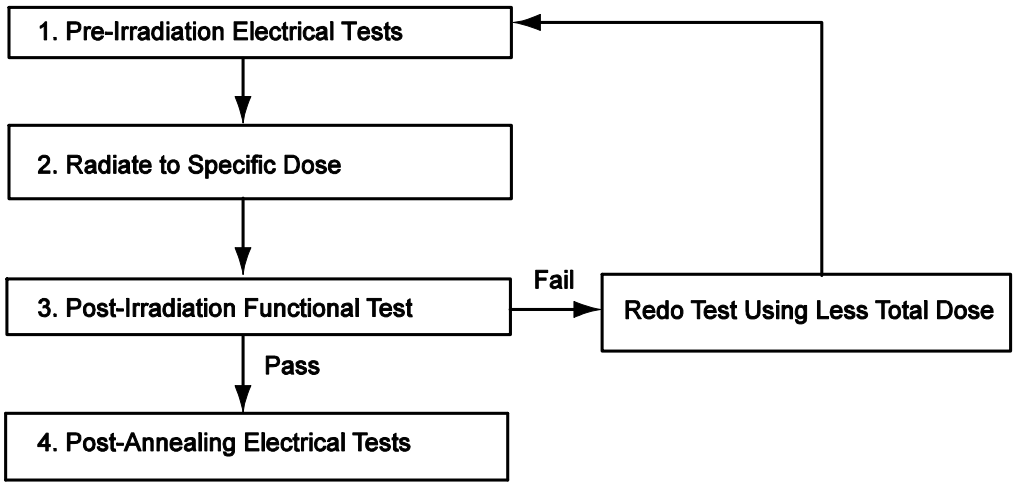


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000S are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 12 days.

C. Design and Parametric Measurements

The DUT uses a high utilization, generic design (EAQ_RTAX2000S_rev1) to evaluate total dose effects for typical space applications. Appendix B contains the schematics that illustrate this design.

Table 2 lists measured electrical parameters and the corresponding logic design. The functionality is measured on the output pins including the embedded RAM.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively.

The input logic threshold (VIL/VIH) is measured on inputs A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2, oe, Reset_n, Set_n, ShiftFrequency_0, ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1.

The output-drive voltage (VOL/VOH) is measured on Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0. The propagation delay is measured on the output of the buffer string; the definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output, are shown as oscilloscope captures.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key logic functions, and outputs of embedded RAM
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Inputs (A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2 , oe, Reset_n, Set_n, ShiftFrequency_0 , ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1)
4. Output Drive (V_{OL}/V_{OH})	Outputs (Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0)
5. Propagation Delay	String of buffers (IO_Clock to delay_out[0])
6. Transition Characteristic	String of buffers output (delay_out[0])

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT. Table 3 summarizes the pre-irradiation, post-irradiation and post-annealing ICC. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

Table 3 Pre-Irradiation, Post-Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad(SiO_2)	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
8371	300 krad	3	14	2	6	82	26
8377	300 krad	3	22	3	8	82	25
8378	300 krad	2	27	2	8	122	27
8381	200 krad	2	3	2	8	31	11
8383	200 krad	5	8	6	6	29	10

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the RTAXS datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT. Based on these PIPL, post-annealed DUT passes both the ICCA and ICCI specification for 300 krad (SiO2).

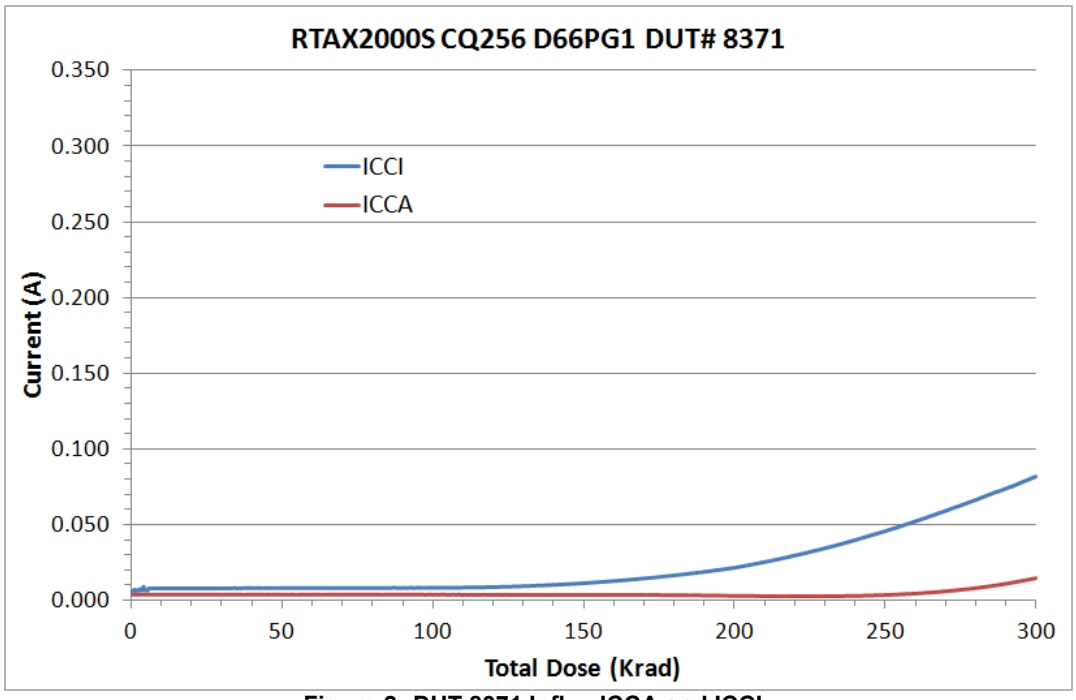


Figure 2 DUT 8371 Influx ICCA and ICCI

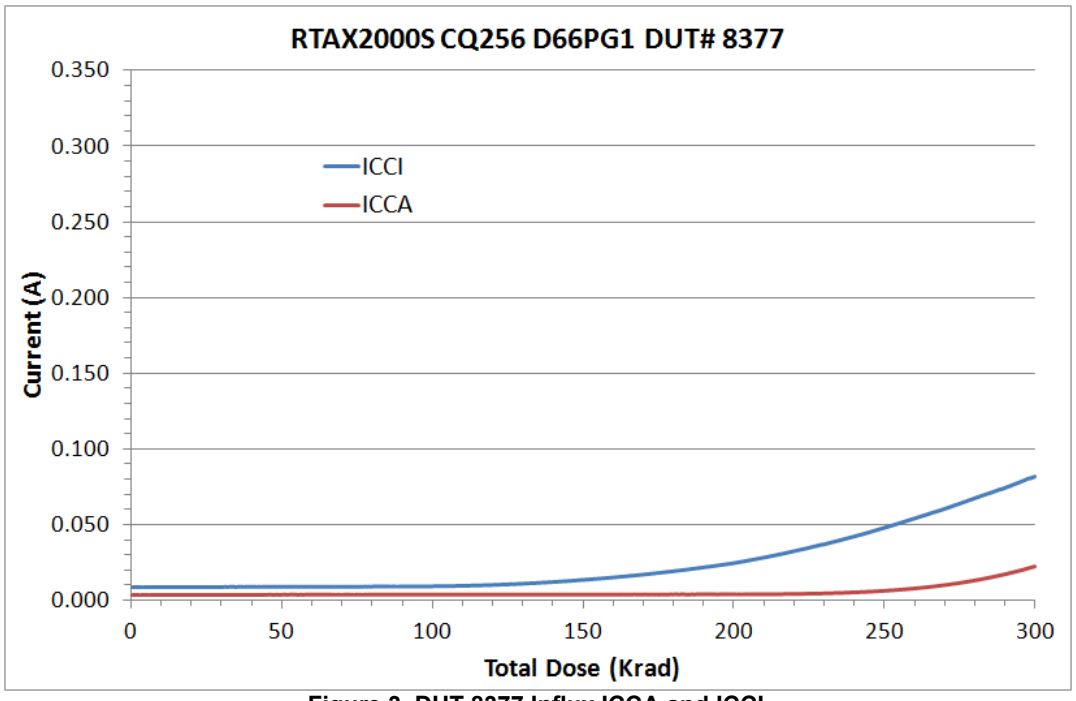


Figure 3 DUT 8377 Influx ICCA and ICCI

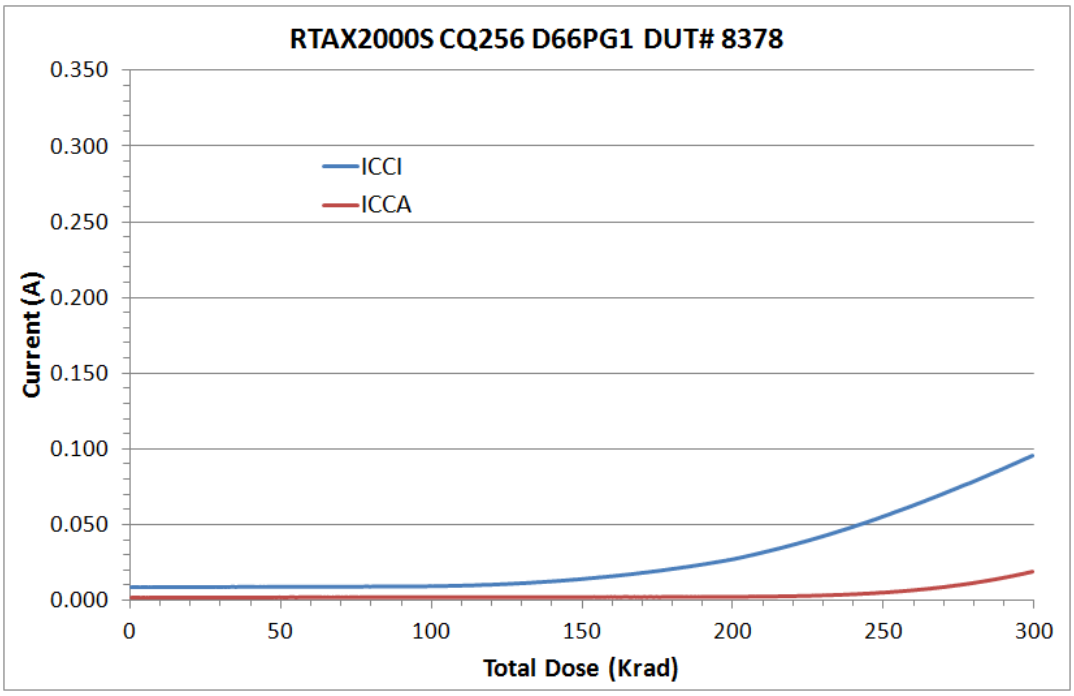


Figure 4 DUT 8378 Influx ICCA and ICCI

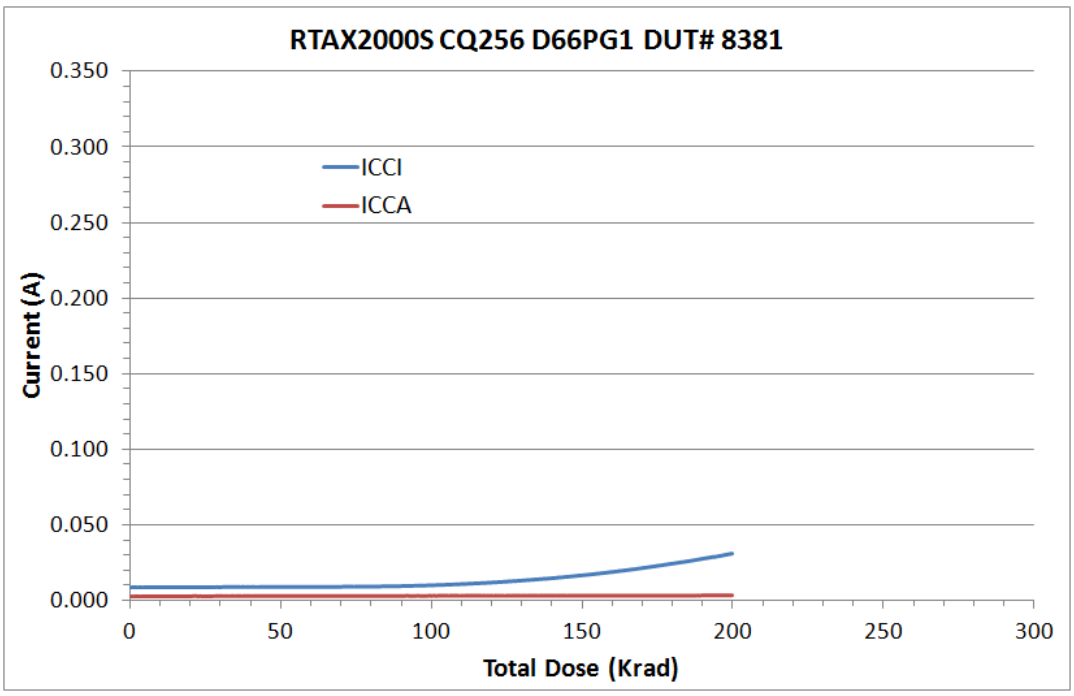


Figure 5 DUT 8381 Influx ICCA and ICCI

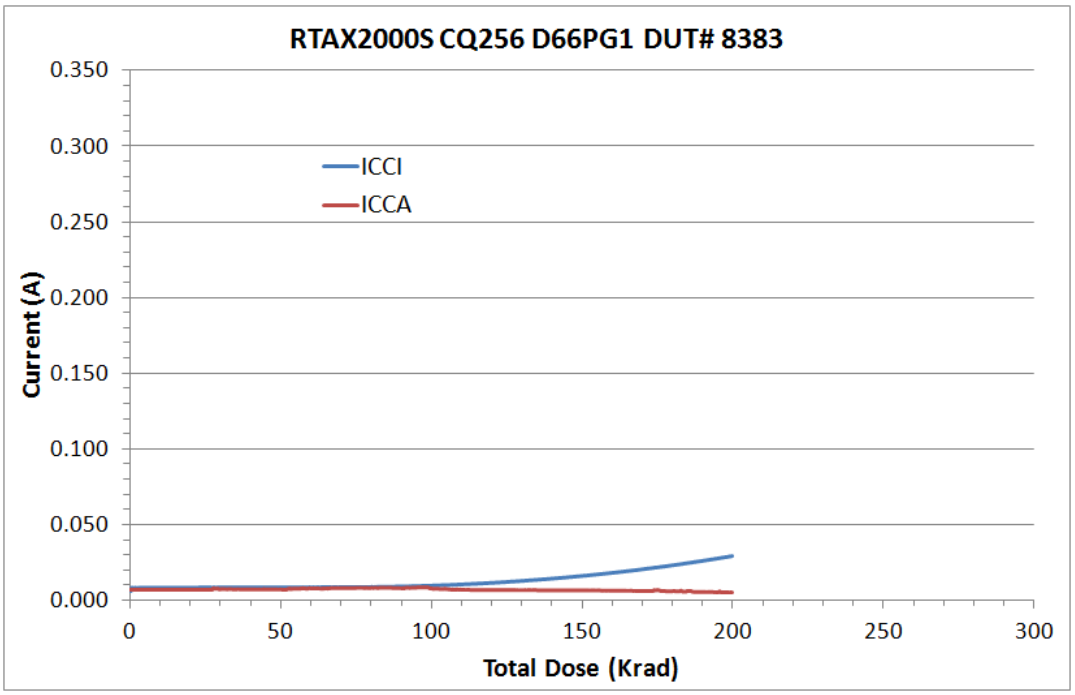


Figure 6 DUT 8383 Influx ICCA and ICCI

C. Input Threshold VIL

Table 4 lists the pre-irradiation and post-annealing single-ended input threshold. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds VIL (V)

Pin\DUT	8371 (300 krad)		8377 (300 krad)		8378 (300 krad)		8381 (200 krad)		8383 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.360	1.355	1.365	1.355	1.365	1.355	1.365	1.360	1.365	1.360
A_Johnson	1.360	1.355	1.355	1.350	1.360	1.355	1.360	1.355	1.360	1.355
A_Pattern_Length_0	1.370	1.360	1.365	1.360	1.370	1.360	1.375	1.365	1.370	1.365
A_Pattern_Length_1	1.375	1.365	1.370	1.365	1.370	1.360	1.375	1.365	1.375	1.365
A_Pattern_Length_2	1.365	1.355	1.360	1.355	1.365	1.355	1.370	1.360	1.365	1.360
IO_Clock	1.360	1.355	1.355	1.350	1.355	1.355	1.360	1.355	1.360	1.355
IO_Johnson	1.370	1.365	1.370	1.360	1.370	1.360	1.375	1.370	1.370	1.365
IO_Pattern_Length_0	1.360	1.355	1.360	1.355	1.360	1.355	1.365	1.360	1.360	1.355
IO_Pattern_Length_1	1.360	1.355	1.355	1.350	1.360	1.355	1.365	1.355	1.360	1.355
IO_Pattern_Length_2	1.365	1.360	1.365	1.355	1.370	1.360	1.370	1.365	1.370	1.365
oe	1.365	1.355	1.365	1.355	1.365	1.355	1.370	1.360	1.370	1.360
Reset_n	1.365	1.360	1.365	1.355	1.365	1.360	1.370	1.360	1.365	1.360
Set_n	1.355	1.350	1.355	1.350	1.355	1.350	1.355	1.350	1.355	1.355
ShiftFrequency_0	1.365	1.360	1.365	1.360	1.360	1.355	1.370	1.360	1.370	1.365
ShiftFrequency_1	1.365	1.355	1.360	1.355	1.360	1.355	1.370	1.360	1.365	1.360
TOG_n	1.365	1.355	1.365	1.355	1.365	1.355	1.370	1.360	1.370	1.360
zoom	1.360	1.355	1.360	1.355	1.365	1.360	1.365	1.360	1.365	1.360
zoom_sel_n_0	1.365	1.345	1.360	1.340	1.360	1.345	1.370	1.355	1.370	1.355
zoom_sel_n_1	1.360	1.345	1.360	1.340	1.360	1.340	1.365	1.350	1.365	1.350

D. Input Threshold VIH

Table 5 lists the input threshold voltage changes due to irradiations. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing Input Thresholds VIH (V)

Pin\DUT	8371 (300 krad)		8377 (300 krad)		8378 (300 krad)		8381 (200 krad)		8383 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.625	1.620	1.630	1.620	1.625	1.620	1.635	1.625	1.630	1.625
A_Johnson	1.650	1.640	1.650	1.635	1.650	1.640	1.655	1.645	1.655	1.640
A_Pattern_Length_0	1.640	1.630	1.635	1.625	1.640	1.630	1.645	1.635	1.640	1.630
A_Pattern_Length_1	1.645	1.630	1.640	1.630	1.640	1.630	1.645	1.635	1.645	1.635
A_Pattern_Length_2	1.655	1.640	1.655	1.640	1.660	1.640	1.665	1.650	1.660	1.645
IO_Clock	1.650	1.640	1.650	1.640	1.650	1.640	1.655	1.645	1.655	1.640
IO_Johnson	1.640	1.630	1.640	1.625	1.640	1.630	1.650	1.640	1.640	1.630
IO_Pattern_Length_0	1.650	1.640	1.650	1.635	1.650	1.640	1.660	1.645	1.650	1.640
IO_Pattern_Length_1	1.650	1.640	1.650	1.635	1.655	1.640	1.660	1.645	1.655	1.640
IO_Pattern_Length_2	1.635	1.625	1.635	1.620	1.640	1.630	1.645	1.630	1.645	1.630
oe	1.630	1.620	1.630	1.620	1.630	1.620	1.635	1.625	1.635	1.625
Reset_n	1.630	1.620	1.630	1.620	1.630	1.620	1.635	1.625	1.630	1.620
Set_n	1.645	1.635	1.645	1.635	1.650	1.635	1.650	1.640	1.650	1.635
ShiftFrequency_0	1.630	1.620	1.635	1.620	1.630	1.620	1.635	1.625	1.635	1.625
ShiftFrequency_1	1.630	1.620	1.630	1.620	1.625	1.615	1.635	1.625	1.635	1.625
TOG_n	1.630	1.620	1.630	1.620	1.630	1.620	1.635	1.630	1.635	1.625
zoom	1.625	1.620	1.630	1.620	1.630	1.625	1.635	1.630	1.635	1.625
zoom_sel_n_0	1.650	1.625	1.650	1.620	1.650	1.625	1.660	1.635	1.660	1.635
zoom_sel_n_1	1.655	1.625	1.650	1.620	1.650	1.625	1.660	1.635	1.660	1.635

E. Output-Drive Voltage (VOL)

The pre-irradiation and post-annealing VOL are listed in Table 6. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 6 Pre-Irradiation and Post-Annealing Output-Drive VOL (mV)

Pin\DUT	8371 (300 krad)		8377 (300 krad)		8378 (300 krad)		8381 (200 krad)		8383 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	185.5	179.8	187.7	181.3	187.6	180.5	191.8	185.1	186.7	181.3
Array_out_0	178.6	173.3	180.7	174.7	180.3	174.0	184.2	178.3	179.4	174.6
delay_out_0	184.6	175.8	186.3	175.3	185.4	174.6	188.8	178.4	186.2	177.4
Global_Monitor	187.8	181.5	189.7	182.8	189.3	182.6	193.3	186.9	188.0	182.9
IO_Monitor	182.1	175.8	184.7	177.4	184.1	176.5	188.3	180.8	182.9	177.2
IO_Outs_0	182.3	179.9	184.5	181.4	184.9	181.8	182.5	178.9	181.6	178.8
RAM_Monitor	189.9	182.9	191.0	183.7	191.1	184.4	195.0	187.9	190.4	185.3
RAM_out_0	188.9	185.5	191.2	187.0	189.4	185.5	191.0	188.1	190.0	187.3

F. Output-Drive Voltage (VOH)

The pre-irradiation and post-annealing VOH are listed in Table 7. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 7 Pre-Irradiation and Post-Annealing Output-Drive VOH (mV)

Pin\DUT	8371 (300 krad)		8377 (300 krad)		8378 (300 krad)		8381 (200 krad)		8383 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	2724	2718	2723	2717	2723	2718	2724	2720	2725	2722
Array_out_0	2729	2723	2729	2722	2729	2723	2729	2726	2731	2726
delay_out_0	2728	2727	2728	2726	2729	2728	2729	2730	2729	2730
Global_Monitor	2722	2716	2721	2715	2721	2716	2722	2718	2723	2720
IO_Monitor	2725	2720	2725	2719	2726	2721	2726	2723	2727	2724
IO_Outs_0	2726	2723	2726	2722	2724	2721	2729	2727	2728	2726
RAM_Monitor	2719	2714	2720	2714	2719	2714	2720	2716	2720	2717
RAM_out_0	2726	2717	2725	2715	2727	2717	2728	2721	2728	2720

G. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The irradiation was temporarily stopped at each total-dose increment of 100 krad for the measurement. Each measurement has a 2-minute wait after a DUT is removed from the chamber. The results are plotted in Figure 7, and listed in Table 8. As shown in Figure 7, the propagation delay initially decreases with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots, a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

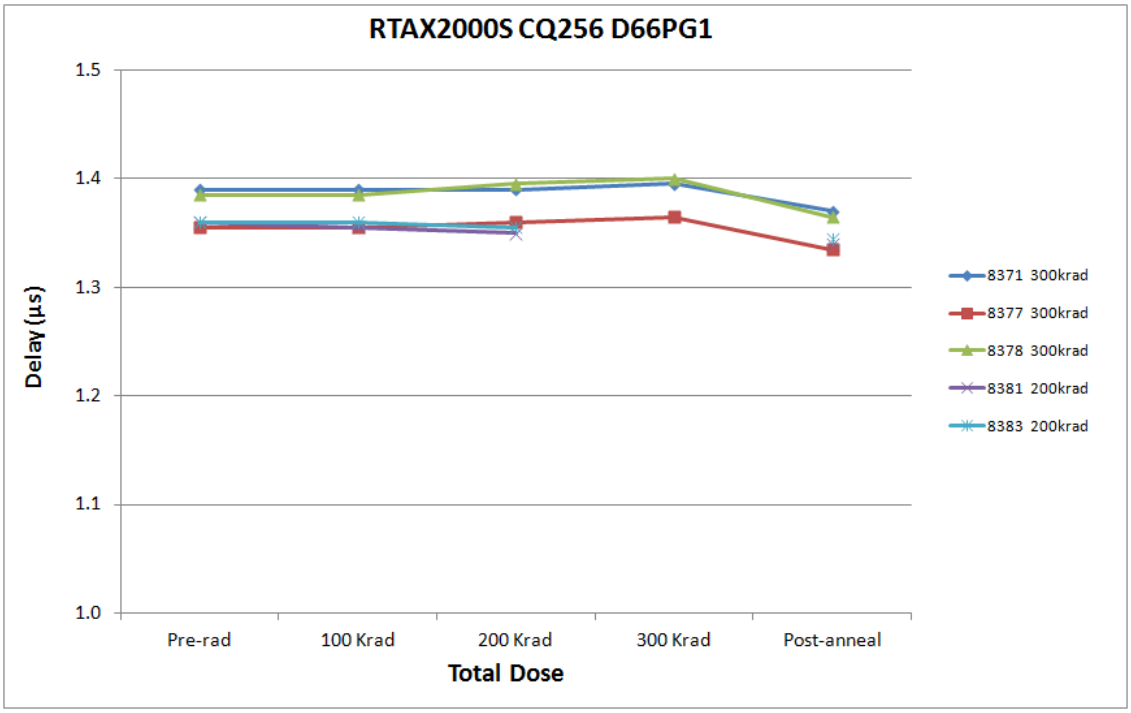


Figure 7 In-Situ Propagation Delay versus Total Dose
The measurement is performed outside the irradiation chamber.

Table 8 Radiation-Induced Propagation-Delay Degradations

	RTAX2000S CQ256 D66PG1						
Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	8371	300 krad	1.39	1.39	1.39	1.40	1.37
	8377	300 krad	1.36	1.36	1.36	1.37	1.34
	8378	300 krad	1.39	1.39	1.40	1.40	1.37
	8381	200 krad	1.36	1.36	1.35	-	1.34
	8383	200 krad	1.36	1.36	1.36	-	1.35
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	8371	300 krad	-	0.00%	0.00%	0.36%	-1.44%
	8377	300 krad	-	0.00%	0.37%	0.74%	-1.48%
	8378	300 krad	-	0.00%	0.72%	1.08%	-1.44%
	8381	200 krad	-	-0.37%	-0.74%	-	-1.47%
	8383	200 krad	-	0.00%	-0.37%	-	-1.10%

H. Transition Characteristics

Figure 8a to Figure 17b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

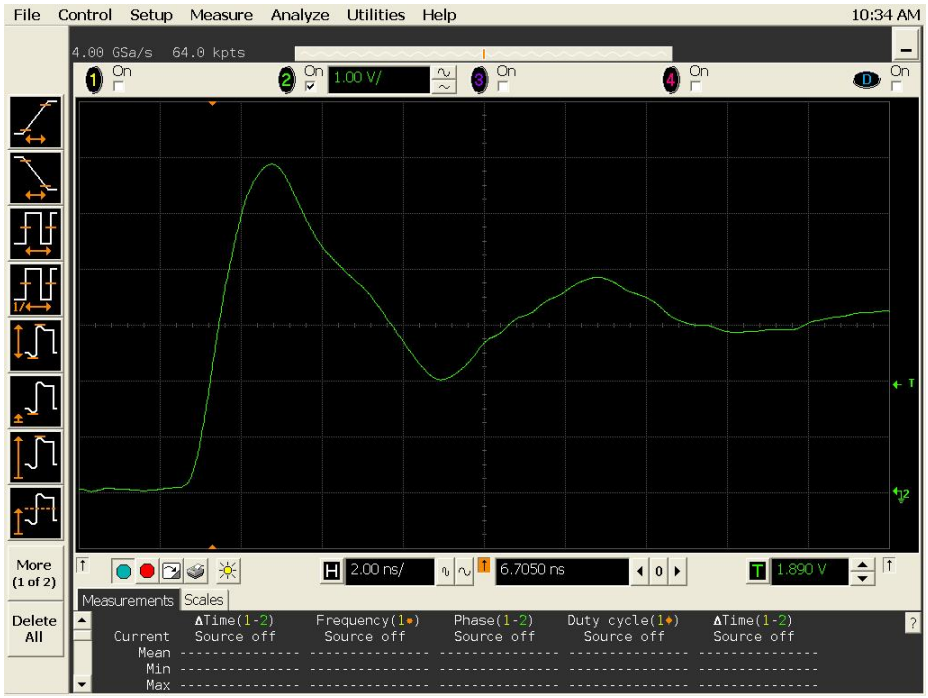


Figure 8a DUT 8371 Pre-Irradiation Rising Edge

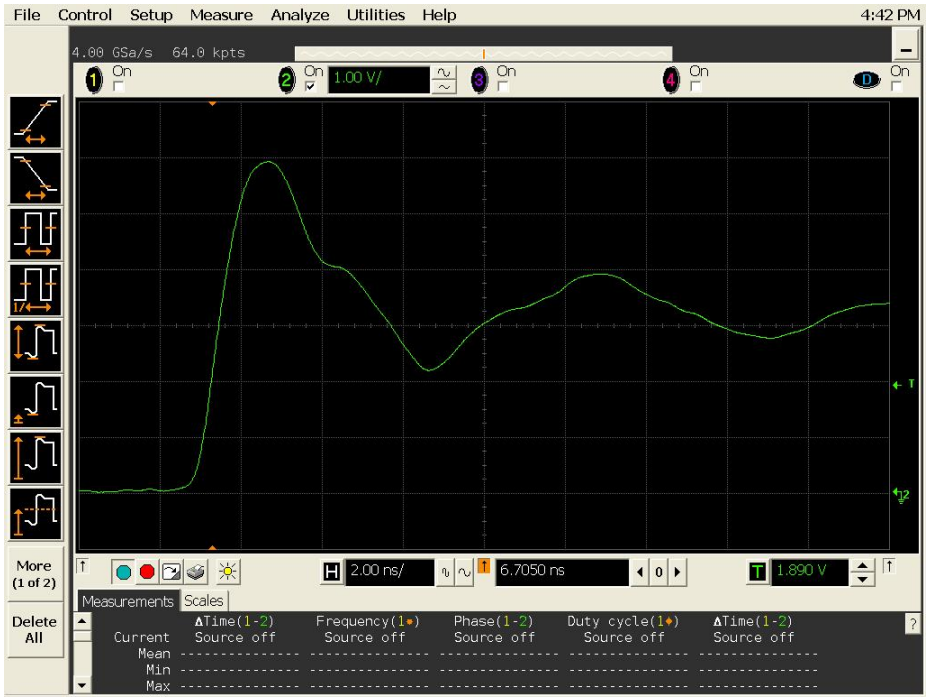


Figure 8b DUT 8371 Post-Annealing Rising Edge

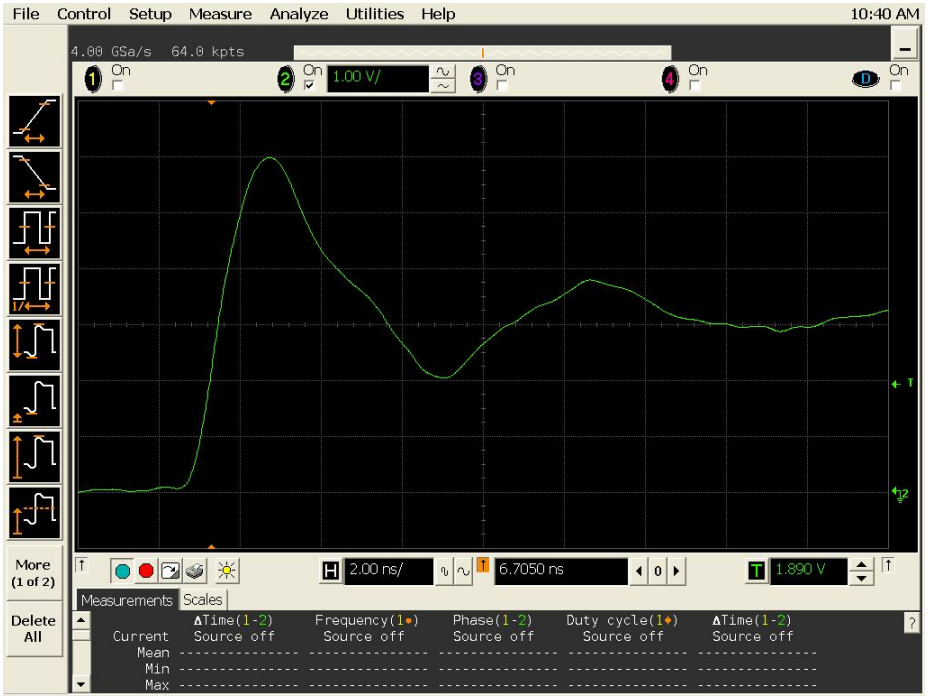


Figure 9a DUT 8377 Pre-Irradiation Rising Edge

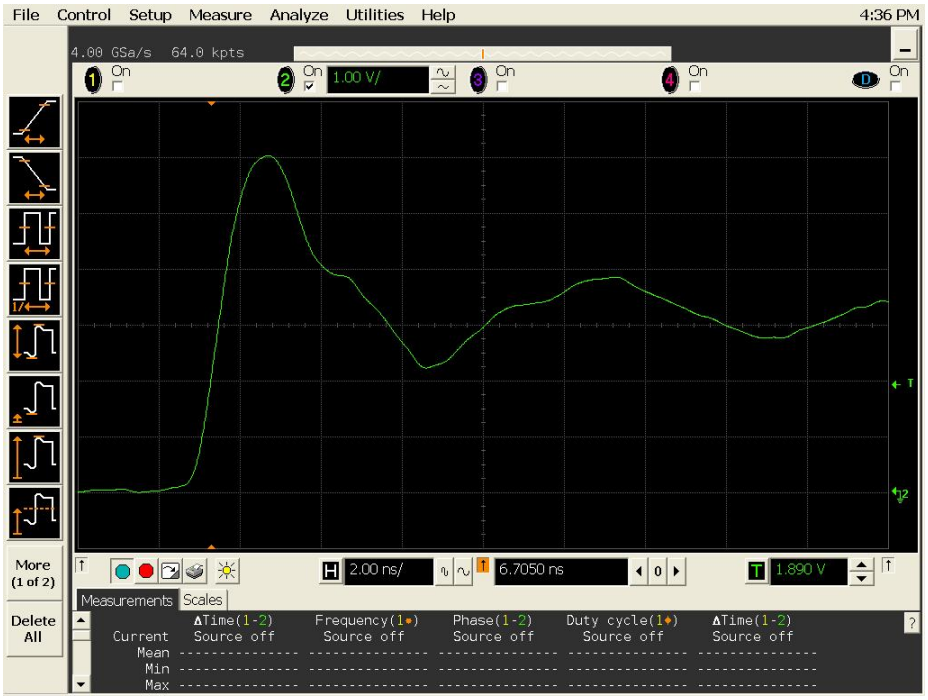


Figure 9b DUT 8377 Post-Annealing Rising Edge

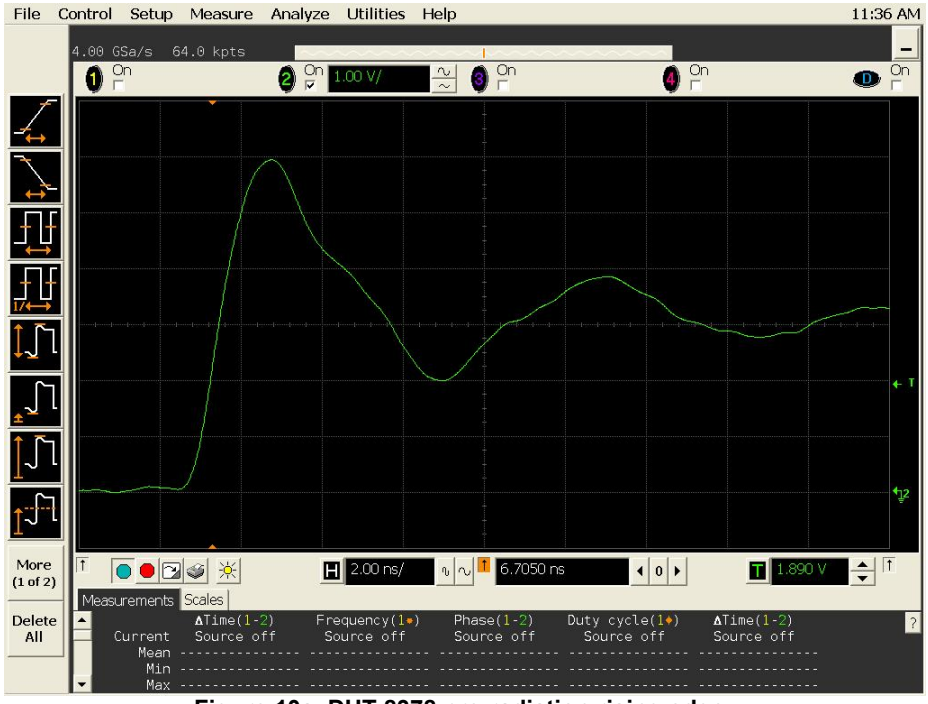


Figure 10a DUT 8378 pre-radiation rising edge.

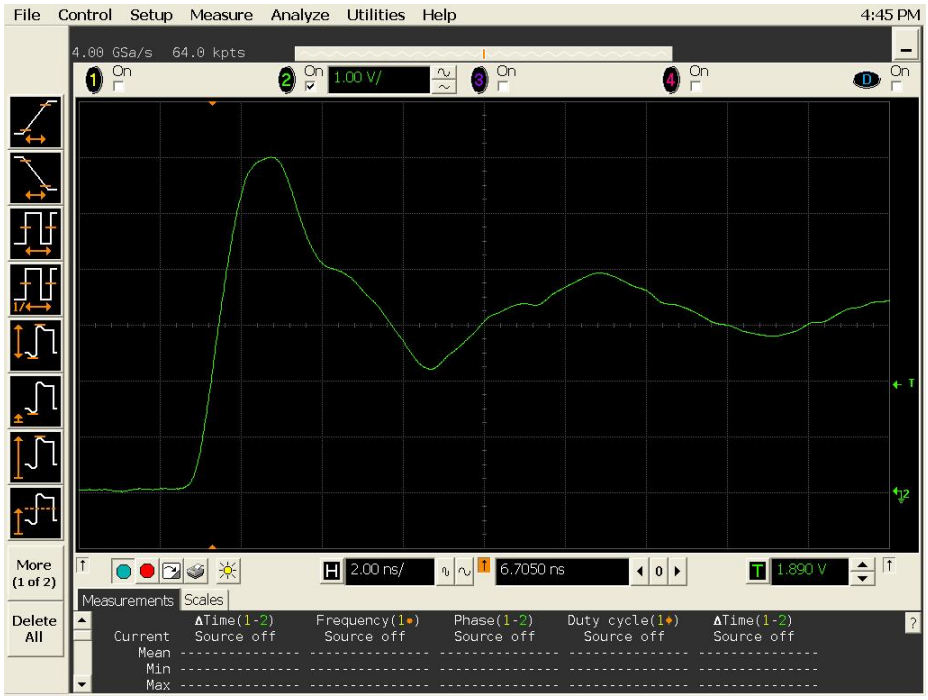


Figure 10b DUT 8378 Post-Annealing Rising Edge

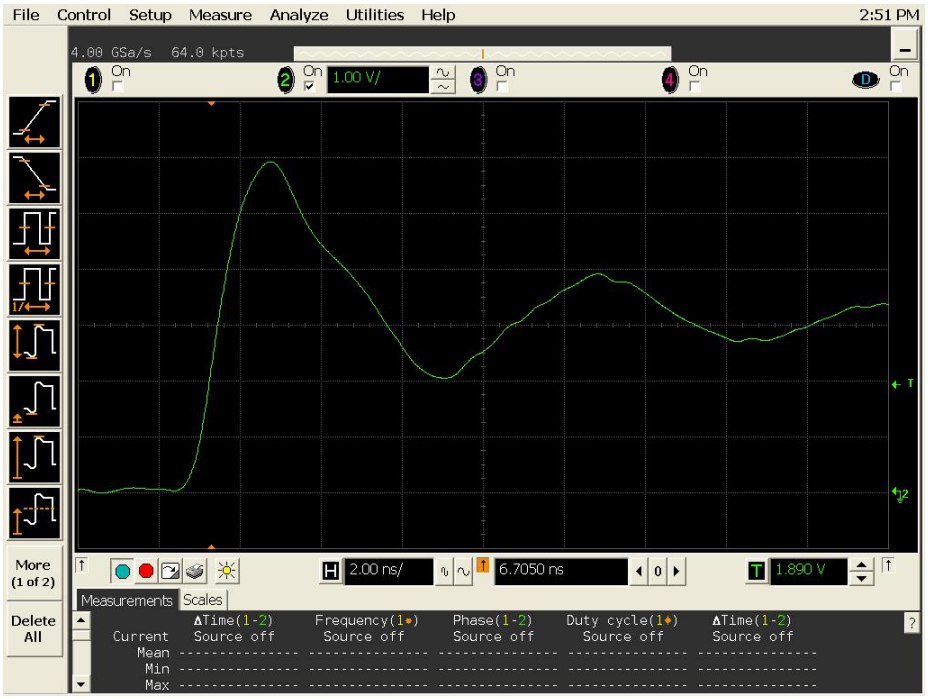


Figure 11a DUT 8381 Pre-Irradiation Rising Edge

Figure 11b DUT 8381 Post-Annealing Rising Edge

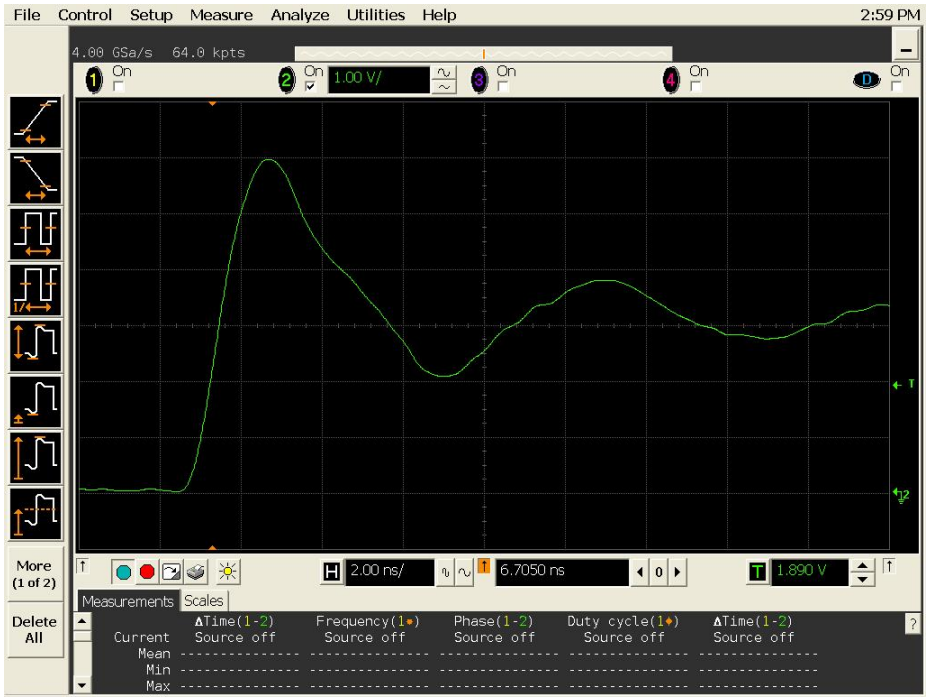


Figure 12a DUT 8383 Pre-Irradiation Rising Edge

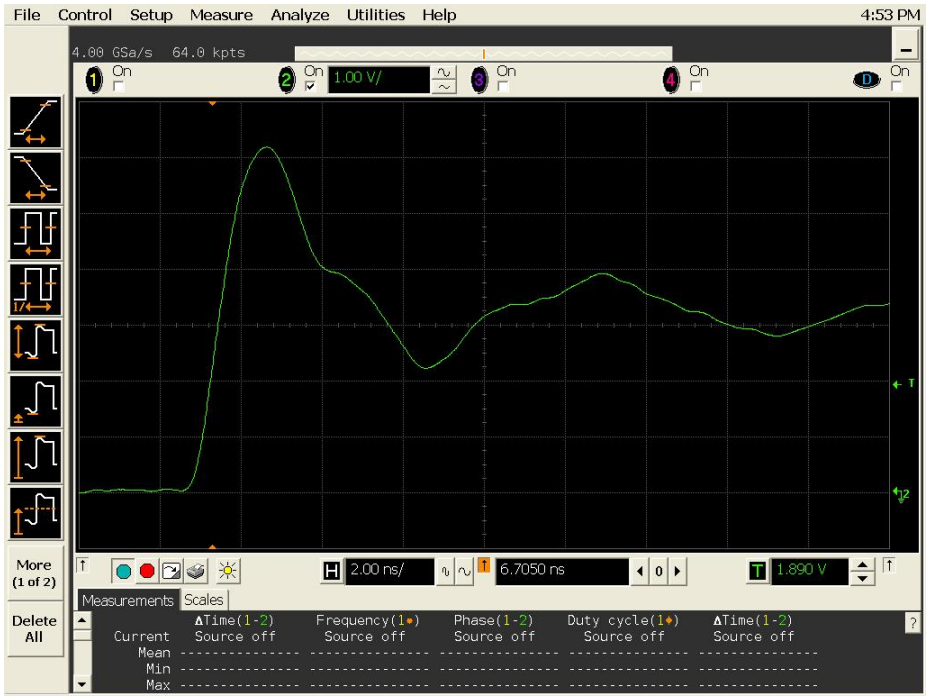


Figure 12b DUT 8383 Post-Annealing Rising Edge

Figure 13a DUT 8371 Pre-Radiation Falling Edge

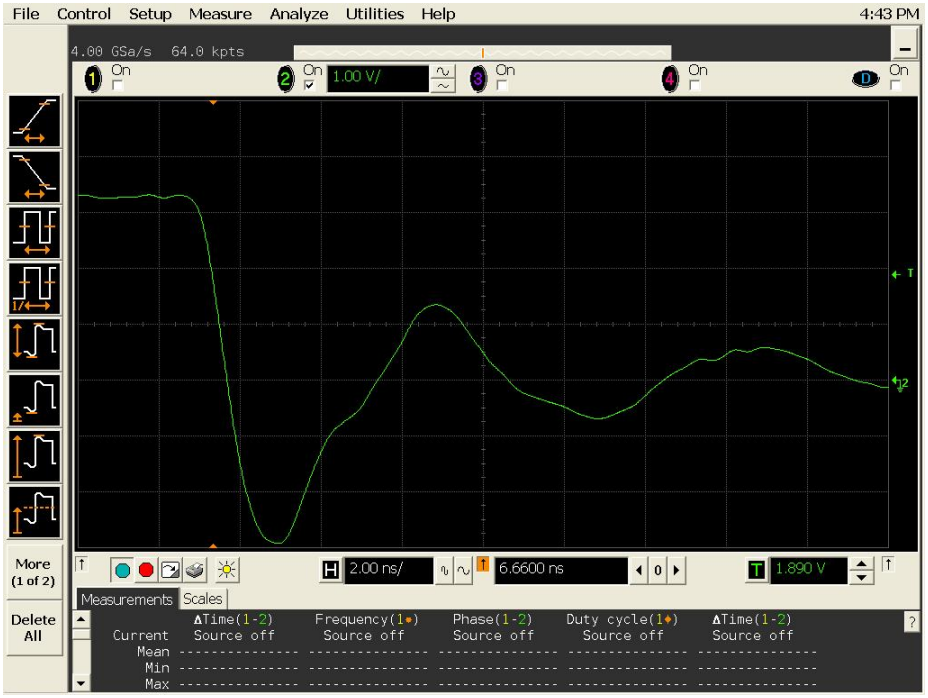


Figure 13b DUT 8371 Post-Annealing Falling Edge

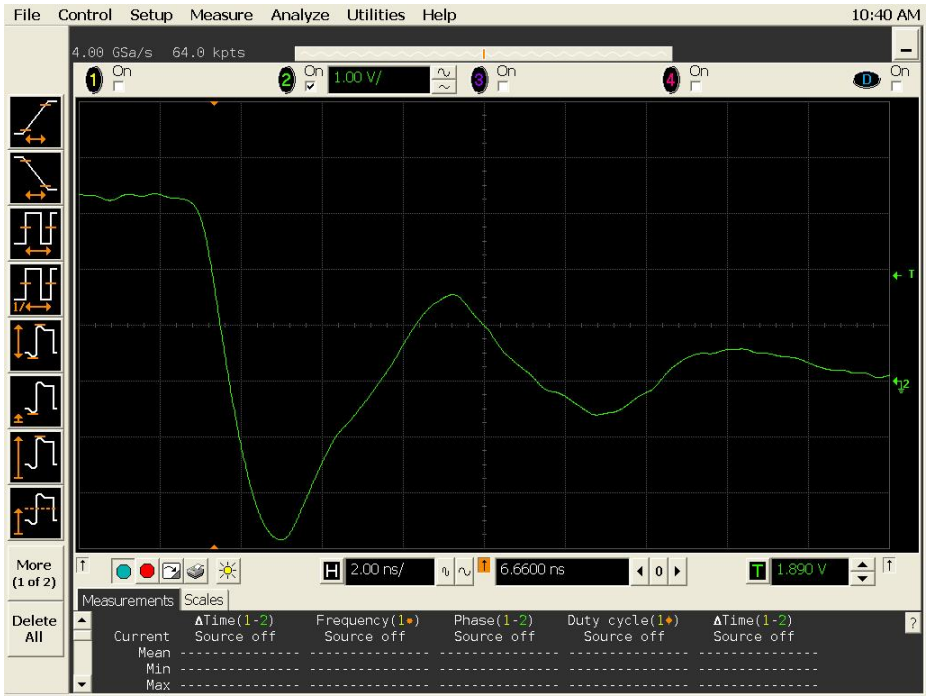


Figure 14a DUT 8377 Pre-Irradiation Falling Edge

Figure 14b DUT 8377 Post-Annealing Falling Edge

Figure 15a DUT 8378 Pre-Irradiation Falling Edge

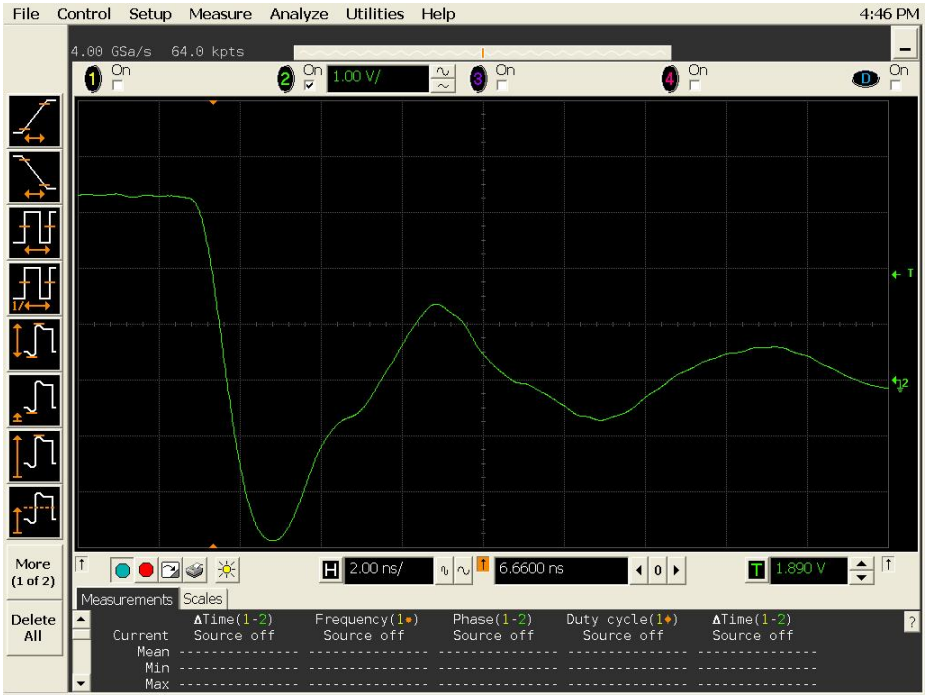


Figure 15b DUT 8378 Post-Annealing Falling Edge

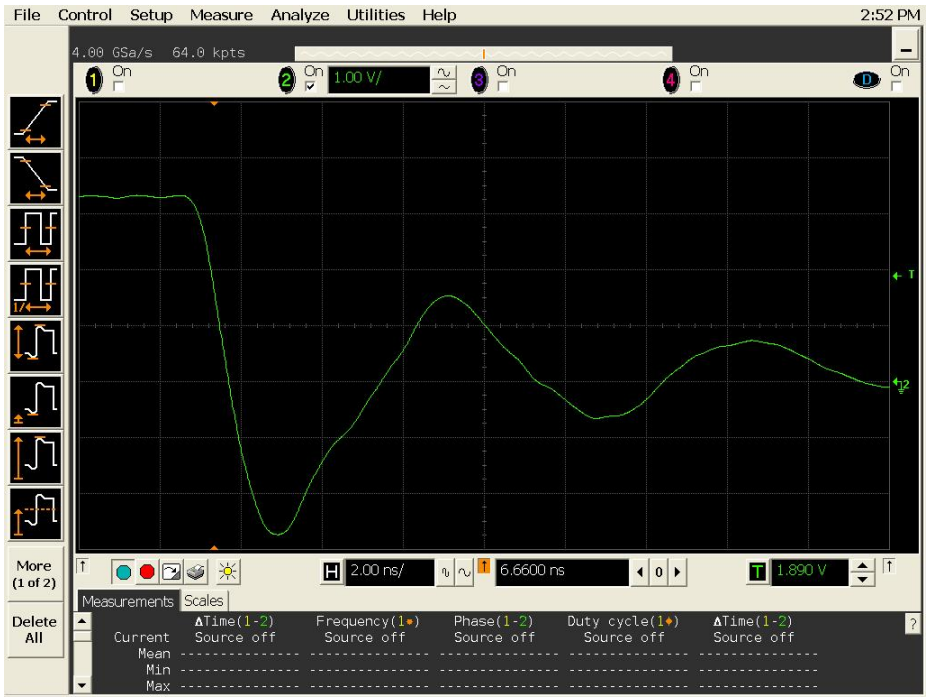


Figure 16a DUT 8381 Pre-Irradiation Falling Edge

Figure 16b DUT 8381 Post-Annealing Falling Edge

Figure 17a DUT 8383 Pre-Irradiation Falling Edge

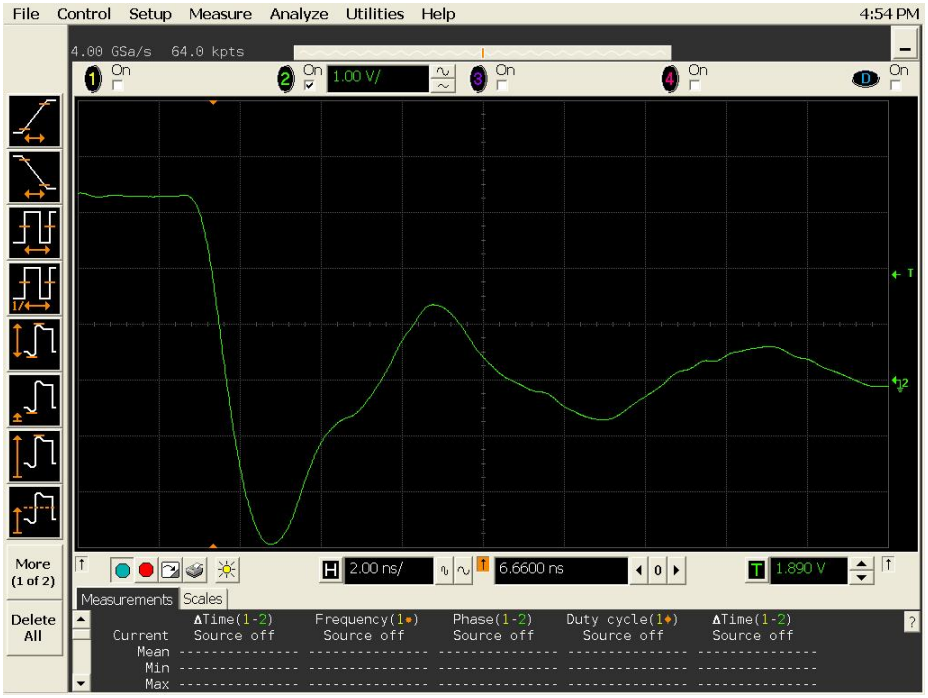


Figure 17b DUT 8383 Post-Annealing Falling Edge

Appendix A: DUT Bias

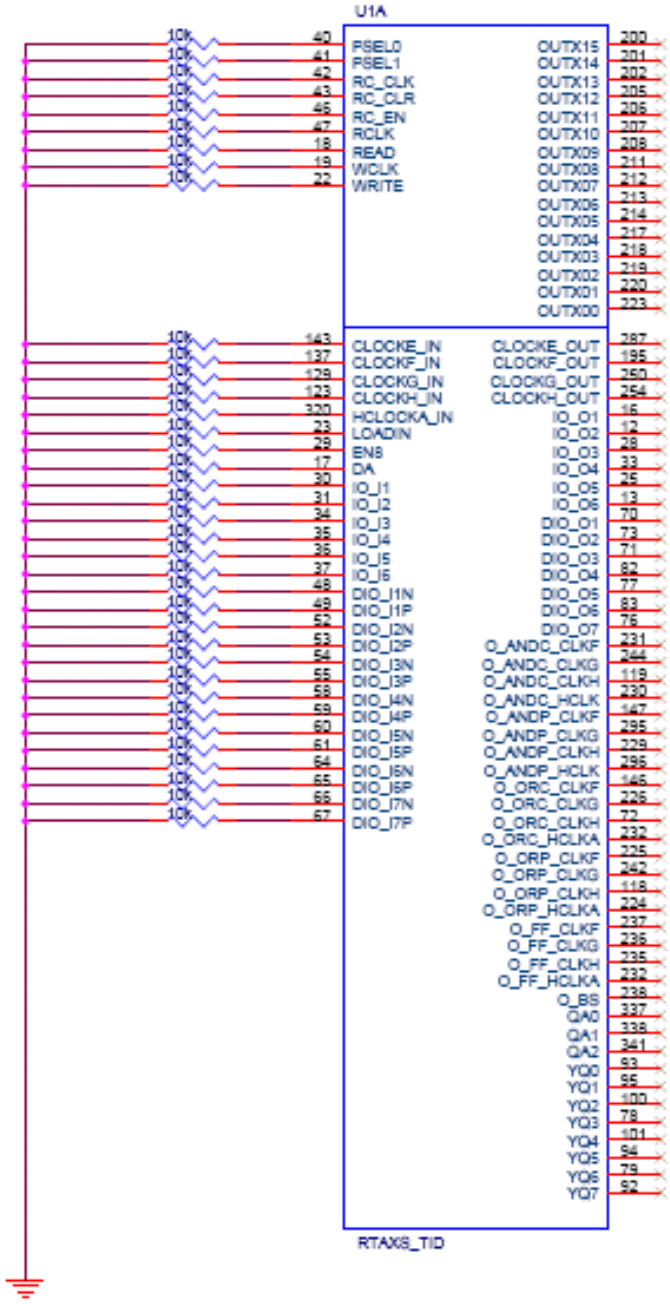


Figure A1 I/O Bias During Irradiation

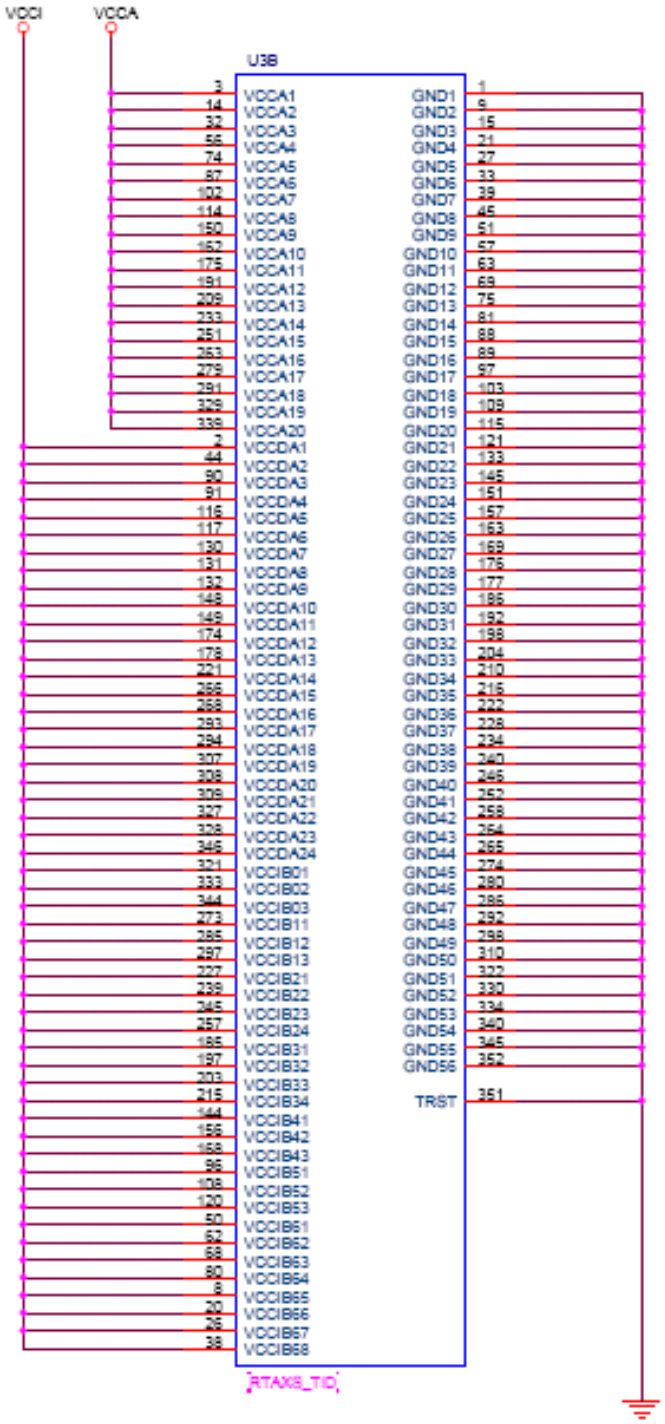
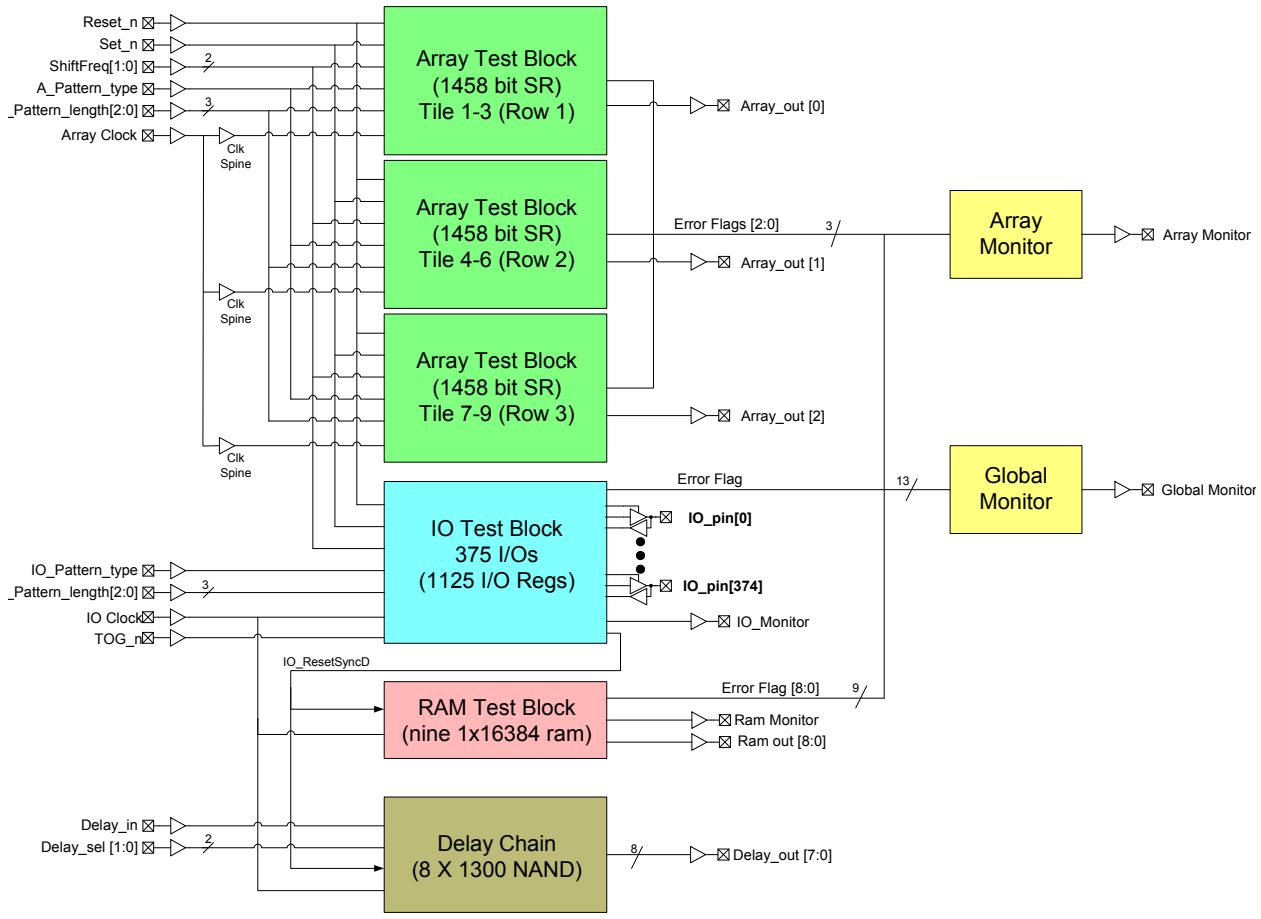


Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

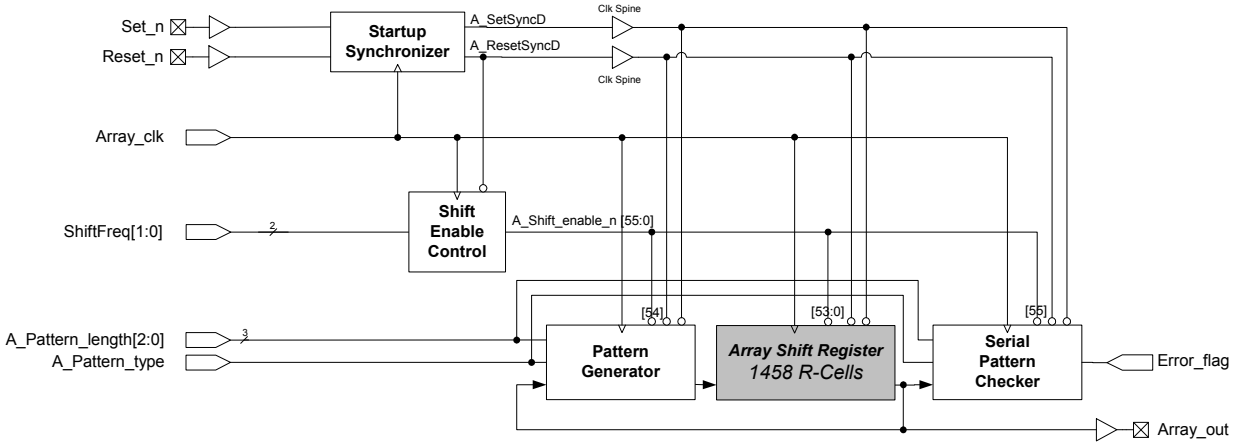
Appendix B: DUT Design Schematics

A. Design Blocks Overview

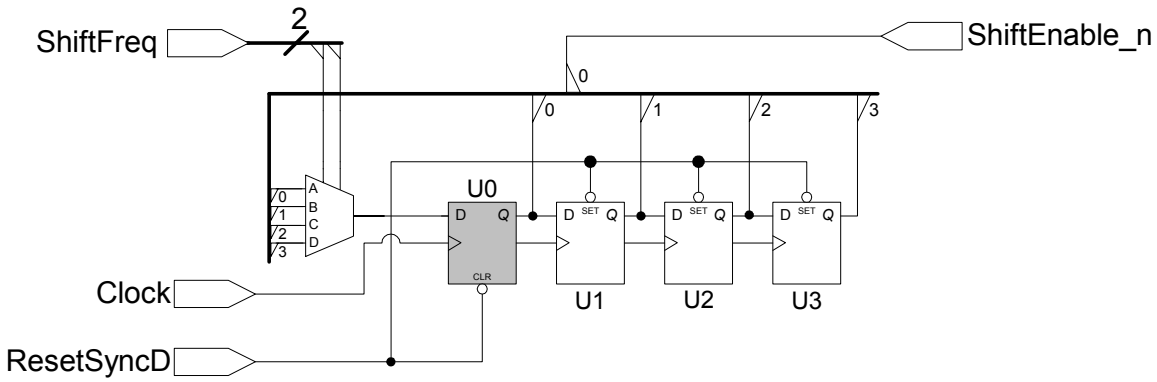
The diagrams in the following pages schematically illustrate the main blocks of the design. The naming could be different to the final pins.



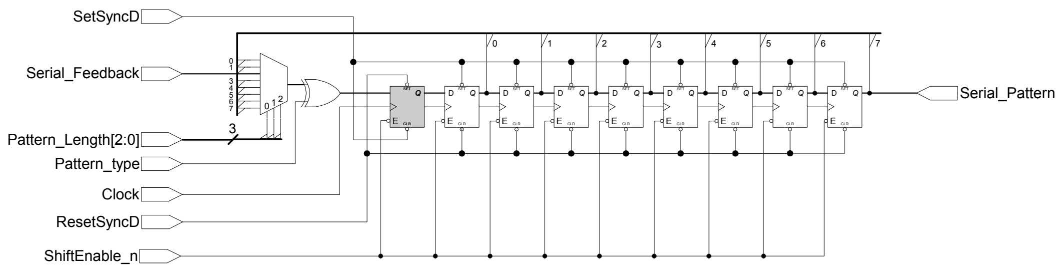
B. Array Test Block



C. Shift Enable Control

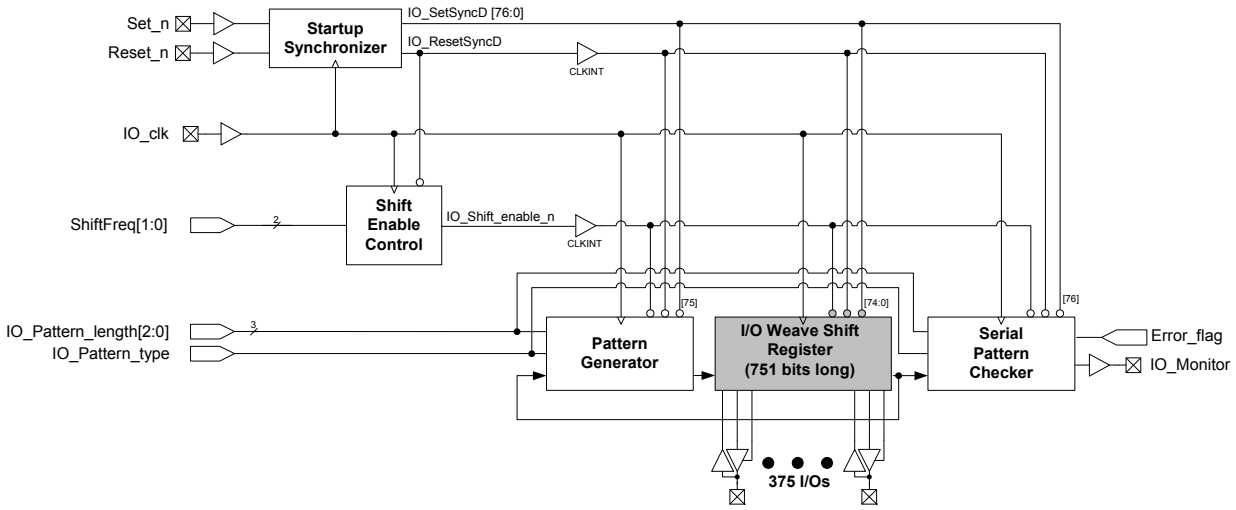


D. Pattern Generator

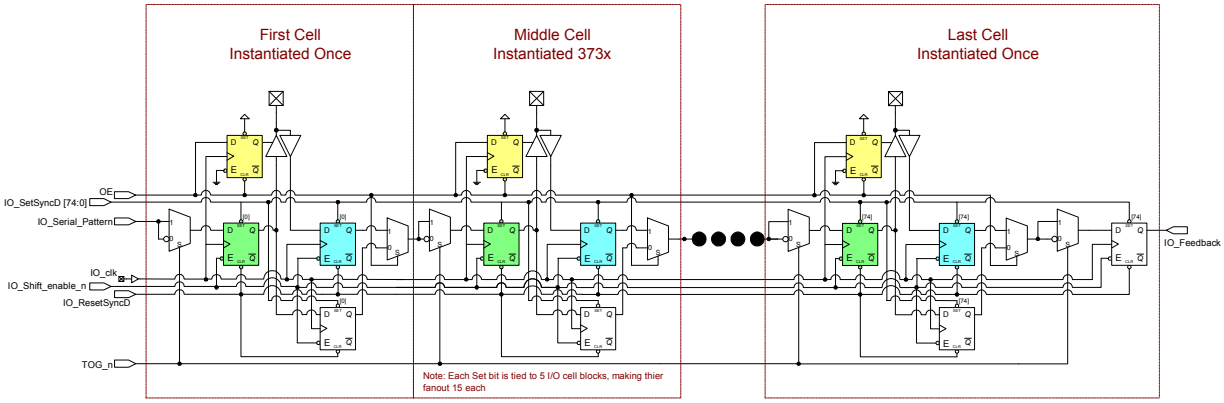


Pattern Type	Pattern Length	Sequence	Code Length	△ Bits	Switching Rate
0	000	1 0 ⇨ 0 1 ↰	2	2	100.00%
0	001	1 0 0 ⇨ 0 1 0 ⇨ 0 0 1 ↰	3	2	66.67%
0	010	**One hot I/O at a time switching in entire I/O ring**	#Bits+9	2	N/A
0	011	1 0 0 0 0 ⇨ 0 1 0 0 0 ⇨ 0 0 1 0 0 ⇨ 0 0 0 1 0 ⇨ 0 0 0 0 1 ↰	5	2	40.00%
0	100	1 0 0 0 0 0 ⇨ 0 1 0 0 0 0 ⇨ 0 0 1 0 0 0 ⇨ 0 0 0 1 0 0 ⇨ 0 0 0 0 1 0 ⇨ 0 0 0 0 0 1 ↰	6	2	33.33%
0	101	1 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 ⇨ 0 0 0 1 0 0 0 ⇨ 0 0 0 0 1 0 0 ⇨ 0 0	7	2	28.57%
0	110	1 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 ⇨ 0 0 0 0 1 0	8	2	25.00%
0	111	1 0 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 0 ⇨ 0 0	9	2	22.22%
1	000	1 0 ⇨ 1 1 ⇨ 0 1 ⇨ 0 0 ↰	2	1	50.00%
1	001	1 0 0 ⇨ 1 1 0 ⇨ 1 1 1 ⇨ 0 1 1 ⇨ 0 0 1 ⇨ 0 0 0 ↰	3	1	33.33%
1	010	**Wave of 0's followed by wave of 1's**	#Bits+9	1	N/A
1	011	1 0 0 0 0 ⇨ 1 1 0 0 0 ⇨ 1 1 1 0 0 ⇨ 1 1 1 1 0 ⇨ 1 1 1 1 1 ⇨ 0 1 1 1 1 ⇨ 0 0 1 1 1 ⇨	5	1	20.00%
1	100	1 0 0 0 0 0 ⇨ 1 1 0 0 0 0 ⇨ 1 1 1 0 0 0 ⇨ 1 1 1 1 0 0 ⇨ 1 1 1 1 1 0 ⇨ 1 1 1 1 1 1 ⇨	6	1	16.67%
1	101	1 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 ⇨ 1 1 1 1 0 0 0 ⇨ 1 1 1 1 1 0 0 ⇨ 1 1	7	1	14.29%
1	110	1 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 ⇨ 1 1 1 1 1 0	8	1	12.50%
1	111	1 0 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 0 ⇨ 1 1	9	1	11.11%

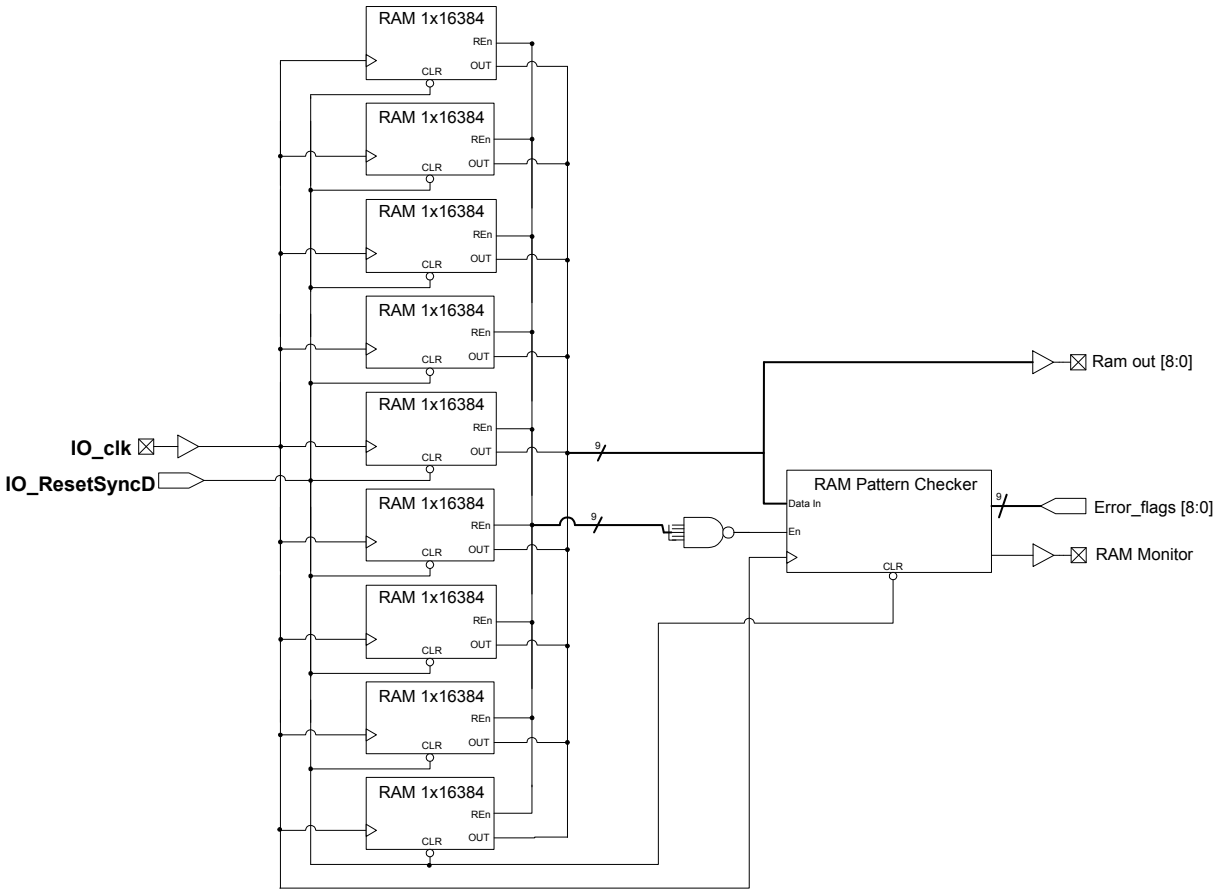
E. I/O Test Block



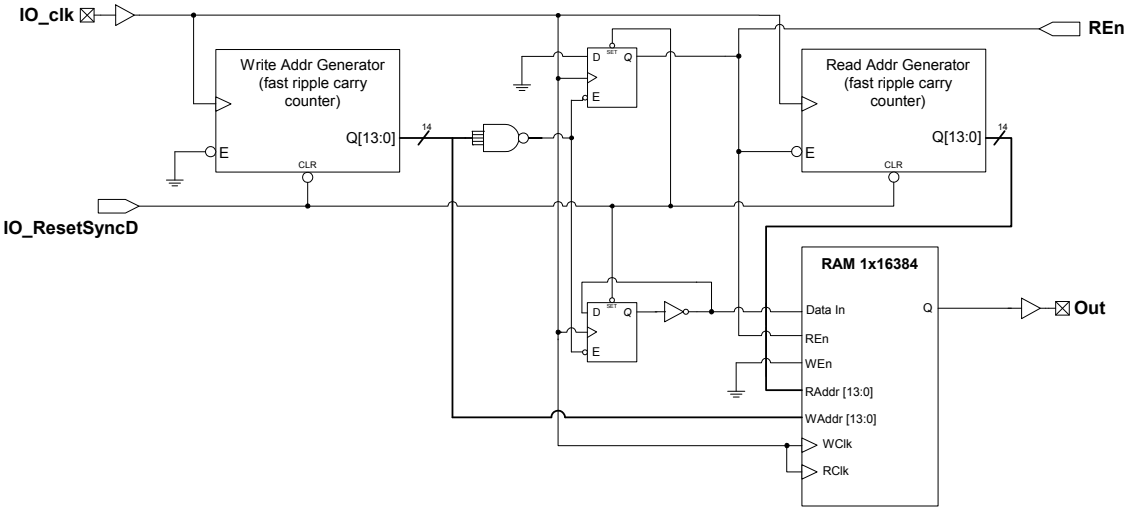
F. I/O Weave Structure



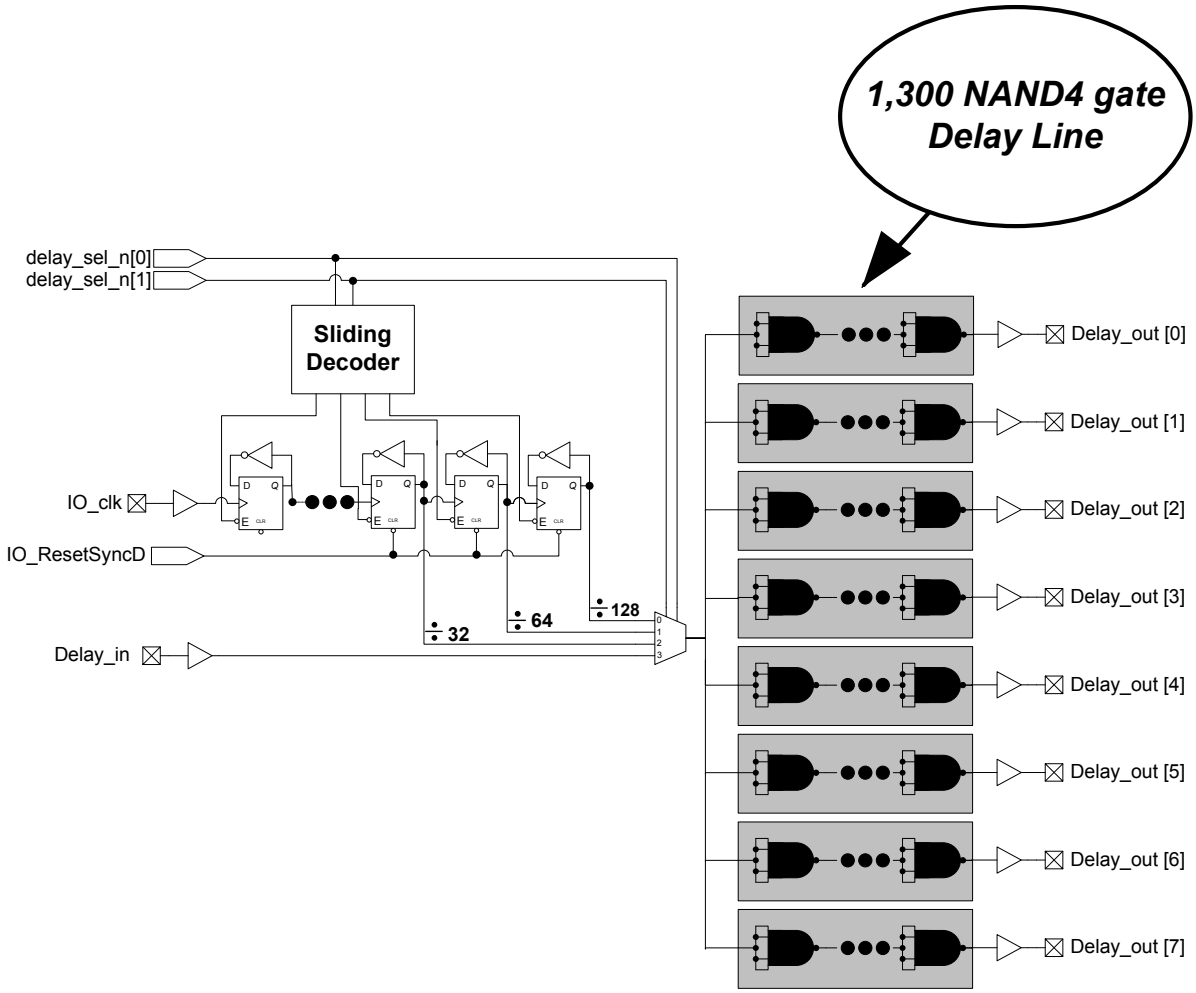
G. RAM Test Block



H. RAM 1x16384



I. Delay Chains



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