Total Ionizing Dose Test Report

No. 12T-RTAX2000S-CG624-D5S2W1

September 25, 2012

Table of Contents

I. Summary Table 3

II. Total Ionizing Dose (TID) Testing 3

A. Device-Under-Test (DUT) and Irradiation Parameters 3
B. Test Method 4
C. Design and Parametric Measurements 5

III. Test Results 6

A. Functionality 6
B. Power Supply Current (ICCA and ICCI) 6
C. Single-Ended Input Logic Threshold (VIL/VIH) 10
D. Differential Input (LVPECL) Threshold Voltage (VIL/VIH) 12
E. Output-Drive Voltage (VOL/VOH) 13
F. Propagation Delay 16
G. Transition Characteristics 18

Appendix A: DUT Design Schematics 30

TOTAL IONIZING DOSE TEST REPORT

No. 12T-RTAX2000S-CG624-D5S2W1

September 25, 2012

CK Huang and J.J. Wang

(408) 643-6136, (408) 643-6302

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation and annealing, each input is grounded.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	rtax2000_CG624_Top
Die Lot Number	D5S2W1
Quantity Tested	6
Serial Number	300 krad(SiO_2): 5254, 5263, 5264 200 krad(SiO_2): 5275, 5278, 5282
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V

B. Test Method

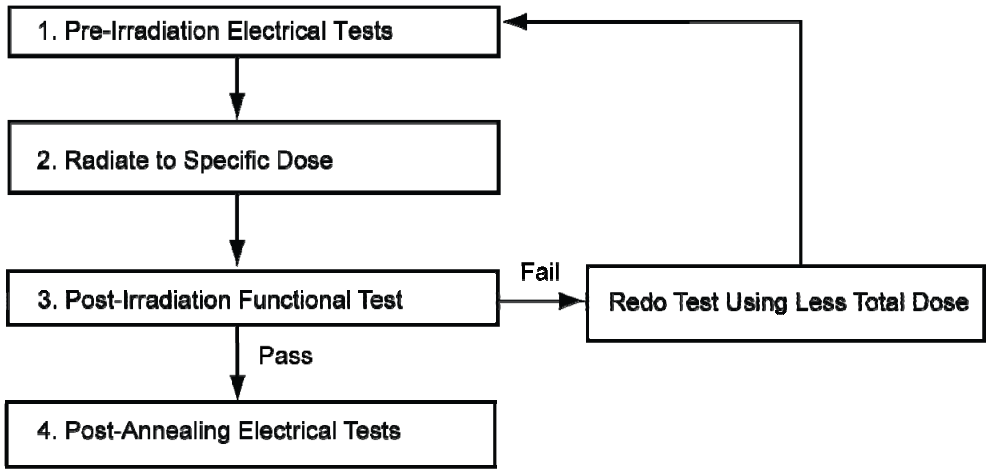


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000S are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 1 week.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design, rtax2000_CG624_Top, for testing total dose effects. These logic designs are described in the following subsections. Appendix A shows the block diagram.

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby I_{CC} includes I_{CCI} and I_{CCA}. Except propagation delay and the transition characteristic, which is measured on the output O_BS, all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

1. Embedded SRAM

This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

2. Unidirectional LVTTL Input and Output

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

3. Bidirectional LVTTL IO

This design is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for radiation effects testing.

4. LVPECL Input

This design is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

5. Shift Registers

This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

6. Long Buffer String

This design is to measure the radiation effects on the propagation delay. The input of the design using a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK_IN and the output switching due to this clock edge at O_BS is defined as propagation delay high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the radiation effects. A more than 10% of propagation change is considered as failure.

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests. The as-irradiated DUT is functionally tested on the output (O_FF_HCLKA) of the largest shift register.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of *the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs* datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
5254	300 krad	4	58	8	25	303	160
5263	300 krad	8	67	9	24	288	110
5264	300 krad	8	70	9	24	299	140
5275	200 krad	5	6	6	24	76	30
5278	200 krad	6	10	7	25	96	40
5282	200 krad	5	5	6	24	62	30

Based on these PIPL, post-annealed DUT passes both the ICCA and ICCI spec for 200 krad (SiO2).

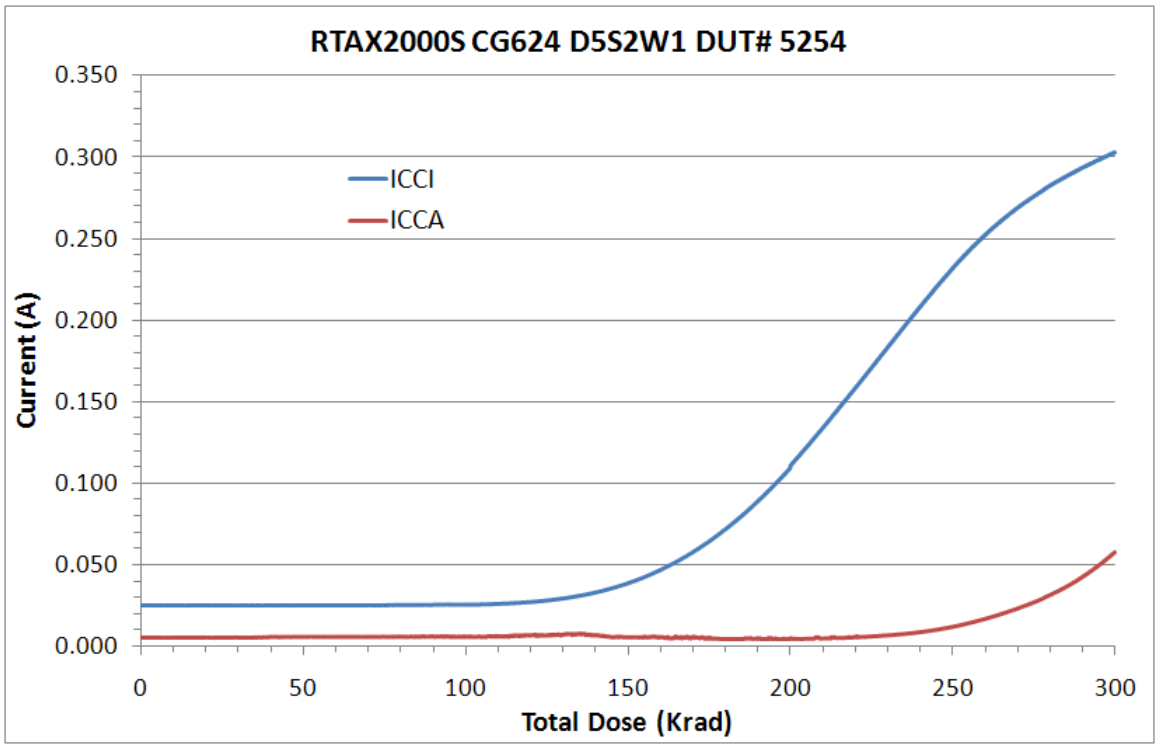


Figure 2 DUT 5254 Influx ICCA and ICCI

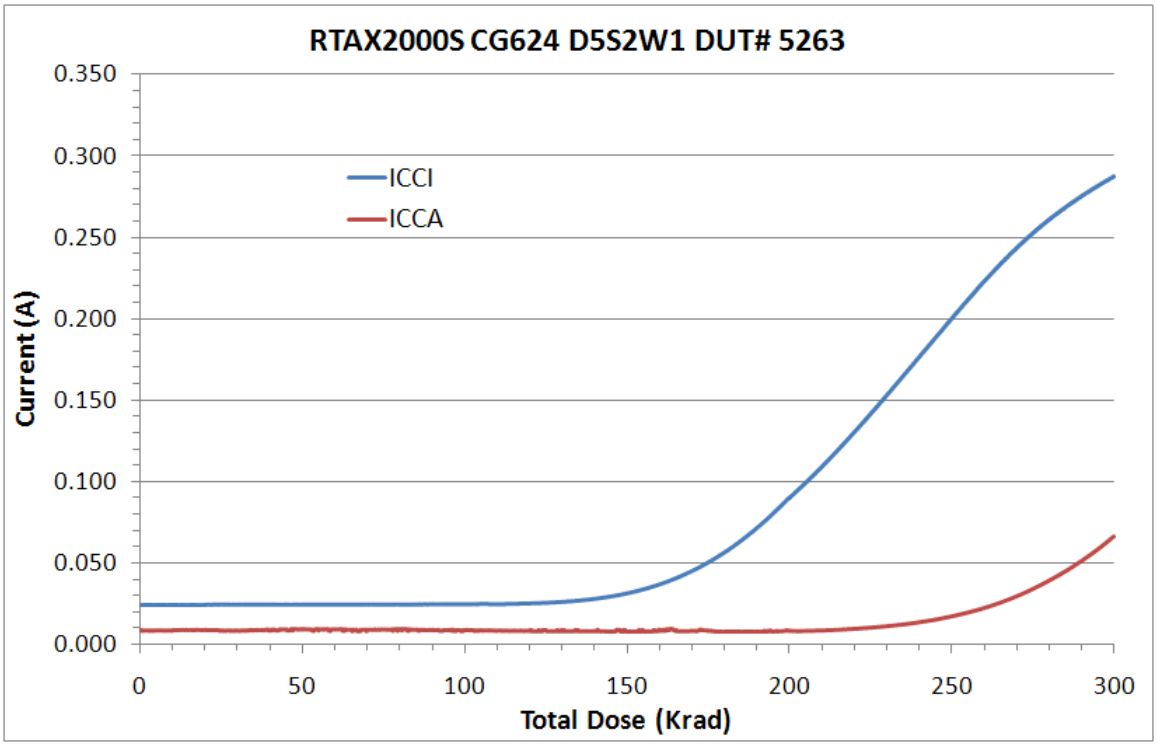


Figure 3 DUT 5263 Influx ICCA and ICCI

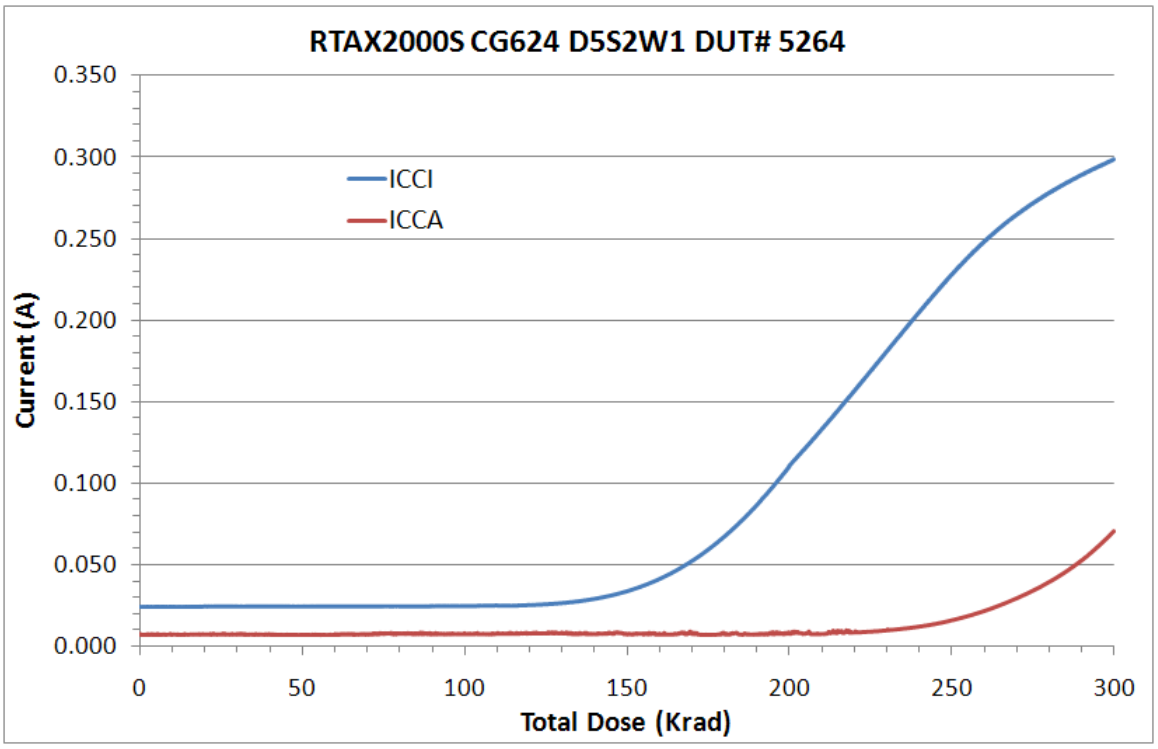


Figure 4 DUT 5264 Influx ICCA and ICCI

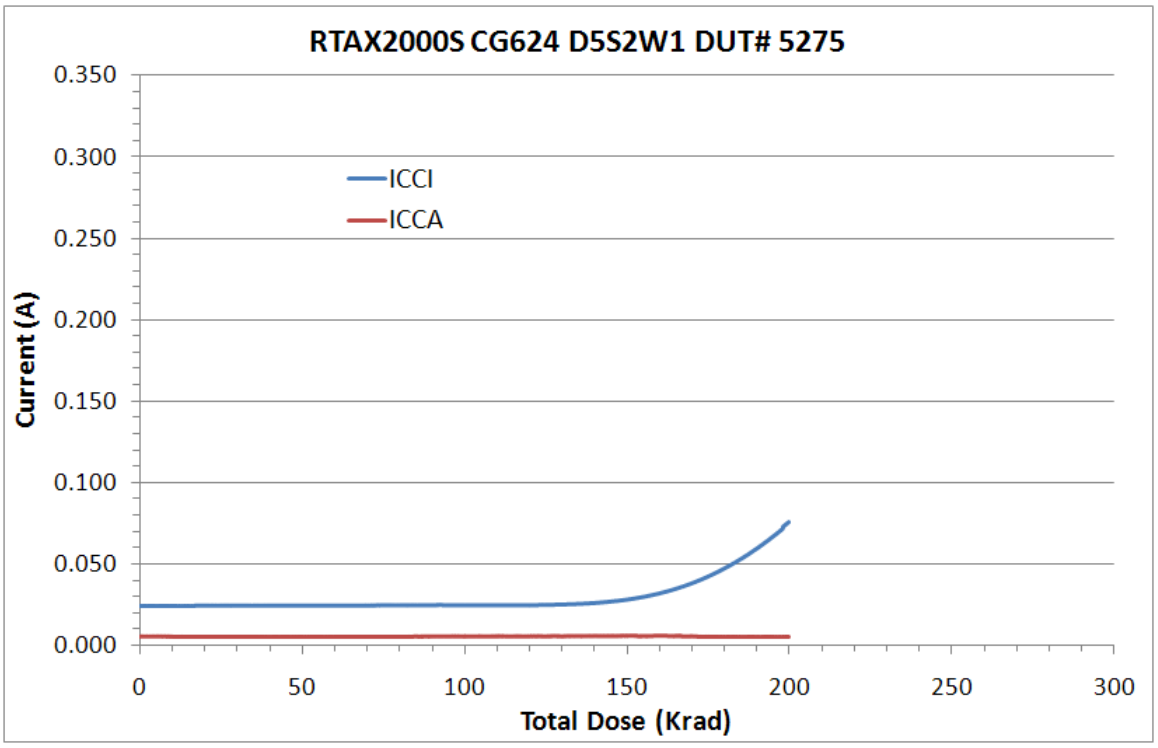


Figure 5 DUT 5275 Influx ICCA and ICCI

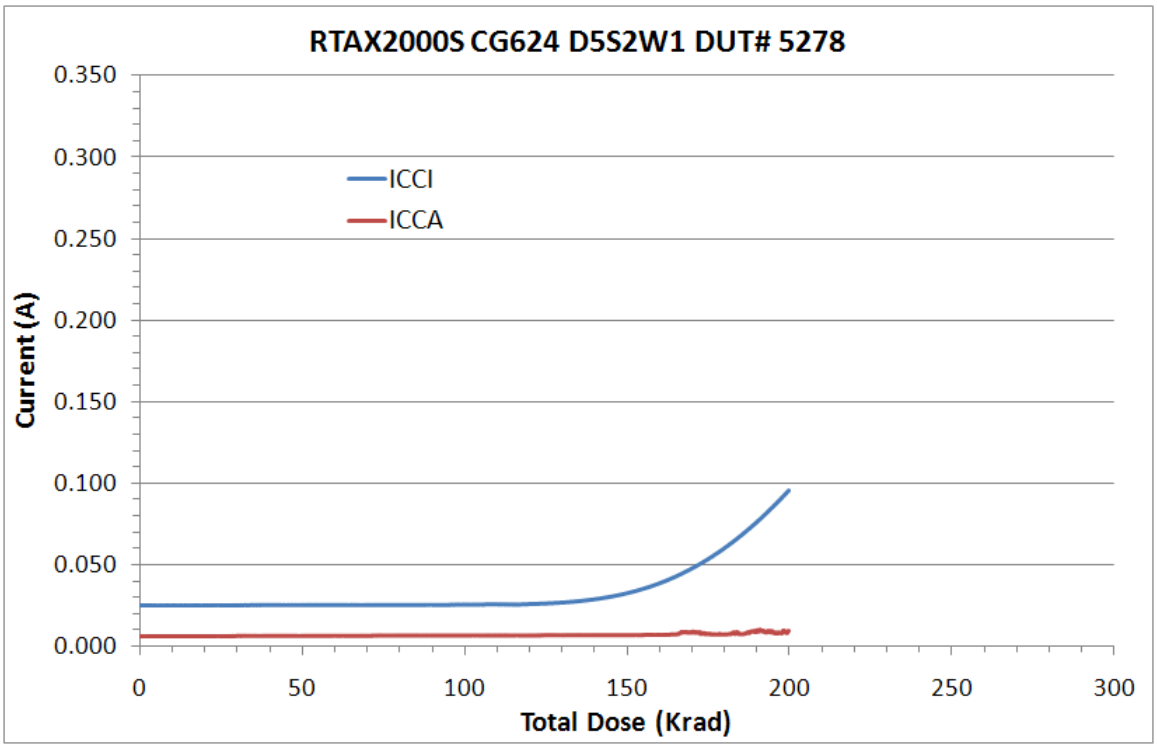


Figure 6 DUT 5278 Influx ICCA and ICCI

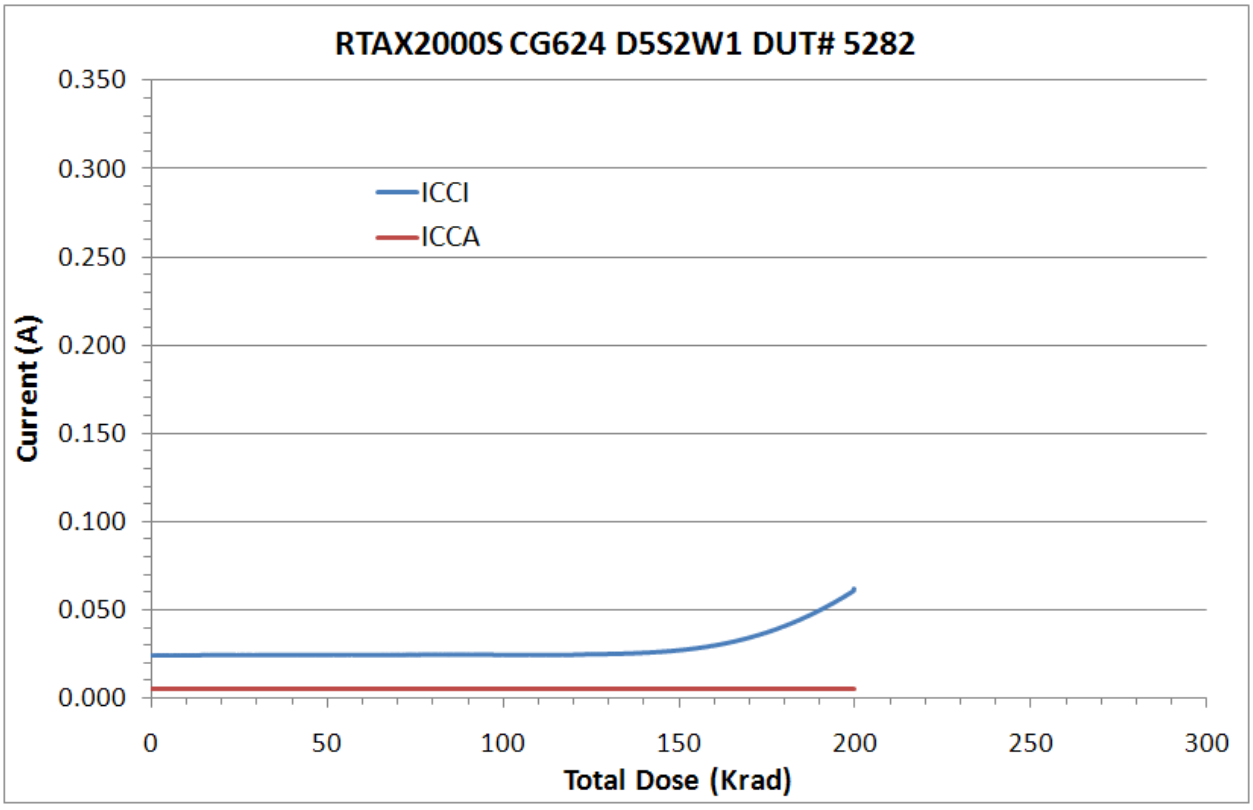


Figure 7 DUT 5282 Influx ICCA and ICCI

C. Single-Ended Input Logic Threshold (VIL/VIH)

Table 3a through Table 3c list the pre-irradiation and post-annealing single-ended input logic thresholds. All data are within the specification limits. The post-annealing shift in every case is very small.

Table 3a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5254 (300 krad)				5263 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1400	1385	1400	1385	1395	1390	1395	1395
Bi_D_6	1385	1370	1410	1395	1380	1375	1405	1400
Bi_D_5	1395	1380	1405	1390	1385	1385	1400	1400
Bi_D_4	1395	1380	1395	1385	1390	1385	1390	1390
Bi_D_3	1390	1380	1405	1400	1390	1380	1405	1400
Bi_D_2	1390	1375	1410	1395	1380	1375	1400	1400
Bi_D_1	1390	1375	1410	1390	1380	1370	1395	1400
DA	1415	1390	1430	1420	1385	1415	1415	1435
EN8	1360	1345	1480	1470	1355	1355	1410	1475
IO_I_6	1380	1365	1445	1440	1375	1370	1440	1435
IO_I_5	1360	1360	1455	1420	1375	1365	1420	1445
IO_I_4	1425	1415	1415	1410	1420	1420	1415	1415
IO_I_3	1415	1390	1425	1420	1395	1405	1415	1420
IO_I_2	1425	1415	1415	1410	1420	1415	1415	1415
IO_I_1	1420	1405	1425	1415	1415	1415	1420	1415
RCLK1P	1460	1450	1455	1445	1455	1455	1450	1445
RCLK2P	1460	1450	1455	1450	1455	1460	1450	1450

Table 3b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5264 (300 krad)				5275 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1390	1380	1390	1380	1380	1370	1380	1375
Bi_D_6	1375	1360	1395	1390	1365	1360	1390	1385
Bi_D_5	1385	1375	1395	1385	1375	1365	1385	1375
Bi_D_4	1390	1380	1390	1380	1375	1370	1380	1370
Bi_D_3	1385	1370	1395	1390	1375	1370	1390	1385
Bi_D_2	1375	1370	1395	1390	1370	1360	1390	1380
Bi_D_1	1375	1365	1395	1385	1370	1360	1385	1380
DA	1385	1385	1395	1410	1385	1365	1400	1395
EN8	1355	1355	1470	1420	1345	1335	1445	1415
IO_I_6	1370	1360	1435	1425	1360	1355	1425	1420
IO_I_5	1360	1360	1435	1445	1345	1355	1395	1430
IO_I_4	1415	1405	1405	1400	1400	1395	1395	1390
IO_I_3	1410	1385	1415	1410	1375	1385	1400	1400
IO_I_2	1415	1410	1405	1400	1400	1395	1395	1390
IO_I_1	1405	1405	1415	1410	1390	1385	1400	1380
RCLK1P	1455	1450	1445	1440	1440	1440	1430	1435
RCLK2P	1450	1450	1450	1445	1435	1440	1435	1440

Table 3c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5278 (200 krad)				5282 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1390	1380	1390	1385	1385	1375	1385	1375
Bi_D_6	1375	1365	1400	1390	1370	1360	1390	1385
Bi_D_5	1385	1375	1395	1390	1380	1370	1390	1380
Bi_D_4	1385	1380	1390	1380	1380	1370	1380	1375
Bi_D_3	1390	1380	1400	1395	1380	1370	1390	1385
Bi_D_2	1380	1370	1400	1395	1370	1365	1390	1385
Bi_D_1	1375	1370	1395	1385	1370	1365	1385	1380
DA	1385	1385	1415	1405	1385	1385	1410	1405
EN8	1355	1330	1470	1420	1355	1330	1465	1455
IO_I_6	1370	1360	1435	1425	1365	1355	1430	1420
IO_I_5	1360	1355	1445	1440	1355	1355	1445	1435
IO_I_4	1415	1405	1405	1400	1410	1400	1405	1390
IO_I_3	1390	1400	1415	1410	1390	1385	1415	1405
IO_I_2	1415	1405	1405	1400	1410	1395	1400	1395
IO_I_1	1405	1405	1415	1410	1400	1395	1410	1400
RCLK1P	1455	1450	1445	1445	1445	1435	1435	1430
RCLK2P	1455	1450	1450	1450	1440	1435	1435	1435

D. Differential Input (LVPECL) Threshold Voltage (VIL/VIH)

Table 4a through Table 4c list the LVPECL differential input threshold voltage changes due to irradiations. All pins show negligible changes, and all the data are within the specification.

Table 4a Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5254 (300 krad)				5263 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	110	80	110	80	95	95	95	95
DIO_IP_6	105	105	100	105	120	90	115	90
DIO_IP_5	115	90	110	90	105	100	105	95
DIO_IP_4	85	70	80	65	85	70	80	70
DIO_IP_3	90	75	90	75	90	80	90	75
DIO_IP_2	90	65	85	60	80	75	75	75
DIO_IP_1	80	60	85	65	70	70	75	70

Table 4b Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5264 (300 krad)				5275 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	100	85	95	80	110	105	110	100
DIO_IP_6	110	90	105	90	105	100	105	100
DIO_IP_5	100	85	95	80	105	95	100	95
DIO_IP_4	85	70	85	65	90	85	85	80
DIO_IP_3	90	75	90	75	80	70	75	70
DIO_IP_2	85	65	85	65	85	80	80	75
DIO_IP_1	70	60	75	65	80	70	85	75

Table 4c Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5278 (200 krad)				5282 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	105	100	105	100	110	105	110	105
DIO_IP_6	115	110	110	110	100	95	100	90
DIO_IP_5	115	105	110	105	115	110	115	105
DIO_IP_4	90	80	85	80	90	85	90	80
DIO_IP_3	90	85	90	80	75	70	75	65
DIO_IP_2	80	75	80	75	85	75	80	75
DIO_IP_1	75	75	80	75	70	70	75	70

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Table 5a through Table 5c. The post-annealing data are within the specification limits.

Table 5a Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5254 (300 krad)				5263 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2970	2965	35	35	2970	2965
Bi_IO_6	35	35	2970	2965	35	35	2965	2960
Bi_IO_5	35	40	2970	2960	35	40	2970	2960
Bi_IO_4	35	35	2965	2965	35	35	2965	2965
Bi_IO_3	30	35	2970	2965	35	35	2965	2965
Bi_IO_2	35	40	2970	2960	35	40	2965	2960
Bi_IO_1	35	35	2965	2965	35	35	2970	2965
Bi_Y_7	25	30	2985	2980	30	25	2985	2980
Bi_Y_6	25	25	2985	2980	25	25	2985	2980
Bi_Y_5	25	30	2985	2980	25	30	2985	2980
Bi_Y_4	25	25	2985	2980	25	25	2985	2980
Bi_Y_3	25	30	2985	2980	25	25	2985	2980
Bi_Y_2	25	25	2985	2980	25	25	2985	2980
Bi_Y_1	30	30	2985	2980	30	30	2980	2980
CLOCK	20	20	2970	2970	20	25	2970	2970
CLOCK	20	25	2970	2970	20	25	2970	2970
QA_2	20	25	2970	2960	20	20	2970	2965
QA_1	20	20	2970	2965	20	20	2970	2965
QA_0	20	20	2970	2965	20	20	2970	2965

Table 5b Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5264 (300 krad)				5275 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2970	2965	35	35	2970	2965
Bi_IO_6	35	35	2965	2965	35	30	2965	2965
Bi_IO_5	35	40	2970	2960	35	40	2970	2960
Bi_IO_4	35	35	2965	2965	35	35	2965	2965
Bi_IO_3	30	35	2970	2965	35	35	2965	2965
Bi_IO_2	35	40	2965	2960	35	35	2965	2965
Bi_IO_1	35	35	2965	2965	35	40	2965	2960
Bi_Y_7	30	25	2985	2980	30	25	2985	2980
Bi_Y_6	25	25	2985	2980	25	25	2985	2980
Bi_Y_5	25	30	2985	2980	25	25	2985	2980
Bi_Y_4	25	25	2985	2980	25	25	2985	2980
Bi_Y_3	25	25	2985	2980	25	25	2985	2980
Bi_Y_2	25	25	2980	2980	25	25	2980	2980
Bi_Y_1	30	30	2985	2980	30	30	2985	2980
CLOCK	20	20	2970	2970	20	20	2970	2970
CLOCK	20	25	2970	2970	20	20	2970	2970
QA_2	20	20	2970	2965	20	20	2970	2970
QA_1	20	20	2970	2965	20	20	2970	2965
QA_0	20	20	2970	2965	20	20	2970	2970

Table 5c Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5278 (200 krad)				5282 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2970	2965	35	35	2970	2965
Bi_IO_6	35	30	2965	2965	35	30	2965	2965
Bi_IO_5	35	40	2970	2960	35	40	2970	2960
Bi_IO_4	35	35	2965	2965	35	35	2965	2965
Bi_IO_3	30	35	2970	2965	30	35	2970	2965
Bi_IO_2	35	35	2970	2965	35	35	2965	2965
Bi_IO_1	35	35	2965	2965	35	35	2965	2965
Bi_Y_7	30	25	2985	2980	30	25	2985	2980
Bi_Y_6	25	25	2985	2980	25	25	2985	2980
Bi_Y_5	25	30	2985	2980	25	30	2985	2980
Bi_Y_4	25	25	2985	2980	25	25	2980	2980
Bi_Y_3	25	25	2985	2980	25	25	2985	2980
Bi_Y_2	25	25	2985	2980	25	25	2980	2980
Bi_Y_1	30	30	2985	2980	30	30	2980	2980
CLOCK	20	20	2970	2970	20	20	2970	2970
CLOCK	20	20	2970	2970	20	20	2970	2970
QA_2	20	20	2970	2965	20	20	2970	2970
QA_1	20	20	2970	2965	20	20	2970	2965
QA_0	20	20	2970	2970	20	20	2970	2970

F. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The irradiation was temporarily stopped at each total-dose increment of 100 krad for the measurement (however, the post-irradiation data of this lot are accidentally erased, only data before irradiation and after anneal are presented). The results are plotted in Figure 8, and listed in Table 6. As shown in Figure 8, the propagation delay initially decreases with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots (Figure 2 through Figure 7), a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

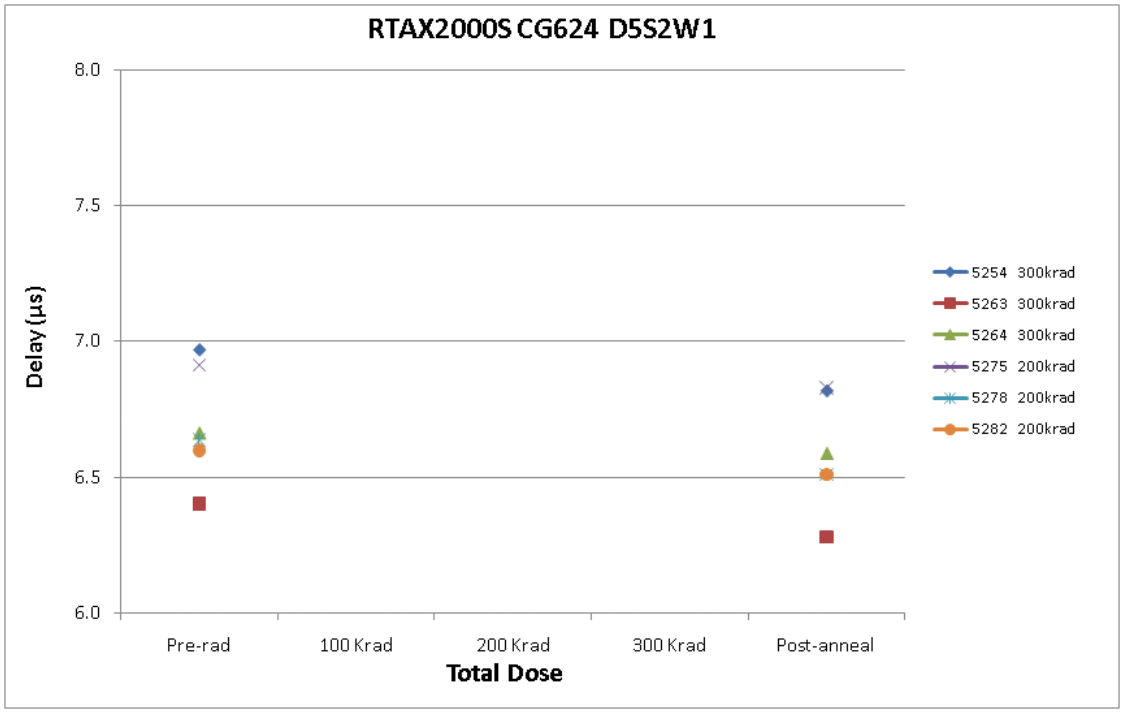


Figure 8 In-Situ Propagation Delay versus Total Dose.

Table 6 Radiation-Induced Propagation Delay Degradations

	RTAX2000S CG624 D5S2W1						
Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5254	300 krad	6.97	-	-	-	6.82
	5263	300 krad	6.40	-	-	-	6.28
	5264	300 krad	6.66	-	-	-	6.59
	5275	200 krad	6.91	-	-	-	6.83
	5278	200 krad	6.64	-	-	-	6.51
	5282	200 krad	6.60	-	-	-	6.51
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5254	300 krad	-	-	-	-	-2.12%
	5263	300 krad	-	-	-	-	-1.92%
	5264	300 krad	-	-	-	-	-1.12%
	5275	200 krad	-	-	-	-	-1.22%
	5278	200 krad	-	-	-	-	-1.92%
	5282	200 krad	-	-	-	-	-1.36%

G. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

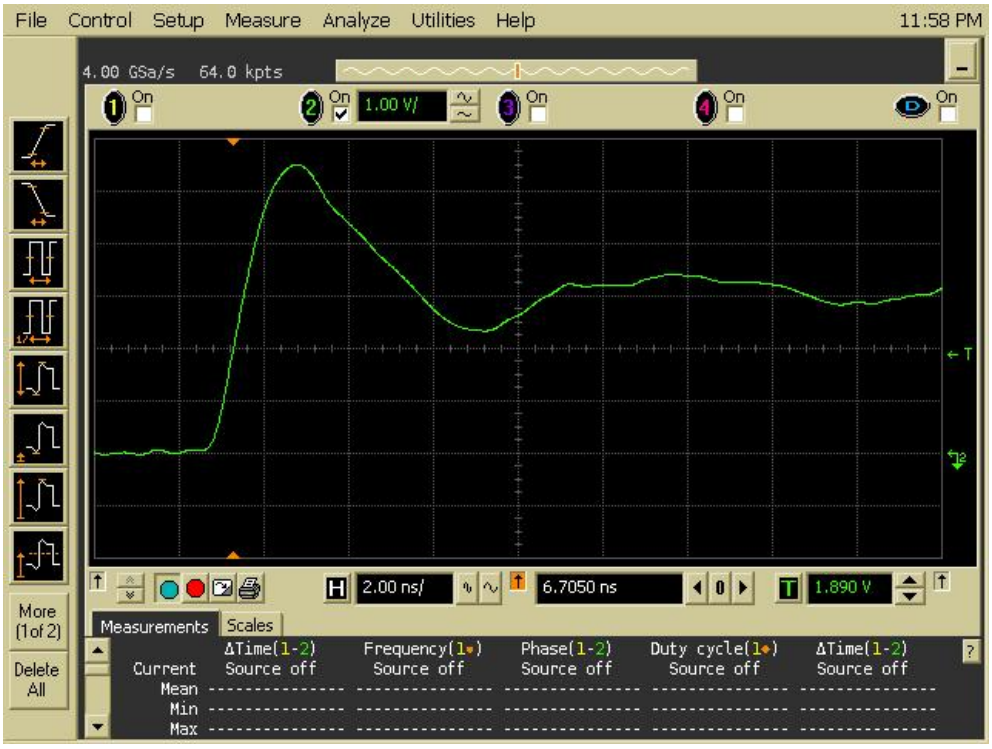


Figure 9a DUT 5254 Pre-Irradiation Rising Edge

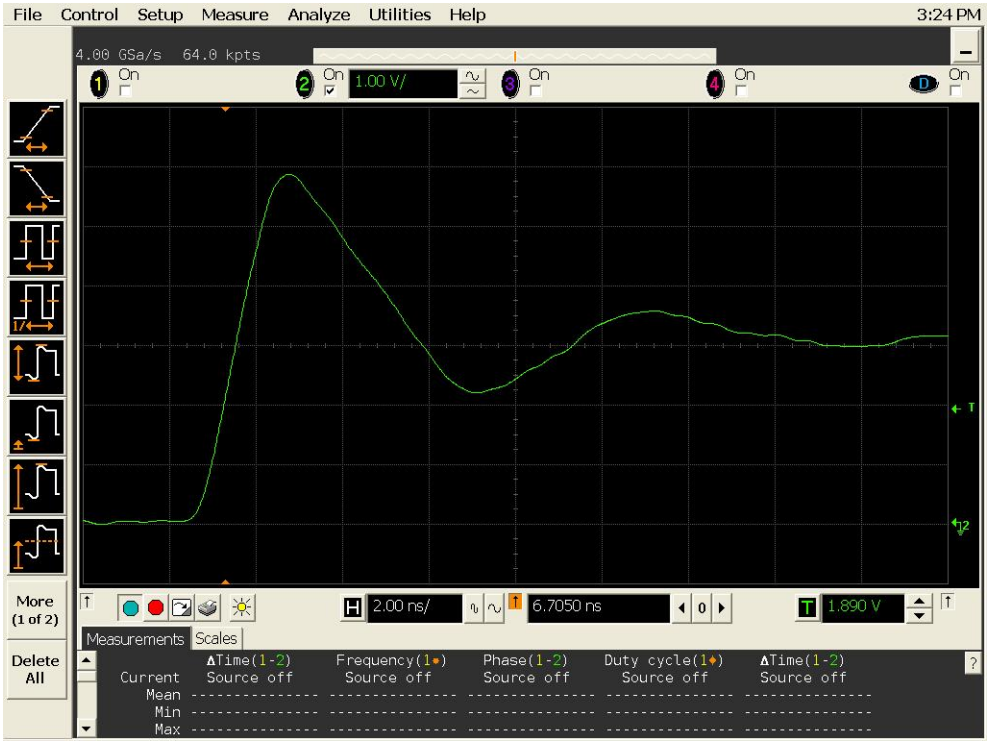


Figure 9b DUT 5254 Post-Annealing Rising Edge

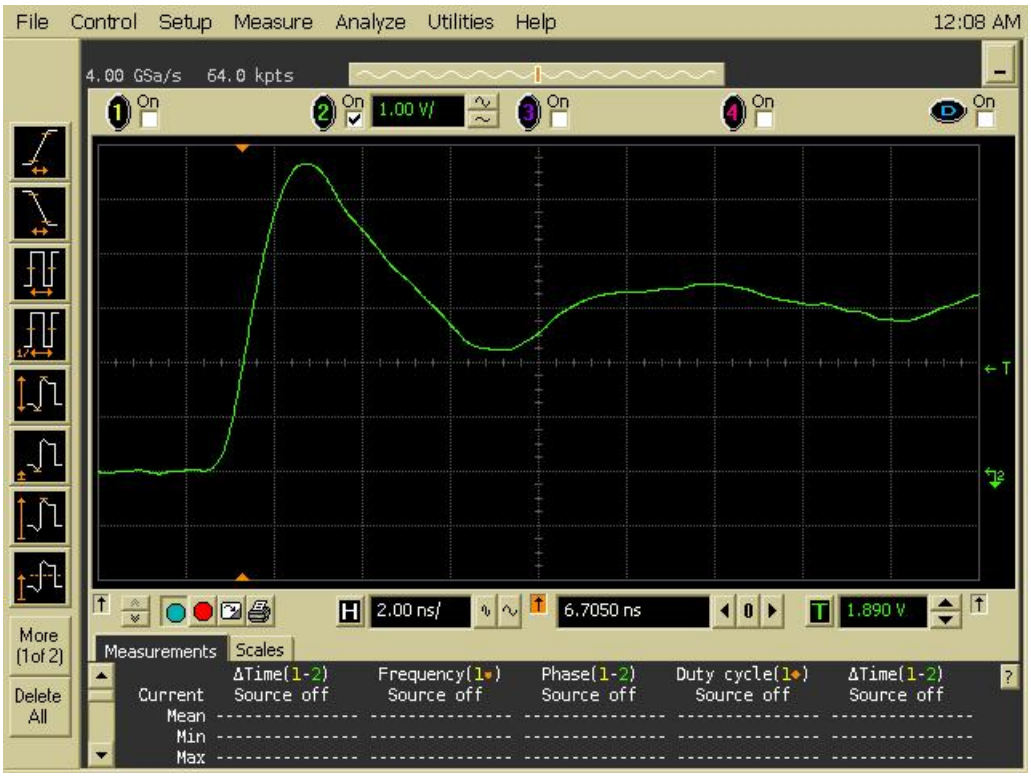


Figure 10a DUT 5263 Pre-Irradiation Rising Edge

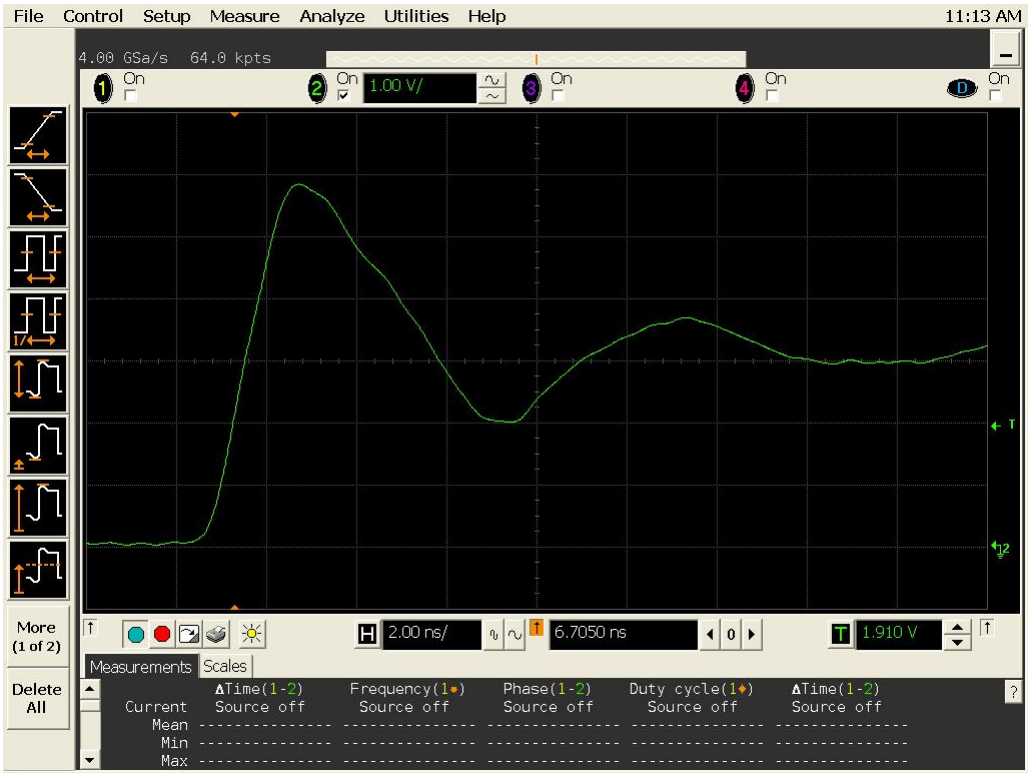


Figure 10b DUT 5263 Post-Annealing Rising Edge



Figure 11a DUT 5264 Pre-Radiation Rising Edge

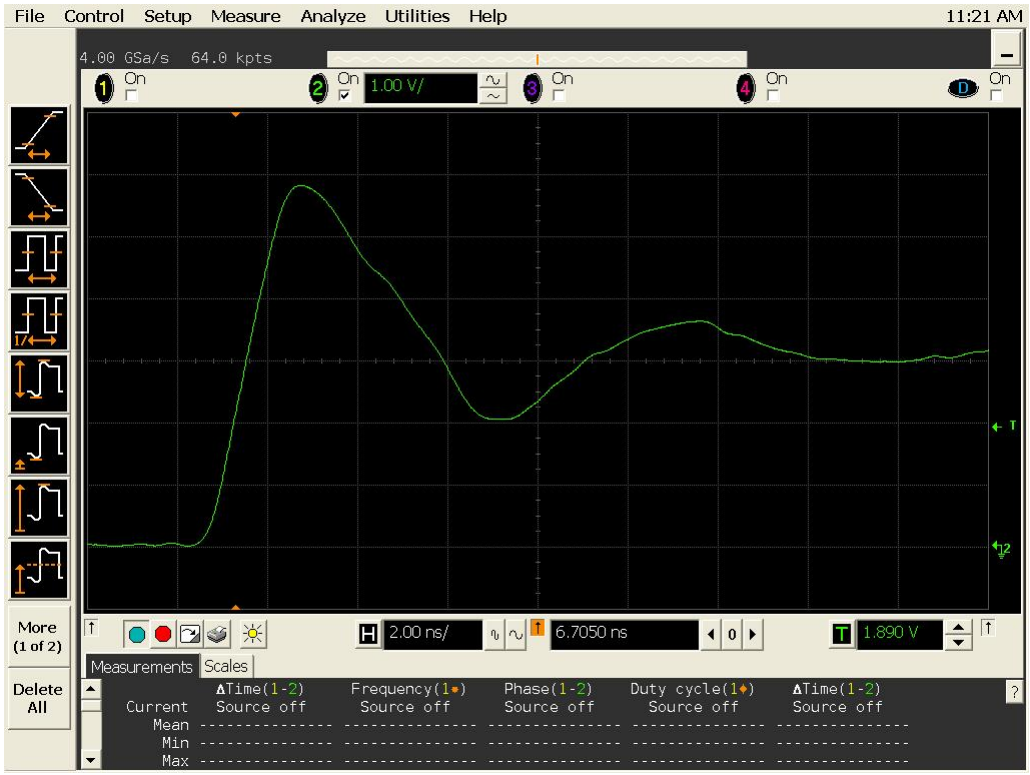


Figure 11b DUT 5264 Post-Annealing Rising edge

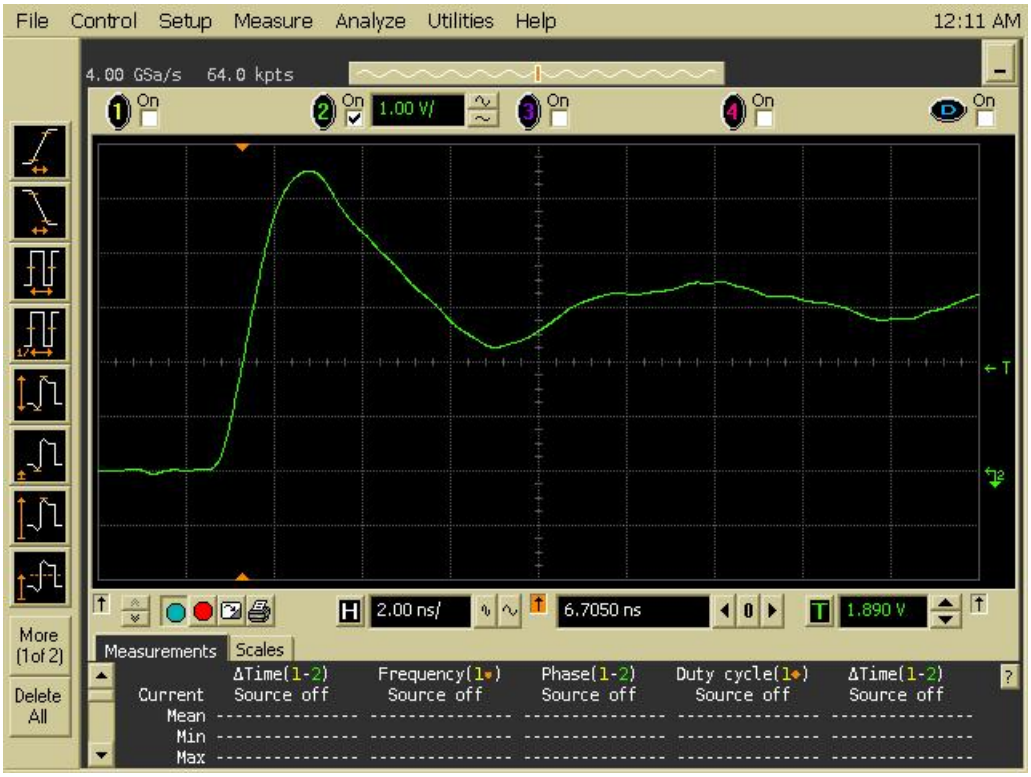


Figure 12a DUT 5275 Pre-Irradiation Rising Edge

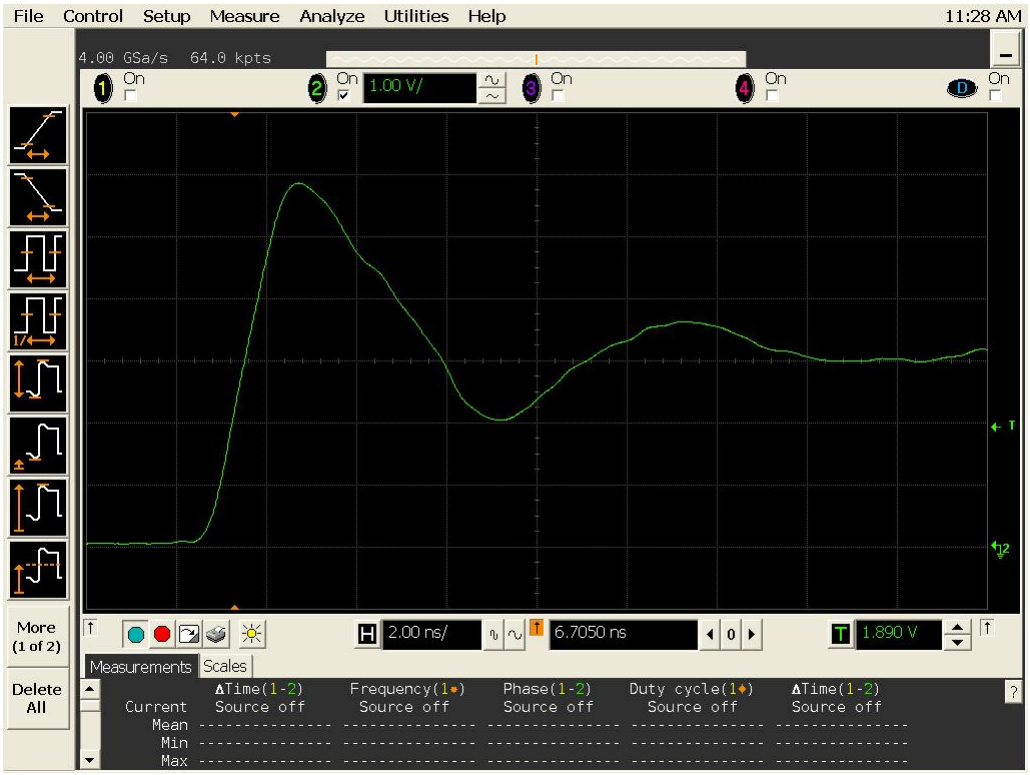


Figure 12b DUT 5275 Post-Annealing Rising Edge

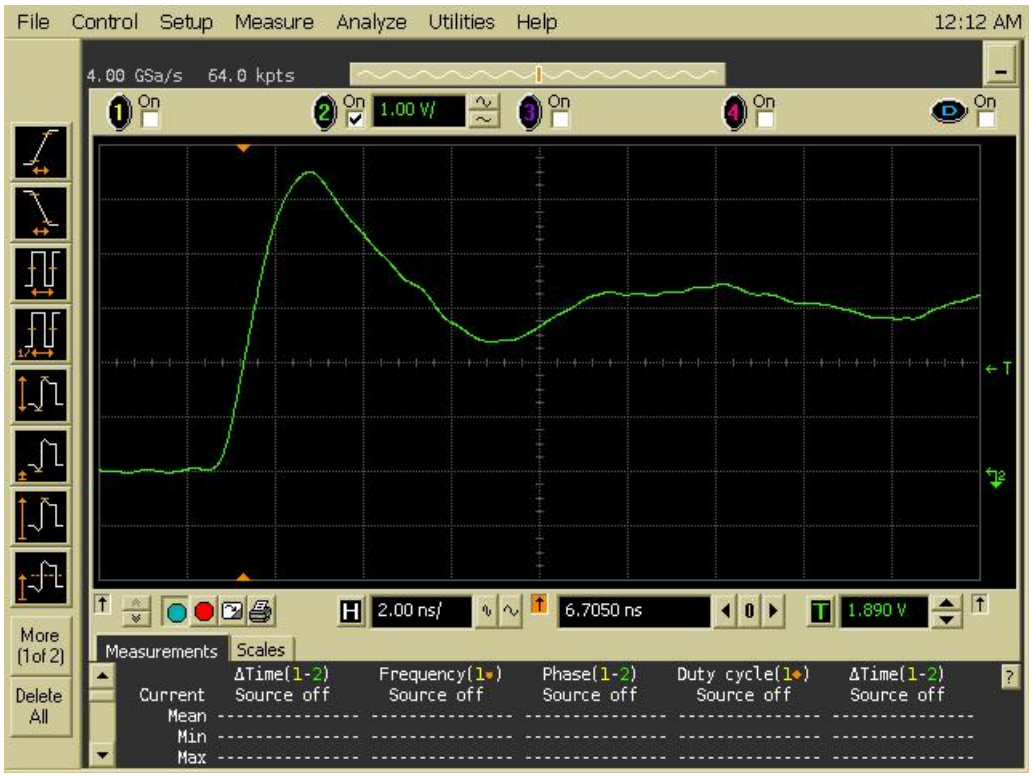


Figure 13a DUT 5278 Pre-Irradiation Rising Edge

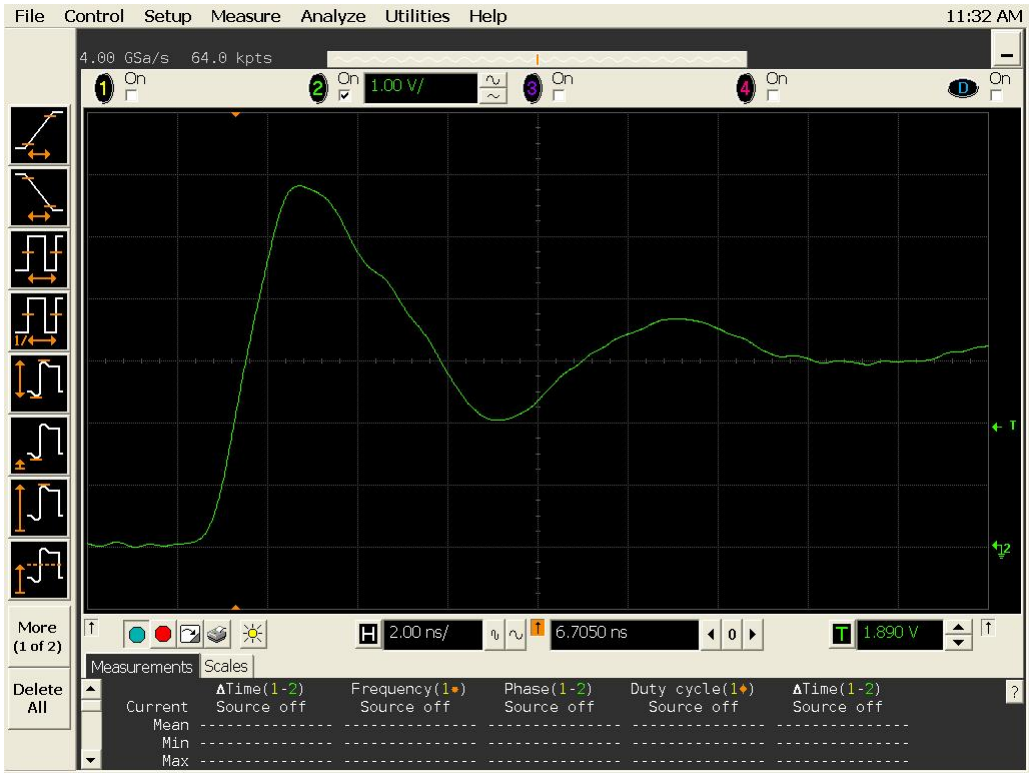


Figure 13b DUT 5278 Post-Annealing Rising Edge

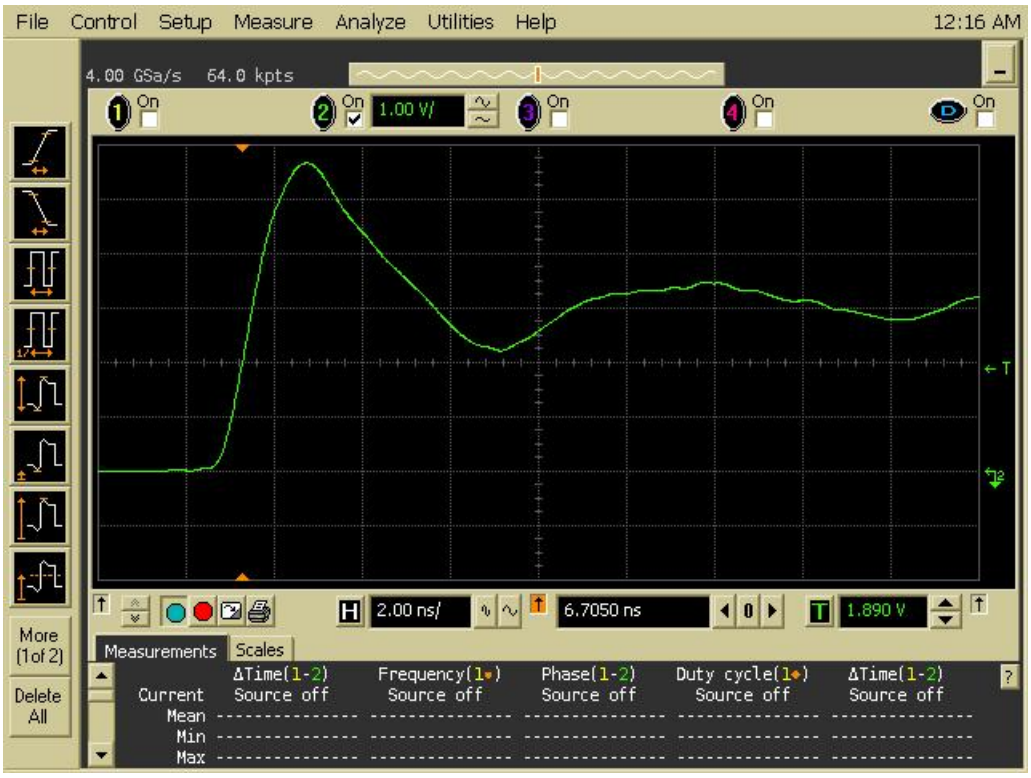


Figure 14a DUT 5282 Pre-Irradiation Rising Edge

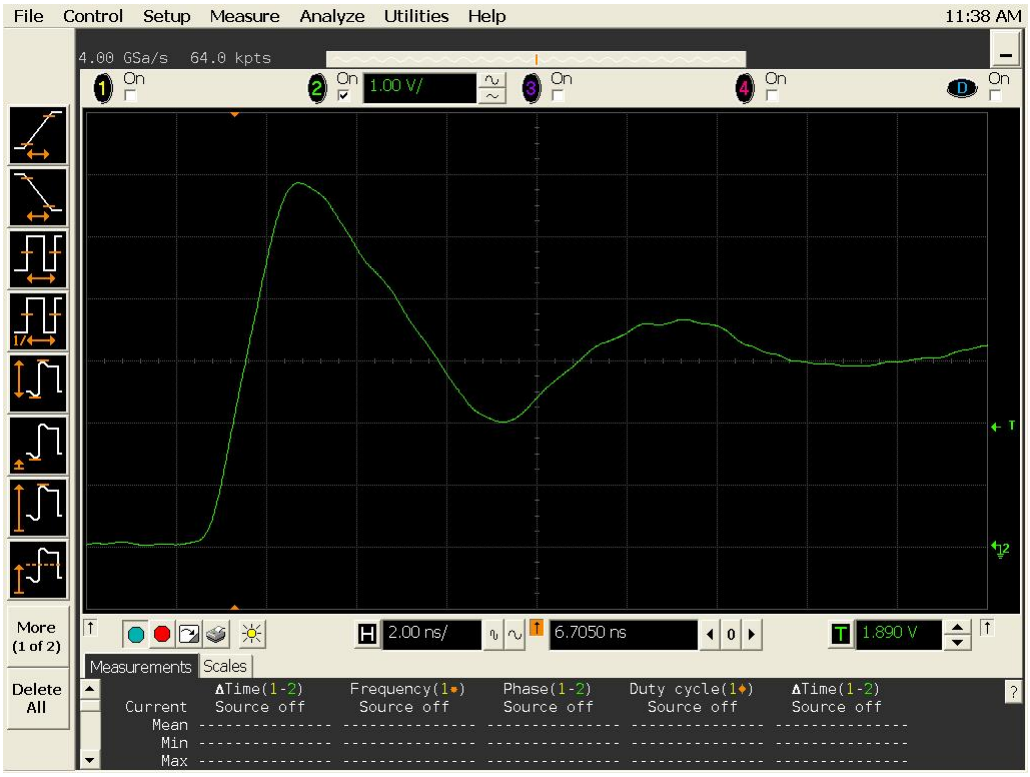


Figure 14b DUT 5282 Post-Annealing Rising Edge



Figure 15a DUT 5254 Pre-Radiation Falling Edge

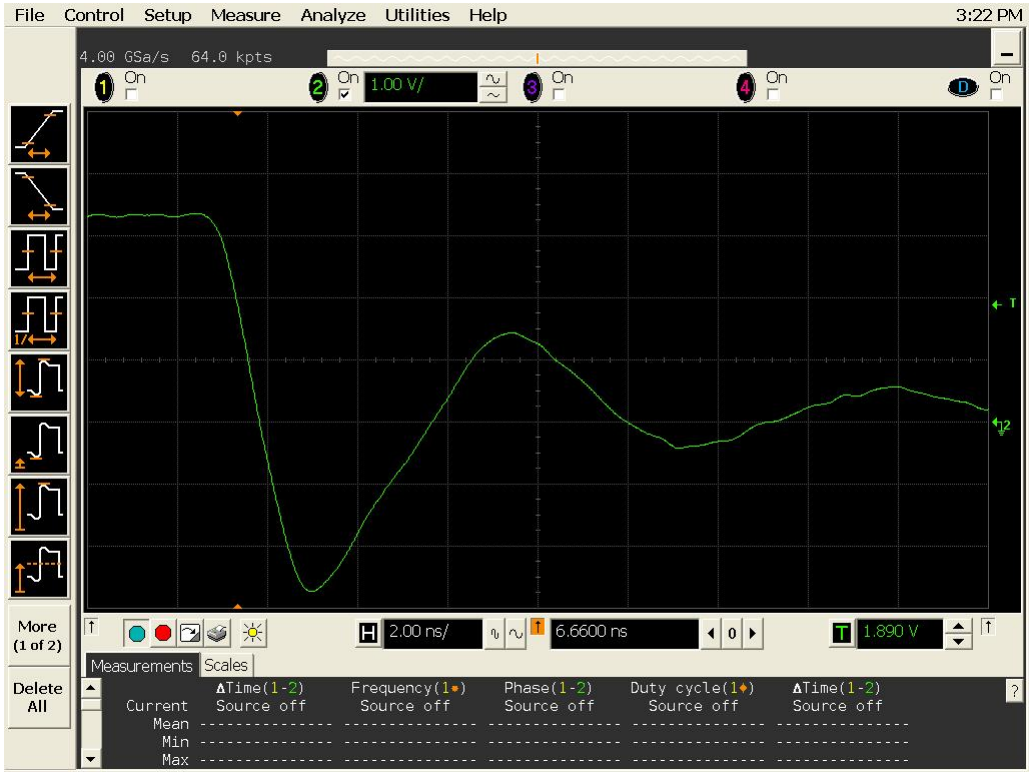


Figure 15b DUT 5254 Post-Annealing Falling Edge



Figure 16a DUT 5263 Pre-Irradiation Falling Edge

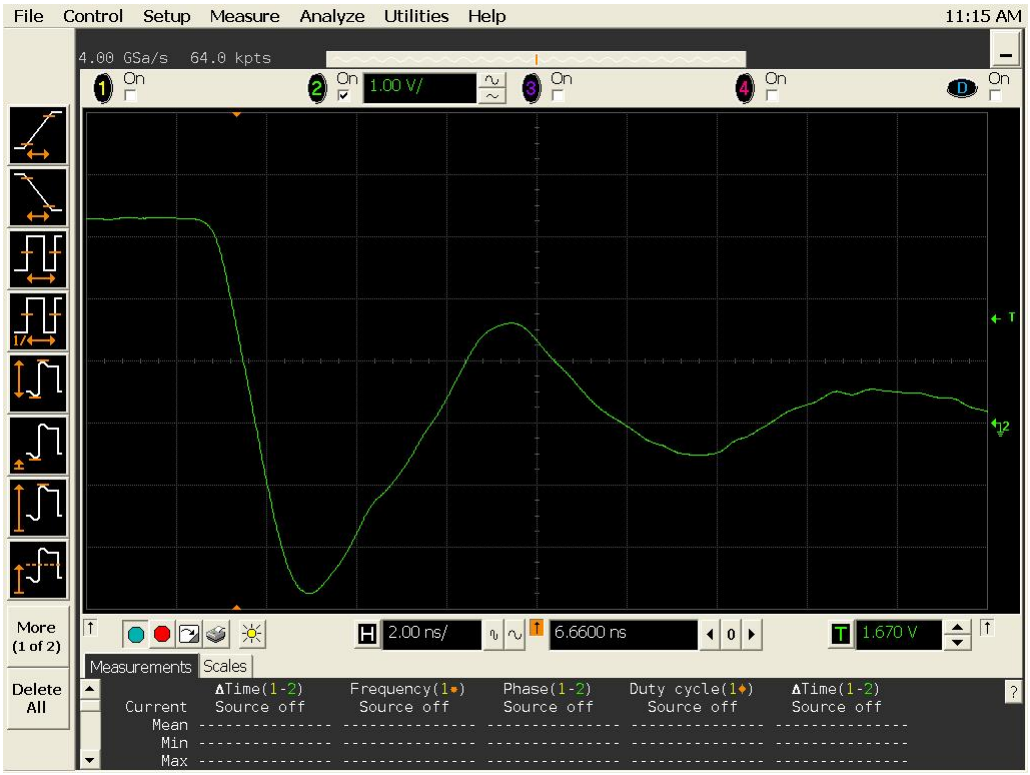


Figure 16b DUT 5263 Post-Annealing Falling Edge

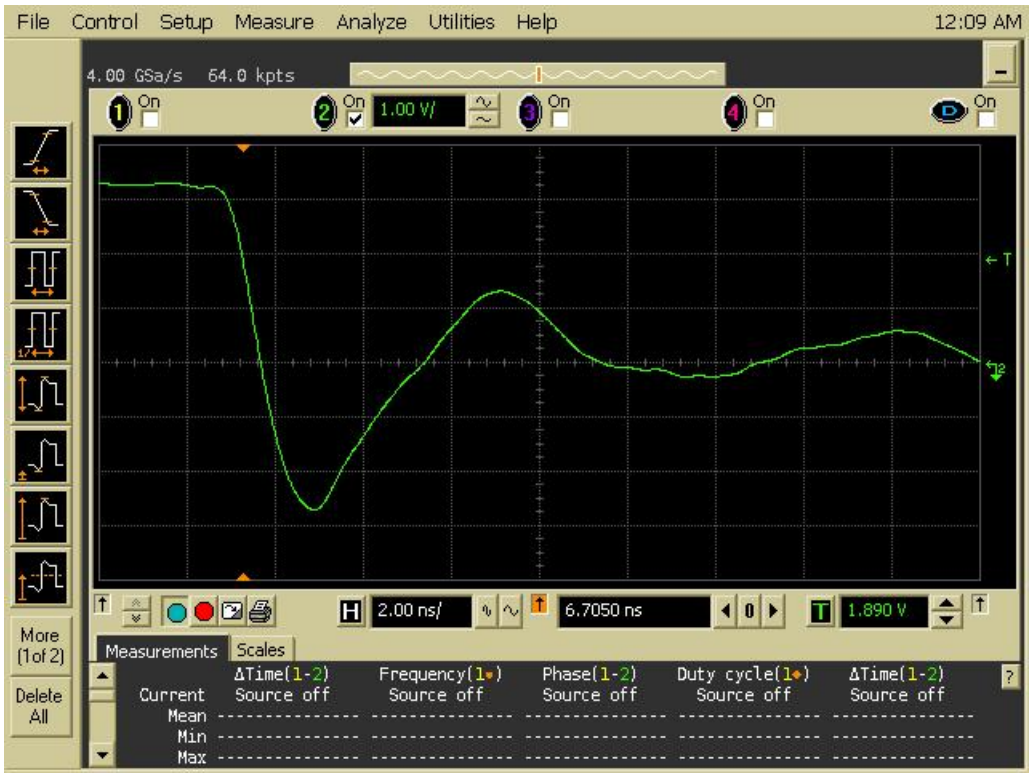


Figure 17a DUT 5264 Pre-Irradiation Falling Edge

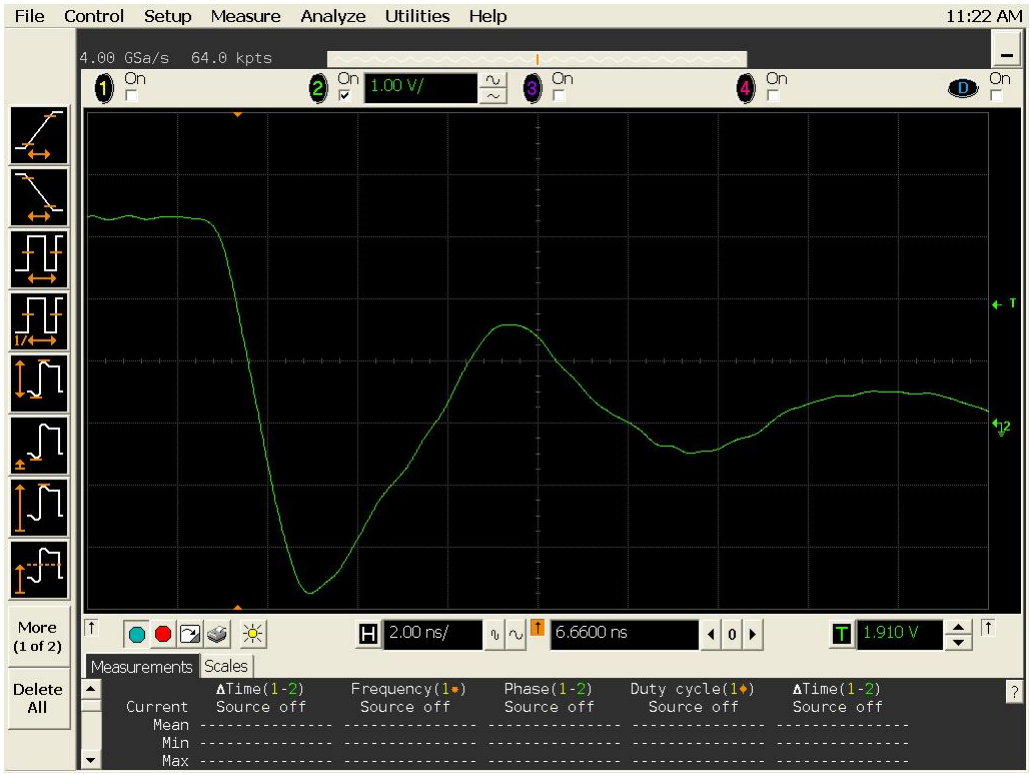


Figure 17b DUT 5264 Post-Annealing Falling Edge



Figure 18a DUT 5275 Pre-Irradiation Falling Edge

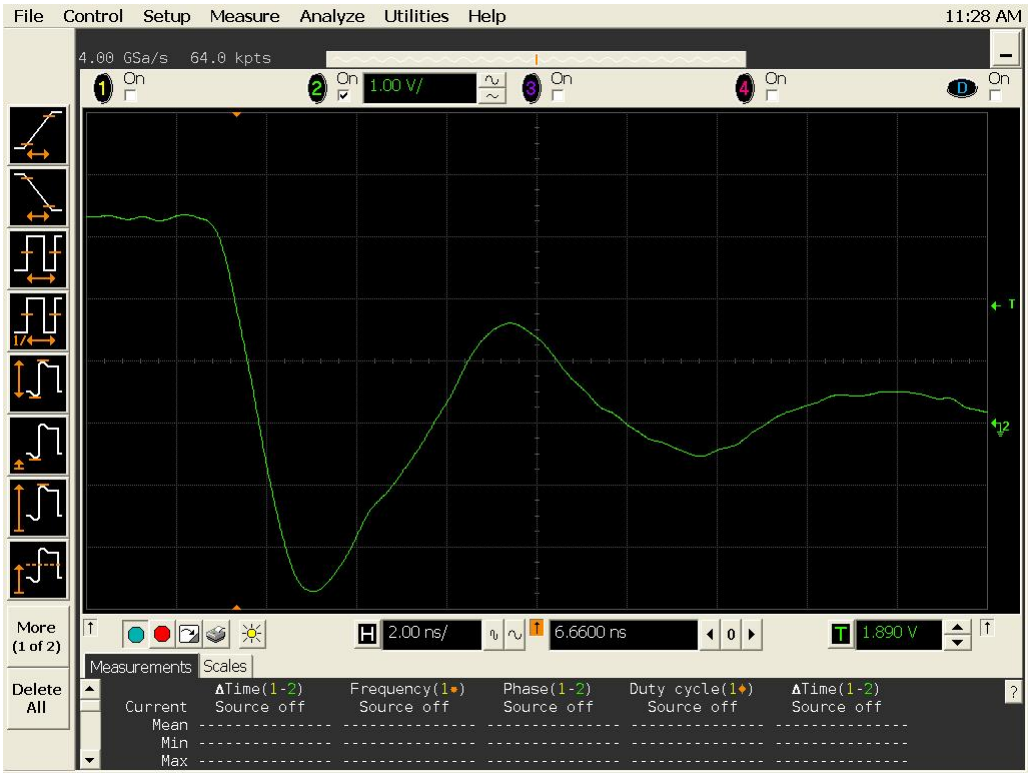


Figure 18b DUT 5275 Post-Annealing Falling Edge



Figure 19a DUT 5278 Pre-Irradiation Falling Edge

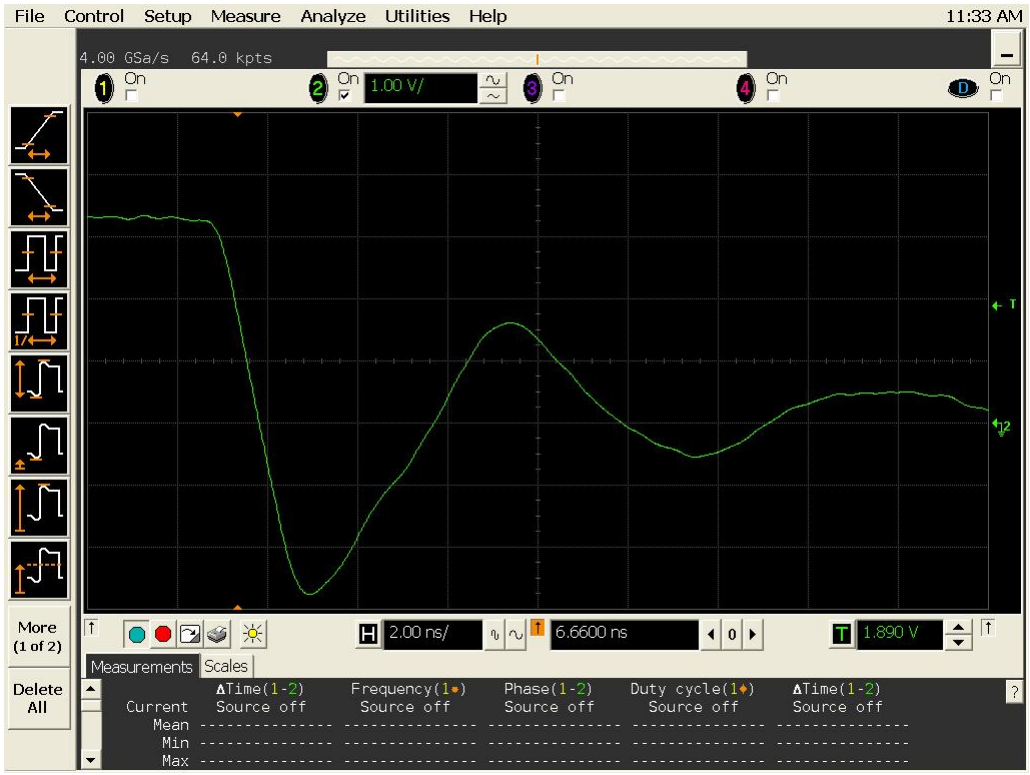


Figure 19b DUT 5278 Post-Annealing Falling Edge



Figure 20a DUT 5282 Pre-Irradiation Falling Edge

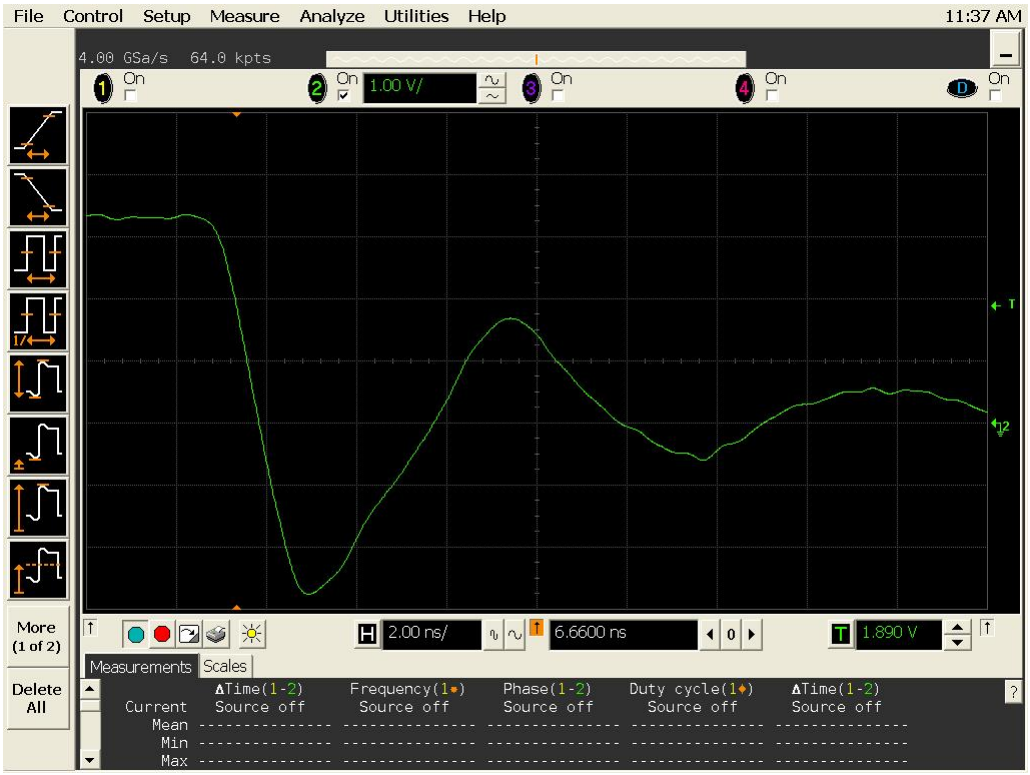
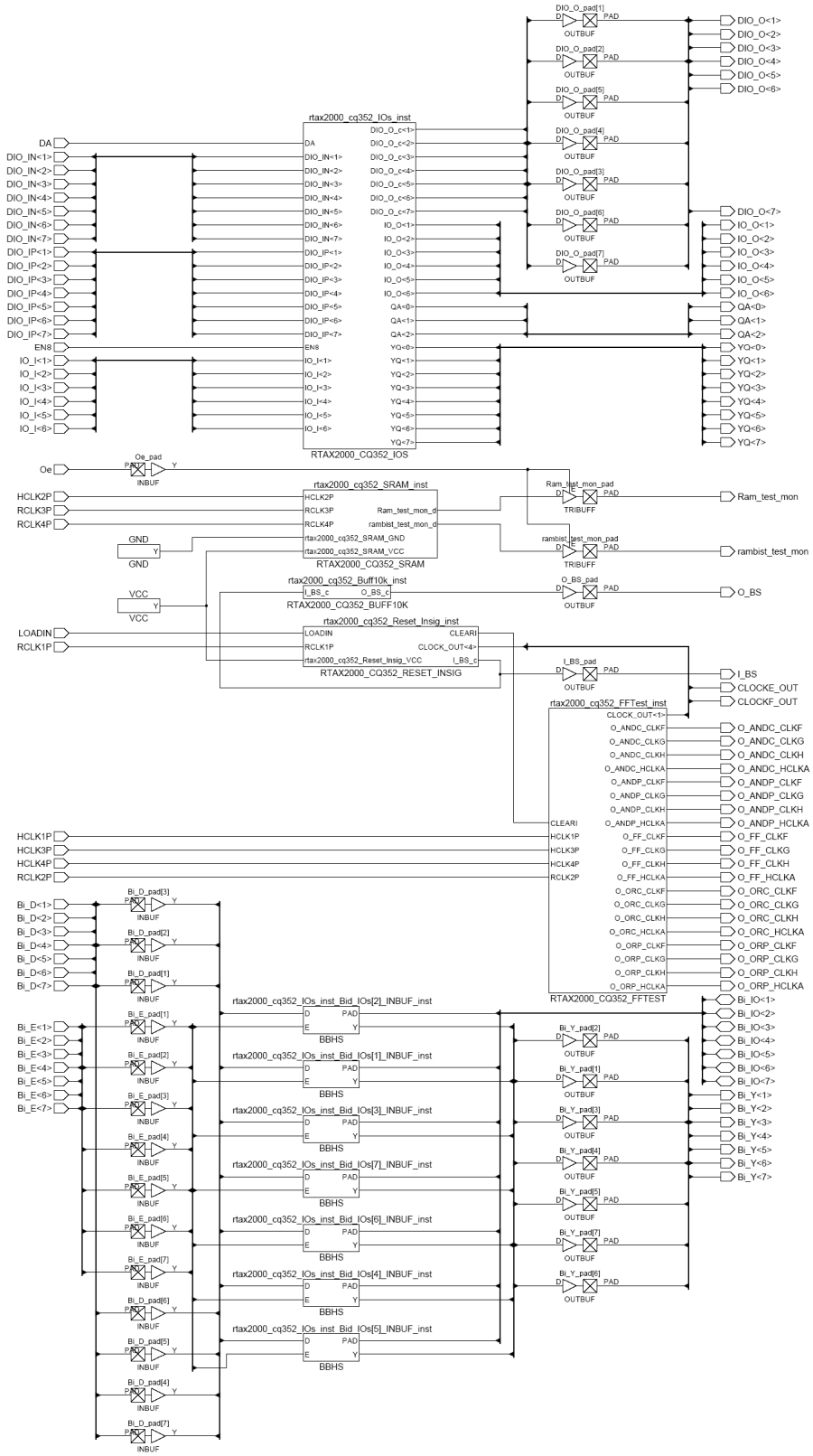


Figure 20b DUT 5282 Post-Annealing Falling Edge

Appendix A: DUT Design Schematics





Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

© 2012 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.