Total Ionizing Dose Test Report

No. 11T-RTSX72SU-CQ208-D1WW91

January 24, 2011

Table of Contents

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January 24, 20110
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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO_2)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 60 krad (SiO_2) per 25-mA spec after 7-day room temperature annealing
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (SiO_2)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (SiO_2)
5. Propagation Delay	Passed 100 krad (SiO_2) per 10%-degradation criterion
6. Transition Time	Passed 100 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGAs in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input is grounded through a jumper; during annealing each input is grounded through a 1 kohm resistor.

Table 1 DUT and Irradiation Parameters

Part Number	**RTSX72SU**
Package	CQFP208
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72SCQ208_25strings_mod
Die Lot Number	D1WW91
Quantity Tested	6
Serial Number	40 krad: 7190, 7191 60 krad: 7194, 7238 100 krad: 7254, 7282
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO2)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

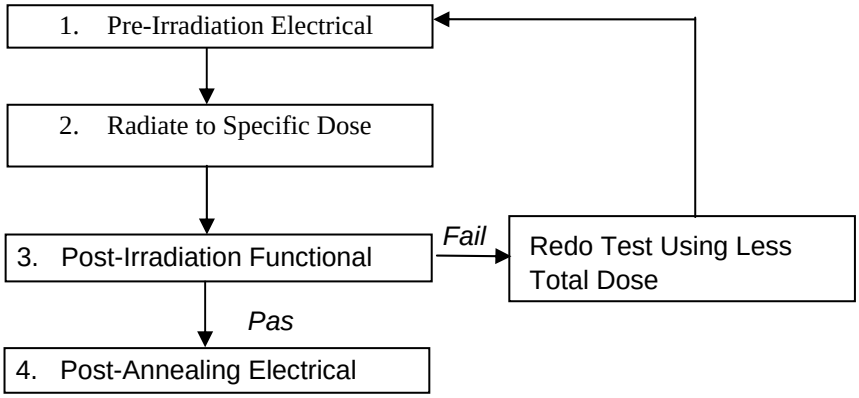


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in Microsemi products manufactured by sub-micron CMOS technology. To prove this point, test data with a high dose rate (1 krad (Si)/min) are compared to test data with a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. The results always show the low-dose-rate degradation less than the high-dose-rate degradation, thus indicating that the elevated rebound annealing would artificially reduce the radiation effects. Therefore, only room temperature annealing is performed in this report.

The duration of the room temperature annealing is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design, TDSX72SCQ208_25strings_mod, to test total dose effects in typical space applications. Appendix A contains the schematics illustrating the logic design.

Table 2 lists each tested electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and on the output pins (O_OR4 and O_NAND4) of a shift register with 1536 flip-flops. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on combinational nets listed in Row 3 and 4 of Table 2.

The propagation delays are measured on the O_AND4 output of one buffer string. The delay is measured as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Table 3 shows the pre-irradiation, post-irradiation, and post-annealing I_{CCA} and I_{CCI}. It indicates that the post-annealing I_{CCA} and I_{CCI} for 60 krad(SiO_2)-irradiated DUTs pass the specification of 25 mA.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-rad	Post-rad	Post-ann	Pre-rad	Post-rad	Post-ann
7190	40 krad	1.42	10.94	2.81	3.63	6.20	1.62
7191	40 krad	1.38	5.24	2.57	4.02	6.89	3.07
7194	60 krad	1.38	20.50	15.74	1.57	41.01	21.75
7238	60 krad	1.79	20.72	17.66	4.64	47.63	23.84
7254	100 krad	1.65	269.00	115.39	3.91	279.10	124.36
7282	100 krad	2.14	268.80	127.55	4.49	277.50	106.79

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4a through Table 4f list the pre-irradiation and post-annealing input logic thresholds. All data are within the specification limits; for each measurement, the post-annealing value is within ±10% of pre-irradiated value.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA/QA0				DAH/QA0H			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.43	1.43	1.41	1.50	1.24	1.44	1.42	1.44
7191	40 krad	1.41	1.40	1.40	1.40	1.15	1.24	1.41	1.41
7194	60 krad	1.41	1.41	1.40	1.42	1.15	1.18	1.46	1.45
7238	60 krad	1.42	1.42	1.41	1.47	1.24	1.21	1.46	1.41
7254	100 krad	1.42	1.43	1.41	1.53	1.15	1.16	1.41	1.44
7282	100 krad	1.41	1.44	1.41	1.53	1.23	1.22	1.41	1.45

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR/YO0				ENCNTRH/YO0H			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.45	1.45	1.43	1.57	1.43	1.46	1.42	1.42
7191	40 krad	1.44	1.45	1.40	1.39	1.42	1.45	1.40	1.40
7194	60 krad	1.44	1.43	1.40	1.39	1.40	1.44	1.40	1.39
7238	60 krad	1.44	1.46	1.41	1.40	1.42	1.45	1.40	1.39
7254	100 krad	1.44	1.23	1.42	1.44	1.42	1.44	1.40	1.41
7282	100 krad	1.44	1.47	1.41	1.44	1.42	1.41	1.41	1.43

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0/IDIO0				IDII1/IDIO1			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.44	1.47	1.45	1.46	1.42	1.46	1.46	1.46
7191	40 krad	1.43	1.42	1.44	1.40	1.33	1.35	1.43	1.45
7194	60 krad	1.43	1.45	1.44	1.41	1.35	1.38	1.42	1.44
7238	60 krad	1.43	1.45	1.44	1.41	1.31	1.35	1.42	1.45
7254	100 krad	1.44	1.43	1.44	1.46	1.39	1.37	1.44	1.48
7282	100 krad	1.43	1.45	1.43	1.50	1.38	1.40	1.42	1.59

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2/IDIO2				IDII3/IDIO3			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.38	1.33	1.43	1.42	1.39	1.38	1.46	1.45
7191	40 krad	1.34	1.33	1.43	1.43	1.36	1.43	1.53	1.44
7194	60 krad	1.34	1.34	1.44	1.39	1.36	1.43	1.50	1.45
7238	60 krad	1.34	1.33	1.44	1.39	1.36	1.37	1.53	1.45
7254	100 krad	1.35	1.43	1.45	1.47	1.37	1.40	1.44	1.57
7282	100 krad	1.33	1.43	1.43	1.46	1.36	1.49	1.53	1.51

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4/IDIO4				IDII5/IDIO5			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.45	1.41	1.57	1.44	1.43	1.46	1.44	1.44
7191	40 krad	1.42	1.40	1.40	1.41	1.39	1.42	1.42	1.42
7194	60 krad	1.14	1.42	1.41	1.41	1.41	1.39	1.43	1.42
7238	60 krad	1.14	1.41	1.40	1.41	1.41	1.42	1.42	1.42
7254	100 krad	1.43	1.39	1.40	1.43	1.41	1.47	1.43	1.47
7282	100 krad	1.42	1.40	1.40	1.44	1.42	1.46	1.43	1.45

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6/IDIO6				IDII7/IDIO7			
DUT	Total Dose	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann	Pre-Rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
7190	40 krad	1.36	1.15	1.44	1.48	1.37	1.45	1.44	1.45
7191	40 krad	1.33	1.34	1.42	1.41	1.40	1.33	1.42	1.41
7194	60 krad	1.32	1.35	1.42	1.49	1.38	1.38	1.41	1.42
7238	60 krad	1.31	1.34	1.42	1.41	1.40	1.40	1.42	1.42
7254	100 krad	1.35	1.21	1.43	1.40	1.37	1.39	1.50	1.46
7282	100 krad	1.32	1.40	1.41	1.40	1.39	1.42	1.42	1.50

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Table 5 and Table 6. The post-annealing data are within the specification limits; in each case, the post-annealing data varies insignificantly.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An
7190	40 krad	0.011	0.011	0.123	0.121	0.204	0.201	0.512	0.504	1.049	1.032
7191	40 krad	0.011	0.011	0.122	0.120	0.202	0.199	0.508	0.499	1.040	1.022
7194	60 krad	0.011	0.011	0.122	0.120	0.203	0.200	0.510	0.501	1.044	1.024
7238	60 krad	0.011	0.011	0.120	0.120	0.199	0.198	0.501	0.497	1.026	1.017
7254	100 krad	0.011	0.012	0.122	0.121	0.202	0.200	0.508	0.500	1.039	1.022
7282	100 krad	0.011	0.011	0.119	0.118	0.197	0.195	0.496	0.488	1.015	0.998

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An	Pre-Rad	Pos-An
7190	40 krad	4.978	4.981	4.846	4.849	4.615	4.618	3.994	3.996	2.619	2.601
7191	40 krad	4.977	4.980	4.845	4.848	4.613	4.616	3.985	3.988	2.575	2.558
7194	60 krad	4.977	4.979	4.844	4.845	4.609	4.610	3.973	3.972	2.522	2.489
7238	60 krad	4.977	4.979	4.843	4.845	4.607	4.609	3.968	3.969	2.491	2.475
7254	100 krad	4.977	4.977	4.845	4.843	4.613	4.609	3.985	3.972	2.574	2.490
7282	100 krad	4.978	4.978	4.845	4.843	4.612	4.608	3.981	3.966	2.532	2.433

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. All DUTs pass the 10%-degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Irradiation (µs)	Post-Annealing (µs)	Degradation (%)
7190	40 krad	1.397	1.397	1.392	-0.36%
7191	40 krad	1.432	1.430	1.425	-0.49%
7194	60 krad	1.417	1.432	1.419	0.14%
7238	60 krad	1.418	1.429	1.433	1.06%
7254	100 krad	1.447	1.648	1.538	6.29%
7282	100 krad	1.419	1.555	1.545	8.88%

F. Transition Time

Figure 2a to Figure 13b show pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

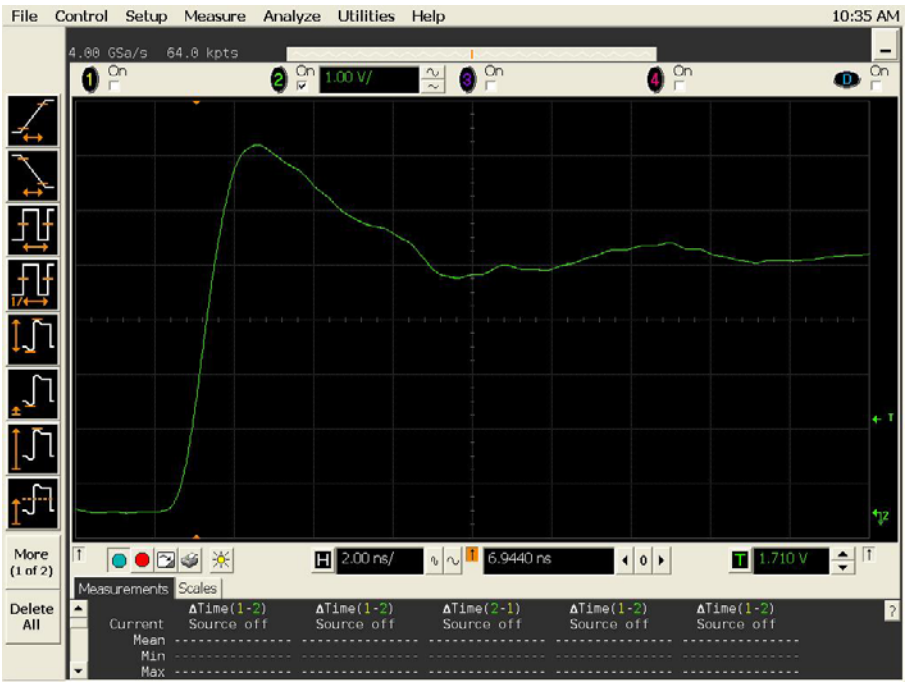


Figure 2a DUT 7190 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

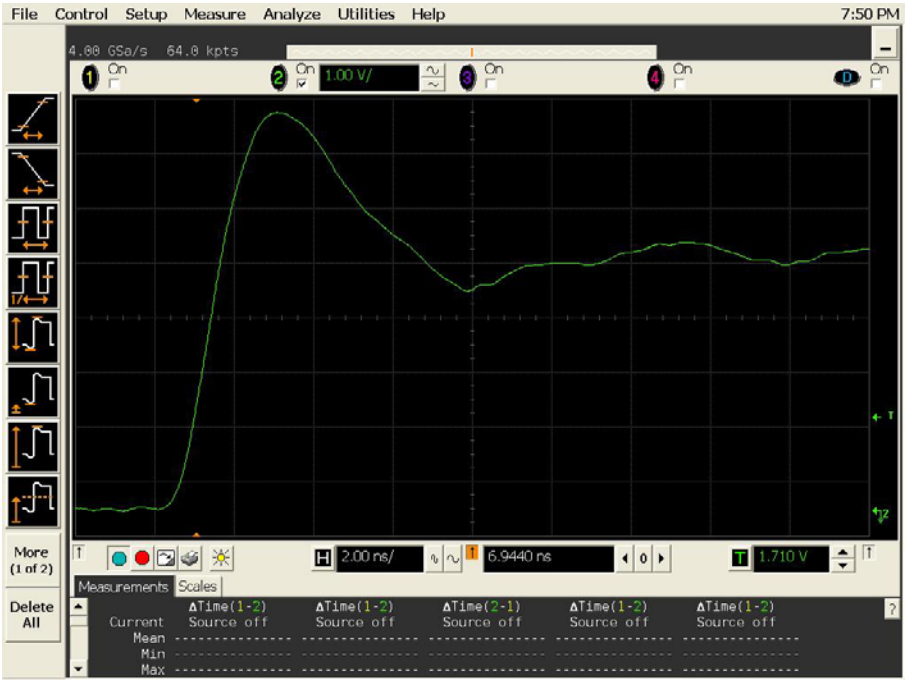


Figure 2b DUT 7190 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

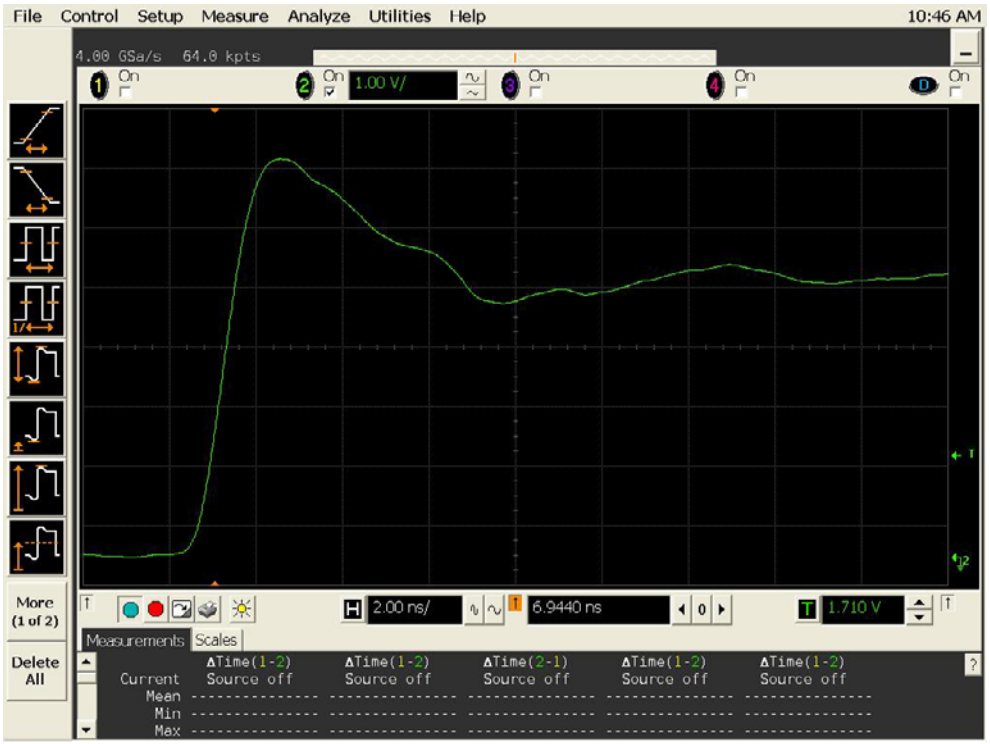


Figure 3a DUT 7191 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

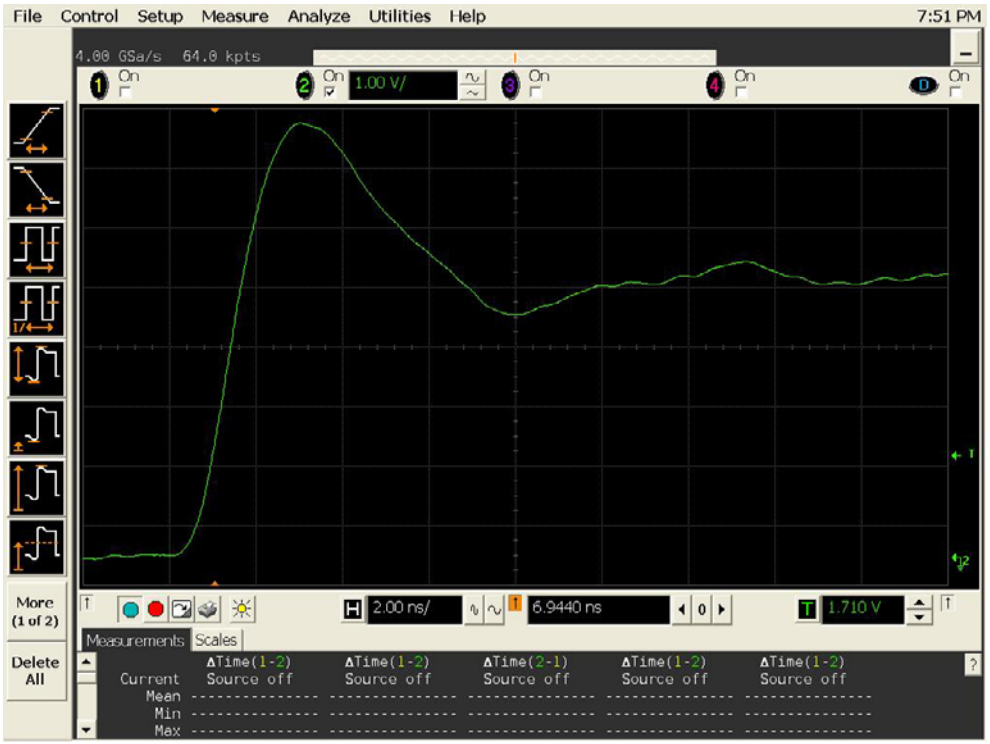


Figure 3b DUT 7191 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

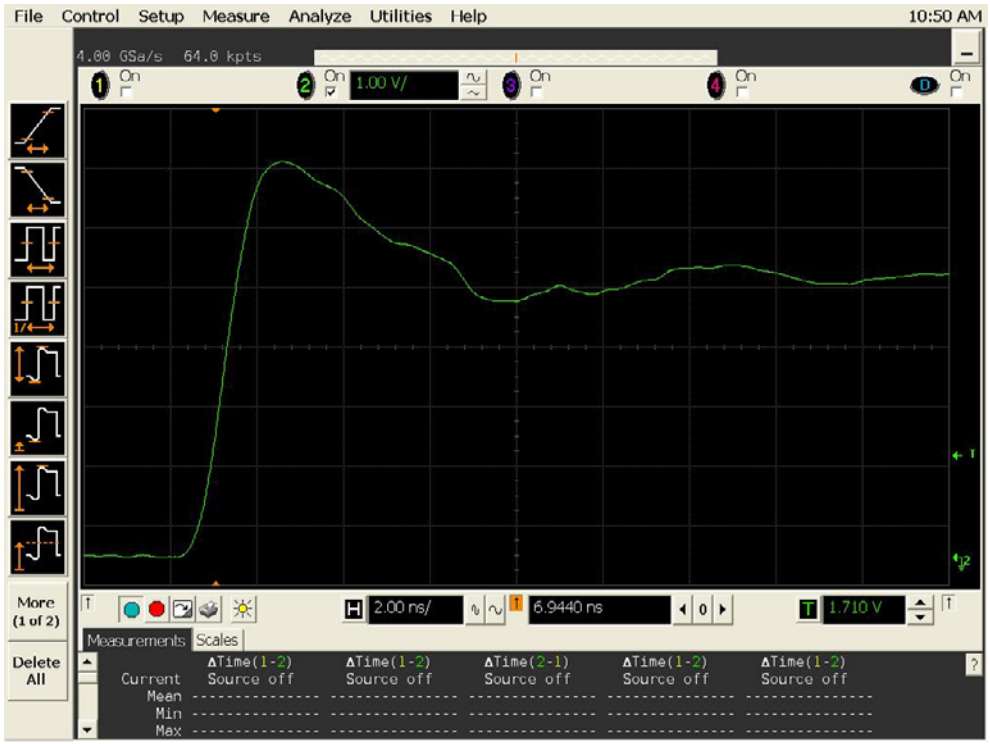


Figure 4a DUT 7194 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

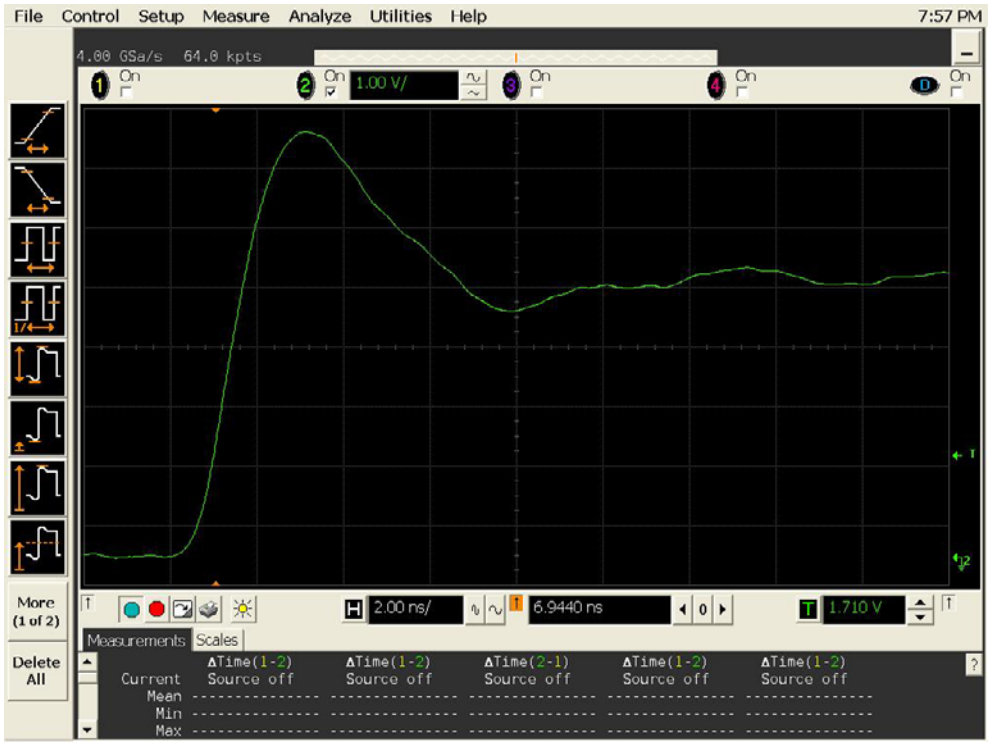


Figure 4b DUT 7194 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

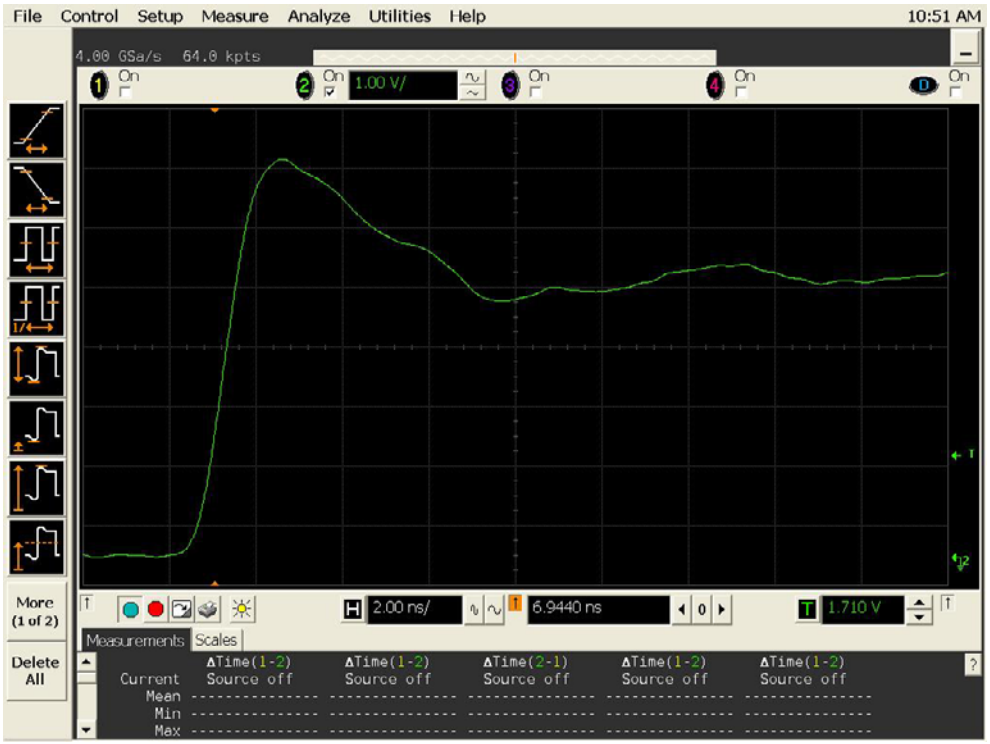


Figure 5a DUT 7238 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

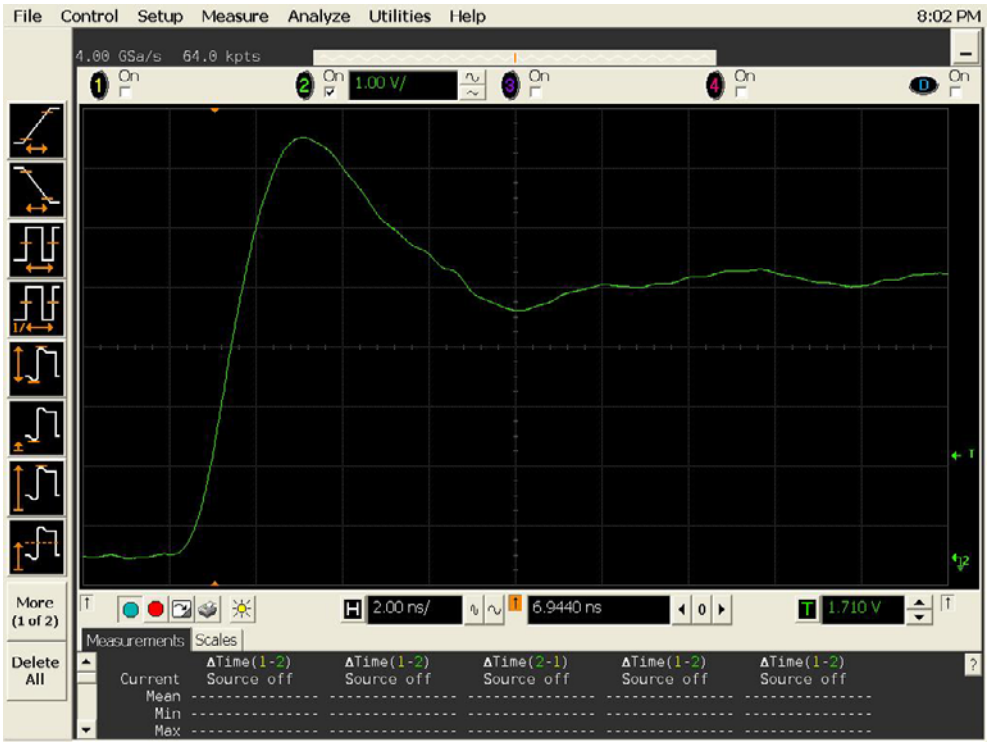


Figure 5b DUT 7238 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

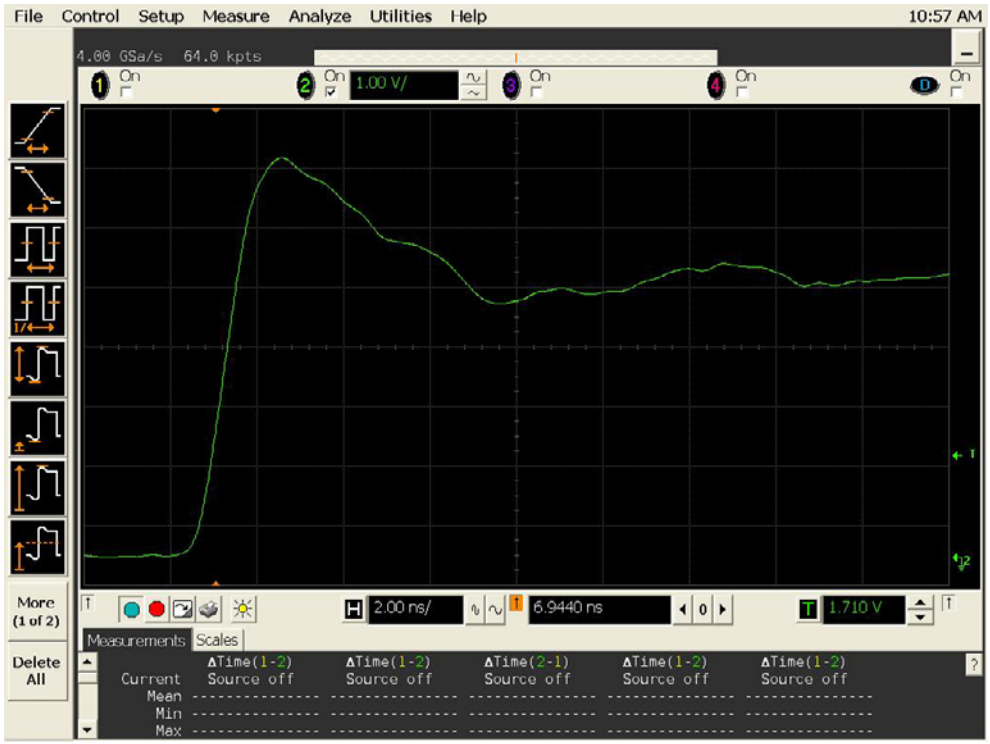


Figure 6a DUT 7254 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

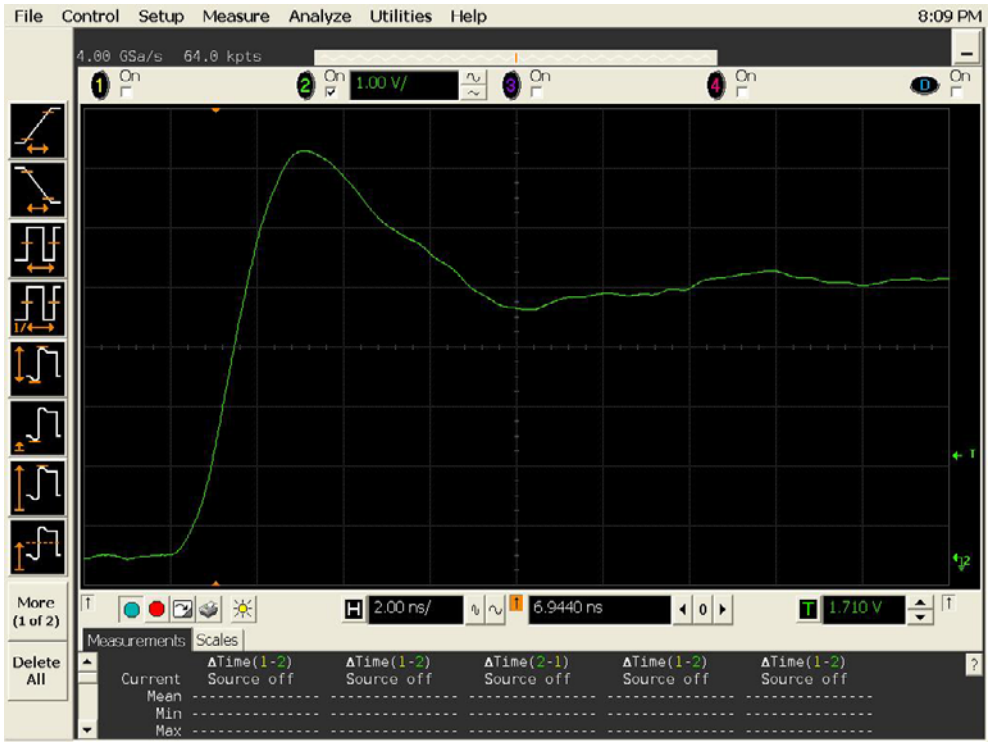


Figure 6b DUT 7254 Post-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

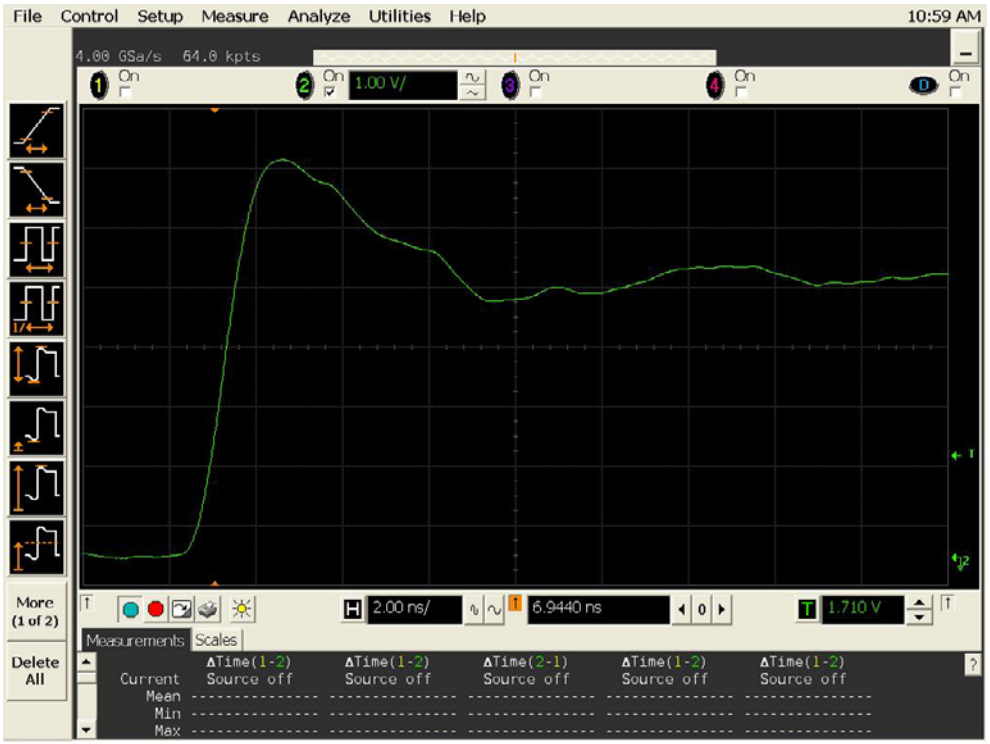


Figure 7a DUT 7282 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

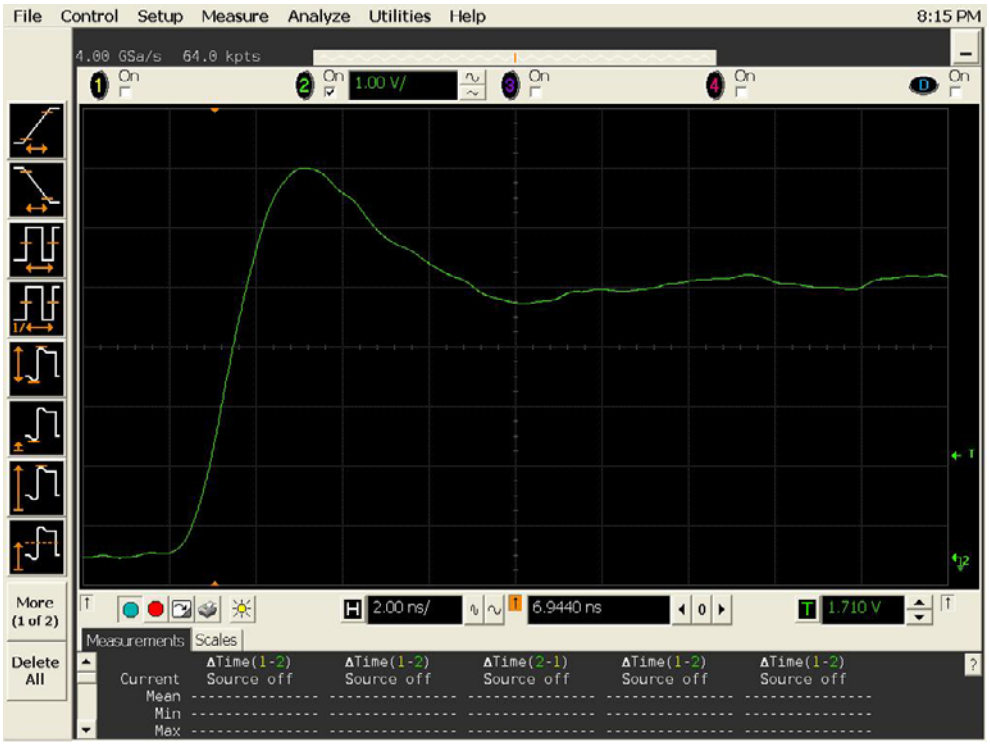


Figure 7b DUT 7282 Post-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

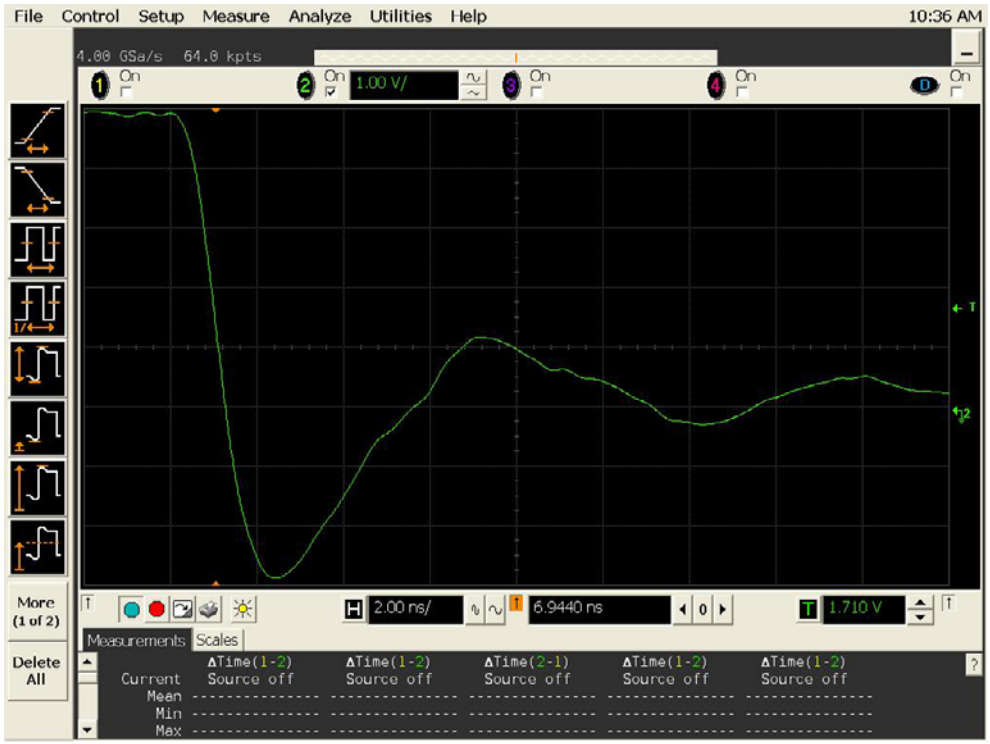


Figure 8a DUT 7190 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

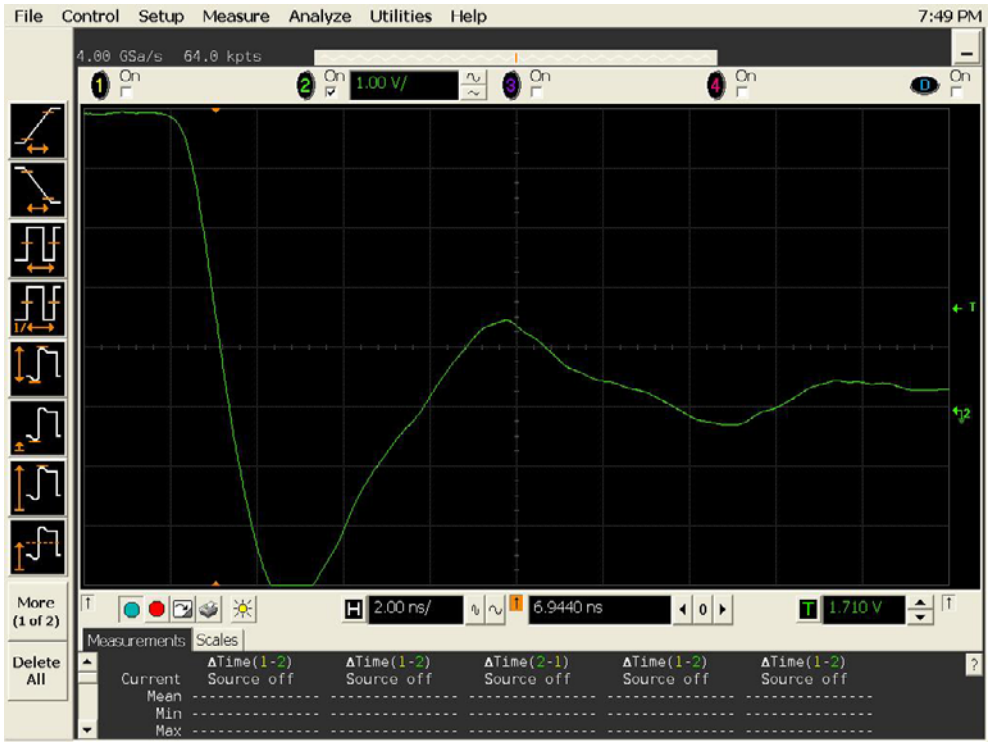


Figure 8b DUT 7190 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

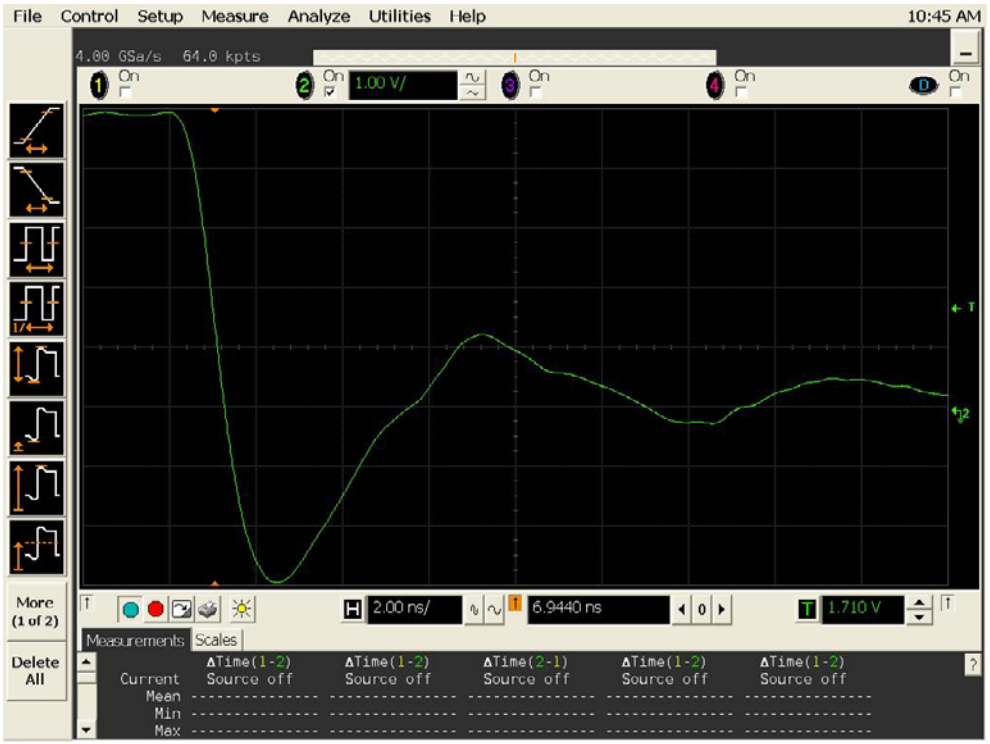


Figure 9a DUT 7191 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

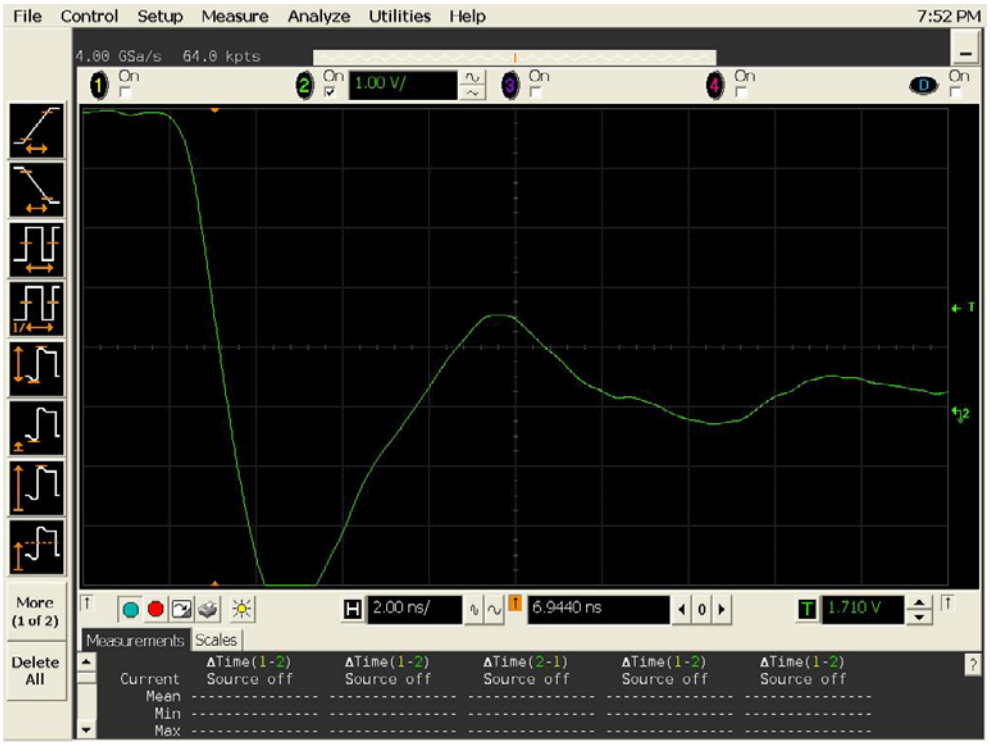


Figure 9b DUT 7191 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

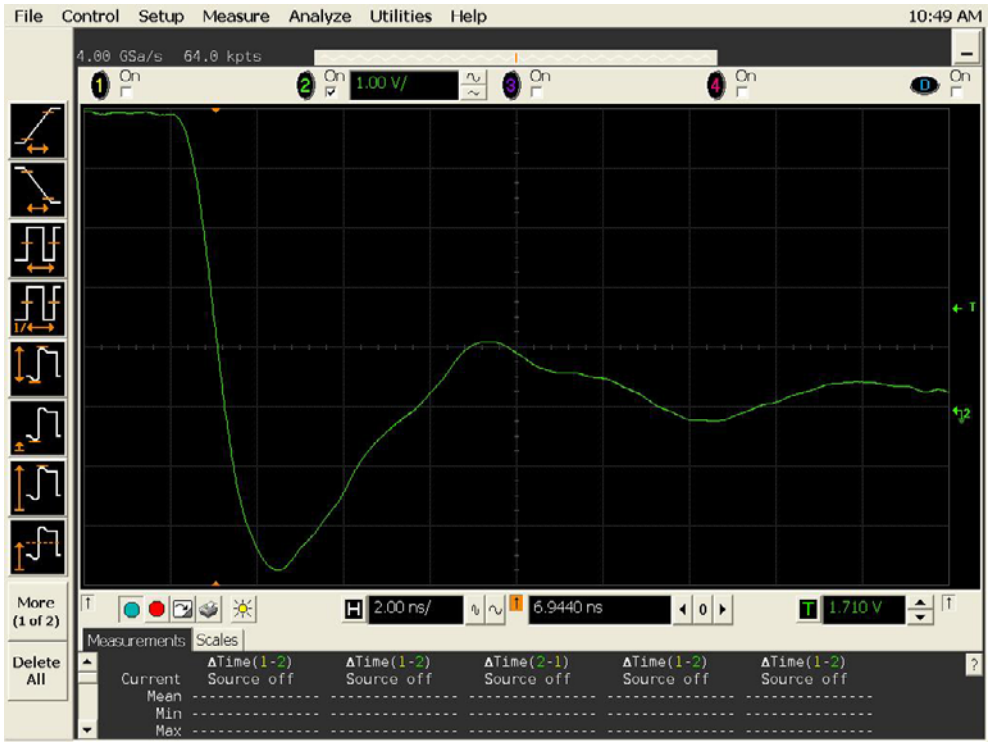


Figure 10(a) DUT 7194 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

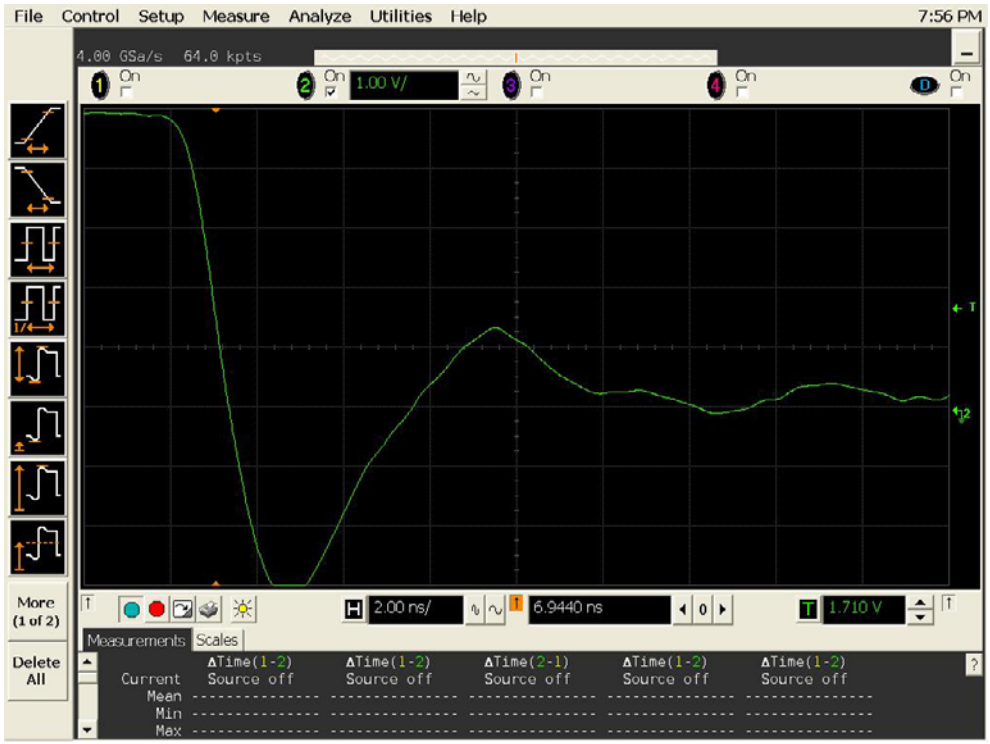


Figure 10b DUT 7194 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

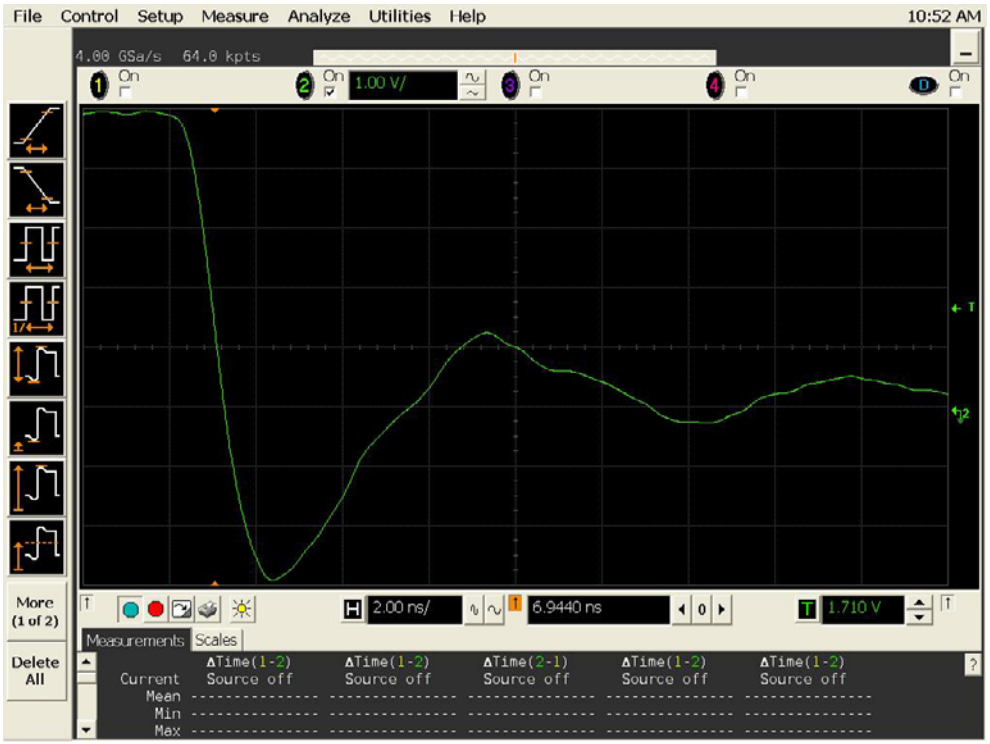


Figure 11a DUT 7238 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

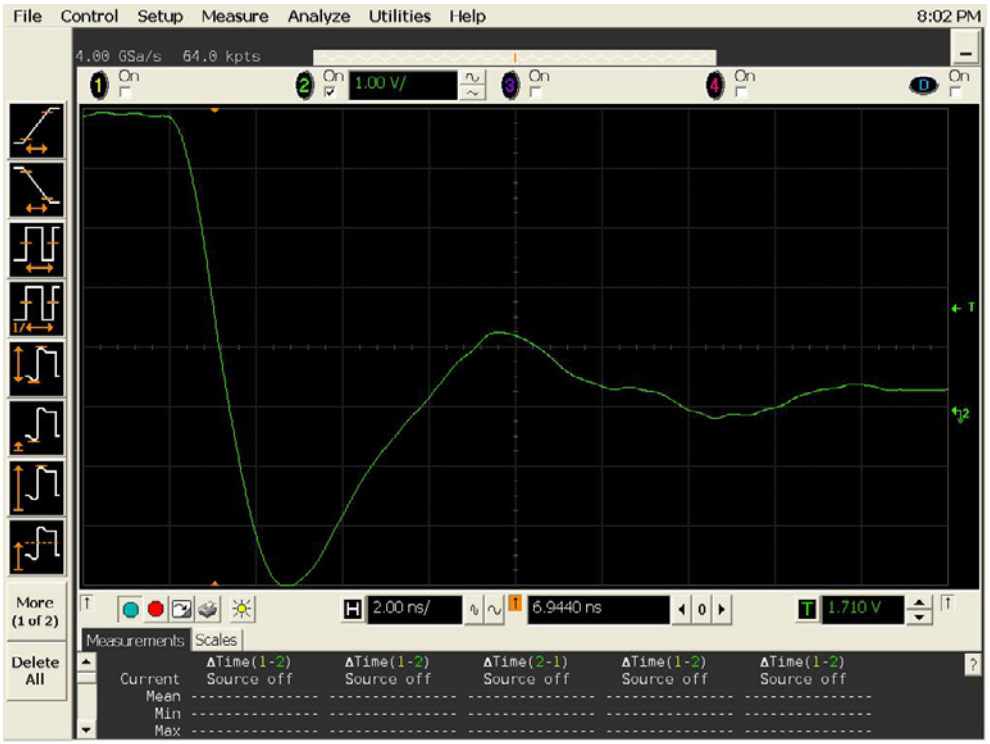


Figure 11b DUT 7238 Post-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

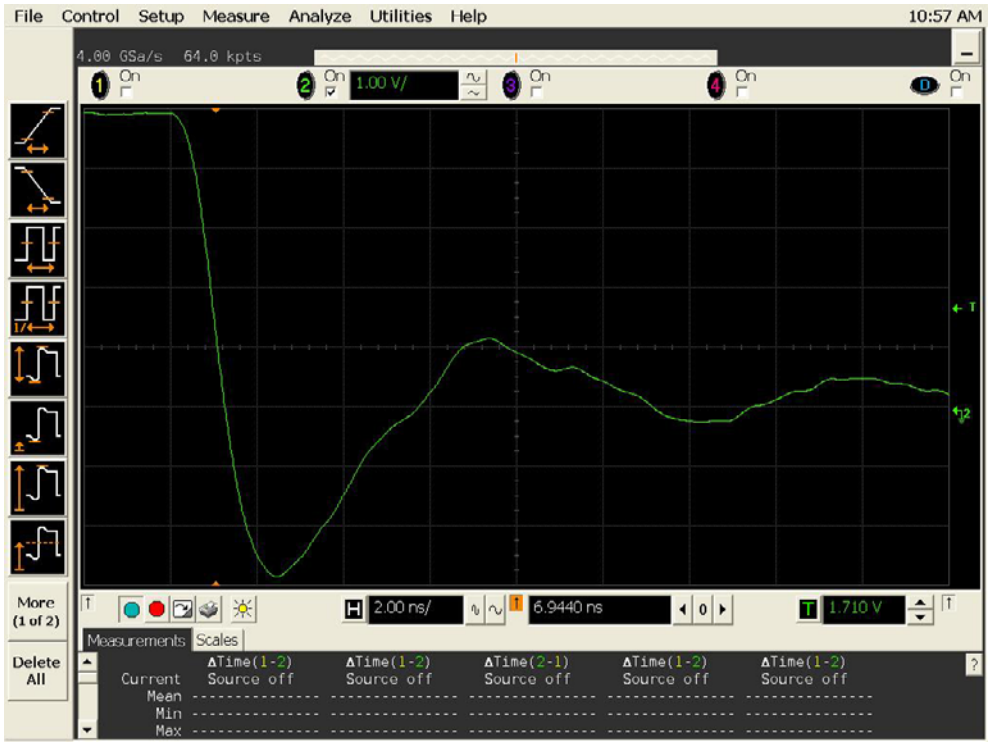


Figure 12a DUT 7254 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

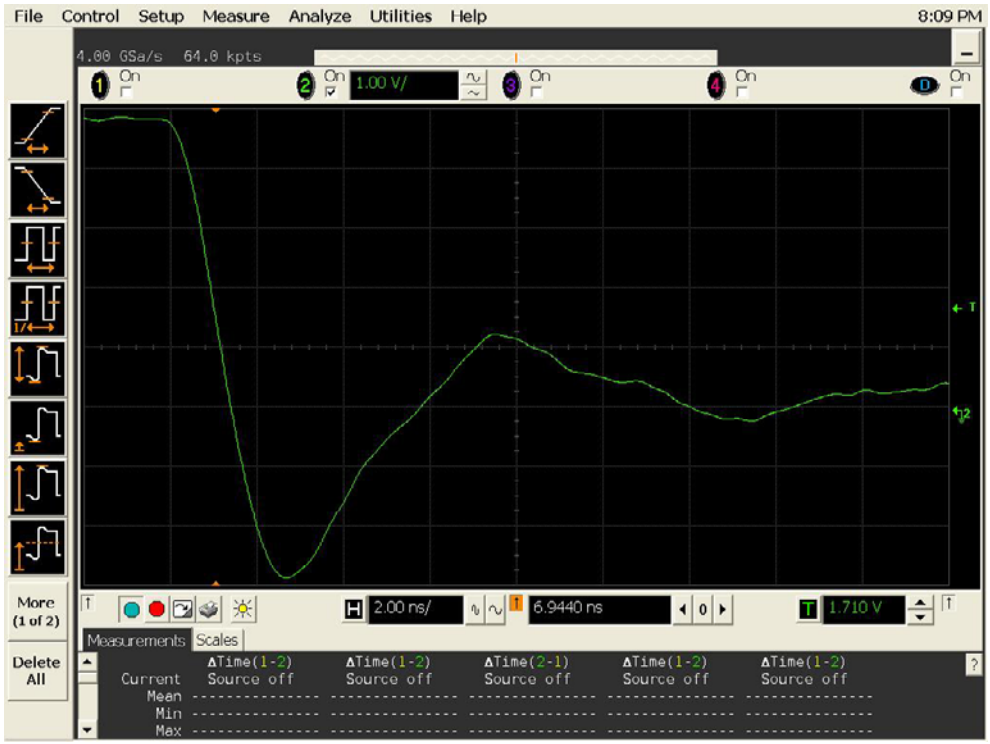


Figure 12b DUT 7254 Post-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

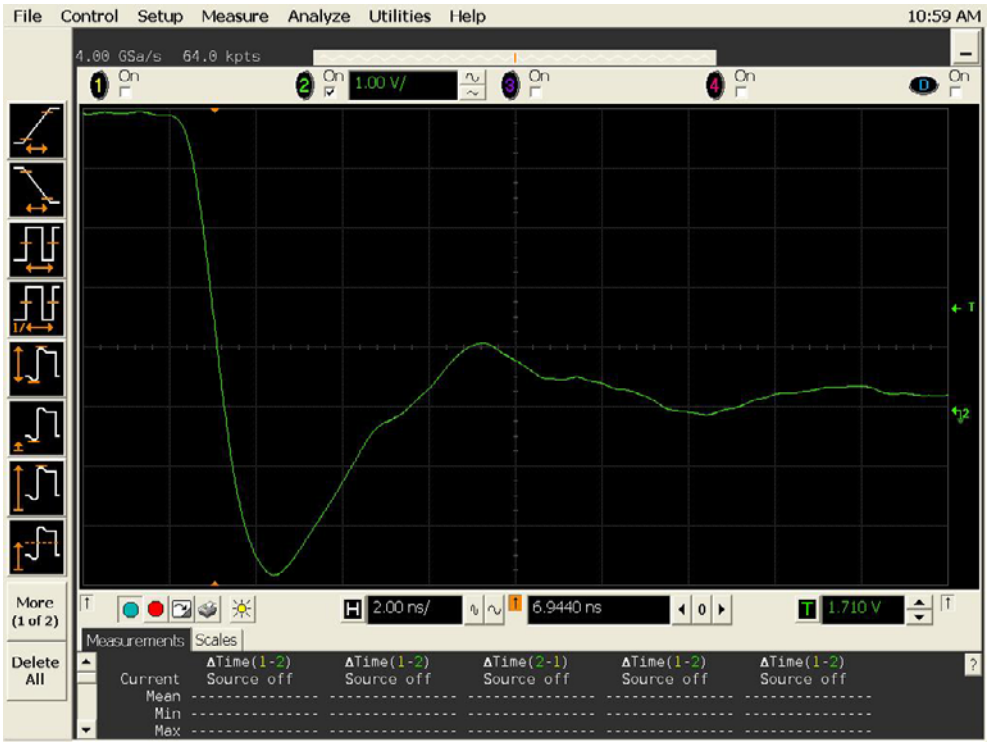


Figure 13a DUT 7282 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

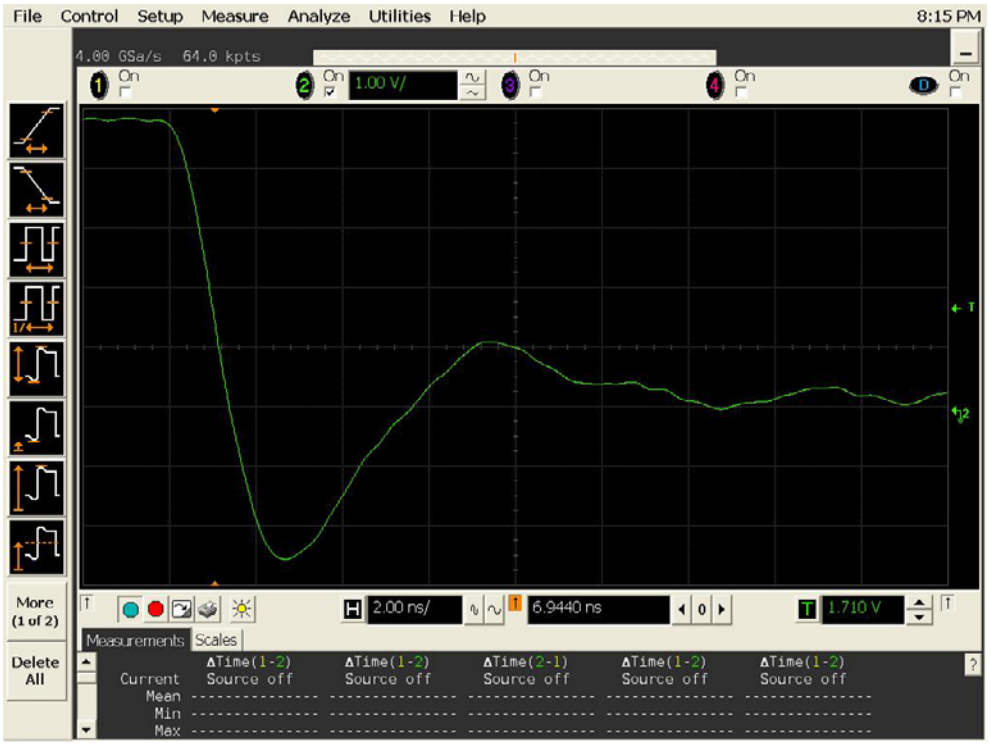
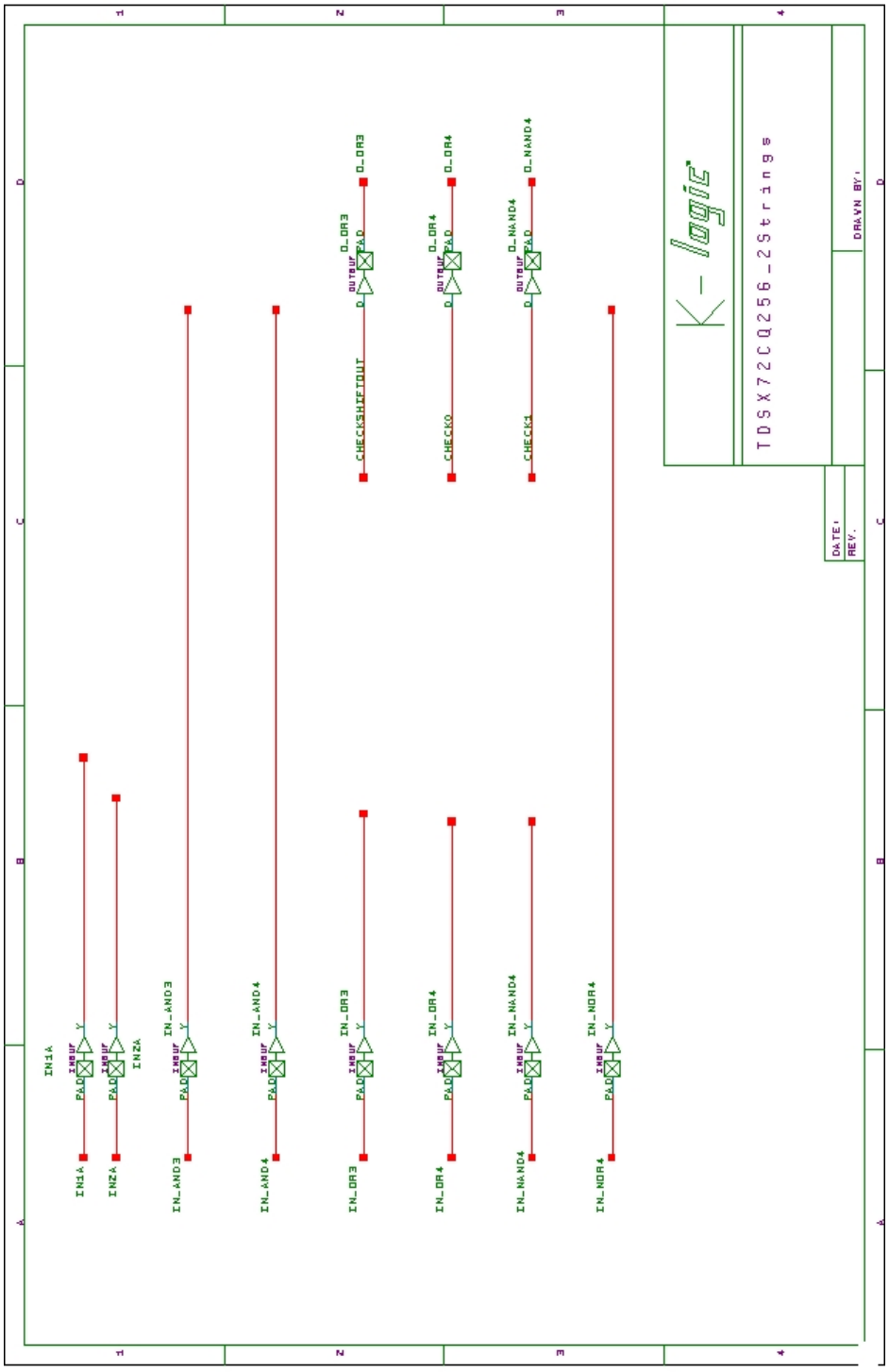
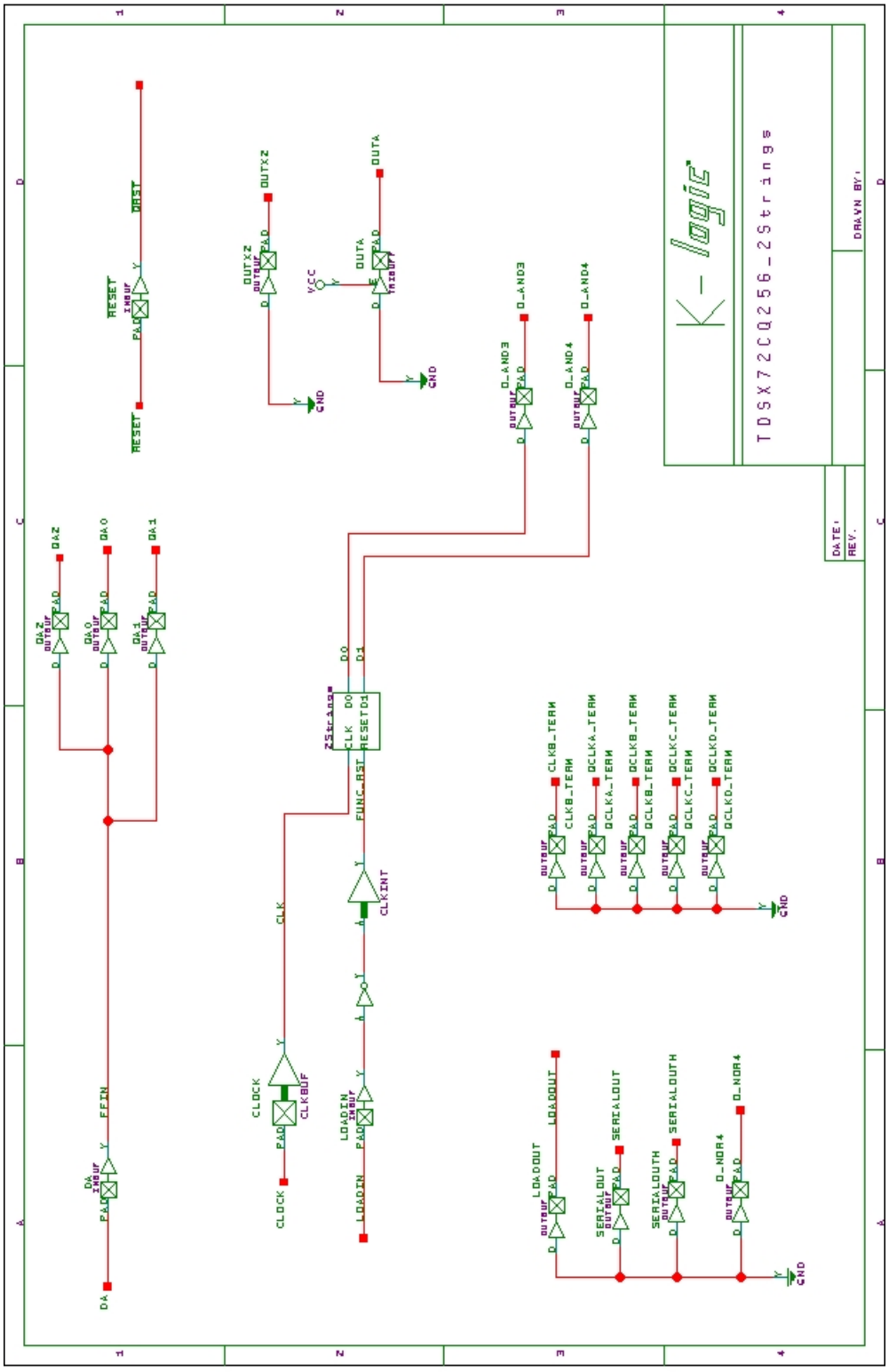
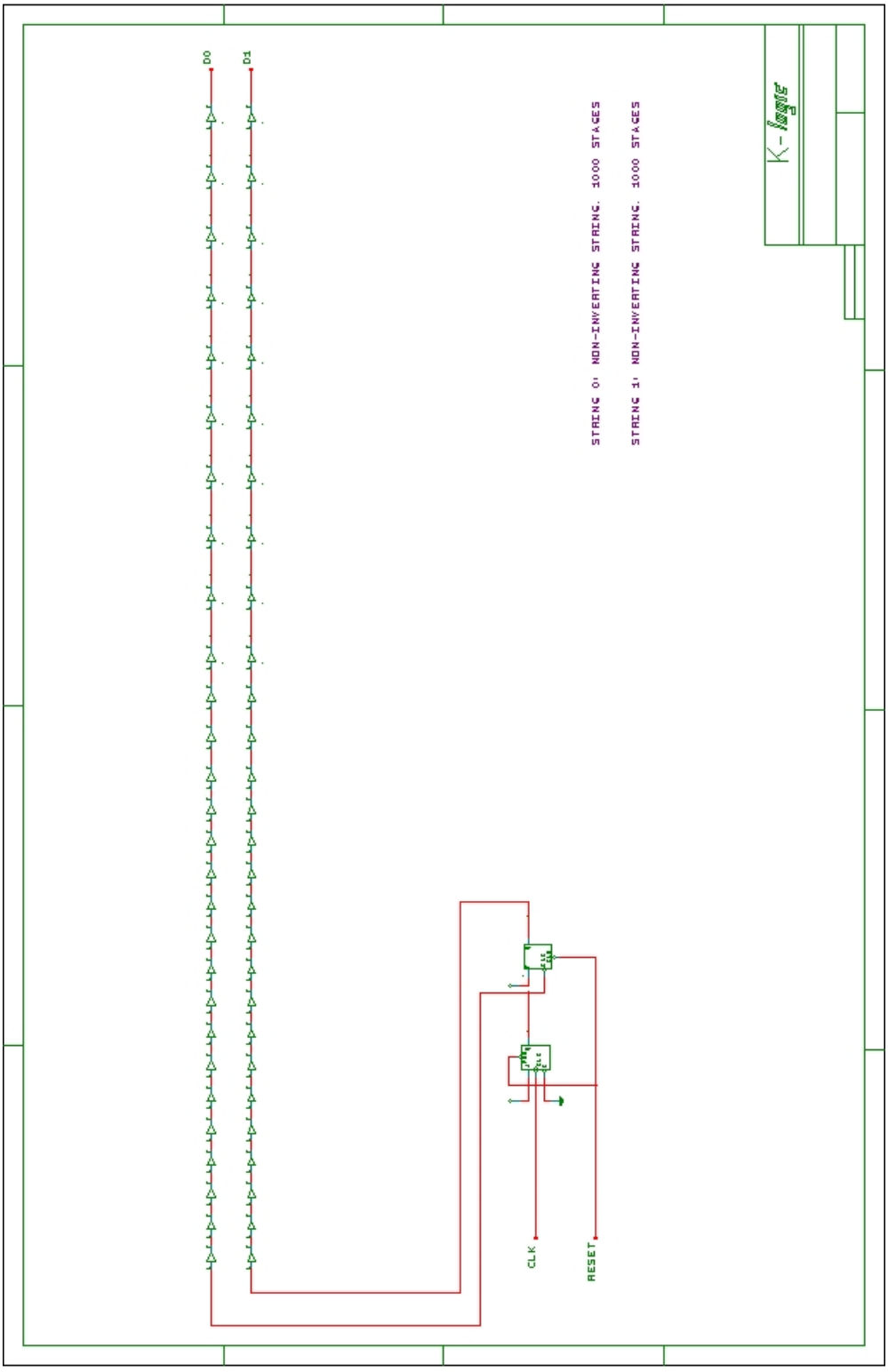


Figure 13b DUT 7282 Post-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

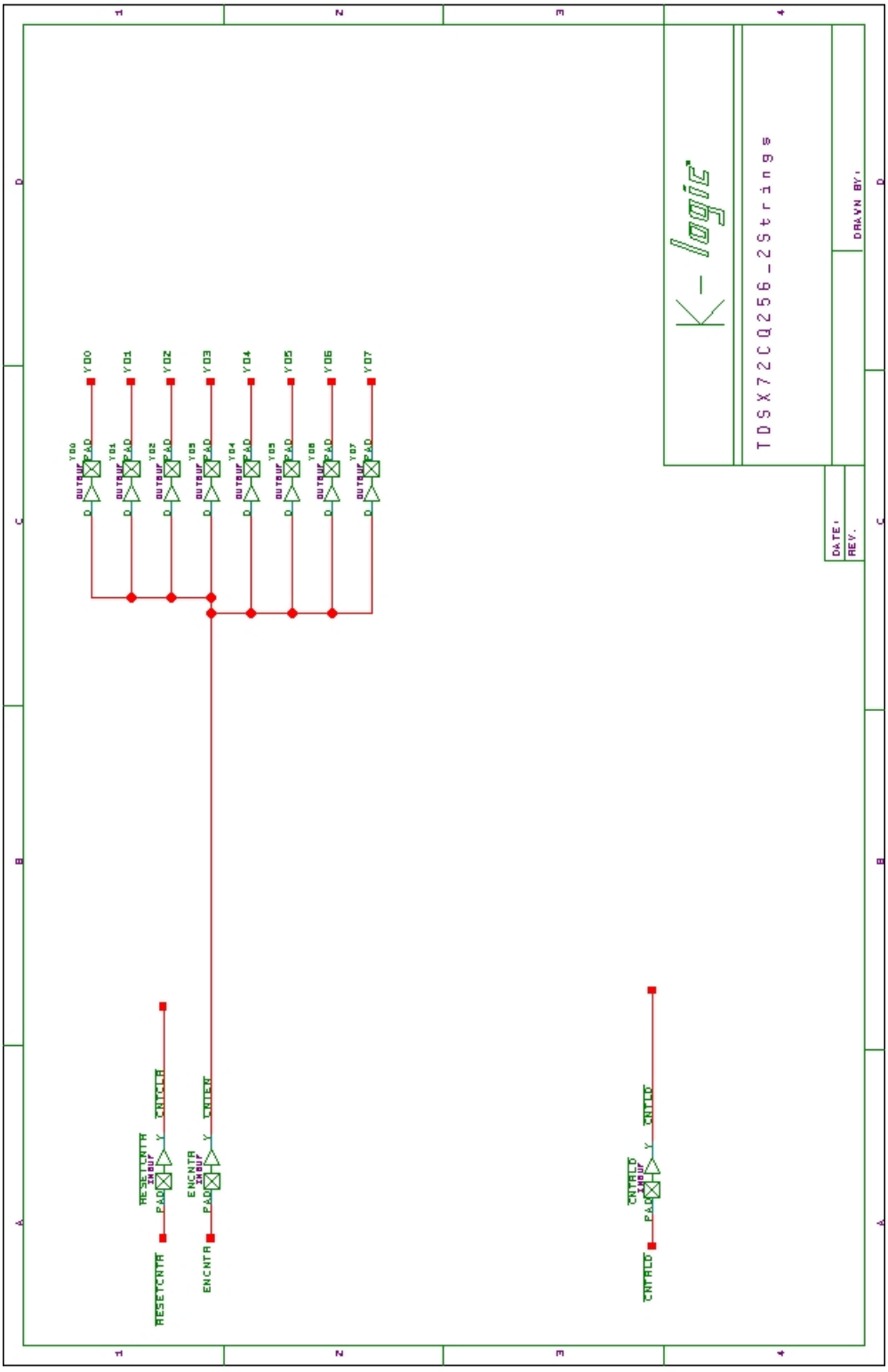
Appendix A DUT Design Schematics

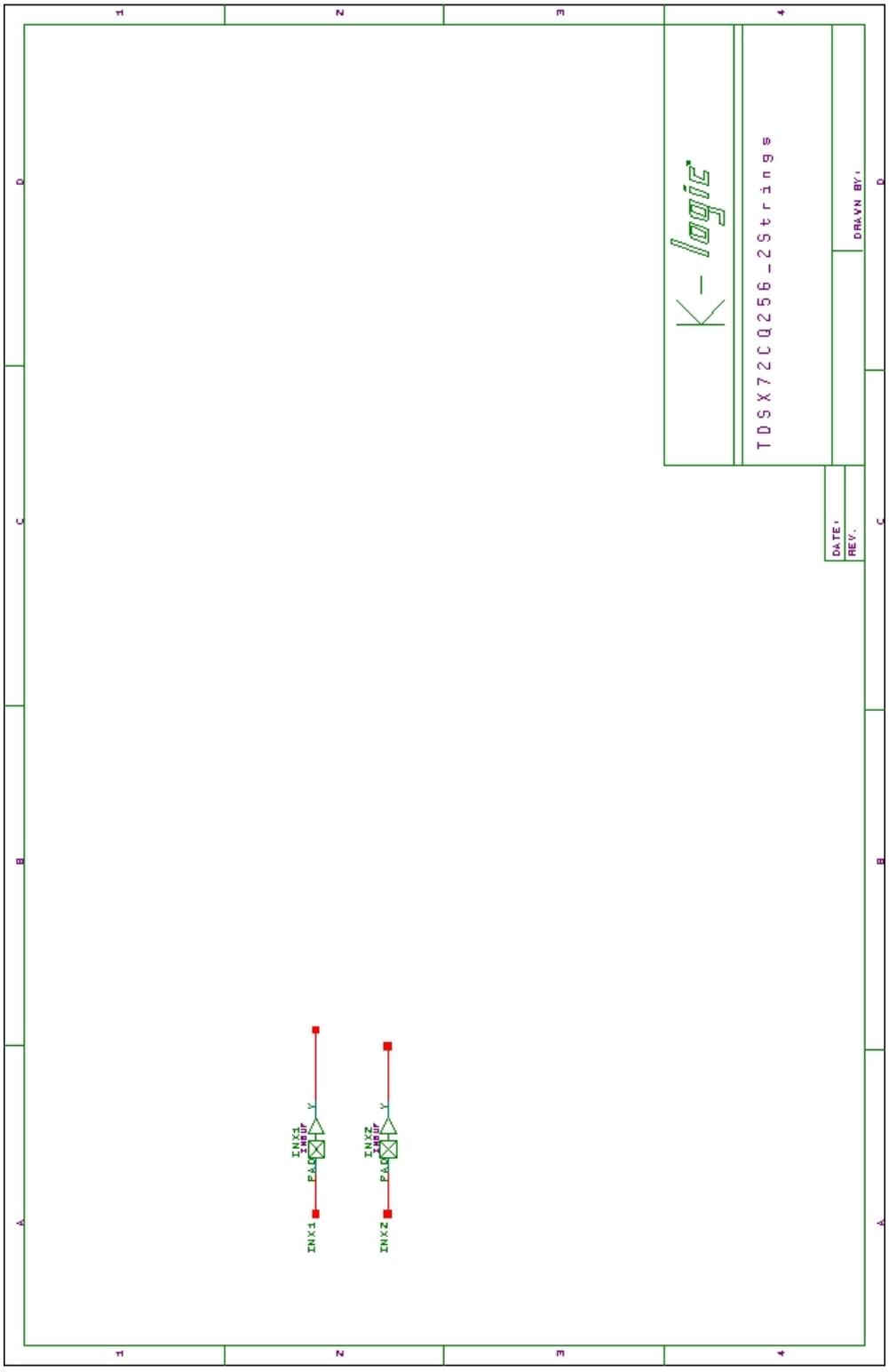


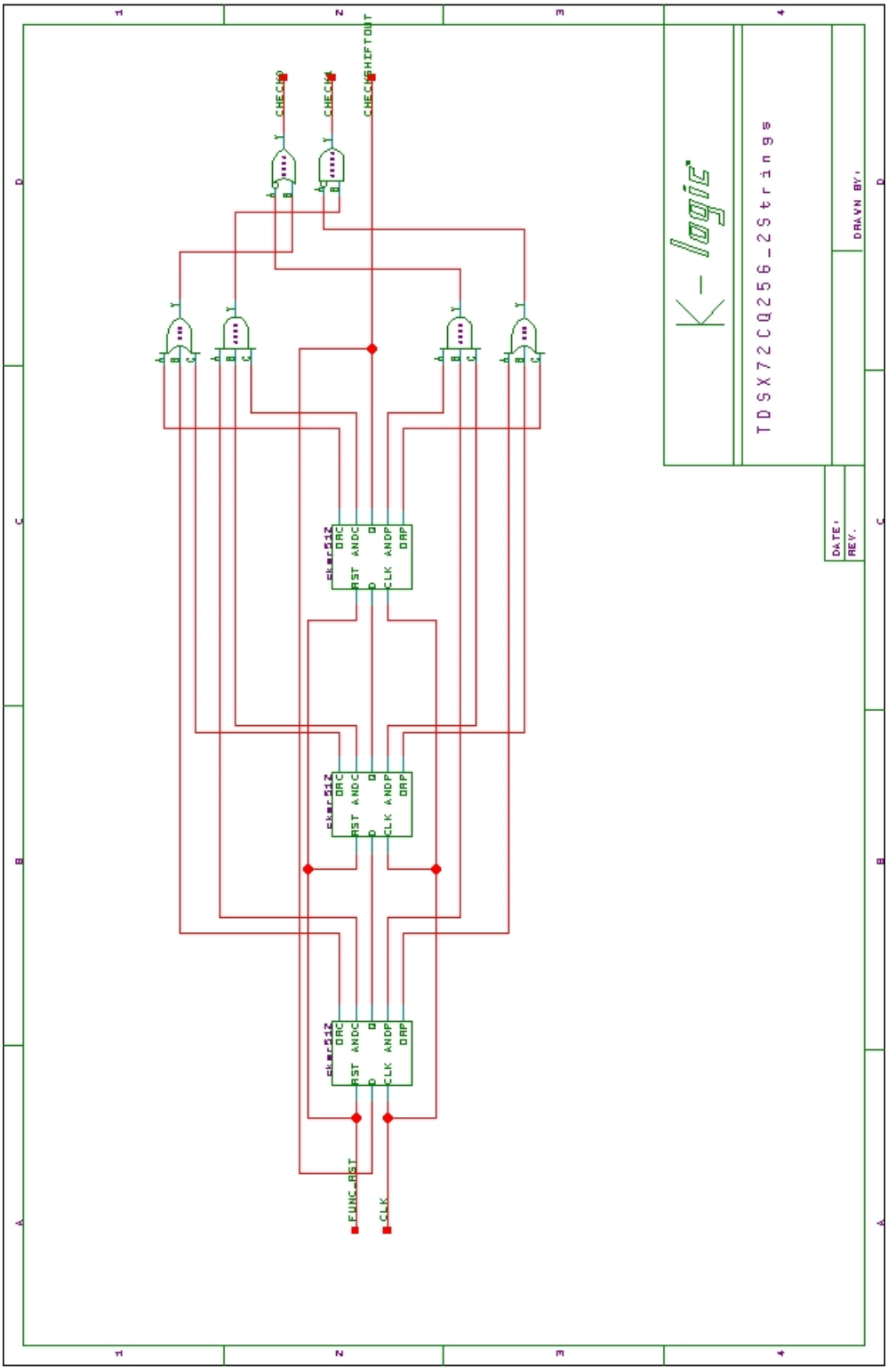

K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
CLOCK
CLKBUF
LOADIN
CLKINT
2Strang
CLK
D0
D1
RESET
FUNC_RST
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

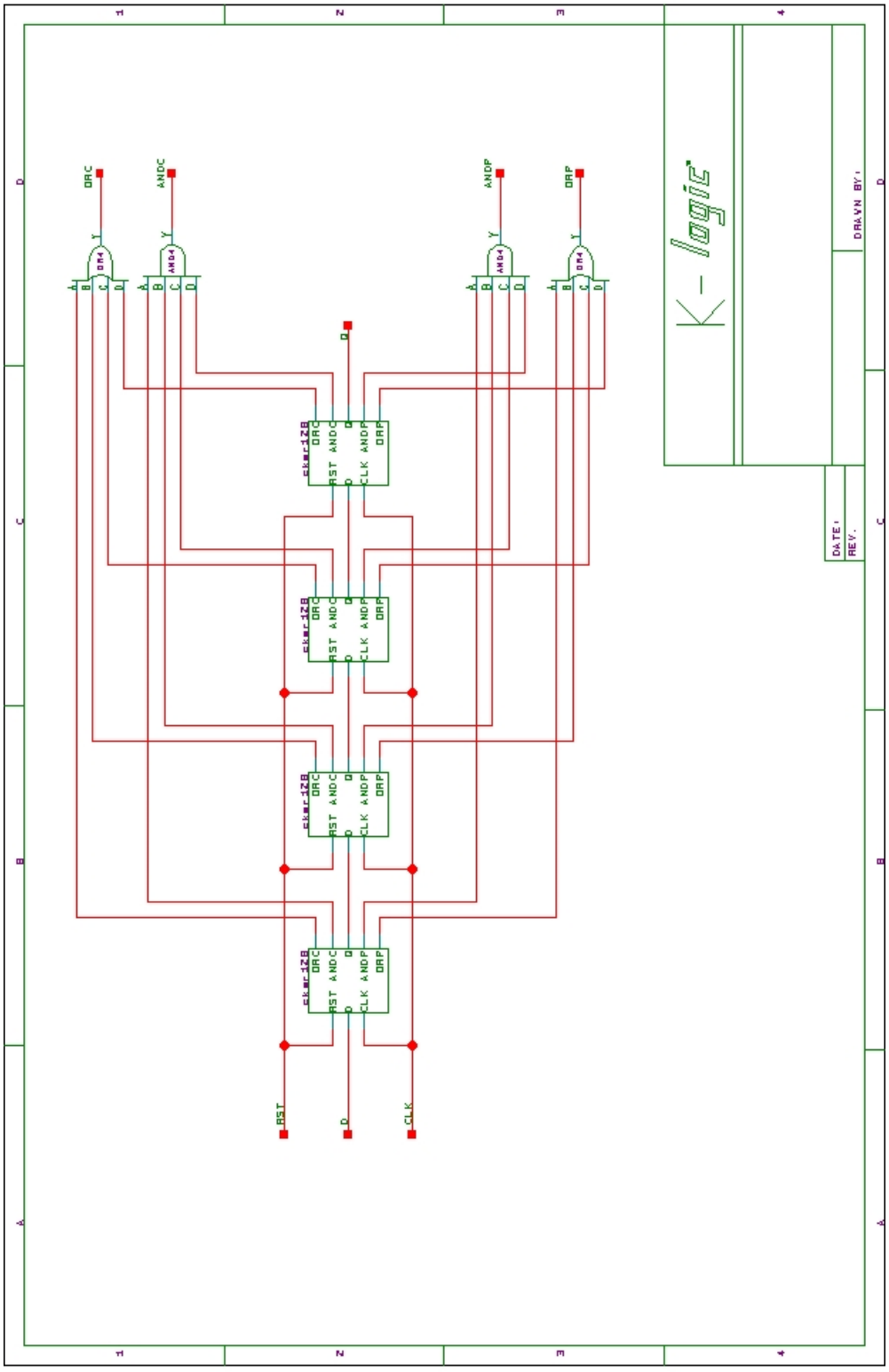

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-logic
CLK
RESET

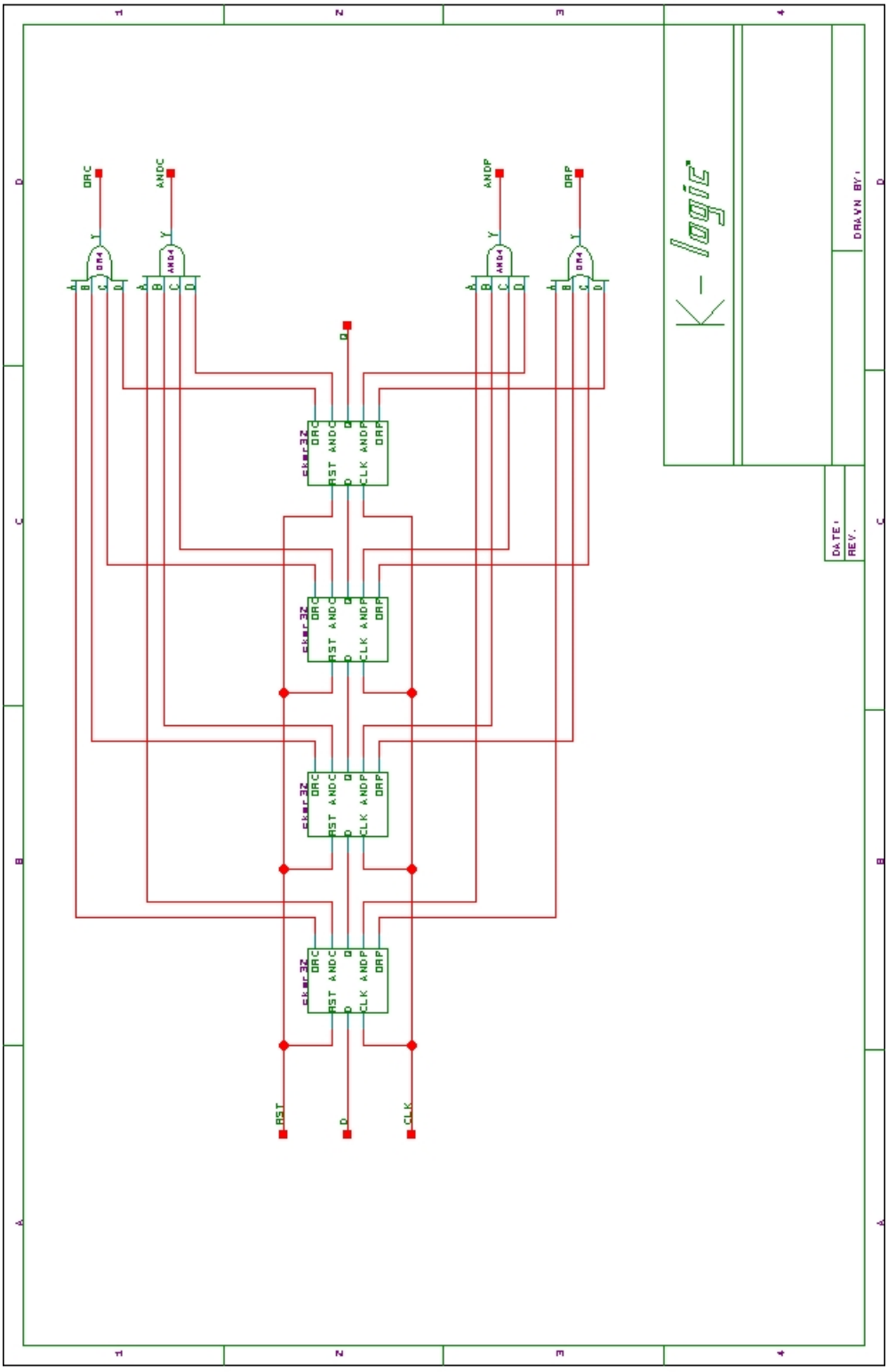

TDACT35XCQ\BUF50NINV
K-logic
DRAWN BY: ABK
DATE:
REV.
YPRESERVE A
Y

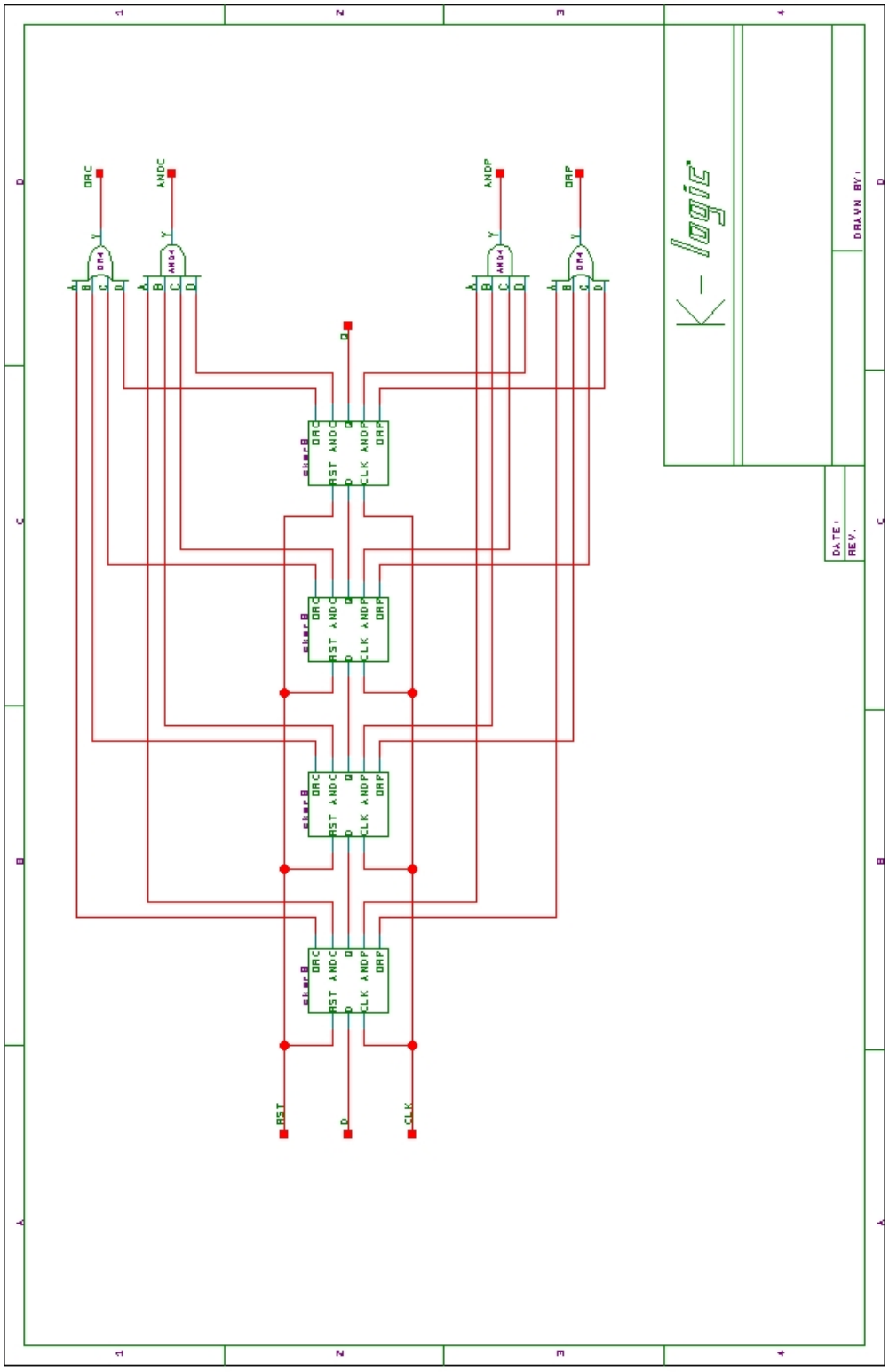

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
RESETCNTR
ENCNTR
CNTRLD

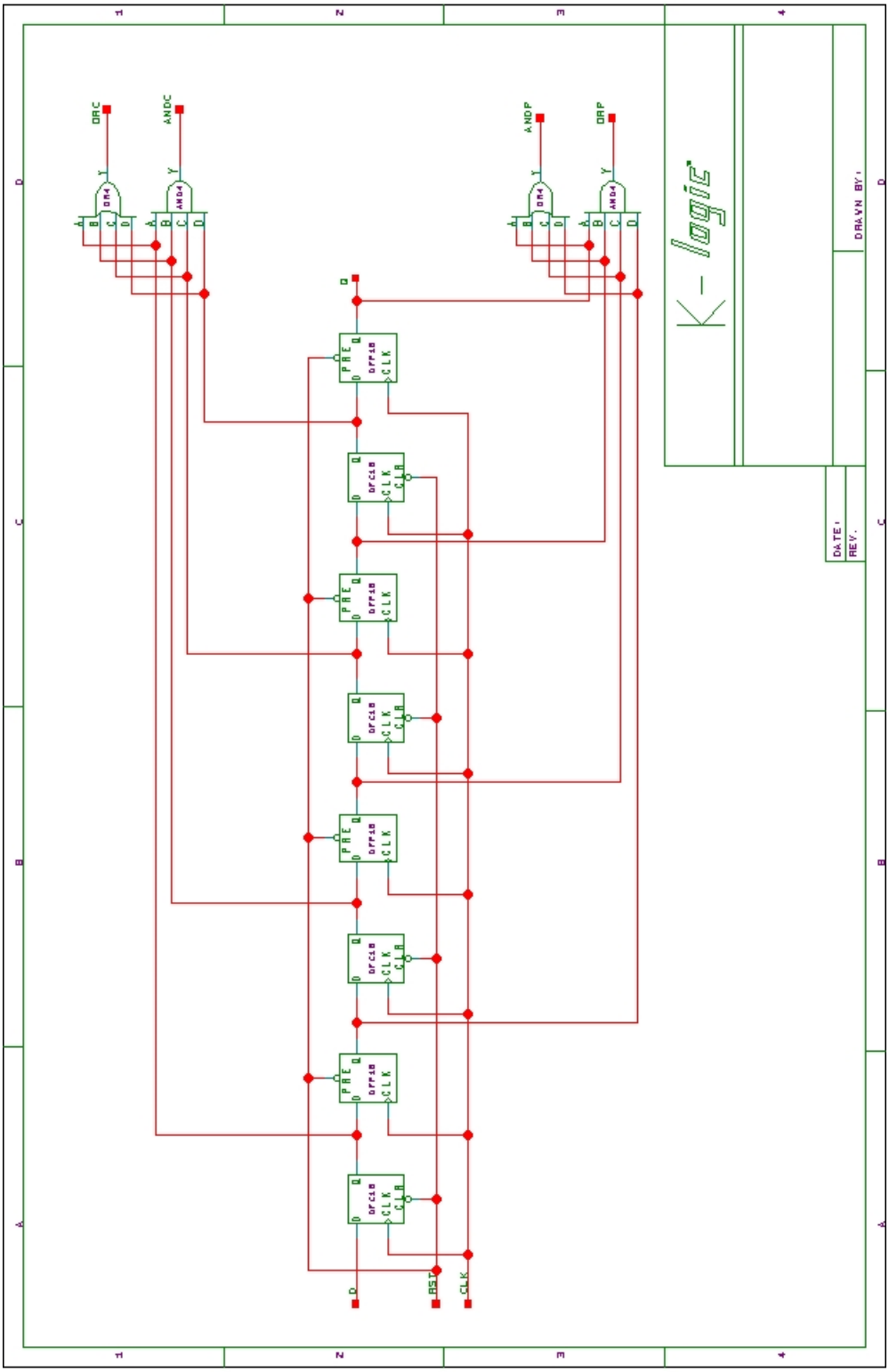

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

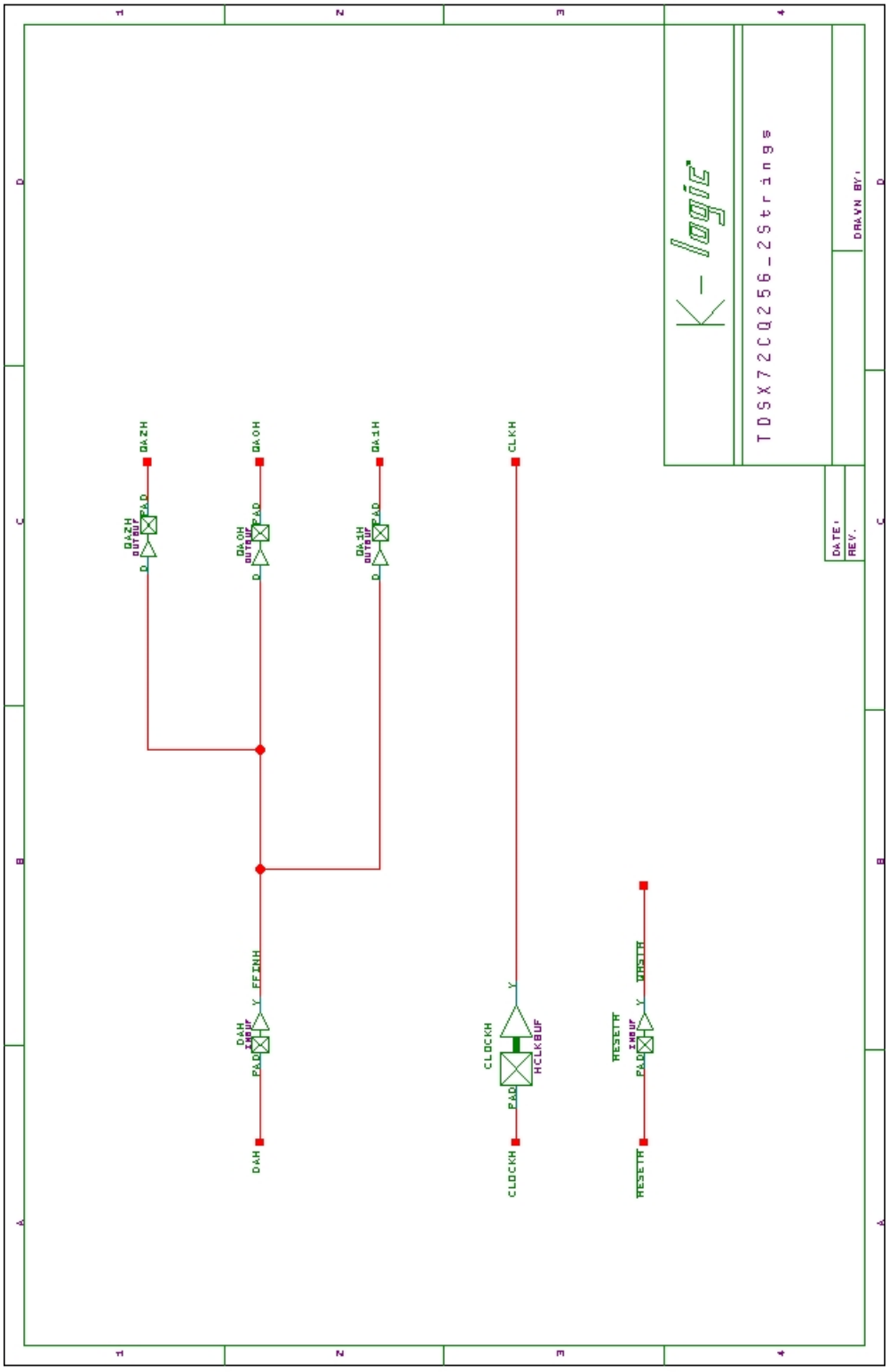

CHECK0
CHECK1
CHECKSHIFTOUT
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
FUNC_RST
CLK

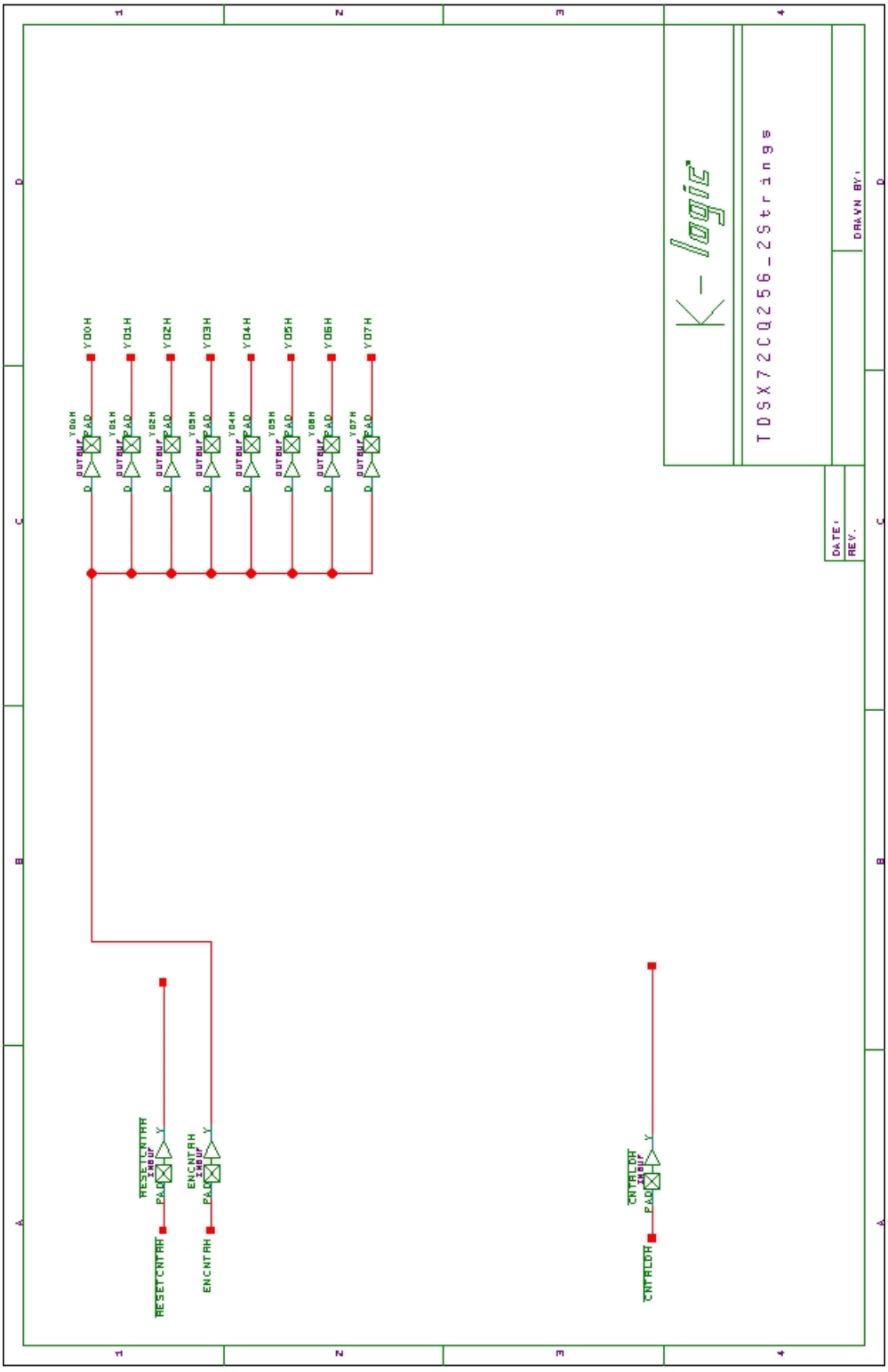

DRC
ANDC
ANDP
DRP
D
RST
CLK
DRAWN BY:
DATE:
REV:

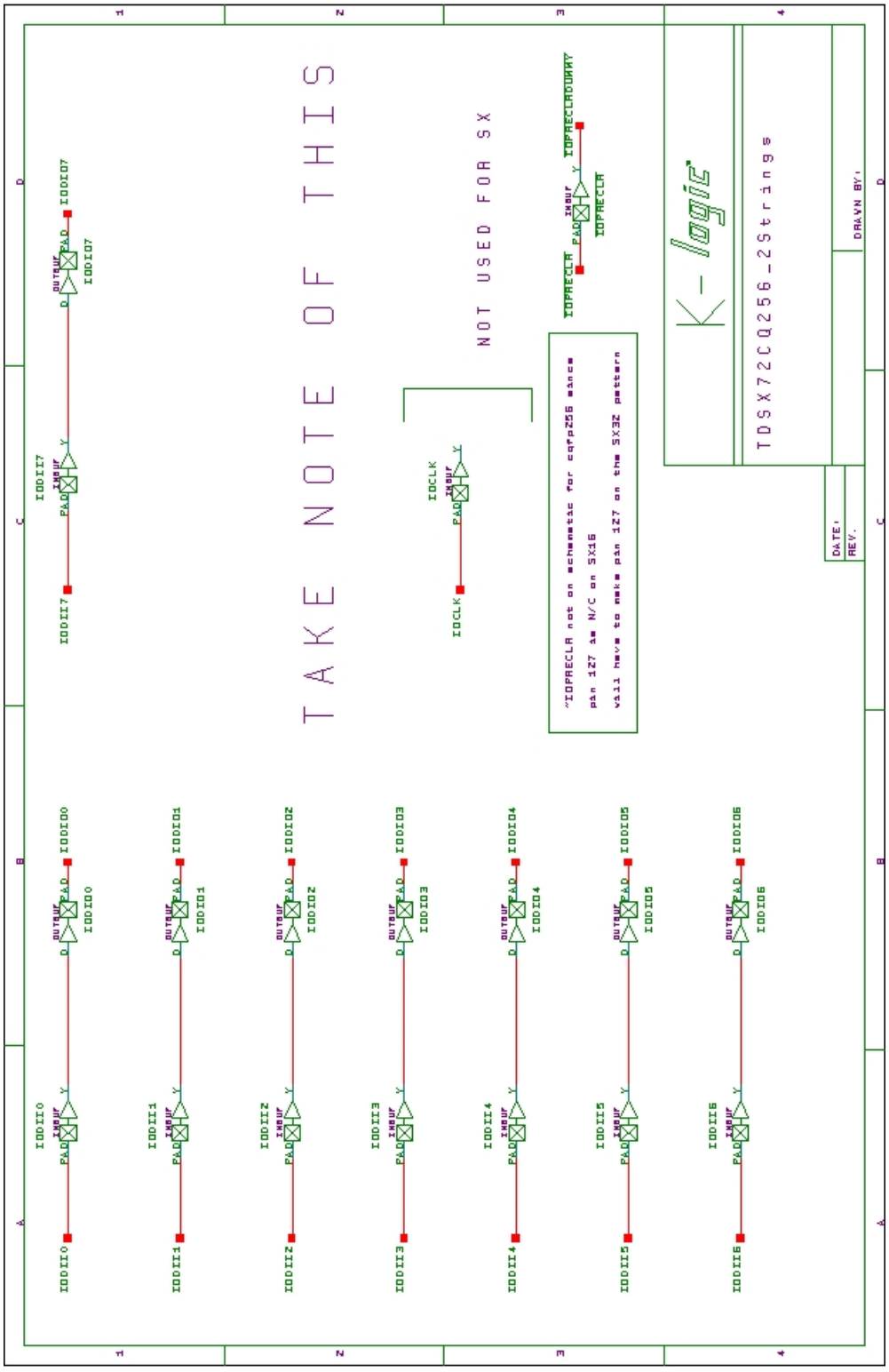

DRC
ANDC
ANDP
DRP
AND4
RST
D
CLK
DRAWN BY:
DATE:
REV.

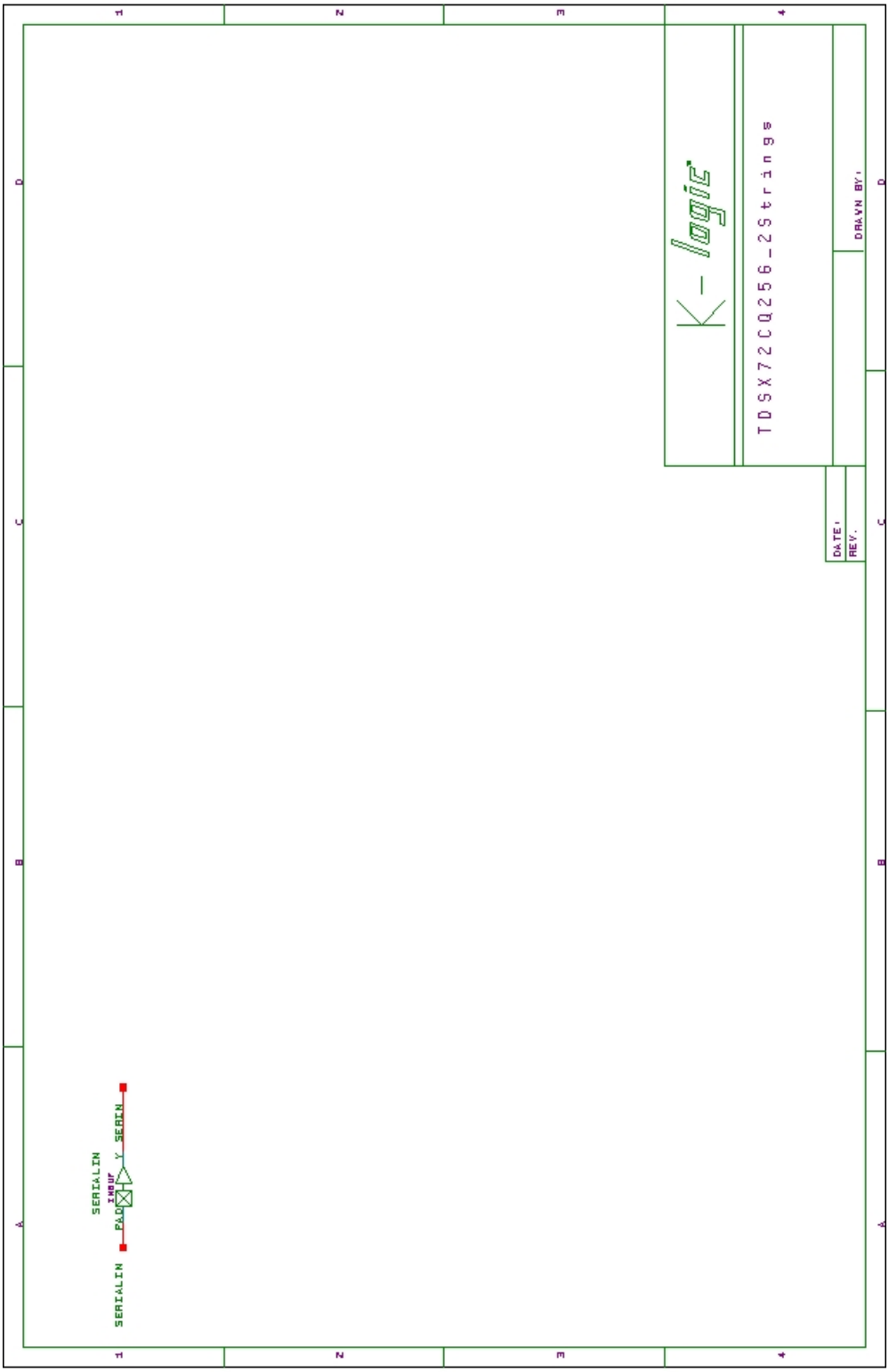

DRC
ANDC
ANDP
DRP
AND4
FSMRB
RST
CLK
D
DRAWN BY:
DATE:
REV.

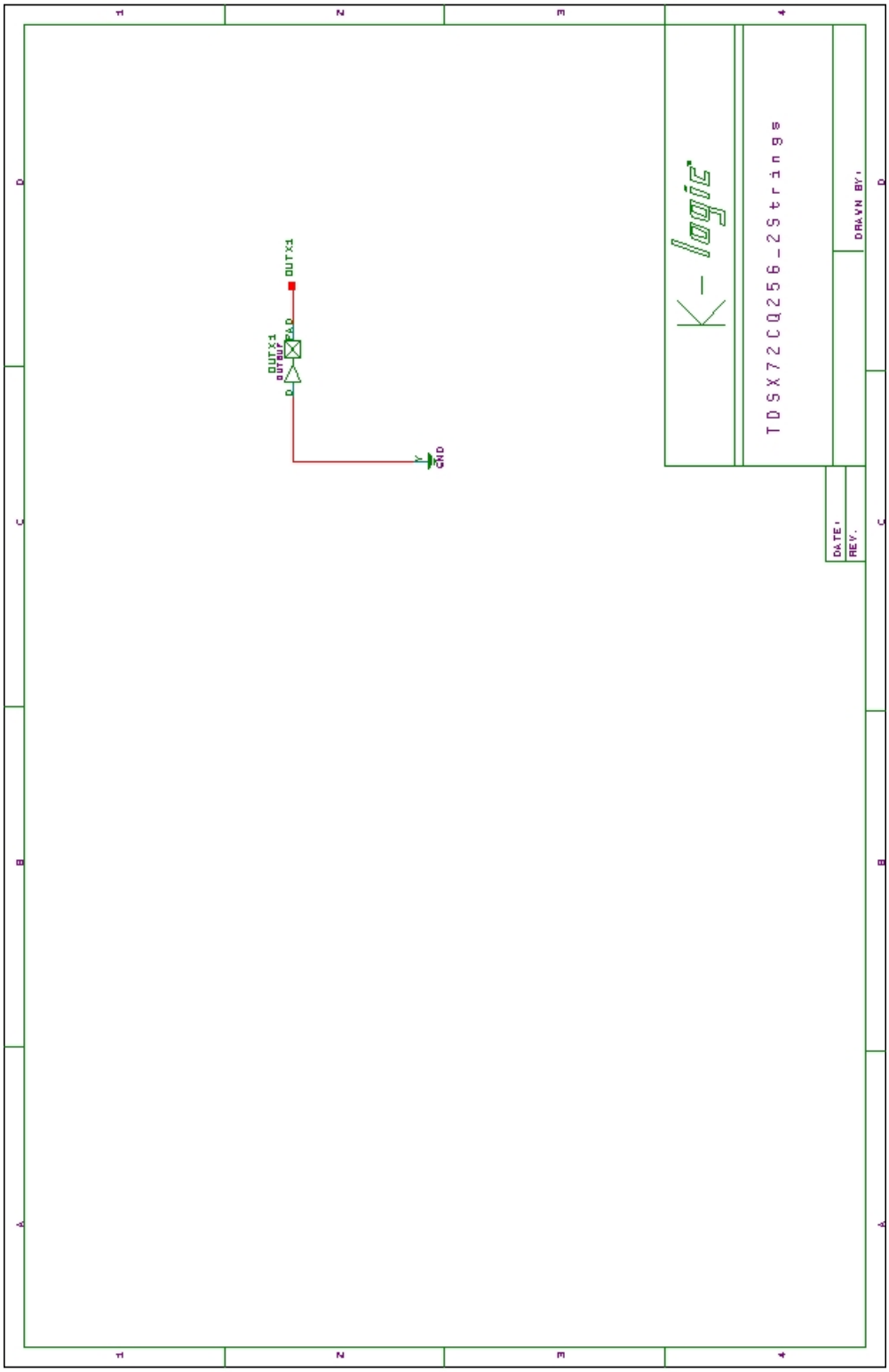

ORC
ANDC
ANDF
ORF
OR4
AND4
PRE
CLR
CLK
RST
CLK
K - logic
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF PAD
DA0H OUTBUF PAD
DA1H OUTBUF PAD
DAH IMBUF PAD Y CFINH
CLOCKH PAD HCLKBUF Y
RESETH IMBUF PAD Y RRSTH
DAH
CLOCKH
RESETH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOPRECLR
IOPRECLRQUANY
IOCLK
IOOII7
IOOII0
IOOII1
IOOII2
IOOII3
IOOII4
IOOII5
IOOII6
IOOIO7
IOOIO0
IOOIO1
IOOIO2
IOOIO3
IOOIO4
IOOIO5
IOOIO6


TDSX72CQ256_2Strings
K - logic
DRAWN BY:
DATE:
REV.
SERIALIN
PAD
IMUX
SERIALIN


OUTx1
OUTBUF
PAD
GND
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.

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