Microsemi

Total Ionizing Dose Test Report

No. 11T-RTAX4000S-LG1272-D41891

October 27, 2011

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I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 10 days. Every DUT passes the major specifications listed in the table for 300 krad(SiO2) of irradiation, except for ICCI, which passes 150 krad(SiO2) and is expected to pass 200 krad(SiO2) after an additional 20 days of anneal.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 150 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation and annealing, each input or output is tied to either the ground or VCCI with a jumper.

Table 2 DUT and Irradiation Parameters

Part Number	**RTAX4000S**
Package	LGA-1272
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	D41891
Quantity Tested	5
Serial Number	300 krad: 8196, 8231 200 krad: 8198, 8236, 8237
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

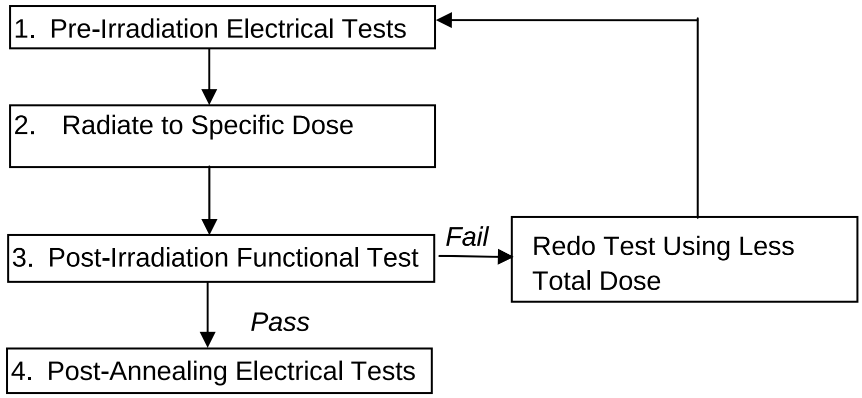

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 10 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (Master_RTAX4000S_Design) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-S/SL Devices

SUPPLY VOLTAGE	MINIMUM	RECOMMENDED	MAXIMUM
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-6 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC should be defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the RTAXS specifications document posted on the Actel website; the link is

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 500 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
8196	300 krad	22	34	26	16	384	218
8198	200 krad	27	32	27	16	90	59
8231	300 krad	36	66	29	17	401	283
8236	200 krad	31	36	30	16	81	73
8237	200 krad	22	27	20	16	101	92

Based on these PIPL, the post-annealed DUT is expected to pass both the ICCA and ICCI specification for 200 krad(SiO_2) after additional 20 days of annealing.

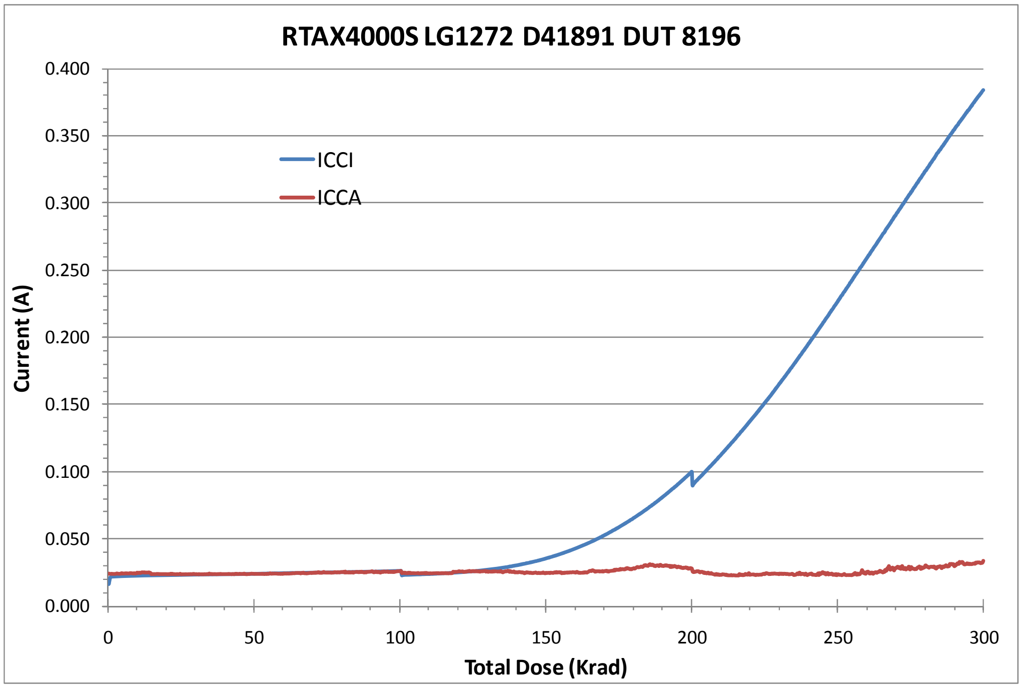

Figure 2 DUT 8196 Influx ICCI and ICCA

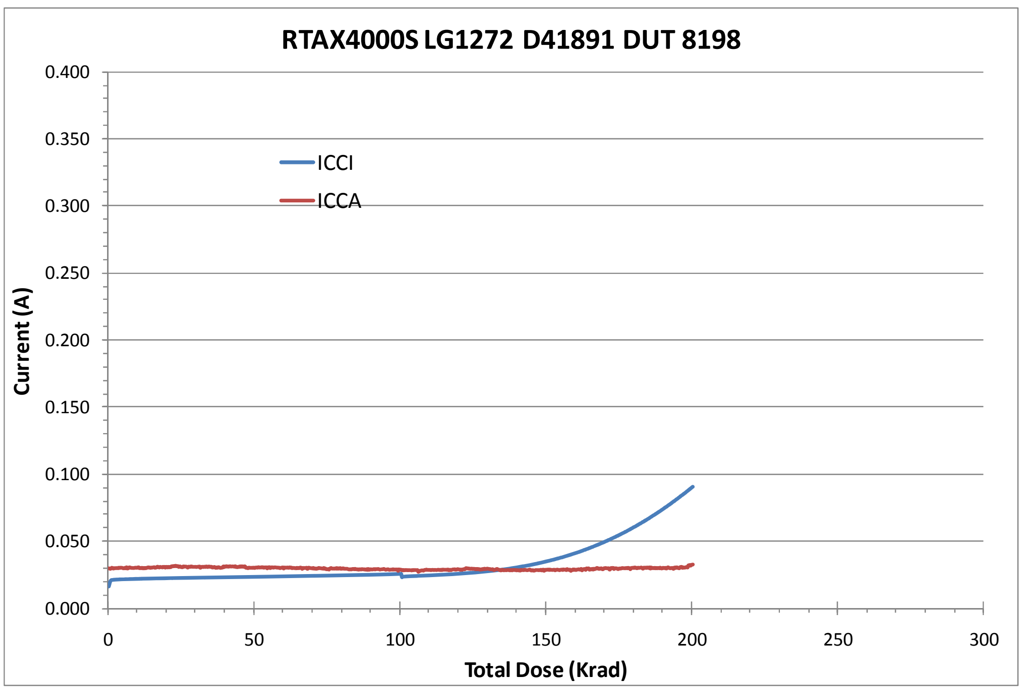

Figure 3 DUT 8198 Influx ICCI and ICCA

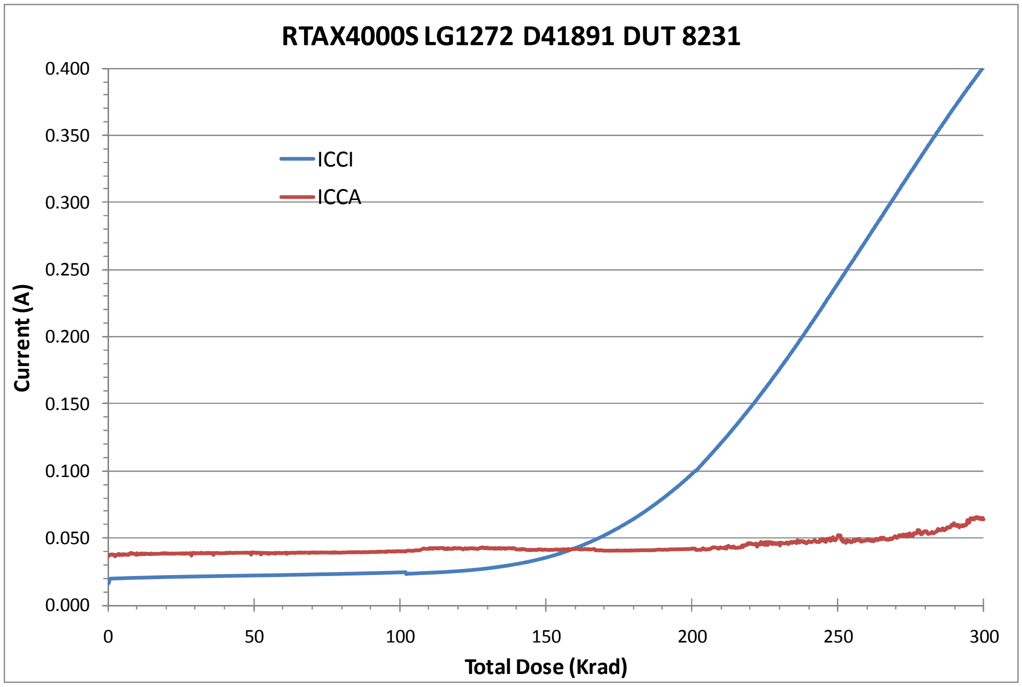

Figure 4 DUT 8231 Influx ICCI and ICCA

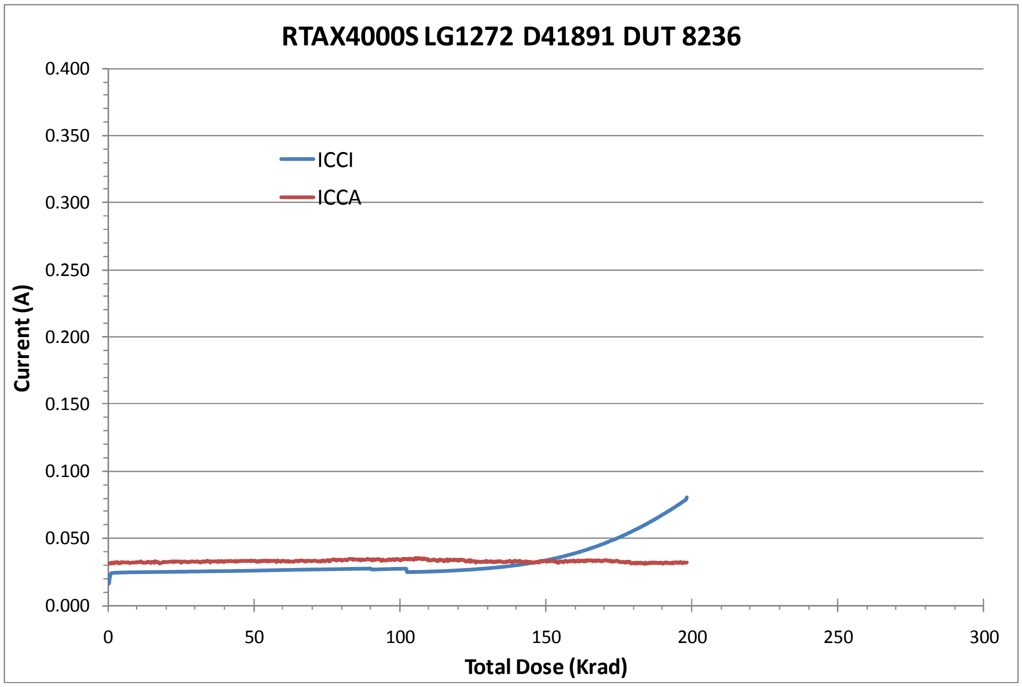

Figure 5 DUT 8236 influx ICCI and ICCA

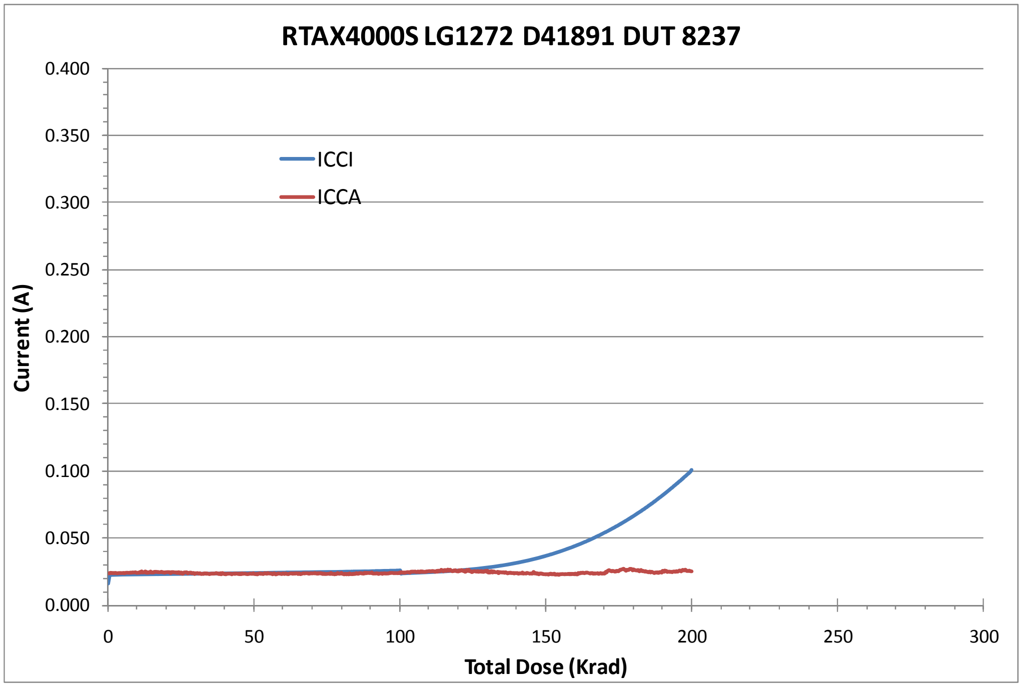

Figure 6 DUT 8237 Influx ICCI and ICCA

C. Single-Ended 3.3 V-LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design often just input and output buffers starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

The pre-irradiation and post-annealing single-ended VIL and VIH are tested and recorded as pass or fail. In each case, the pre-irradiation and post-annealing both passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	8196 (300 krad)		8198 (200 krad)		8231 (300 krad)		8236 (200 krad)		8237 (200 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	197.0	163.1	191.2	163.3	178.7	163.3	188.1	164.3	192.5	166.9
Array_out_EAQ_1	184.6	174.3	178.8	172.5	180.5	172.2	186.6	172.5	179.9	173.4
Array_out_EAQ_2	183.8	177.3	193.3	177.8	195.6	176.0	176.7	200.6	188.8	191.5
Global_Monitor_EAQ	191.7	161.0	177.5	160.7	184.9	163.0	179.6	160.7	196.9	164.4
Shiftout3	189.1	176.5	227.1	189.0	188.6	189.0	210.8	181.7	192.5	178.3
Shiftout7	201.3	189.8	196.5	186.8	206.3	190.0	193.6	190.9	202.7	186.6
Shiftout8	202.0	229.0	211.3	192.5	199.7	193.6	216.9	197.4	205.5	205.0
RAM_Monitor_EAQ	225.1	193.9	221.5	194.4	233.6	191.8	223.0	194.4	235.4	196.4
RAM_out_EAQ_0	197.0	163.1	191.2	166.9	178.7	163.3	188.1	164.3	192.5	166.9
RAM_out_EAQ_4	140.2	134.0	139.5	136.4	139.1	133.1	140.3	136.4	140.4	135.1
RAM_out_EAQ_8	220.7	205.8	218.0	205.6	218.0	203.7	218.3	205.6	217.1	207.0

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	8196 (300 krad)		8198 (200 krad)		8231 (300 krad)		8236 (200 krad)		8237 (200 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.77	2.77	2.77	2.77	2.77	2.77	2.77	2.77	2.77	2.77
Array_out_EAQ_1	2.73	2.73	2.74	2.73	2.74	2.73	2.73	2.73	2.74	2.73
Array_out_EAQ_2	2.73	2.73	2.73	2.73	2.72	2.73	2.74	2.71	2.73	2.71
Global_Monitor_EAQ	2.72	2.74	2.74	2.73	2.73	2.74	2.73	2.74	2.70	2.74
Shiftout3	2.72	2.72	2.70	2.73	2.73	2.71	2.70	2.72	2.72	2.72
Shiftout7	2.71	2.71	2.72	2.72	2.71	2.71	2.72	2.71	2.71	2.72
Shiftout8	2.71	2.67	2.70	2.71	2.71	2.71	2.69	2.70	2.71	2.70
RAM_Monitor_EAQ	2.69	2.71	2.69	2.71	2.68	2.71	2.69	2.71	2.68	2.71
RAM_out_EAQ_0	2.71	2.74	2.72	2.74	2.73	2.74	2.72	2.74	2.72	2.74
RAM_out_EAQ_4	2.78	2.77	2.78	2.78	2.78	2.78	2.78	2.77	2.78	2.77
RAM_out_EAQ_8	2.69	2.70	2.70	2.70	2.70	2.70	2.69	2.70	2.69	2.70

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (ns)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
8196	300 krad	1.089	1.080	1.083	1.098	1.138
8198	200 krad	1.084	1.073	1.085		1.095
8231	300 krad	1.042	1.032	1.045	1.061	1.069
8236	200 krad	1.102	1.077	1.081		1.066
8237	200 krad	1.103	1.104	1.100		1.107

Radiation Δ (%)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
8196	300 krad	–	-0.8%	-0.6%	0.8%	4.5%
8198	200 krad	–	-1.0%	0.1%	–	1.0%
8231	300 krad	–	-1.0%	0.3%	1.8%	2.6%
8236	200 krad	–	-2.3%	-1.9%	–	-3.3%
8237	200 krad	–	0.1%	-0.3%	–	0.3%

F. Transition Time

Figure 7a to Figure 16b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

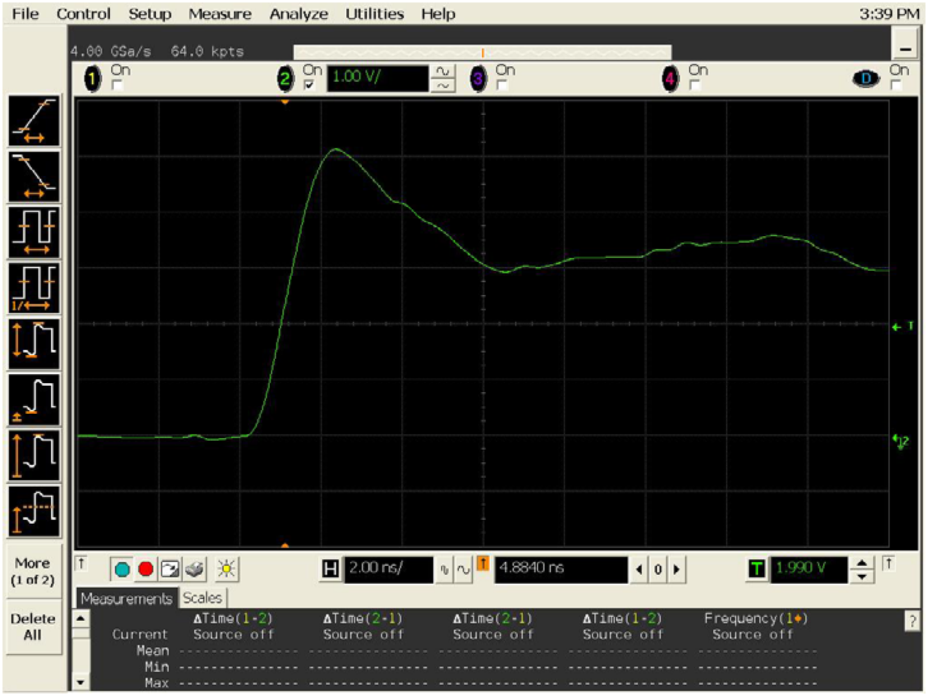

Figure 7a DUT 8196 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

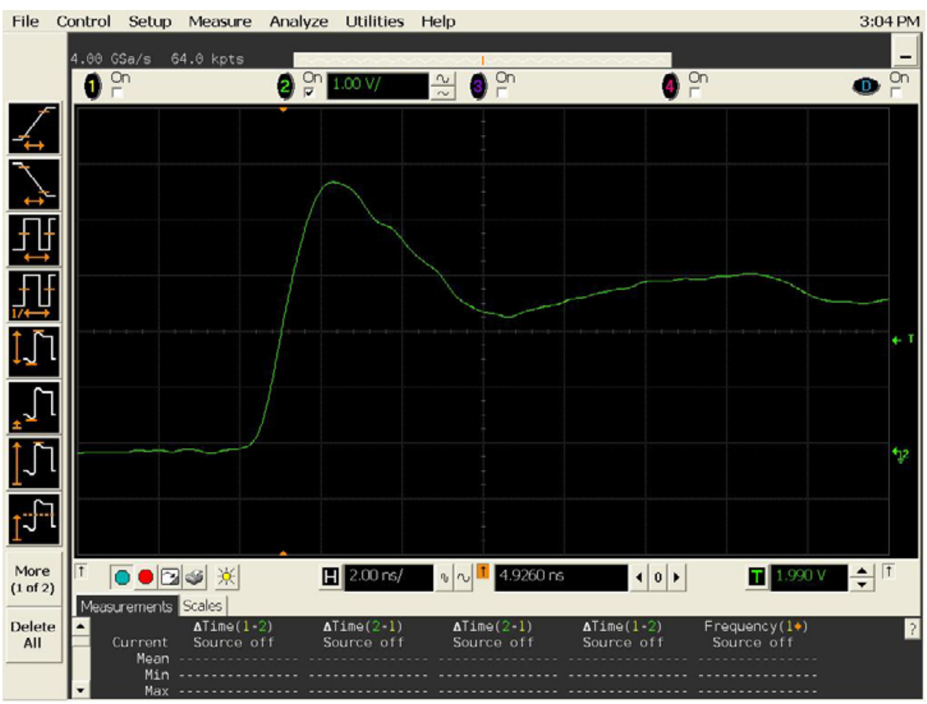

Figure 7b DUT 8196 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

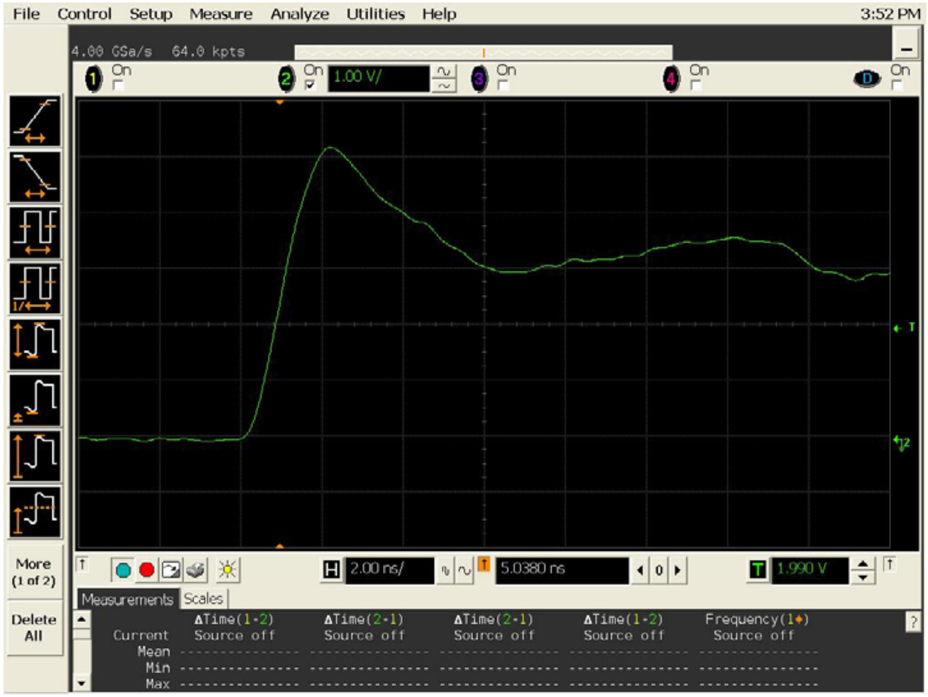

Figure 8a DUT 8198 Pre-irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

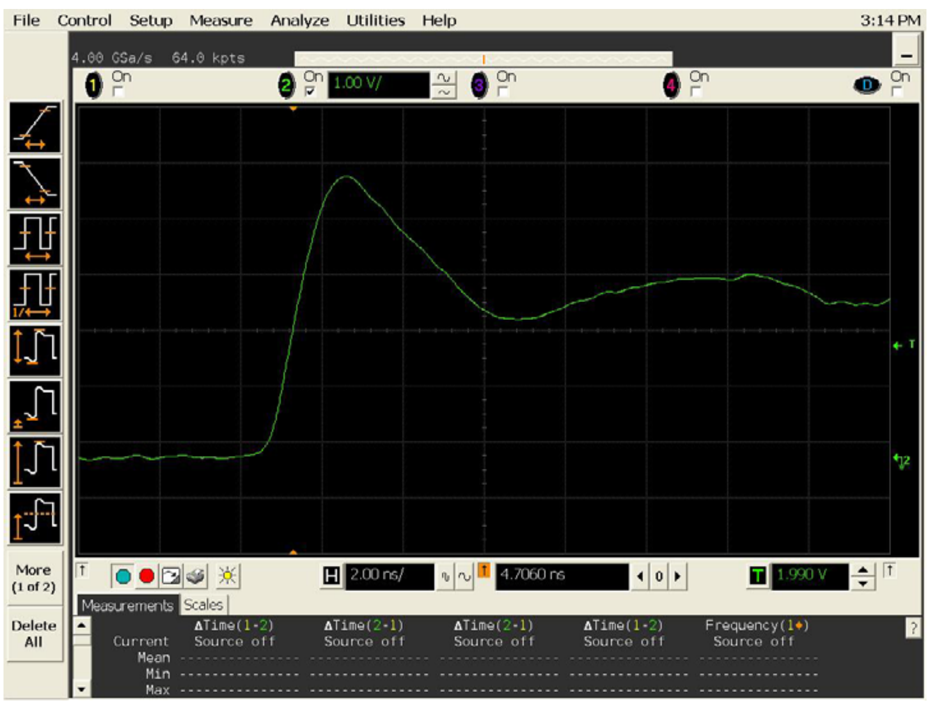

Figure 8b DUT 8198 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

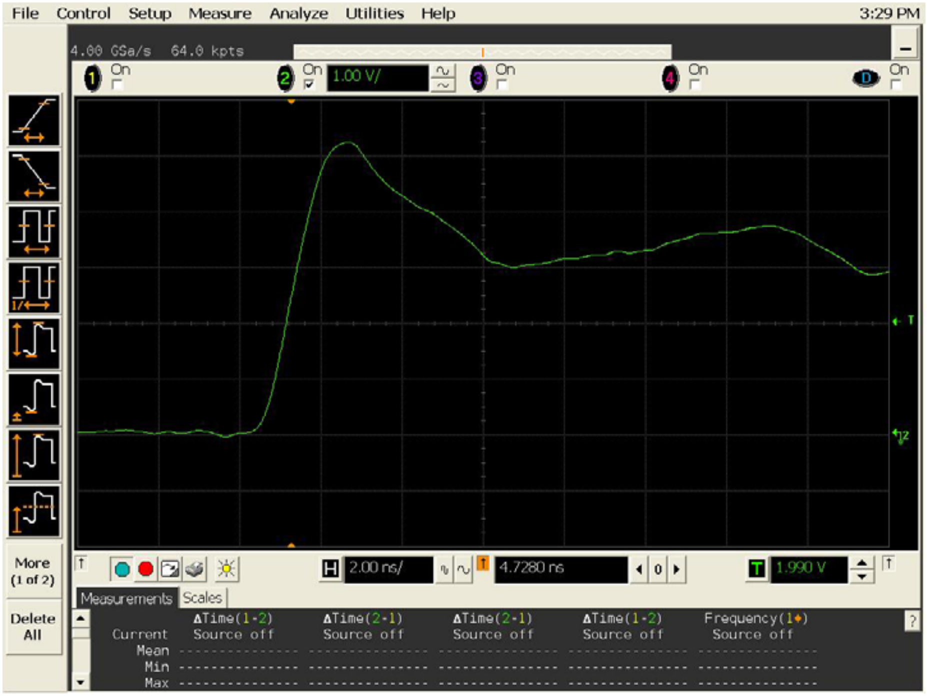

Figure 9a DUT 8231 Pre-Irradiation Rising Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

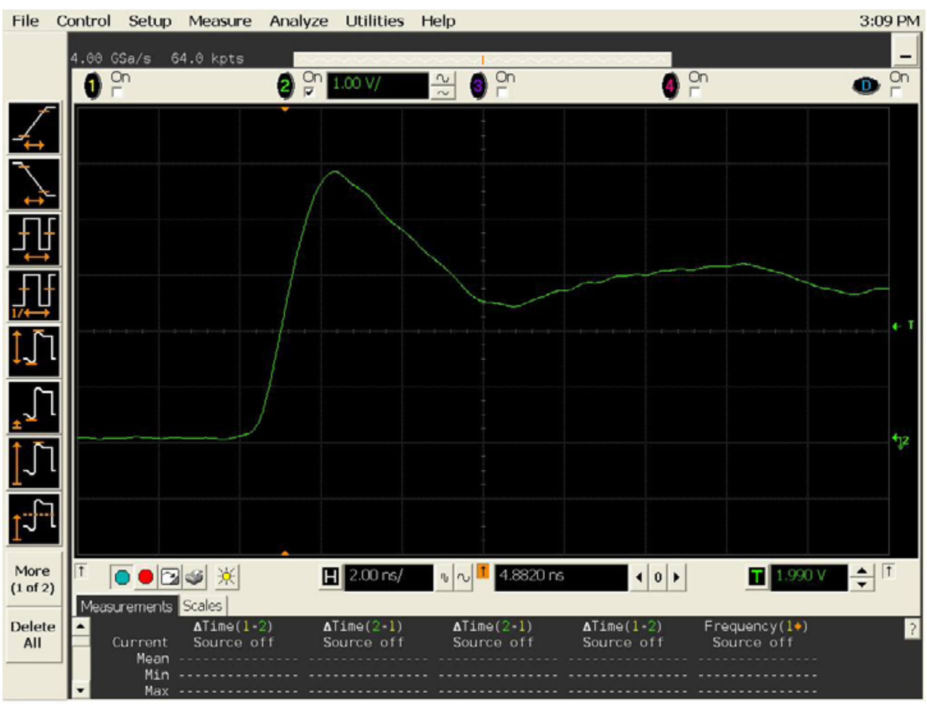

Figure 9b DUT 8231 Post-Annealing Rising Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

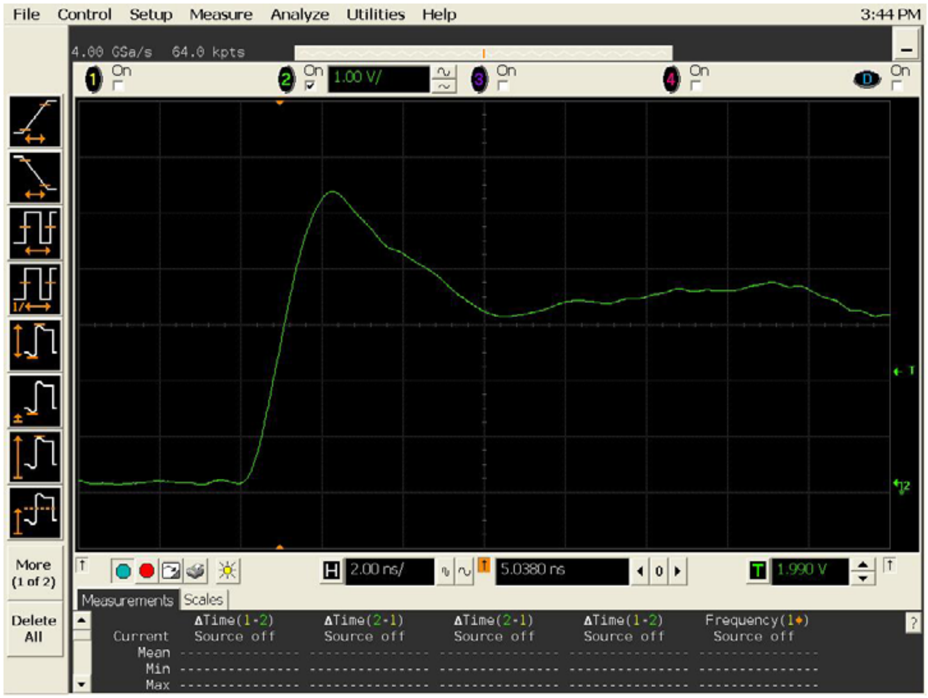

Figure 10a DUT 8236 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

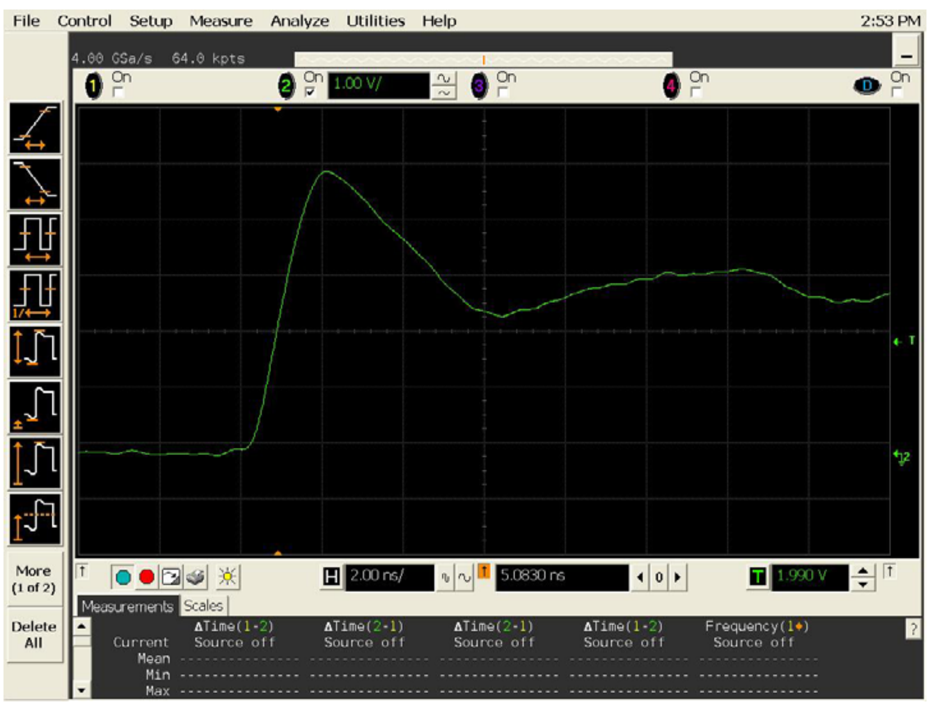

Figure 10b DUT 8236 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

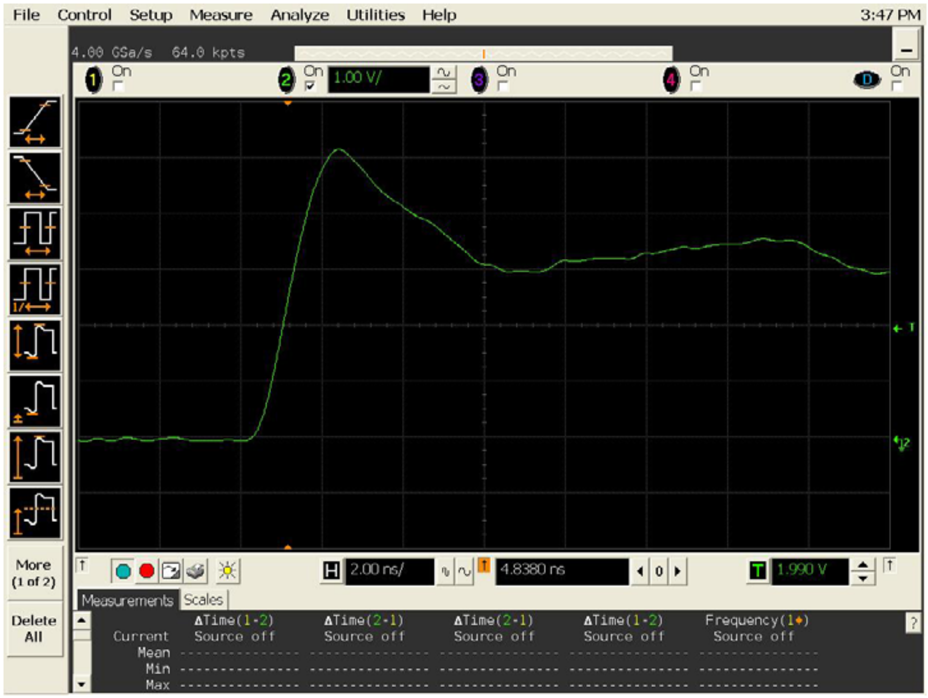

Figure 11a DUT 8237 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

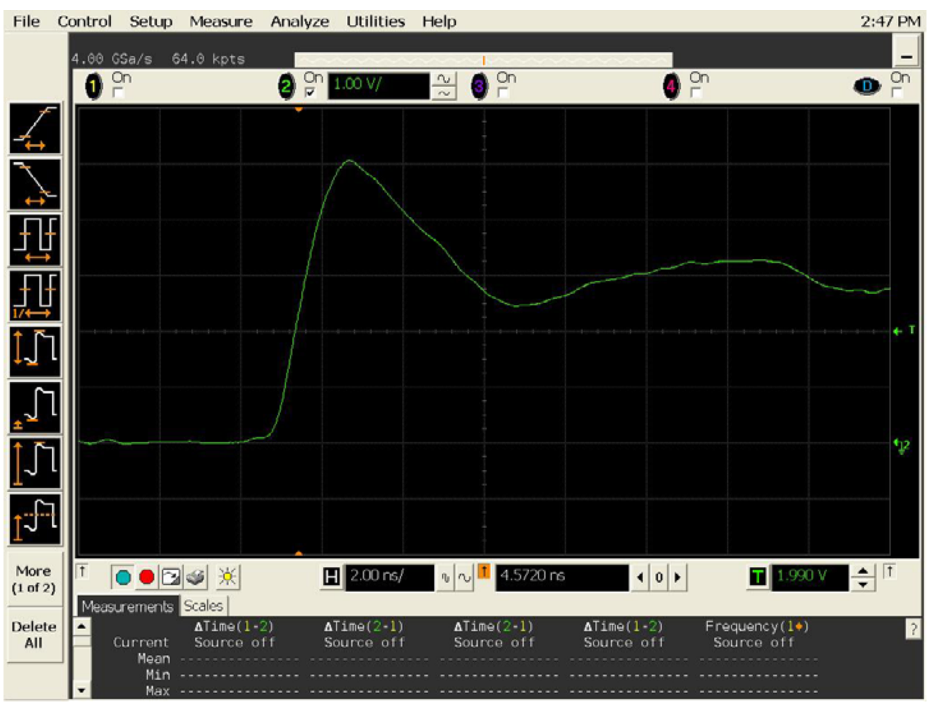

Figure 11b DUT 8237 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

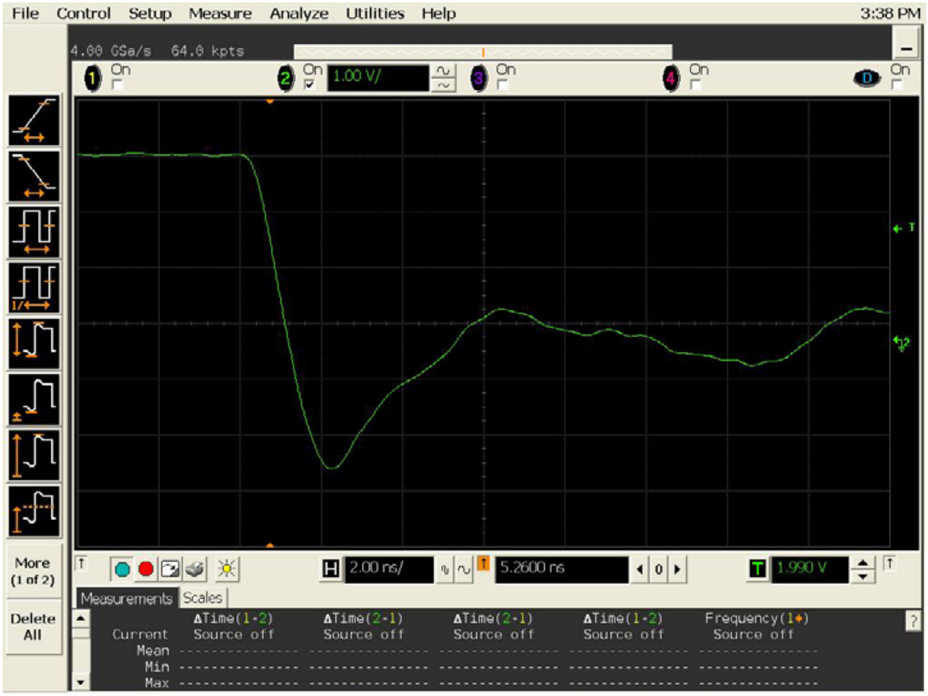

Figure 12a DUT 8196 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

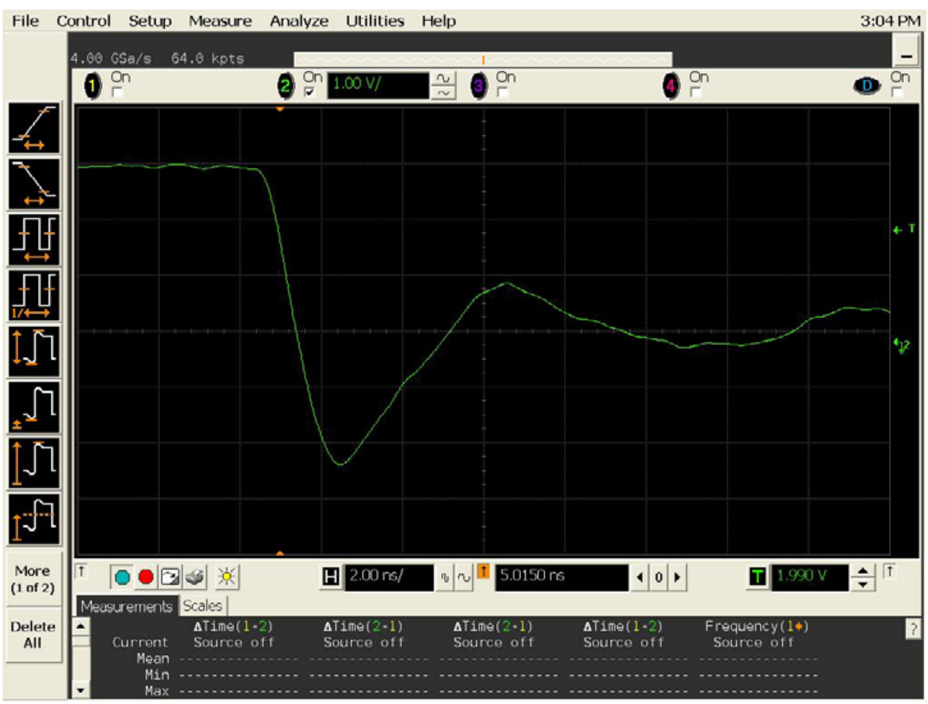

Figure 12b DUT 8196 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

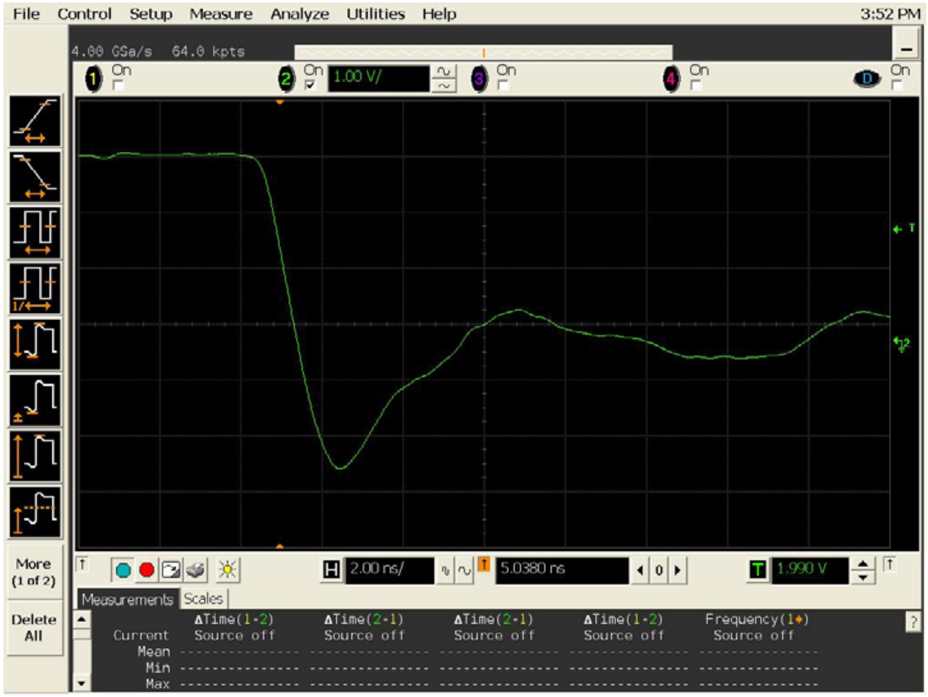

Figure 13a DUT 8198 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

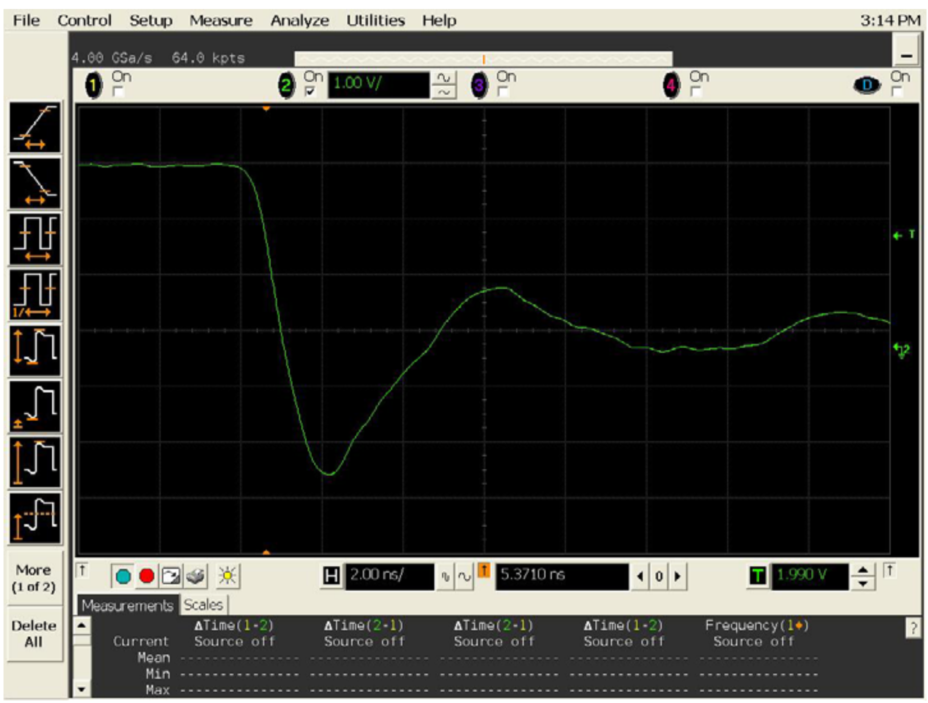

Figure 13b DUT 8198 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

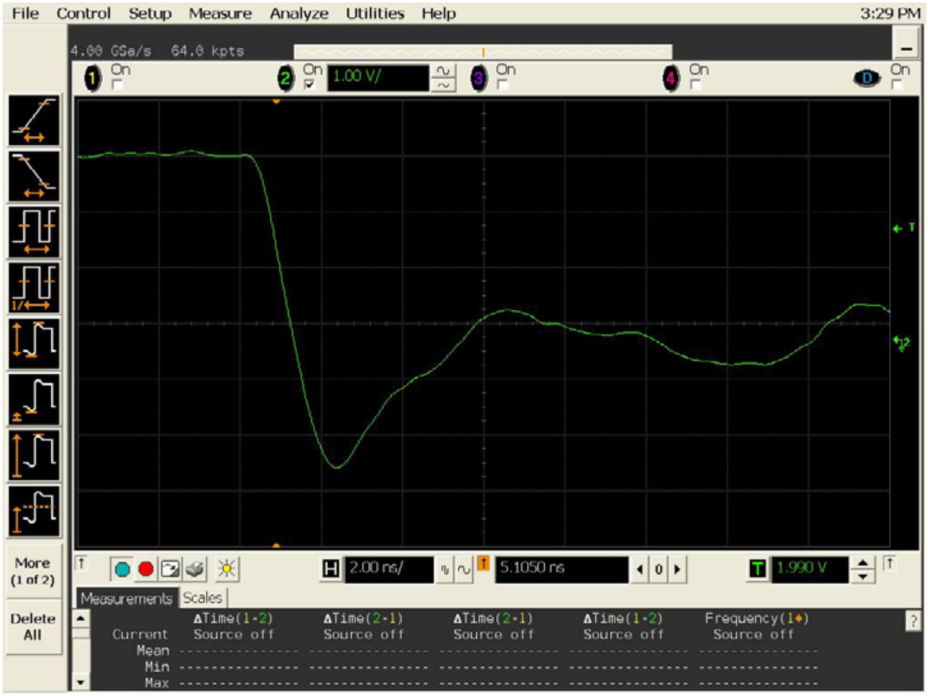

Figure 14a DUT 8231 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

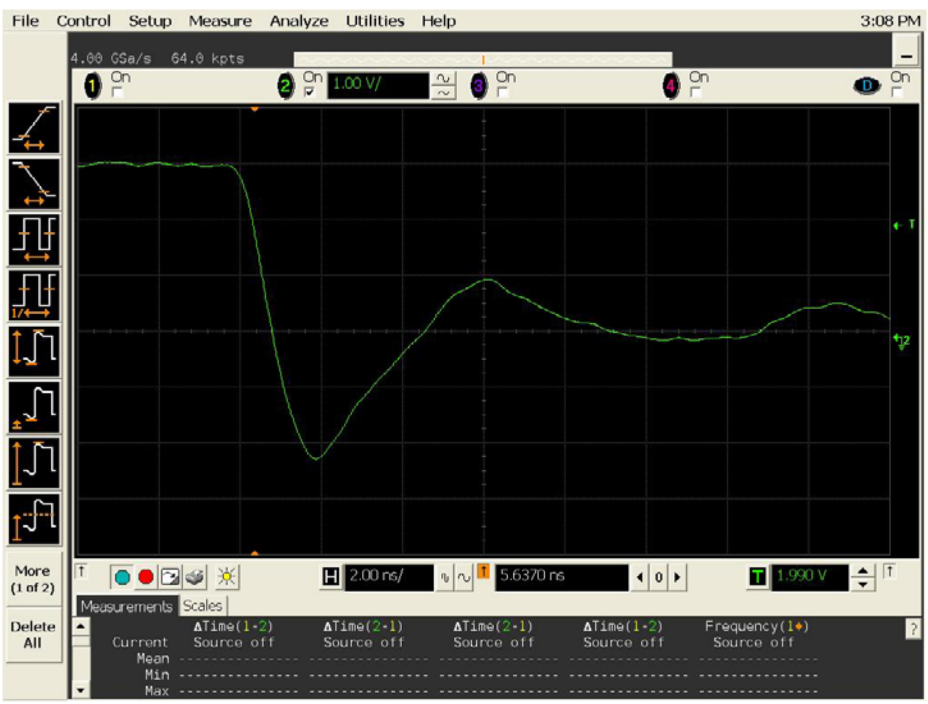

Figure 14b DUT 8231 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

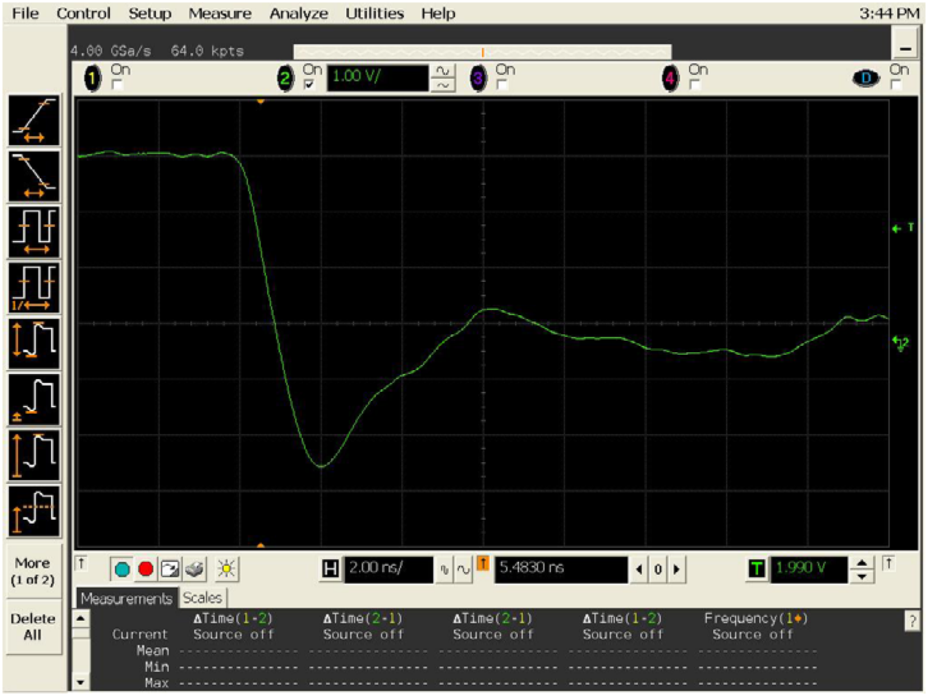

Figure 15a DUT 8236 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

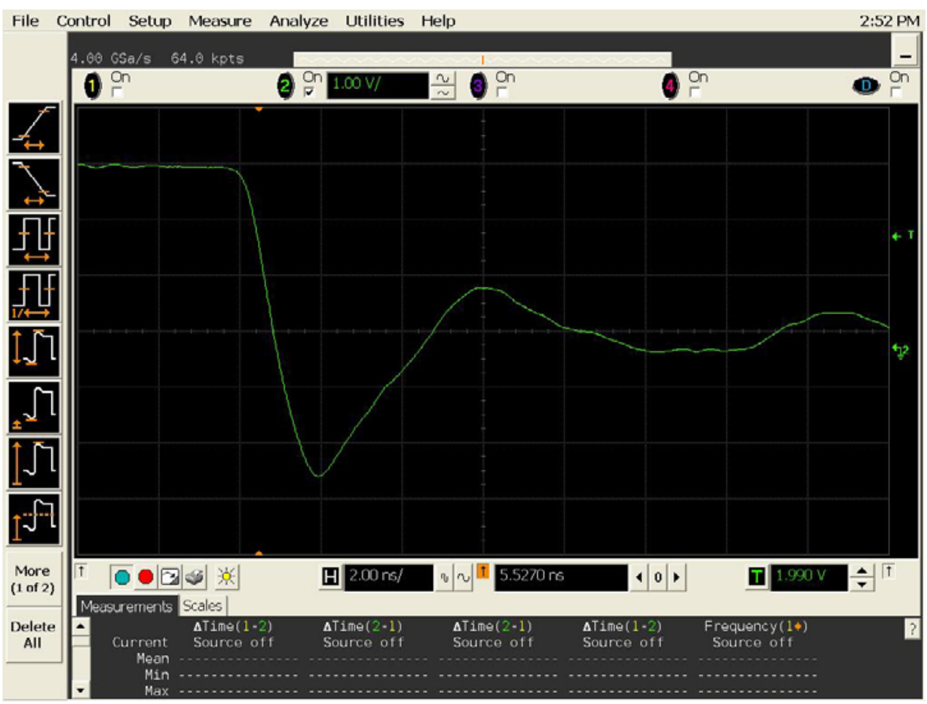

Figure 15b DUT 8236 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

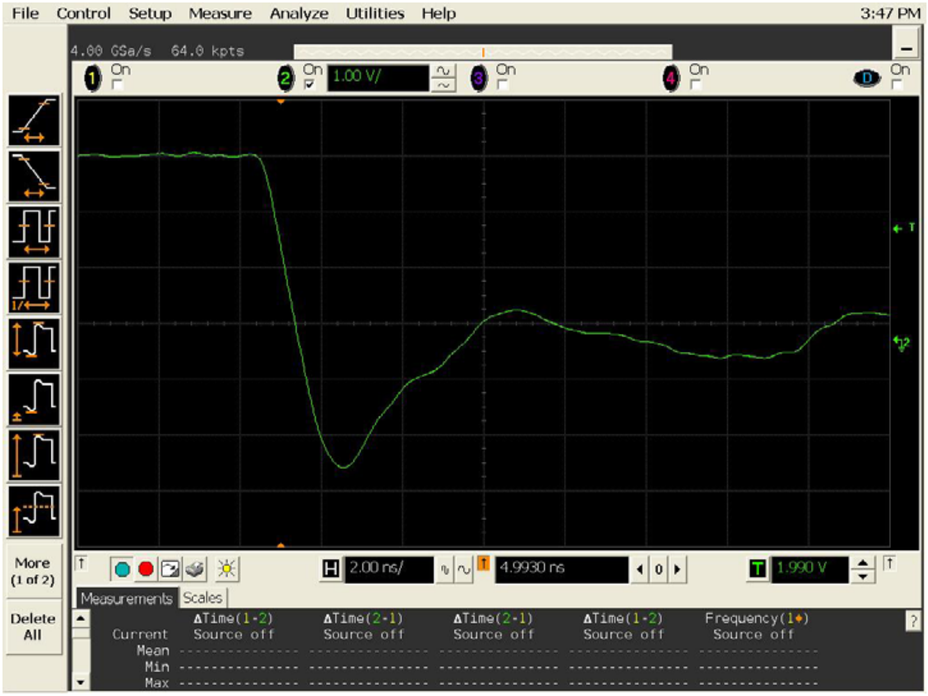

Figure 16a DUT 8237 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

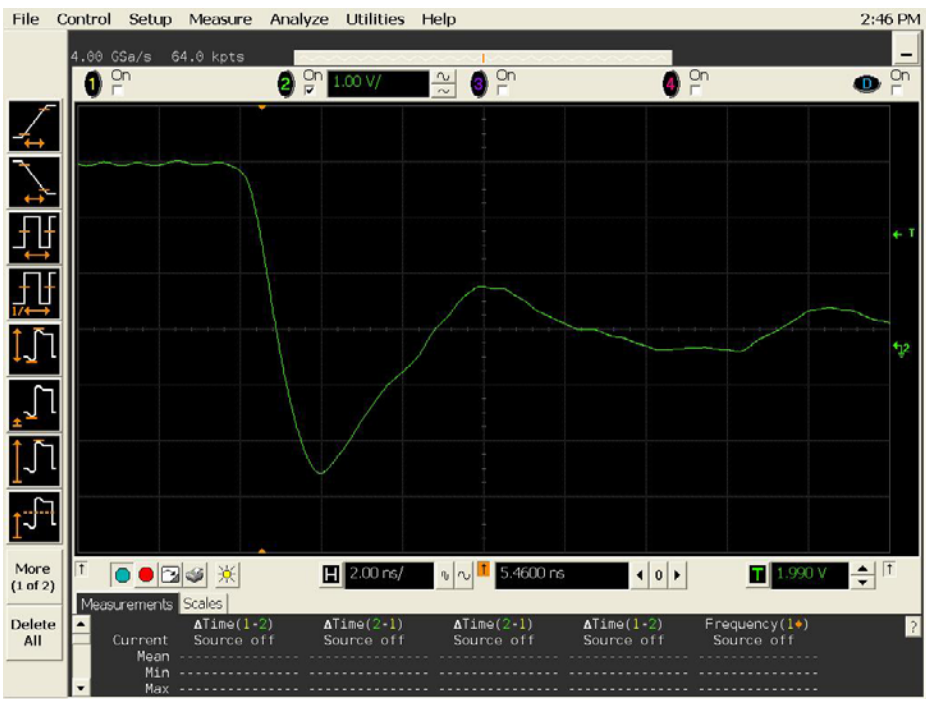

Figure 16b DUT 8237 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

Appendix A: DUT Bias Diagram

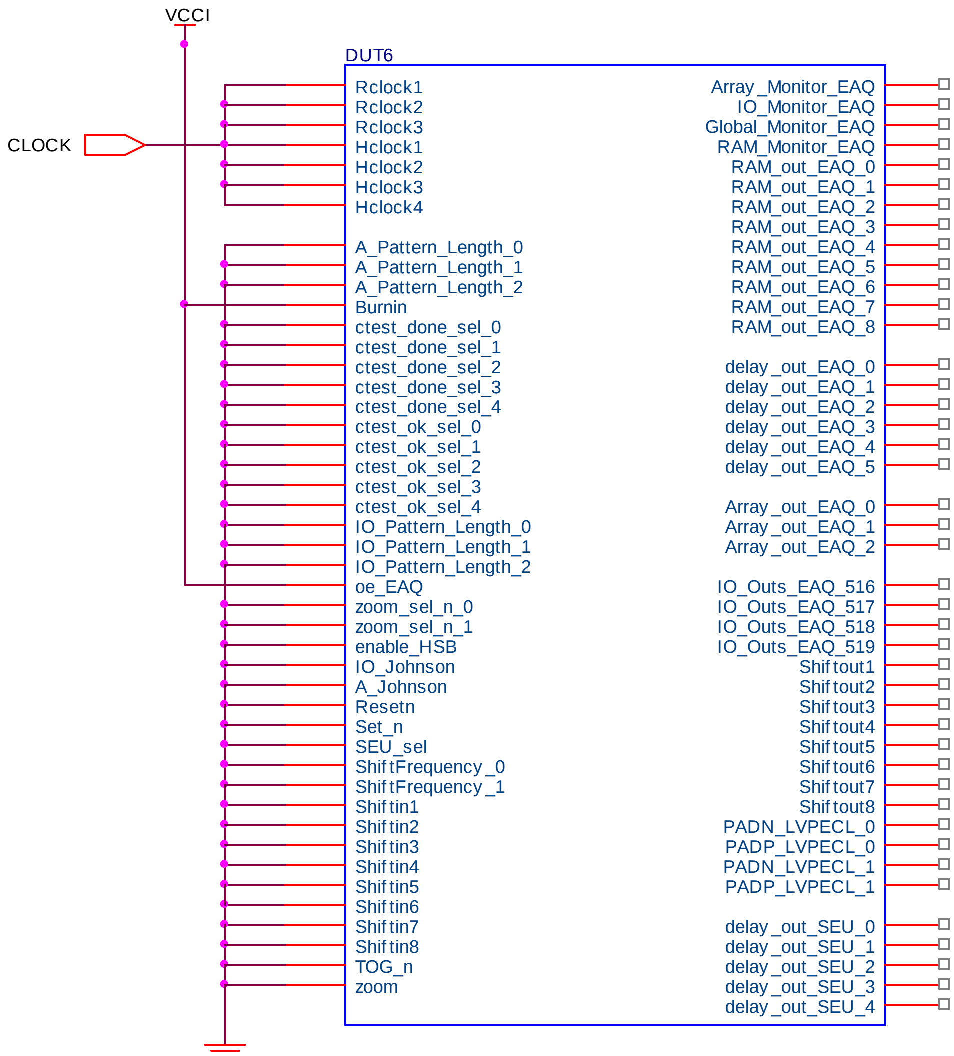

Figure A1 I/O bias During Irradiation

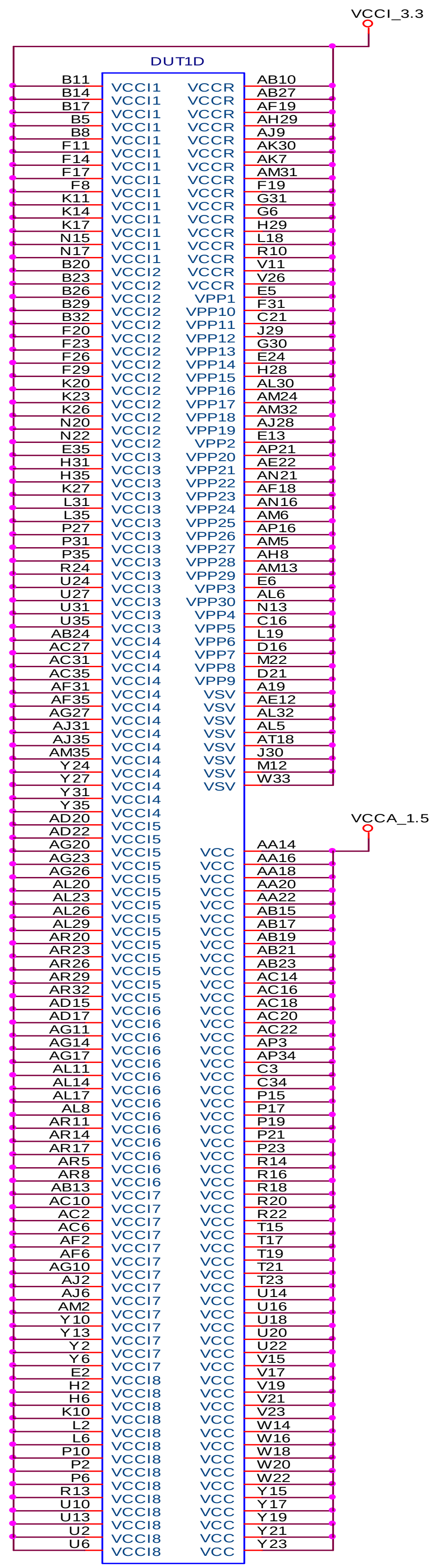

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation

Appendix B: Functionality Tests

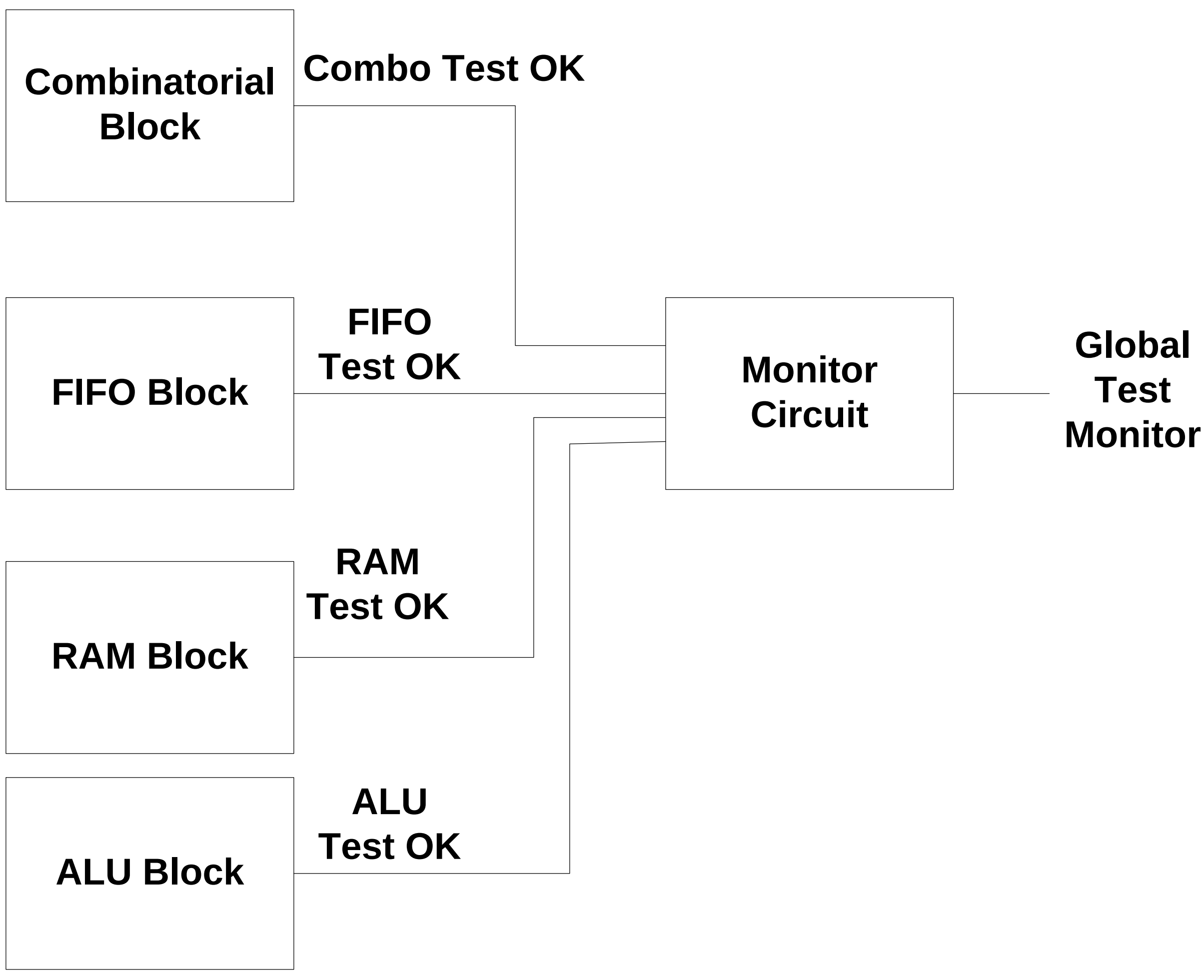

Figure B1 QBI Block – Top-Level Design

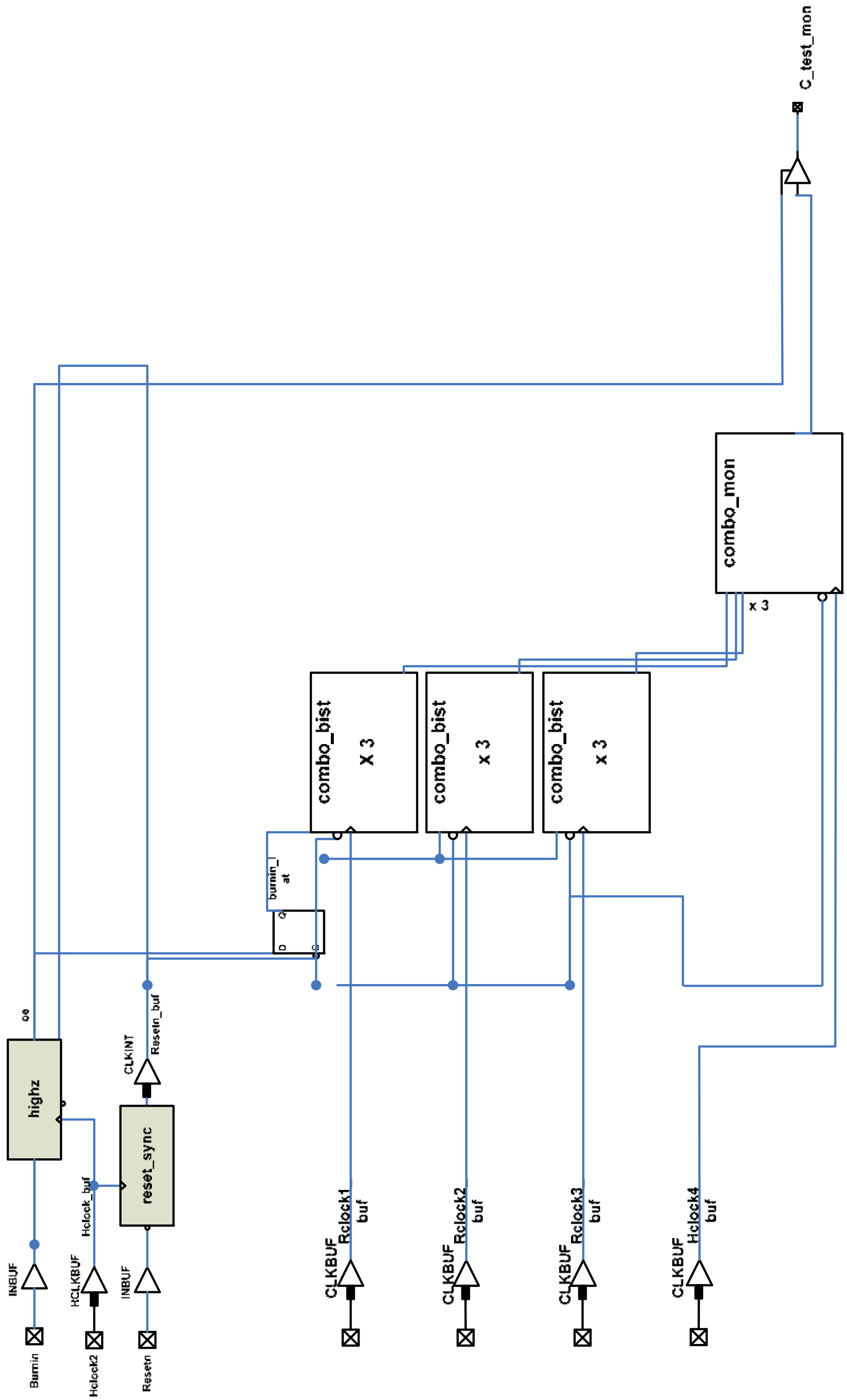

Figure B2 QBI Block – Combinatorial Test (Top Level)

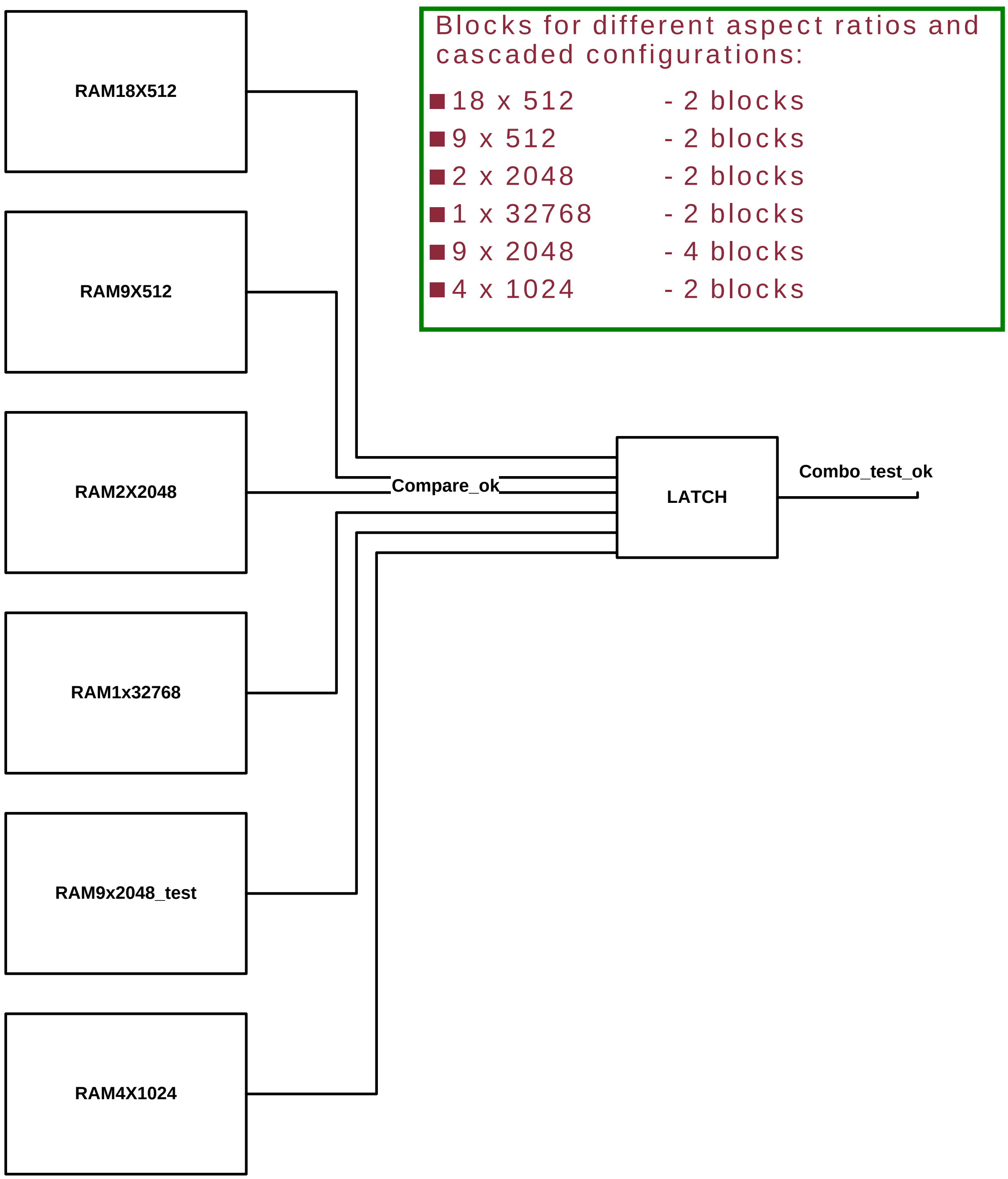

Figure B3 QBI Block – RAM Test (Top Level)

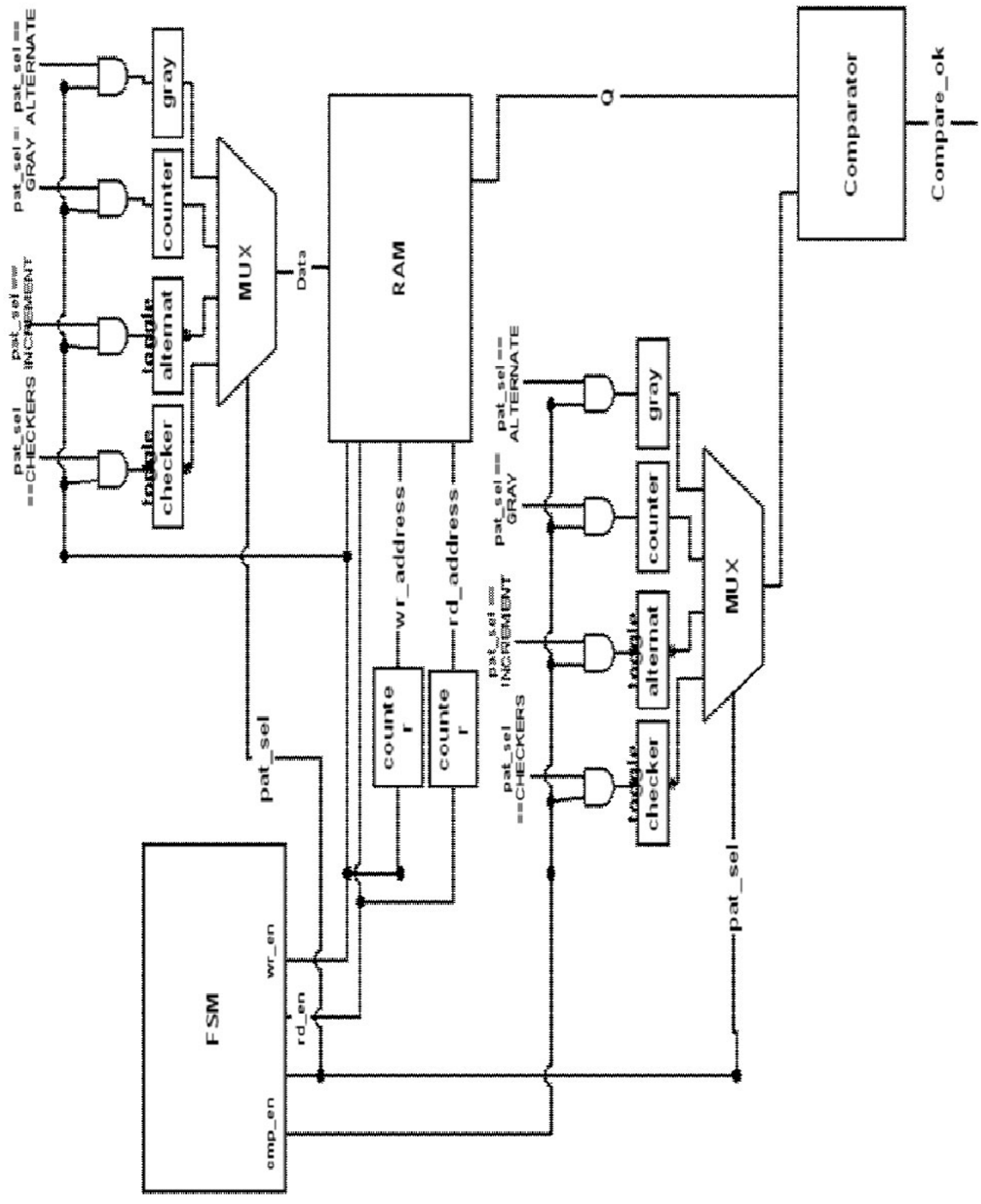

Figure B4 QBI Block – RAM Block

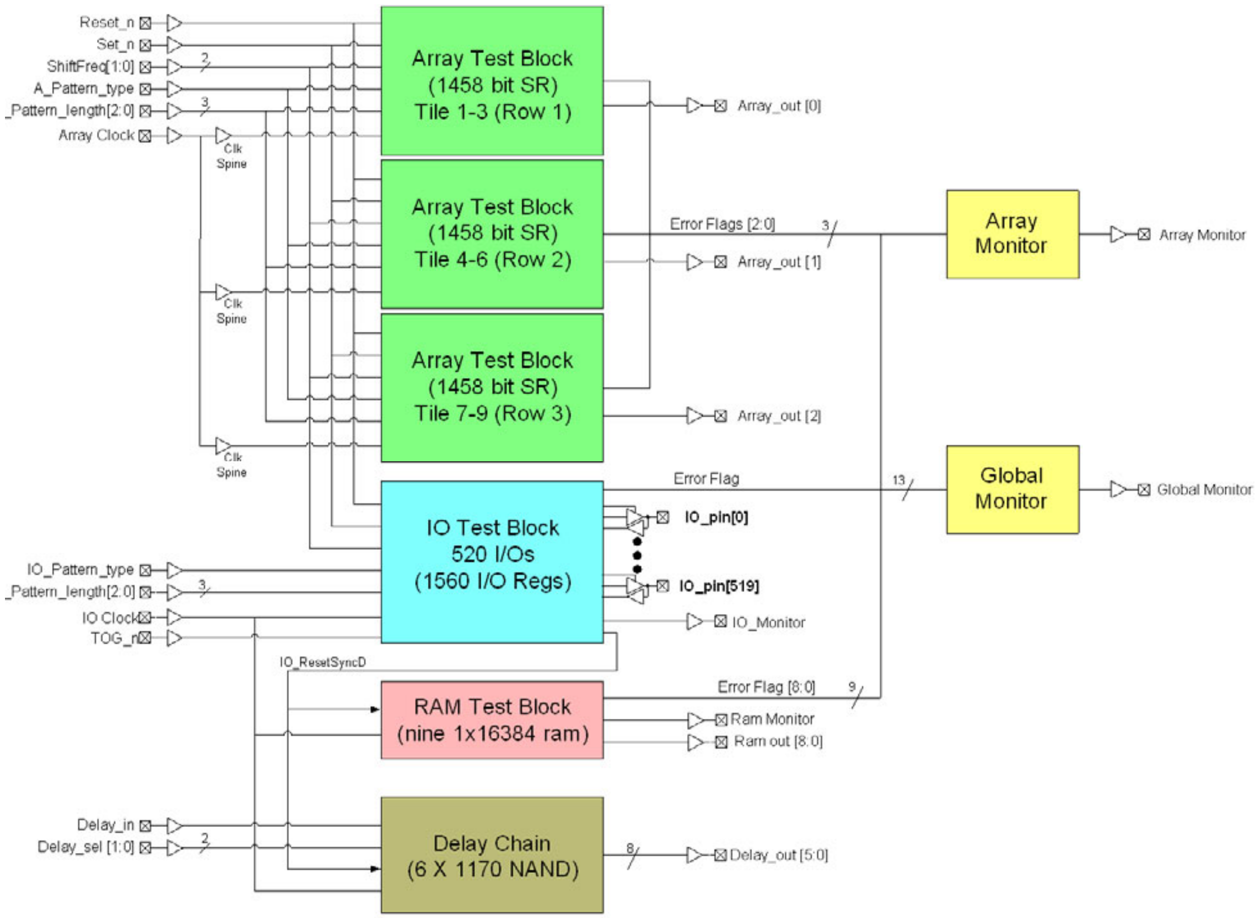

Figure B5 EAQ Block – Top Level

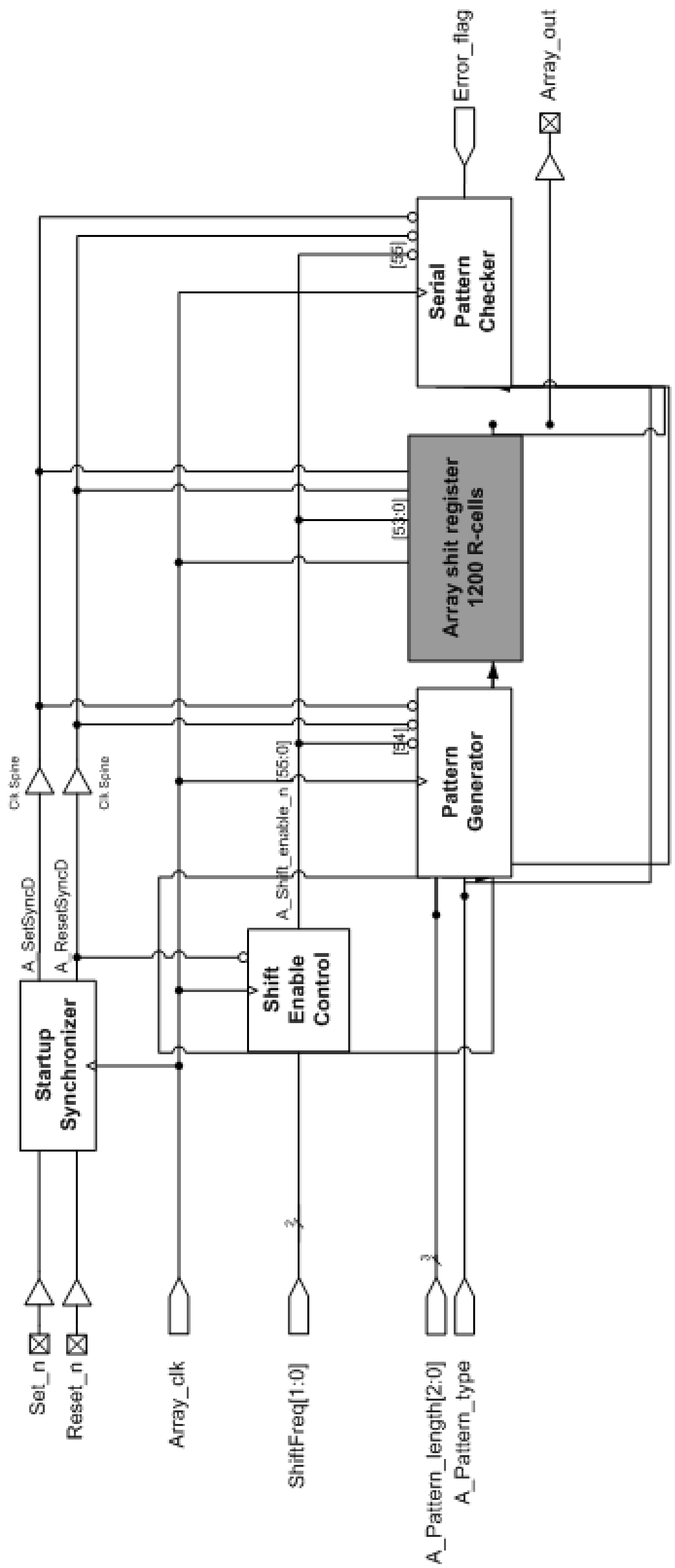

Figure B6 EAQ Block – Array Test (Shift Register)

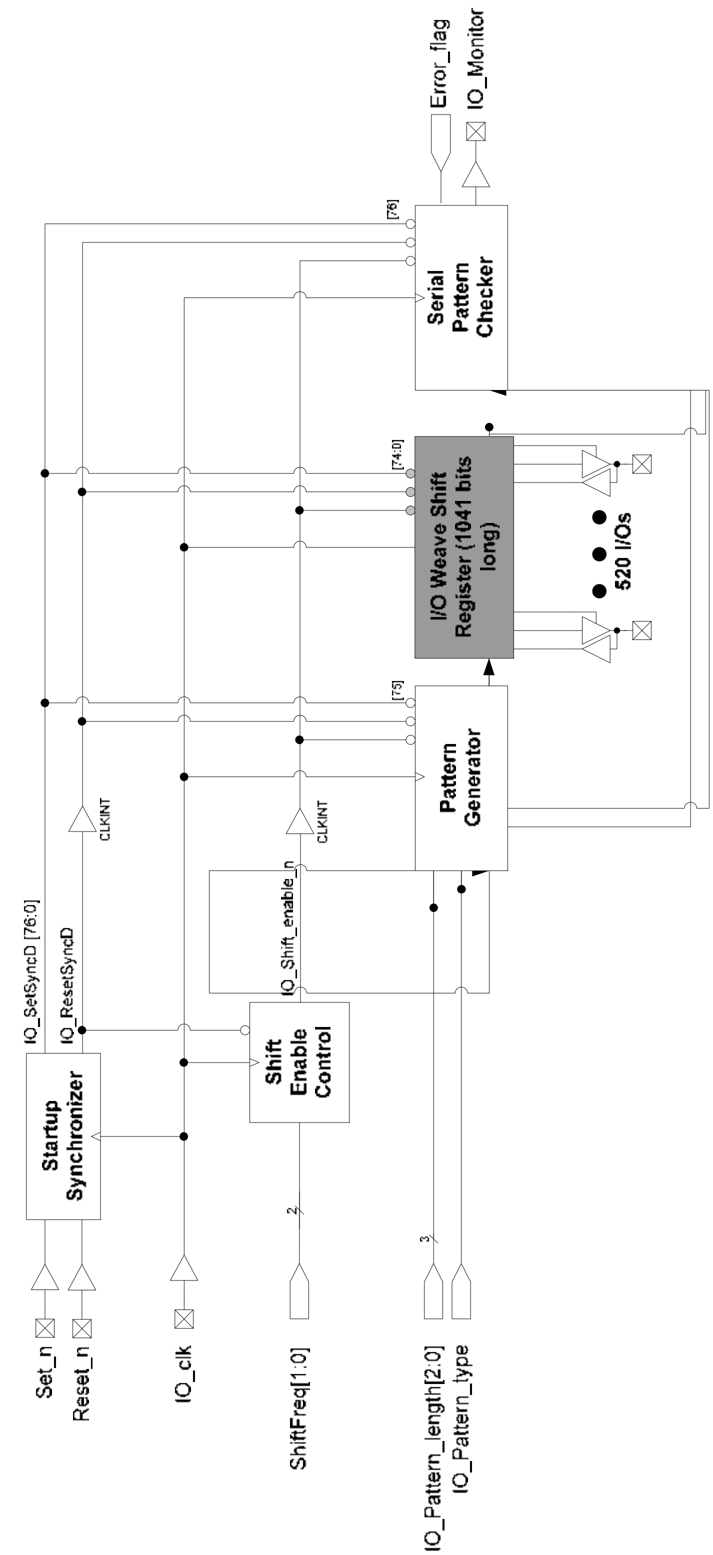

Figure B7 EAQ Block – I/O Test (Top Level)

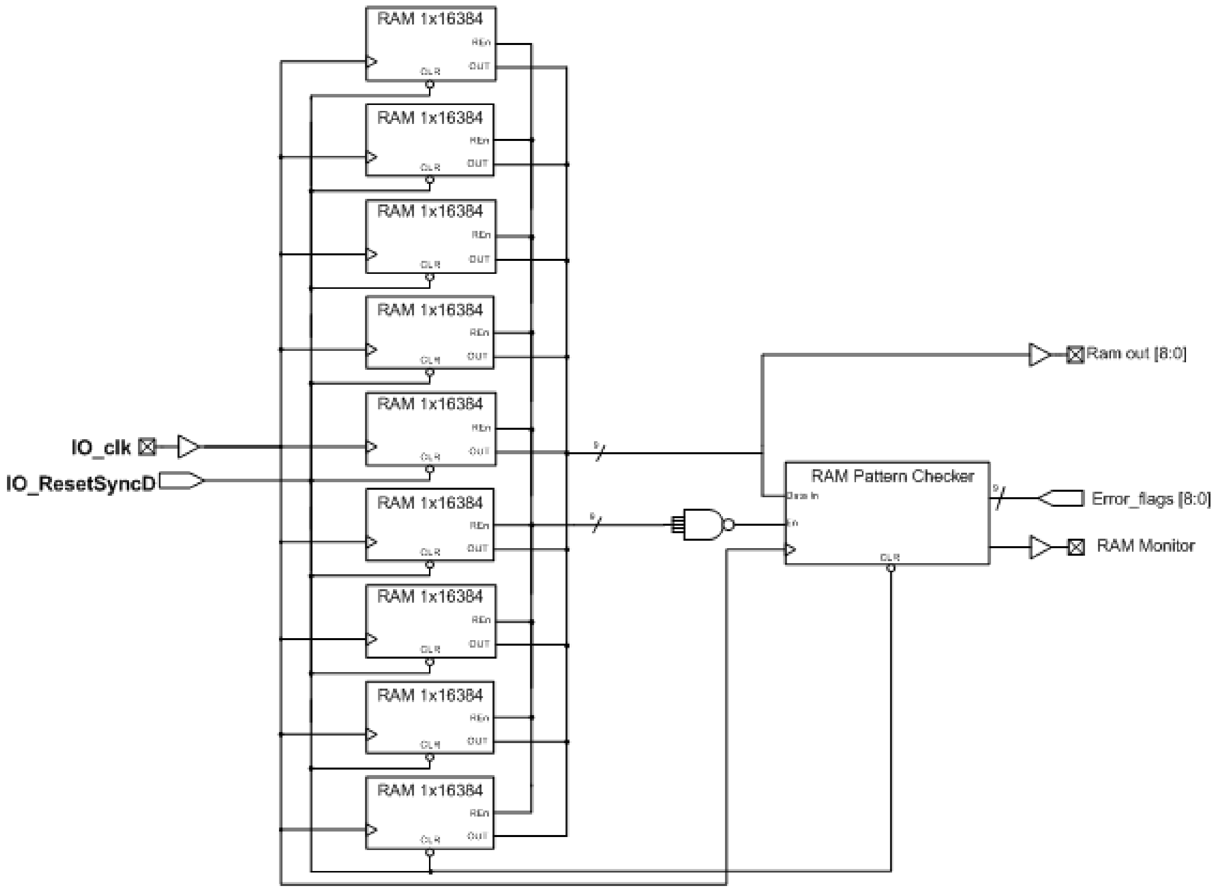

Figure B8 EAQ Block – SRAM Test (Top Level)

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