TOTAL IONIZING DOSE TEST REPORT

No. 09T-RTAX1000S-D1PQ01
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I. SUMMARY TABLE

Table 1 summarizes the TID tolerance for each tested parameters. The overall tolerance is limited by the standby power-supply current (I_{CC}). Because of logistical limitations, the room temperature annealing allowed by TM1019 to anneal down I_{CC} is performed for approximately 10 days. Every DUT passes all the listed specs in Table 1 for 300 krad(SiO_2) irradiation.

Table 1 Tolerances for each tested parameter

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 300 krad(SiO_2)
3. Input Switching Threshold (V_{IHL}/V_{ILH})	Passed 300 krad(SiO_2)
4. Output Threshold (V_{OL}/V_{OH})	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion
6. Transition Time	Passed 300 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes device under test (DUT), irradiation facility and parameters, test method, test design, and electrical parameter measurements. This TID testing, in various slightly modified forms, had been used to accumulate an extensive TID database for many generations of antifuse-based FPGAs; the link to access this TID database is attached in below:

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

The part name of the DUTs is RTAX1000S; the package is CG624. UMC used 0.15 µm technologies to manufacture it. The particular lot is numbered D1PQ01.

The Gamma Irradiator in radiation facility of Defense Microelectronics Activity is used to irradiate DUTs with Gamma rays: number 6613 and number 6615 are irradiated to 200 krad(SiO_2); number 6609, number 6611, and number 6612 are irradiated to 300 krad(SiO_2). The dose rate is constant at 7.5 krad(SiO_2)/min (condition A), and the environment is kept at 25°C.

B. Test Method

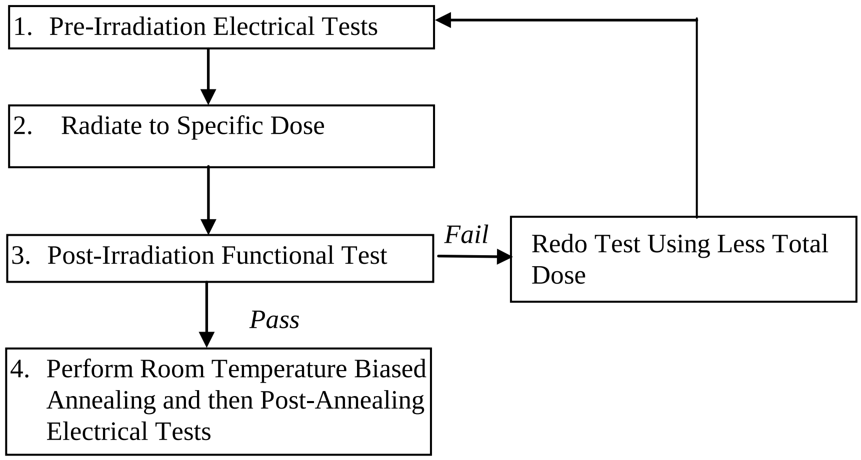

Figure 1 Parametric test flow chart

The test method is based on the military standard TM1019.6. Figure 1 shows the test flow. During irradiation, the DUT is statically biased with V_{CCI}/V_{CCA} = 3.3V/1.5V and all the inputs grounded. The accelerated annealing test in TM1019.6, section 3.12 has been done on sample lots of RTAXS, and the results show that post-irradiation annealing recovers the electrical characteristics rather than adversely affects the electrical performance. This is consistent with the general belief that the dominant TID effects in deep submicron CMOS devices are due to hole-rapping-in-field-oxide induced leakage currents and these leakages decreases with annealing temperatures. For a lot testing such as the one in this report, the accelerated annealing test is omitted because it has been proven by the above information that the annealing effect is not adverse.

TM1019.6, Section 3.11 “extended room temperature anneal test” has been applied for approximately 10-days of annealing. The data measured after this annealing is named “Post Annealing” in section III Test Results.

C. DUT Logic Design

The DUT design is a high utilization and generic design. It is similar to the design for RTAX2000S_CG624. Figure 2 shows a block diagram of the design for RTAX2000S_CG624; the Verilog file (rtax2000_CG624_Top.v) is in the aforementioned link. The functional test is performed on every sub-design with inputs and outputs; most inputs, including global clocks, are tested for leakage current; selected inputs are tested for threshold voltage, the standby I_{CC} test includes measuring static IO current (I_{CCI}) and static logic array current (I_{CCA}). Except propagation delay and the transition characteristic, which are measured on bench from the output pin O_BS, all other parameter measurements are performed on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench by measuring the expected outputs from shift registers and long buffer string (sub-design 5 and 6 described in the following).

<u>Sub-design 1 Embedded SRAM</u>

This is to test the function of the embedded RAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

<u>Sub-design 2 Unidirectional LVTTL Inputs and Outputs</u>

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. LVTTL is used because it is the worst case among all the single-ended standards.

Sub-design 3 Bidirectional 3.3V-LVTTL IO

This is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for testing.

Sub-design 4 3.3V-LVPECL Input

This is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst possible differential input standard. There are 7 channels.

Sub-design 5 Shift Registers

This is to test the radiation effects on the function of flip-flops, which are configured R-Cells.

Sub-design 6 Long Buffer String

This is to measure the radiation effects on the propagation delay. A clock signal feeding a toggle flip-flop generates a checkerboard signal; this signal is then fed into a buffer string with approximately 5,000 stages. The time delay between the input clock edge and the output switching at the end of the buffer string due to this clock edge is defined as propagation delay, which can be high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the total-dose tolerance. The total dose to cause 10% of propagation degradation is considered as the critical tolerance.

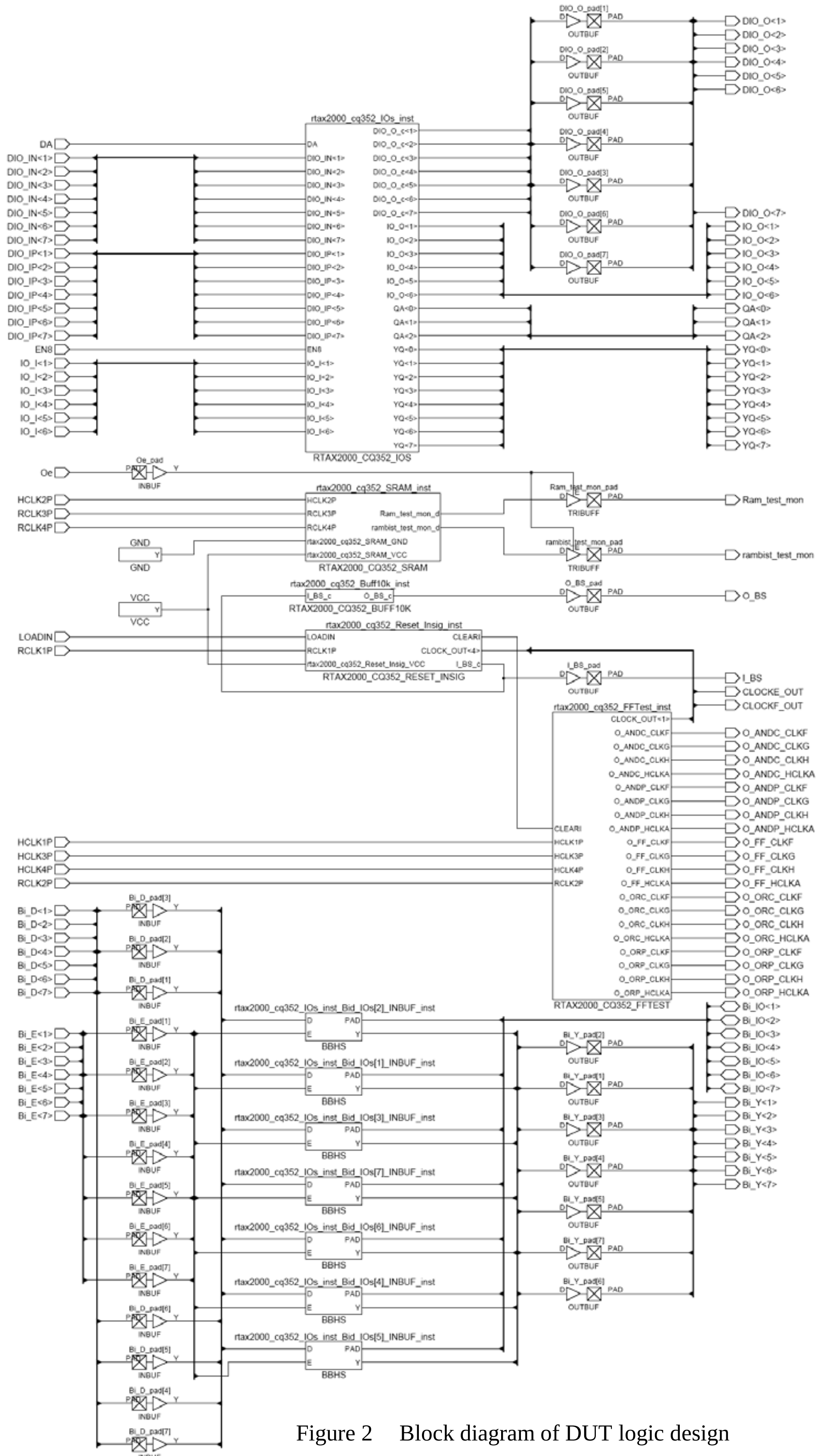

Figure 2 Block diagram of DUT logic design

III. TEST RESULTS

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing. As mentioned previously, right after the irradiation and before annealing only the functionality of shift registers and long buffer string were tested on bench.

A. Functional Test

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester. Every DUT also passed post-irradiation and pre-annealing functional tests of the shift registers and buffer string by using a bench setup.

B. Standby Power Supply Current (I_{CCA} and I_{CCI})

The logic-array power supply, V_{CCA}, is 1.5V, and the IO power supply, V_{CCI}, is 3.3V. Their standby currents, I_{CCA} and I_{CCI}, are monitored in-flux; Figure 3-8 show the plots of I_{CCA} and I_{CCI} versus total dose for the DUTs.

Referring to TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} should be defined as the addition of highest I_{CCI}, I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS spec sheet in the document posted on the Actel website; the link is attached in below:

http://www.actel.com/documents/RTAXS_DS.pdf

Therefor, the PIPL for I_{CCA} is 500 mA, and the PIPL of I_{CCI} is 35+10+3.13×7 = 66.91(mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation• right after irradiation and before annealing, and post-annealing I_{CCA} and I_{CCI} data: the post-annealing I_{CCA} or I_{CCI} of every DUT, either irradiated to 200 krad(SiO_2) or 300 krad(SiO_2) is below the PIPL.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing I_{CCA} and I_{CCI}

DUT	Total Dose krad (SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
6609	300	5	10	6	22	155	66
6611	300	5	7	7	22	153	65
6612	300	5	10	8	21	154	63
6613	200	5	6	6	22	53	29
6615	200	2	3	3	21	61	31

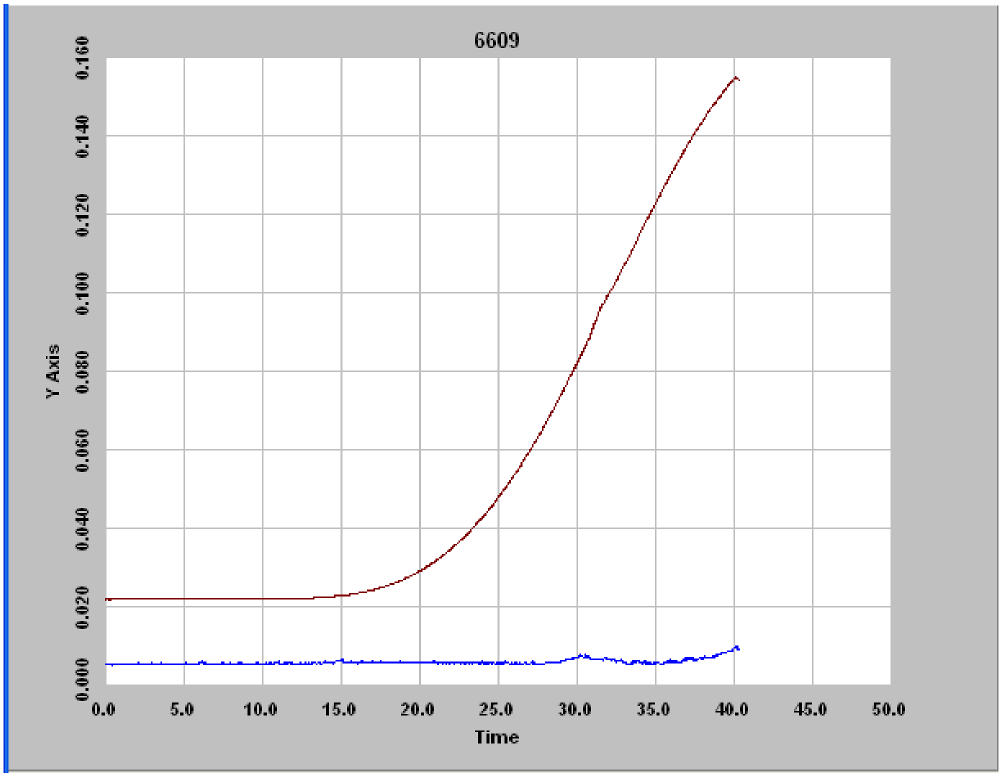

Figure 3 DUT 6609 in-flux I_{CCA} and I_{CCI}. The Y-Axis is current in Amp; Time is in minutes, the total dose can be calculated by dose rate (7.5krad/min) x Time.

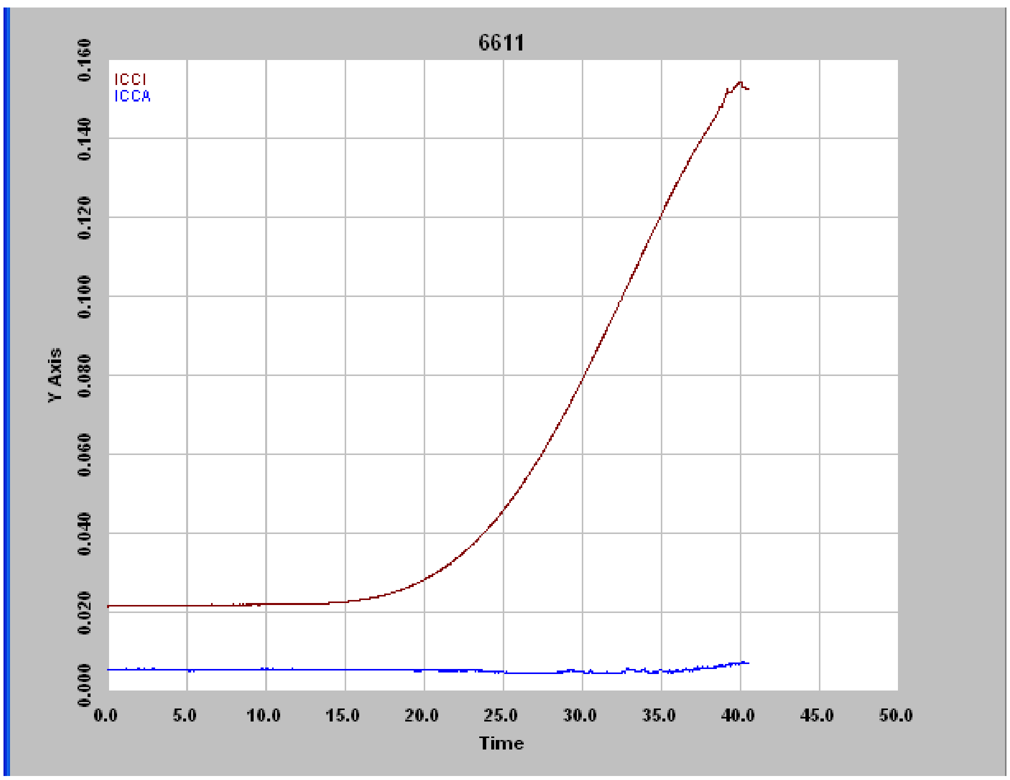

Figure 4 DUT 6611 in-flux I_{CCA} and I_{CCI}

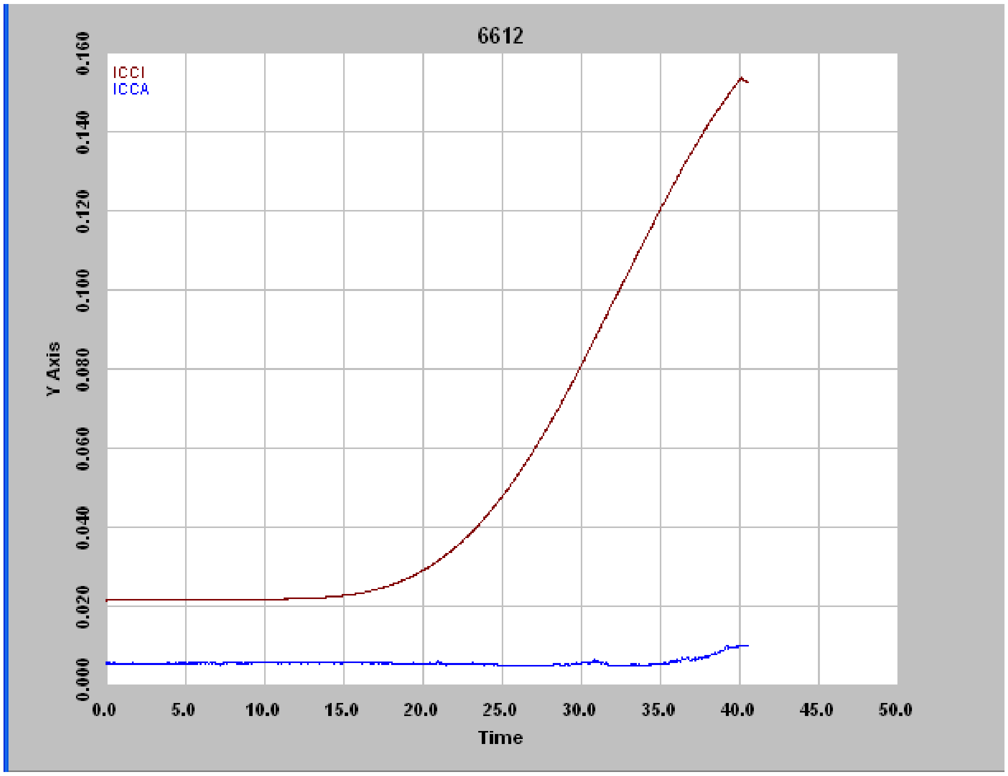

Figure 5 DUT 6612 in-flux I_{CCA} and I_{CCI}

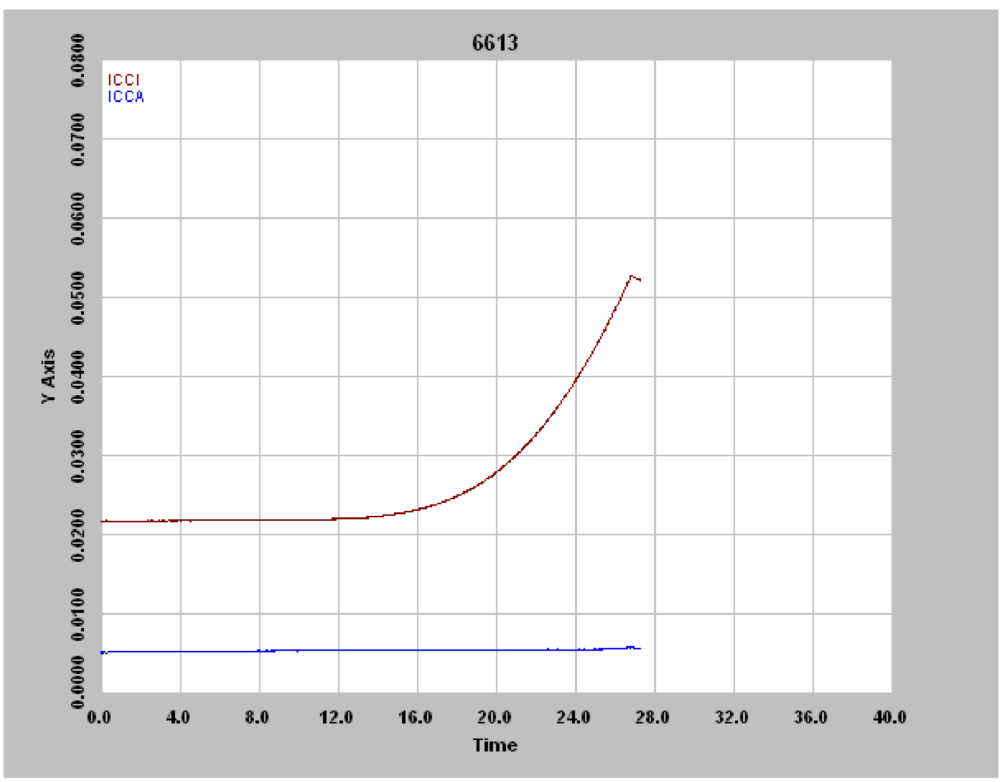

Figure 6 DUT 6613 in-flux I_{CCA} and I_{CCI}

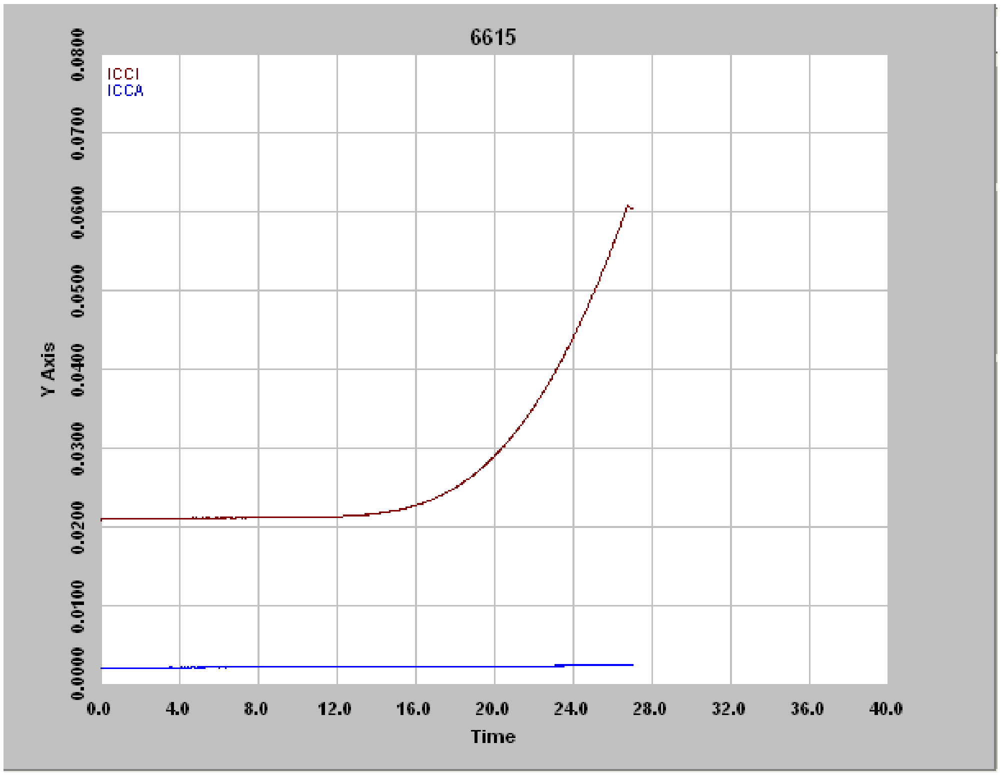

Figure 7 DUT 6615 in-flux I_{CCA} and I_{CCI}

C. Single-Ended 3.3V-LVTTL V_{IHL}/V_{ILH} and I_{IL}/I_{IH}

The input switching thresholds, or trip point, is defined as the applied input voltage at which the output of the design• often just input and output buffers• starts to switch: V_{IHL} is the input trip point when the input is going high to low; V_{ILH} is the input trip point when the input is going low to high.

Tables 3a and 3b list the pre-irradiation and post-annealing single-ended V_{IHL}. In each case, the difference between the pre-irradiation and post-annealing data is negligibly small. Tables 4a and 4b show the pre-irradiation and post-annealing single-ended V_{ILH}; again the difference between the pre-irradiation and post-annealing data is negligibly small.

I_{IL} is the current sink into an input being forced to low, and I_{IH} is the current source from an input being forced to high. The PIPL for both of them is 5µA.

Tables 5a and 5b show the pre-irradiation and the post-annealing I_{IL} data. Tables 6a and 6b show the pre-irradiation and post-annealing I_{IH} data. The post-annealing data of both I_{IL} and I_{IH} for every tested input in every DUT is below the 5µA PIPL.

Table 3a Single-ended $V_{IH\,L}$

DUT		6609		6611		6612	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DA	1.355	1.345	1.345	1.34	1.35	1.35
bi_levels_vil	EN8	1.32	1.31	1.315	1.305	1.31	1.31
bi_levels_vil	IO_I_6	1.34	1.33	1.33	1.325	1.335	1.33
bi_levels_vil	IO_I_5	1.31	1.305	1.315	1.31	1.31	1.305
bi_levels_vil	IO_I_4	1.365	1.36	1.36	1.355	1.365	1.36
bi_levels_vil	IO_I_3	1.36	1.35	1.36	1.355	1.36	1.355
bi_levels_vil	IO_I_2	1.365	1.36	1.365	1.355	1.36	1.36
bi_levels_vil	IO_I_1	1.365	1.36	1.365	1.355	1.365	1.355

Table 3b Single-ended $V_{IH\,L}$

DUT		6613		6615	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DA	1.35	1.345	1.35	1.34
bi_levels_vil	EN8	1.32	1.31	1.32	1.31
bi_levels_vil	IO_I_6	1.355	1.345	1.33	1.32
bi_levels_vil	IO_I_5	1.315	1.3	1.325	1.305
bi_levels_vil	IO_I_4	1.365	1.355	1.36	1.35
bi_levels_vil	IO_I_3	1.355	1.355	1.365	1.355
bi_levels_vil	IO_I_2	1.365	1.36	1.37	1.36
bi_levels_vil	IO_I_1	1.37	1.36	1.365	1.355

Table 4a Single-ended $V_{IL\,H}$

DUT		6609		6611		6612	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DA	1.39	1.385	1.38	1.365	1.38	1.375
bi_levels_vih	EN8	1.43	1.42	1.425	1.42	1.43	1.42
bi_levels_vih	IO_I_6	1.375	1.375	1.385	1.375	1.38	1.375
bi_levels_vih	IO_I_5	1.4	1.37	1.385	1.39	1.405	1.375
bi_levels_vih	IO_I_4	1.37	1.36	1.36	1.355	1.37	1.36
bi_levels_vih	IO_I_3	1.37	1.365	1.37	1.35	1.375	1.365
bi_levels_vih	IO_I_2	1.37	1.365	1.365	1.355	1.37	1.365
bi_levels_vih	IO_I_1	1.37	1.365	1.365	1.36	1.37	1.36

Table 4b Single-ended $V_{IL\,H}$

DUT		6613		6615	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DA	1.385	1.385	1.375	1.37
bi_levels_vih	EN8	1.43	1.42	1.43	1.415
bi_levels_vih	IO_I_6	1.385	1.38	1.385	1.38
bi_levels_vih	IO_I_5	1.4	1.4	1.4	1.39
bi_levels_vih	IO_I_4	1.37	1.36	1.365	1.36
bi_levels_vih	IO_I_3	1.365	1.37	1.37	1.365
bi_levels_vih	IO_I_2	1.375	1.365	1.37	1.36
bi_levels_vih	IO_I_1	1.37	1.365	1.37	1.365

Table 5a I_{IL} data

DUT		6609				6611				6612			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIL_Inputs_Max_	Bi_D_1	-1.8591	nA	-5.8383	nA	-4.7911	nA	-8.3515	nA	-3.3251	nA	-6.0477	nA
IIL_Inputs_Max_	Bi_D_2	-2.9062	nA	-2.6968	nA	-3.1157	nA	-2.9062	nA	-2.2779	nA	-3.5345	nA
IIL_Inputs_Max_	Bi_D_3	-1.0213	nA	-2.9062	nA	-3.744	nA	-2.6968	nA	-1.8591	nA	-811.88	pA
IIL_Inputs_Max_	Bi_D_4	-2.1728	nA	-4.0585	nA	-2.5919	nA	-9.2964	nA	-3.2204	nA	-6.9917	nA
IIL_Inputs_Max_	Bi_D_5	-915.73	pA	-2.1728	nA	-6.3631	nA	-3.849	nA	-5.5251	nA	-3.4299	nA
IIL_Inputs_Max_	Bi_D_6	-11.447	nA	-6.6255	nA	-9.3508	nA	-10.1893	nA	-11.2375	nA	-7.6736	nA
IIL_Inputs_Max_	Bi_D_7	-4.5724	nA	-5.4092	nA	-4.3632	nA	-2.2711	nA	-5.4092	nA	-3.3171	nA
IIL_Inputs_Max_	Bi_E_1	-5.4092	nA	-2.0619	nA	-5.8277	nA	-2.8987	nA	-5.4092	nA	-2.0619	nA
IIL_Inputs_Max_	Bi_E_2	-2.6895	nA	-4.154	nA	-5.4092	nA	-2.2711	nA	-2.8987	nA	-2.6895	nA
IIL_Inputs_Max_	Bi_E_3	-3.7356	nA	-2.6895	nA	-3.1079	nA	-4.7816	nA	-2.8987	nA	-3.5264	nA
IIL_Inputs_Max_	Bi_E_4	-4.154	nA	-3.1079	nA	-2.2711	nA	-597.425	pA	-2.4803	nA	-179.01	pA
IIL_Inputs_Max_	Bi_E_5	-4.9908	nA	-3.3171	nA	-4.9908	nA	-2.2711	nA	-2.4803	nA	-2.4803	nA
IIL_Inputs_Max_	Bi_E_6	-4.3632	nA	239.4136	pA	-3.9448	nA	-4.3632	nA	-2.8987	nA	-806.64	pA
IIL_Inputs_Max_	Bi_E_7	-3.3171	nA	-597.425	pA	-806.634	pA	-3.1079	nA	-806.634	pA	-5.2	nA
IIL_Inputs_Max_	DA	-7.2046	nA	-8.4619	nA	-7.8333	nA	-9.9288	nA	-6.3664	nA	-8.2524	nA
IIL_Inputs_Max_	DIO_IN_1	-1.8038	nA	-6.2062	nA	-6.4158	nA	-4.3194	nA	-16.8978	nA	-6.4158	nA
IIL_Inputs_Max_	DIO_IN_2	-5.7378	nA	-5.7378	nA	-8.2524	nA	-5.9473	nA	-3.2232	nA	-5.5282	nA
IIL_Inputs_Max_	DIO_IN_3	-3.0137	nA	-7.2046	nA	-4.8996	nA	-6.3664	nA	-8.0428	nA	-7.2046	nA
IIL_Inputs_Max_	DIO_IN_4	3.2276	nA	-5.9965	nA	-5.7869	nA	-5.9965	nA	-3.2712	nA	-4.1098	nA
IIL_Inputs_Max_	DIO_IN_5	-6.576	nA	-4.69	nA	-4.8996	nA	-8.0428	nA	-4.8996	nA	-6.576	nA
IIL_Inputs_Max_	DIO_IN_6	-1.1277	nA	-6.9951	nA	-5.7378	nA	-6.7855	nA	-708.615	pA	-8.2524	nA
IIL_Inputs_Max_	DIO_IN_7	-2.385	nA	-4.69	nA	-4.4805	nA	-6.3664	nA	-1.9659	nA	-6.7855	nA
IIL_Inputs_Max_	DIO_IP_1	-5.3676	nA	-5.7869	nA	-5.3676	nA	-3.4809	nA	3.4372	nA	-5.7869	nA
IIL_Inputs_Max_	DIO_IP_2	-3.8519	nA	-5.9473	nA	-2.5946	nA	-7.2046	nA	-4.0614	nA	-7.2046	nA
IIL_Inputs_Max_	DIO_IP_3	-336.29	pA	-4.5291	nA	-965.204	pA	-5.9965	nA	-755.566	pA	-5.158	nA
IIL_Inputs_Max_	DIO_IP_4	-1.9659	nA	-7.8333	nA	2.4346	nA	-8.0428	nA	1.3869	nA	-7.6237	nA
IIL_Inputs_Max_	DIO_IP_5	-6.3664	nA	-4.271	nA	-4.69	nA	-4.271	nA	-6.576	nA	-8.0428	nA
IIL_Inputs_Max_	DIO_IP_6	-499.07	pA	-4.8996	nA	-1.9659	nA	-5.9473	nA	-5.5282	nA	-4.4805	nA
IIL_Inputs_Max_	DIO_IP_7	-5.7378	nA	-8.0428	nA	-6.1569	nA	-3.2232	nA	1.806	nA	-4.271	nA
IIL_Inputs_Max_	EN8	-2.8041	nA	-5.7378	nA	-6.576	nA	-5.9473	nA	-6.9951	nA	-8.881	nA
IIL_Inputs_Max_	HCLK1P	-4.9908	nA	-5.2	nA	-4.5724	nA	239.4136	pA	-5.2	nA	-2.6895	nA
IIL_Inputs_Max_	HCLK2P	-5.3676	nA	-4.1098	nA	-4.9483	nA	-4.7387	nA	-5.7869	nA	-7.0447	nA
IIL_Inputs_Max_	HCLK3P	-3.744	nA	-1.2307	nA	-3.5345	nA	-1.6496	nA	-1.2307	nA	-2.0685	nA
IIL_Inputs_Max_	HCLK4P	-4.8965	nA	-5.7346	nA	-3.6394	nA	-6.1536	nA	-1.5443	nA	-1.7538	nA
IIL_Inputs_Max_	IO_I_1	-7.6736	nA	-2.0134	nA	-3.6905	nA	-6.6255	nA	-3.0616	nA	-5.3676	nA
IIL_Inputs_Max_	IO_I_2	-3.3251	nA	-2.0685	nA	-2.6968	nA	-2.9062	nA	-2.0685	nA	-3.3251	nA
IIL_Inputs_Max_	IO_I_3	82.99	pA	-3.6905	nA	-3.9001	nA	-5.9965	nA	7.4203	nA	-4.7387	nA
IIL_Inputs_Max_	IO_I_4	-3.1157	nA	-183.576	pA	-1.4402	nA	-3.744	nA	-1.2307	nA	-4.7911	nA
IIL_Inputs_Max_	IO_I_5	1.3408	nA	-4.9483	nA	-4.5291	nA	-7.0447	nA	-8.9315	nA	-6.4158	nA
IIL_Inputs_Max_	IO_I_6	-4.0614	nA	-4.0614	nA	-2.385	nA	-5.5282	nA	-5.5282	nA	-6.1569	nA
IIL_Inputs_Max_	LOADIN	-6.3334	nA	-5.0779	nA	-8.0074	nA	-474.54	pA	-7.1704	nA	-4.4502	nA
IIL_Inputs_Max_	RCLK1P	-3.6905	nA	-6.2062	nA	-1.5941	nA	-5.158	nA	-5.9965	nA	-2.4327	nA
IIL_Inputs_Max_	RCLK2P	-3.0109	nA	-5.1061	nA	-3.2204	nA	-7.4107	nA	-3.6394	nA	-4.0585	nA
IIL_Inputs_Max_	RCLK3P	-1.8591	nA	-4.5817	nA	-4.7911	nA	-2.4874	nA	-3.5345	nA	-4.1628	nA
IIL_Inputs_Max_	RCLK4P	-7.5013	nA	-1.2251	nA	-1.6435	nA	-1.4343	nA	-4.9908	nA	-2.4803	nA

Actel

Table 5b I_{IL} data

DUT		6613		6615	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	-8.1421 nA	-7.0949 nA	-6.8855 nA	-7.7232 nA
IIL_Inputs_Max_	Bi_D_2	-4.1628 nA	-4.3723 nA	-393.01 pA	-2.6968 nA
IIL_Inputs_Max_	Bi_D_3	-2.2779 nA	-1.8591 nA	2.5391 nA	-4.1628 nA
IIL_Inputs_Max_	Bi_D_4	-7.6202 nA	-4.8965 nA	-5.1061 nA	-6.1536 nA
IIL_Inputs_Max_	Bi_D_5	-2.1728 nA	-5.5251 nA	-2.1728 nA	-4.8965 nA
IIL_Inputs_Max_	Bi_D_6	-12.915 nA	-6.8351 nA	-2.6423 nA	-9.9797 nA
IIL_Inputs_Max_	Bi_D_7	-4.9908 nA	-2.2711 nA	-4.3632 nA	-5.4092 nA
IIL_Inputs_Max_	Bi_E_1	-388.21 pA	-3.9448 nA	-1.0158 nA	-2.0619 nA
IIL_Inputs_Max_	Bi_E_2	-5.2 nA	239.4136 pA	-6.8737 nA	-2.0619 nA
IIL_Inputs_Max_	Bi_E_3	-3.1079 nA	-2.2711 nA	-3.7356 nA	-2.4803 nA
IIL_Inputs_Max_	Bi_E_4	-4.154 nA	-1.4343 nA	-5.2 nA	-4.3632 nA
IIL_Inputs_Max_	Bi_E_5	-3.1079 nA	-4.5724 nA	-5.2 nA	-2.8987 nA
IIL_Inputs_Max_	Bi_E_6	-4.3632 nA	-4.3632 nA	-7.5013 nA	-3.1079 nA
IIL_Inputs_Max_	Bi_E_7	-2.6895 nA	-1.6435 nA	-806.634 pA	-806.63 pA
IIL_Inputs_Max_	DA	-6.1569 nA	-8.0428 nA	-14.958 nA	-9.7192 nA
IIL_Inputs_Max_	DIO_IN_1	-11.866 nA	-6.2062 nA	-2.223 nA	-5.3676 nA
IIL_Inputs_Max_	DIO_IN_2	2.6442 nA	-10.1383 nA	-4.0614 nA	-6.1569 nA
IIL_Inputs_Max_	DIO_IN_3	548.68 pA	-6.3664 nA	-7.4142 nA	-5.3187 nA
IIL_Inputs_Max_	DIO_IN_4	5.5336 nA	-5.9965 nA	2.389 nA	-3.4809 nA
IIL_Inputs_Max_	DIO_IN_5	-7.8333 nA	-6.7855 nA	-6.3664 nA	-5.1091 nA
IIL_Inputs_Max_	DIO_IN_6	5.997 nA	-6.9951 nA	-6.1569 nA	-6.3664 nA
IIL_Inputs_Max_	DIO_IN_7	-6.1569 nA	-4.271 nA	-8.2524 nA	-7.4142 nA
IIL_Inputs_Max_	DIO_IP_1	-11.866 nA	-6.4158 nA	-12.4953 nA	-3.9001 nA
IIL_Inputs_Max_	DIO_IP_2	-5.9473 nA	-7.8333 nA	-5.1091 nA	-8.881 nA
IIL_Inputs_Max_	DIO_IP_3	1.5505 nA	-4.5291 nA	-3.9001 nA	-2.6423 nA
IIL_Inputs_Max_	DIO_IP_4	-5.5282 nA	-9.5097 nA	-2.1755 nA	-6.576 nA
IIL_Inputs_Max_	DIO_IP_5	5.1588 nA	-4.4805 nA	-5.3187 nA	-4.8996 nA
IIL_Inputs_Max_	DIO_IP_6	-1.9659 nA	-4.8996 nA	-2.8041 nA	-5.1091 nA
IIL_Inputs_Max_	DIO_IP_7	-2.385 nA	-6.9951 nA	-5.1091 nA	-5.3187 nA
IIL_Inputs_Max_	EN8	-8.881 nA	-4.69 nA	3.4824 nA	-4.0614 nA
IIL_Inputs_Max_	HCLK1P	-5.2 nA	-5.2 nA	-2.4803 nA	-2.2711 nA
IIL_Inputs_Max_	HCLK2P	-3.4809 nA	-2.223 nA	921.5446 pA	-4.7387 nA
IIL_Inputs_Max_	HCLK3P	-2.4874 nA	-3.9534 nA	-5.21 nA	-3.3251 nA
IIL_Inputs_Max_	HCLK4P	-4.0585 nA	-3.2204 nA	-5.3156 nA	-496.7 pA
IIL_Inputs_Max_	IO_I_1	-8.0929 nA	-4.7387 nA	-5.9965 nA	-3.9001 nA
IIL_Inputs_Max_	IO_I_2	-4.3723 nA	-4.7911 nA	-3.1157 nA	-1.8591 nA
IIL_Inputs_Max_	IO_I_3	-4.9483 nA	-7.2544 nA	-11.0279 nA	-4.9483 nA
IIL_Inputs_Max_	IO_I_4	-811.88 pA	-2.0685 nA	-1.8591 nA	-1.2307 nA
IIL_Inputs_Max_	IO_I_5	2.389 nA	-8.3026 nA	-3.4809 nA	-5.158 nA
IIL_Inputs_Max_	IO_I_6	-4.271 nA	-6.7855 nA	-9.7192 nA	-3.6423 nA
IIL_Inputs_Max_	LOADIN	-4.4502 nA	-2.567 nA	-6.5426 nA	-3.8225 nA
IIL_Inputs_Max_	RCLK1P	-9.3508 nA	-6.6255 nA	-7.0447 nA	-4.9483 nA
IIL_Inputs_Max_	RCLK2P	-496.70 pA	-3.0109 nA	-2.1728 nA	-3.0109 nA
IIL_Inputs_Max_	RCLK3P	-1.8591 nA	-3.9534 nA	-1.6496 nA	-602.44 pA
IIL_Inputs_Max_	RCLK4P	-179.01 pA	-3.1079 nA	-3.9448 nA	-2.6895 nA

Table 6a I_{IH} data

DUT		6609		6611		6612	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	2.1202 nA	3.1674 nA	1.7013 nA	3.3768 nA	-1.2307 nA	-1.231 nA
IIH_Inputs_Max_	Bi_D_2	2.7485 nA	1.4919 nA	863.597 pA	1.9108 nA	-1.2307 nA	-393.01 pA
IIH_Inputs_Max_	Bi_D_3	654.1625 pA	1.4919 nA	1.7013 nA	-1.2307 nA	235.293 pA	-2.9062 nA
IIH_Inputs_Max_	Bi_D_4	131.844 pA	4.7412 nA	2.227 nA	2.646 nA	969.907 pA	4.7412 nA
IIH_Inputs_Max_	Bi_D_5	-287.188 pA	131.844 pA	-4.0585 nA	550.8757 pA	-4.268 nA	1.1794 nA
IIH_Inputs_Max_	Bi_D_6	1.3408 nA	921.5446 pA	-2.0134 nA	1.5505 nA	-336.288 pA	-126.65 pA
IIH_Inputs_Max_	Bi_D_7	2.1223 nA	-2.0619 nA	-597.425 pA	-179.006 pA	1.9131 nA	2.5407 nA
IIH_Inputs_Max_	Bi_E_1	-3.3171 nA	-1.8527 nA	-1.4343 nA	-1.4343 nA	1.0763 nA	30.204 pA
IIH_Inputs_Max_	Bi_E_2	-597.425 pA	30.204 pA	-1.0158 nA	-1.8527 nA	-3.5264 nA	-1.2251 nA
IIH_Inputs_Max_	Bi_E_3	-1.0158 nA	30.204 pA	-597.425 pA	-597.425 pA	239.413 pA	-2.6895 nA
IIH_Inputs_Max_	Bi_E_4	-3.5264 nA	-3.3171 nA	1.0763 nA	-597.425 pA	448.623 pA	1.2855 nA
IIH_Inputs_Max_	Bi_E_5	-1.4343 nA	30.204 pA	-3.7356 nA	-597.425 pA	-2.8987 nA	-1.6435 nA
IIH_Inputs_Max_	Bi_E_6	-3.3171 nA	-806.634 pA	1.9131 nA	30.204 pA	-179.006 pA	-4.3632 nA
IIH_Inputs_Max_	Bi_E_7	3.3776 nA	30.204 pA	-2.0619 nA	448.6232 pA	-2.6895 nA	30.204 pA
IIH_Inputs_Max_	DA	-1.1277 nA	-1.5468 nA	-79.9676 pA	-499.066 pA	-289.517 pA	-2.1755 nA
IIH_Inputs_Max_	DIO_IN_1	8.0493 nA	-3.2712 nA	-2.0134 nA	-3.6905 nA	13.9191 nA	-1.8038 nA
IIH_Inputs_Max_	DIO_IN_2	-1.9659 nA	-3.6423 nA	129.581 pA	-4.8996 nA	5.5779 nA	-5.3187 nA
IIH_Inputs_Max_	DIO_IN_3	-1.7564 nA	-4.69 nA	-1.7564 nA	-3.4328 nA	-499.066 pA	-5.1091 nA
IIH_Inputs_Max_	DIO_IN_4	-3.4809 nA	-1.8038 nA	-1.5941 nA	-1.8038 nA	-1.1748 nA	-6.6255 nA
IIH_Inputs_Max_	DIO_IN_5	-289.517 pA	-4.4805 nA	-3.2232 nA	-3.0137 nA	-5.1091 nA	-2.385 nA
IIH_Inputs_Max_	DIO_IN_6	-4.69 nA	-4.4805 nA	-2.385 nA	-5.7378 nA	-3.6423 nA	-4.4805 nA
IIH_Inputs_Max_	DIO_IN_7	-708.615 pA	-8.0428 nA	129.581 pA	-3.2232 nA	8.5115 nA	-4.4805 nA
IIH_Inputs_Max_	DIO_IP_1	-4.1098 nA	-3.4809 nA	-4.1098 nA	-965.204 pA	502.267 pA	-4.7387 nA
IIH_Inputs_Max_	DIO_IP_2	-4.8996 nA	-5.1091 nA	-1.5468 nA	-4.271 nA	548.679 pA	-5.5282 nA
IIH_Inputs_Max_	DIO_IP_3	-965.204 pA	-1.5941 nA	-126.649 pA	-5.158 nA	-2.4327 nA	-5.3676 nA
IIH_Inputs_Max_	DIO_IP_4	3.9015 nA	-4.8996 nA	-1.7564 nA	-5.3187 nA	339.130 pA	-5.3187 nA
IIH_Inputs_Max_	DIO_IP_5	-4.271 nA	-5.9473 nA	-2.8041 nA	-7.4142 nA	-4.69 nA	-3.6423 nA
IIH_Inputs_Max_	DIO_IP_6	8.0925 nA	-3.2232 nA	-2.8041 nA	-7.2046 nA	12.9121 nA	-7.2046 nA
IIH_Inputs_Max_	DIO_IP_7	-1.3373 nA	-5.1091 nA	-708.615 pA	-5.9473 nA	19.6177 nA	-2.8041 nA
IIH_Inputs_Max_	EN8	-3.2232 nA	-1.3373 nA	-4.69 nA	-4.0614 nA	-4.271 nA	-5.1091 nA
IIH_Inputs_Max_	HCLK1P	-4.7816 nA	1.7039 nA	-1.8527 nA	1.2855 nA	-3.1079 nA	-1.4343 nA
IIH_Inputs_Max_	HCLK2P	-7.0447 nA	-3.6905 nA	-4.5291 nA	-6.2062 nA	-4.7387 nA	-6.6255 nA
IIH_Inputs_Max_	HCLK3P	-1.0213 nA	-2.0685 nA	-1.0213 nA	-2.6968 nA	654.162 pA	-2.0685 nA
IIH_Inputs_Max_	HCLK4P	969.907 pA	-2.1728 nA	-3.6394 nA	-2.8014 nA	2.8555 nA	1.3889 nA
IIH_Inputs_Max_	IO_I_1	-4.5291 nA	-5.3676 nA	2.5987 nA	-2.6423 nA	-8.3026 nA	-2.223 nA
IIH_Inputs_Max_	IO_I_2	235.293 pA	-602.445 pA	-1.6496 nA	235.2933 pA	-2.0685 nA	1.073 nA
IIH_Inputs_Max_	IO_I_3	-965.204 pA	-2.6423 nA	-4.1098 nA	-2.4327 nA	-3.4809 nA	-4.3194 nA
IIH_Inputs_Max_	IO_I_4	-1.4402 nA	-1.6496 nA	-183.576 pA	863.597 pA	-602.445 pA	863.6 pA
IIH_Inputs_Max_	IO_I_5	-1.8038 nA	-1.3845 nA	-2.852 nA	-4.7387 nA	-9.1411 nA	-965.2 pA
IIH_Inputs_Max_	IO_I_6	-7.2046 nA	-4.271 nA	-1.1277 nA	-1.5468 nA	-3.0137 nA	4.3381 nA
IIH_Inputs_Max_	LOADIN	-474.54 pA	153.1952 pA	1.1994 nA	3.0826 nA	2.6641 nA	-5.9965 nA
IIH_Inputs_Max_	RCLK1P	-4.5291 nA	-2.223 nA	-2.6423 nA	-5.3676 nA	502.267 pA	-2.3823 nA
IIH_Inputs_Max_	RCLK2P	550.876 pA	-1.9633 nA	-1.7538 nA	-1.9633 nA	-1.5443 nA	-183.58 pA
IIH_Inputs_Max_	RCLK3P	-1.0213 nA	-2.4874 nA	-2.2779 nA	-1.8591 nA	-602.445 pA	2.7499 nA
IIH_Inputs_Max_	RCLK4P	-4.5724 nA	-3.1079 nA	-1.0158 nA	448.6232 pA	-597.425 pA	-1.9659 nA

Table 6b I_{IH} data

DUT		6613				6615			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIH_Inputs_Max_	Bi_D_1	2.1202	nA	4.424	nA	1.7013	nA	2.9579	nA
IIH_Inputs_Max_	Bi_D_2	1.073	nA	4.424	nA	-602.445	pA	444.728	pA
IIH_Inputs_Max_	Bi_D_3	-183.576	pA	-811.88	pA	3.1674	nA	444.728	pA
IIH_Inputs_Max_	Bi_D_4	-915.735	pA	-1.1253	nA	3.0651	nA	2.0175	nA
IIH_Inputs_Max_	Bi_D_5	1.808	nA	1.3889	nA	-3.6394	nA	341.36	pA
IIH_Inputs_Max_	Bi_D_6	-2.852	nA	292.6283	pA	-1.3845	nA	-545.927	pA
IIH_Inputs_Max_	Bi_D_7	1.9131	nA	2.9591	nA	-1.6435	nA	2.5407	nA
IIH_Inputs_Max_	Bi_E_1	-1.8527	nA	1.9131	nA	-3.3171	nA	2.3315	nA
IIH_Inputs_Max_	Bi_E_2	239.414	pA	867.0423	pA	239.413	pA	867.042	pA
IIH_Inputs_Max_	Bi_E_3	-2.2711	nA	239.4136	pA	-806.634	pA	-1.0158	nA
IIH_Inputs_Max_	Bi_E_4	657.833	pA	-2.6895	nA	867.042	pA	2.3315	nA
IIH_Inputs_Max_	Bi_E_5	-806.634	pA	-388.215	pA	-3.1079	nA	-1.6435	nA
IIH_Inputs_Max_	Bi_E_6	-4.5724	nA	-597.425	pA	-3.1079	nA	-3.5264	nA
IIH_Inputs_Max_	Bi_E_7	-2.4803	nA	448.6232	pA	-2.0619	nA	-3.7356	nA
IIH_Inputs_Max_	DA	-10.5574	nA	-499.066	pA	758.229	pA	-2.1755	nA
IIH_Inputs_Max_	DIO_IN_1	13.2902	nA	-2.0134	nA	11.8228	nA	6.3722	nA
IIH_Inputs_Max_	DIO_IN_2	129.581	pA	-2.5946	nA	-79.9676	pA	-499.066	pA
IIH_Inputs_Max_	DIO_IN_3	-1.7564	nA	-2.5946	nA	-4.4805	nA	-3.4328	nA
IIH_Inputs_Max_	DIO_IN_4	4.9047	nA	-2.6423	nA	-1.5941	nA	-4.1098	nA
IIH_Inputs_Max_	DIO_IN_5	-4.4805	nA	-5.5282	nA	-5.5282	nA	-5.7378	nA
IIH_Inputs_Max_	DIO_IN_6	-5.9473	nA	-5.9473	nA	-6.576	nA	-5.5282	nA
IIH_Inputs_Max_	DIO_IN_7	-3.4328	nA	-5.3187	nA	-3.2232	nA	-3.4328	nA
IIH_Inputs_Max_	DIO_IP_1	-4.7387	nA	-4.1098	nA	-4.7387	nA	-5.158	nA
IIH_Inputs_Max_	DIO_IP_2	-8.2524	nA	-5.5282	nA	-16.2153	nA	-6.9951	nA
IIH_Inputs_Max_	DIO_IP_3	-1.8038	nA	-4.7387	nA	-3.6905	nA	-5.5773	nA
IIH_Inputs_Max_	DIO_IP_4	8.7211	nA	-5.9473	nA	-3.0137	nA	-3.6423	nA
IIH_Inputs_Max_	DIO_IP_5	-3.8519	nA	-3.0137	nA	-1.5468	nA	-4.0614	nA
IIH_Inputs_Max_	DIO_IP_6	-4.69	nA	-5.5282	nA	-8.6715	nA	-5.5282	nA
IIH_Inputs_Max_	DIO_IP_7	1.5964	nA	-4.69	nA	-4.69	nA	-3.8519	nA
IIH_Inputs_Max_	EN8	-19.7776	nA	-1.7564	nA	-2.1755	nA	-2.385	nA
IIH_Inputs_Max_	HCLK1P	448.623	pA	239.4136	pA	-597.425	pA	1.2855	nA
IIH_Inputs_Max_	HCLK2P	-4.3194	nA	-4.3194	nA	-755.566	pA	-4.3194	nA
IIH_Inputs_Max_	HCLK3P	-2.6968	nA	-1.6496	nA	863.597	pA	-2.2779	nA
IIH_Inputs_Max_	HCLK4P	-4.0585	nA	-915.735	pA	-4.687	nA	-2.8014	nA
IIH_Inputs_Max_	IO_I_1	-5.9965	nA	-5.5773	nA	-5.5773	nA	-3.2712	nA
IIH_Inputs_Max_	IO_I_2	-811.88	pA	-1.6496	nA	1.073	nA	-602.445	pA
IIH_Inputs_Max_	IO_I_3	2.389	nA	-7.6736	nA	-13.3339	nA	-4.3194	nA
IIH_Inputs_Max_	IO_I_4	863.597	pA	863.597	pA	863.597	pA	-3.1157	nA
IIH_Inputs_Max_	IO_I_5	-5.158	nA	-5.7869	nA	292.628	pA	-545.927	pA
IIH_Inputs_Max_	IO_I_6	-918.164	pA	-1.7564	nA	-1.9659	nA	-2.5946	nA
IIH_Inputs_Max_	LOADIN	2.6641	nA	3.7104	nA	-265.295	pA	990.175	pA
IIH_Inputs_Max_	RCLK1P	-965.204	pA	-5.5773	nA	-2.852	nA	-5.5773	nA
IIH_Inputs_Max_	RCLK2P	-77.6718	pA	-1.7538	nA	-3.6394	nA	-287.188	pA
IIH_Inputs_Max_	RCLK3P	25.8587	pA	863.597	pA	-1.2307	nA	-393.01	pA
IIH_Inputs_Max_	RCLK4P	-2.4803	nA	-2.0619	nA	-3.7356	nA	-1.2251	nA

D. Differential Input 3.3V-LVPECL Threshold Voltage (V_{IL}/V_{IH})

The LVPECL V_{IL}/V_{IH} is measured as the minimum differential voltage applied between P (positive) and N (negative) to generate a stable output Low/High respectively. For V_{IL} the differential is $V_N - V_P$, and for V_{IH} the differential is $V_P - V_N$. The applied common voltage ($\frac{V_P + V_N}{2}$) is 1.8V. Tables 7a and 7b show the pre-irradiation and post-annealing tested data for V_{IL} of seven LVPECL inputs, and tables 8a and 8b show their pre-irradiation and post-annealing tested data for V_{IH}. In every case, pre-irradiation or post-annealing, the tested data pass the spec of 0.3V.

Table 7a V_{IL} of seven LVPECL inputs

DUT		**6609**		**6611**		**6612**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	110	80	115	95	110	85
bi_levels_vil	DIO_IP_6	105	80	110	90	105	75
bi_levels_vil	DIO_IP_5	115	90	120	95	120	95
bi_levels_vil	DIO_IP_4	75	50	90	70	95	70
bi_levels_vil	DIO_IP_3	85	60	90	70	90	65
bi_levels_vil	DIO_IP_2	85	60	90	70	100	75
bi_levels_vil	DIO_IP_1	80	50	70	50	80	55

Table 7b V_{IL} of seven LVPECL inputs

DUT		**6613**		**6615**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	110	95	95	90
bi_levels_vil	DIO_IP_6	110	95	110	105
bi_levels_vil	DIO_IP_5	110	95	105	100
bi_levels_vil	DIO_IP_4	75	60	85	80
bi_levels_vil	DIO_IP_3	95	85	90	85
bi_levels_vil	DIO_IP_2	90	80	90	85
bi_levels_vil	DIO_IP_1	70	65	75	55

Actel

Table 8a V_{IH} of seven LVPECL inputs

DUT		**6609**		**6611**		**6612**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	105	75	110	90	105	80
bi_levels_vih	DIO_IP_6	100	75	105	85	100	70
bi_levels_vih	DIO_IP_5	110	85	115	90	115	90
bi_levels_vih	DIO_IP_4	70	45	85	65	90	65
bi_levels_vih	DIO_IP_3	85	60	85	65	90	60
bi_levels_vih	DIO_IP_2	80	55	85	65	95	75
bi_levels_vih	DIO_IP_1	85	55	80	60	80	65

Table 8b V_{IH} of seven LVPECL inputs

DUT		**6613**		**6615**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	105	90	100	85
bi_levels_vih	DIO_IP_6	105	90	115	100
bi_levels_vih	DIO_IP_5	105	90	110	95
bi_levels_vih	DIO_IP_4	70	55	90	75
bi_levels_vih	DIO_IP_3	90	80	95	80
bi_levels_vih	DIO_IP_2	85	75	95	80
bi_levels_vih	DIO_IP_1	80	65	70	65

E. 3.3V-LVTTL Output-Drive Voltage (V_{OL}/V_{OH})

The output drive voltage V_{OL}/V_{OH} is measured at an output pin when it is at Low/High state and sinking/sourcing 24 mA current respectively. The spec for V_{OL}/V_{OH} is < 0.4V/ >2.4V respectively. Table 9a and 9b show the pre-irradiation and post-annealing tested data for V_{OL}; in every case the V_{OL} data passes the spec. Table 10a and 10b show the pre-irradiation and post-annealing tested data for V_{OH}; in every case the V_{OH} data passes the spec.

Table 9a 3.3V LVTTL V_{OL}

DUT		**6609**		**6611**		**6612**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	QA_0	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_2	20	20	20	20	20	20

Table 9b 3.3V LVTTL V_{OL}

DUT		**6613**		**6615**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	QA_0	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20
bi_levels_vol	QA_2	20	20	20	20

Table 10a 3.3V LVTTL V_{OH}

DUT		**6609**		**6611**		**6612**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	QA_0	2.98	2.975	2.985	2.97	2.985	2.975
bi_levels_voh	QA_1	2.98	2.98	2.985	2.98	2.99	2.97
bi_levels_voh	QA_2	2.98	2.98	2.98	2.98	2.98	2.975

Table 10b 3.3V LVTTL V_{OH}

DUT		**6613**		**6615**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	QA_0	2.99	2.98	2.99	2.98
bi_levels_voh	QA_1	2.99	2.97	2.98	2.98
bi_levels_voh	QA_2	2.98	2.98	2.98	2.98

F. Propagation Delay

The propagation delay spec for TID testing is defined as ±10% degradation. Table 11 lists the pre-irradiation and post-annealing propagation delays. Every DUT passes the test.

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose krad(SiO_2)	Pre-Irradiation (μs)	Post-Annealing (μs)	Degradation (%)
6609	300	2.5221	2.4946	-1.09%
6611	300	2.60865	2.5855	-0.89%
6612	300	2.55845	2.5355	-0.90%
6613	200	2.494	2.4627	-1.26%
6615	200	2.73945	2.7126	-0.98%

G. *Transition Time*

Figures 8 to 17 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

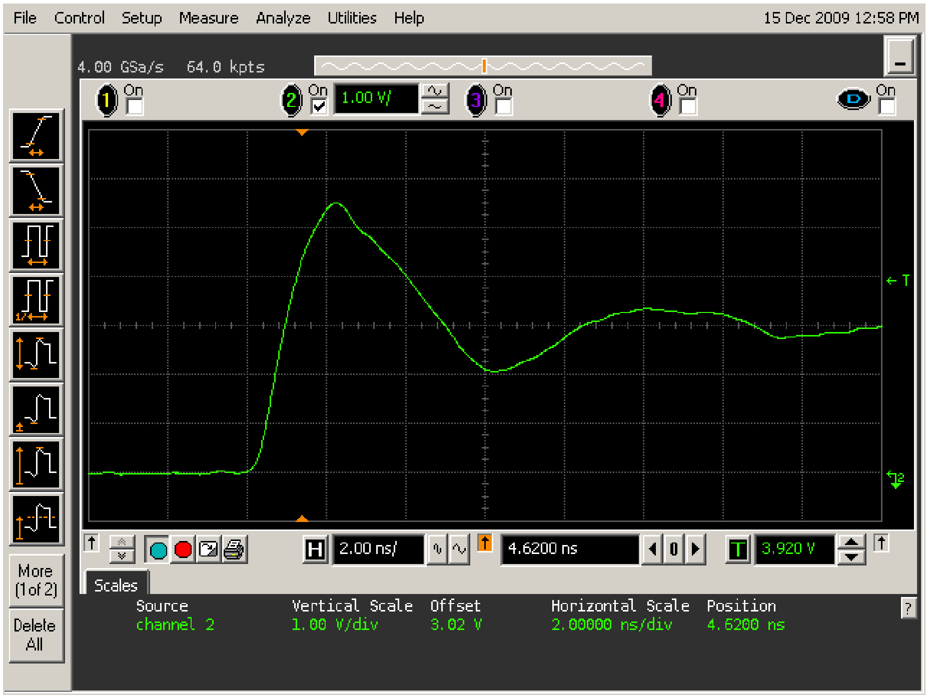

Figure 8(a) DUT 6609 pre-irradiation rising edge.

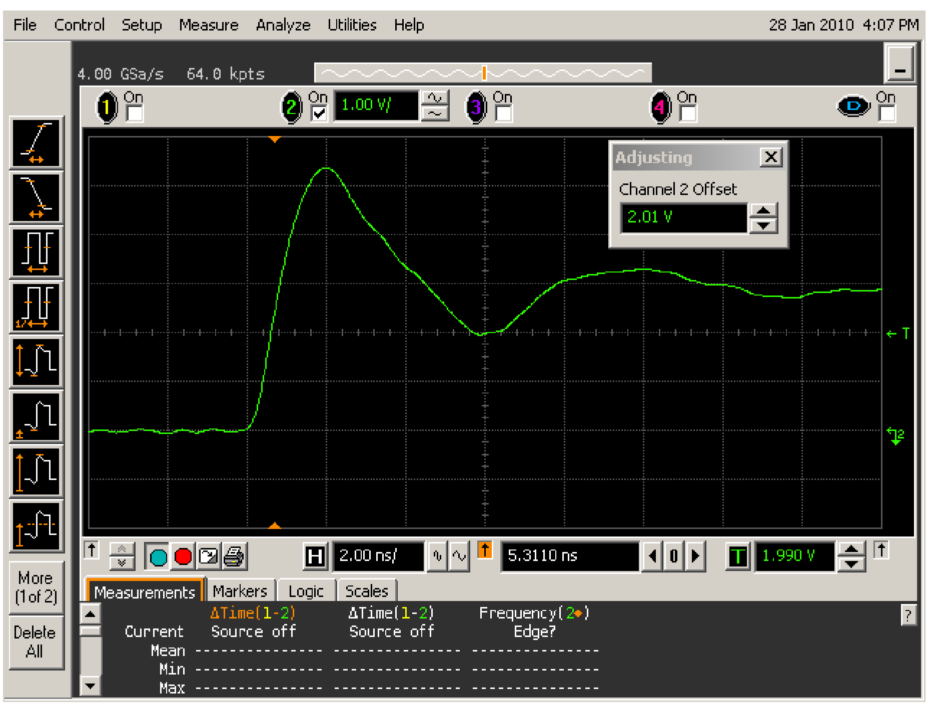

Figure 8(b) DUT 6609 post-annealing rising edge.

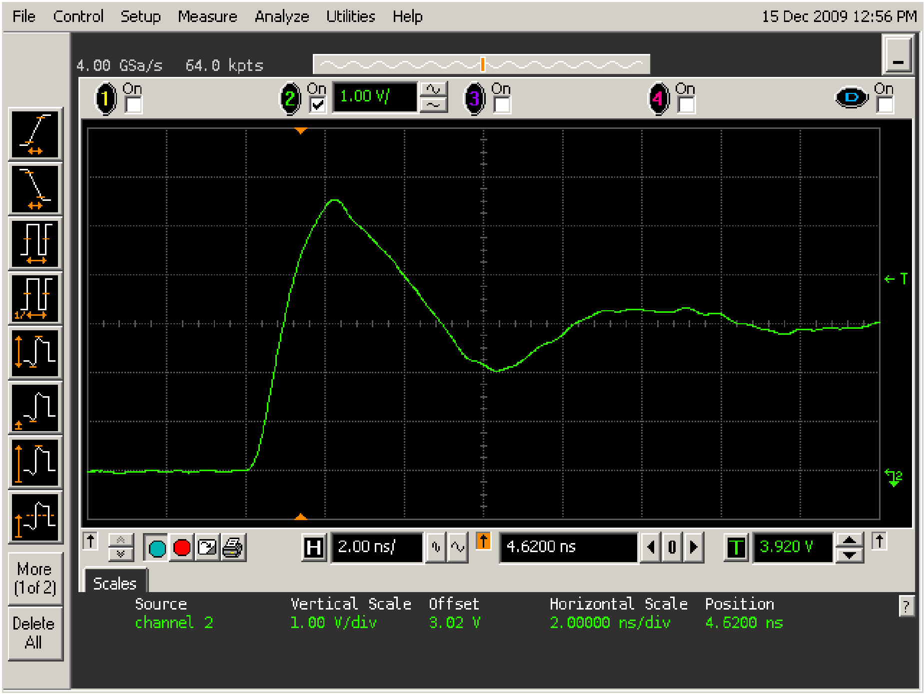

Figure 9(a) DUT 6611 pre-irradiation rising edge.

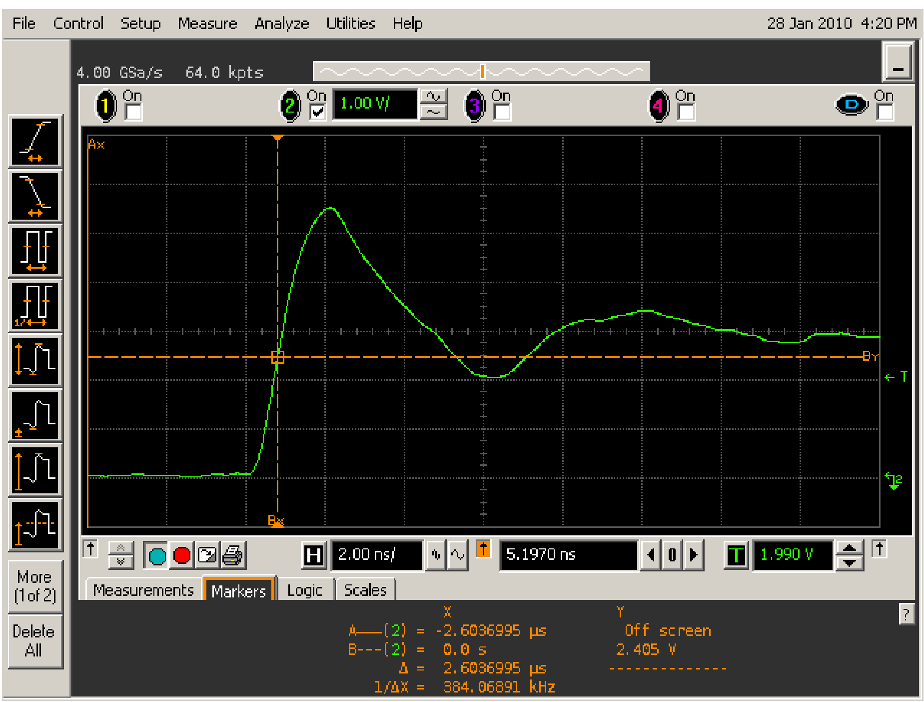

Figure 9(b) DUT 6611 post-annealing rising edge.

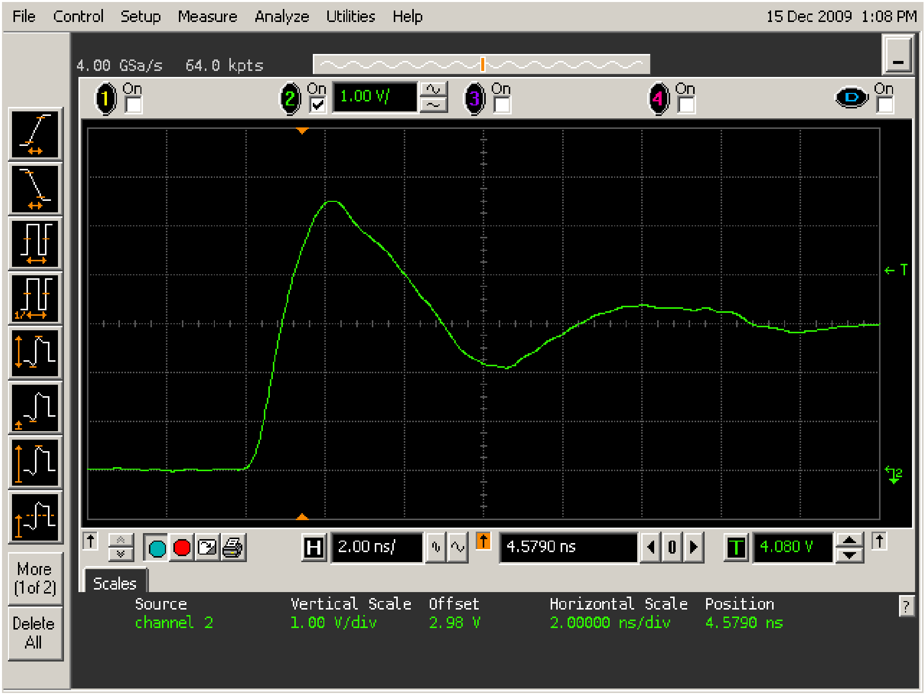

Figure 10(a) DUT 6612 pre-radiation rising edge.

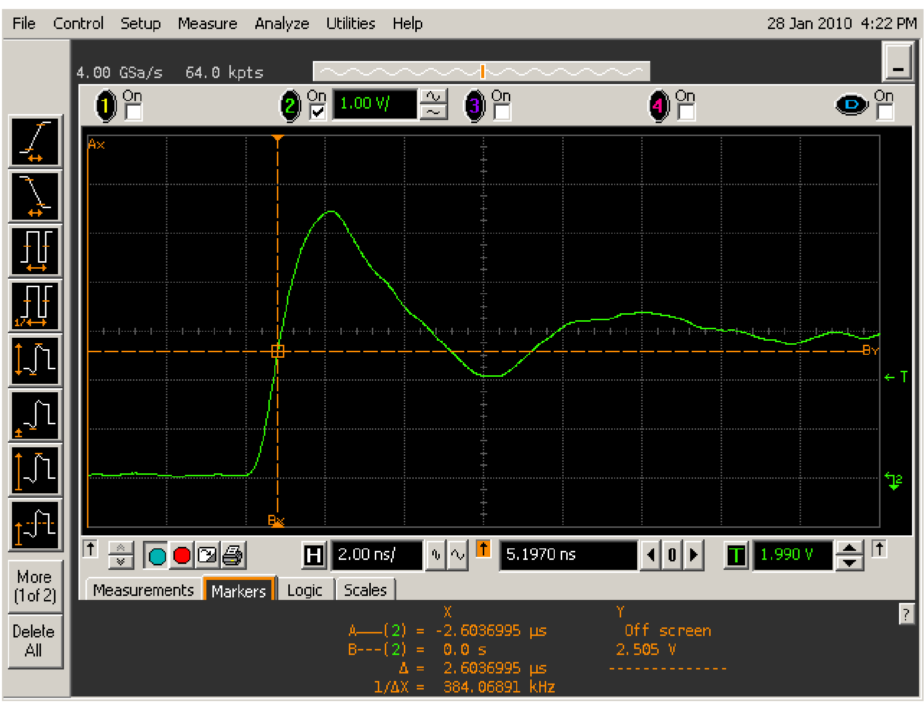

Figure 10(b) DUT 6612 post-annealing rising edge.

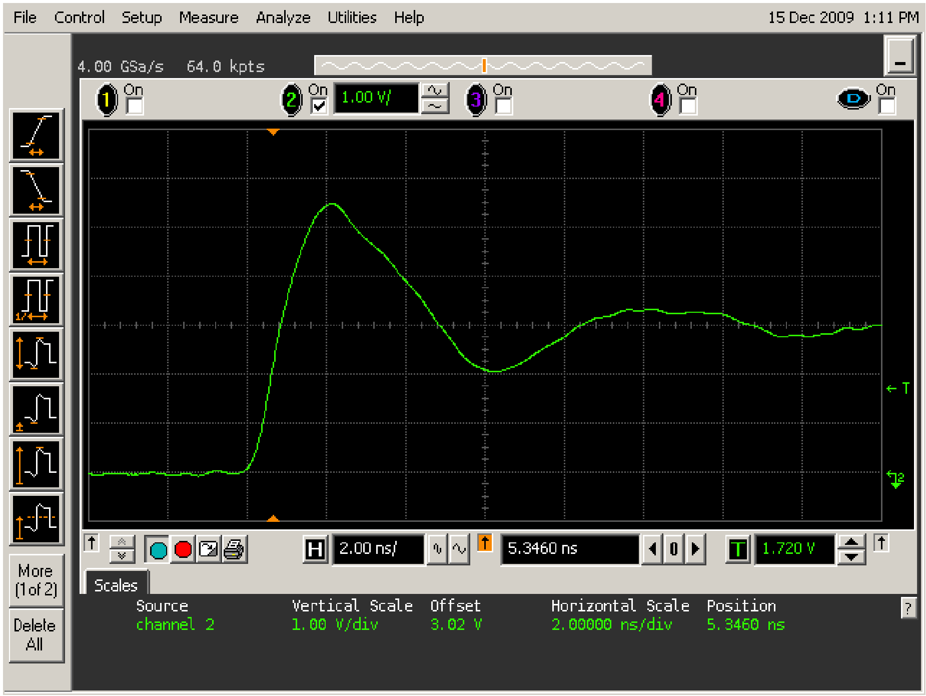

Figure 11(a) DUT 6613 pre-irradiation rising edge.

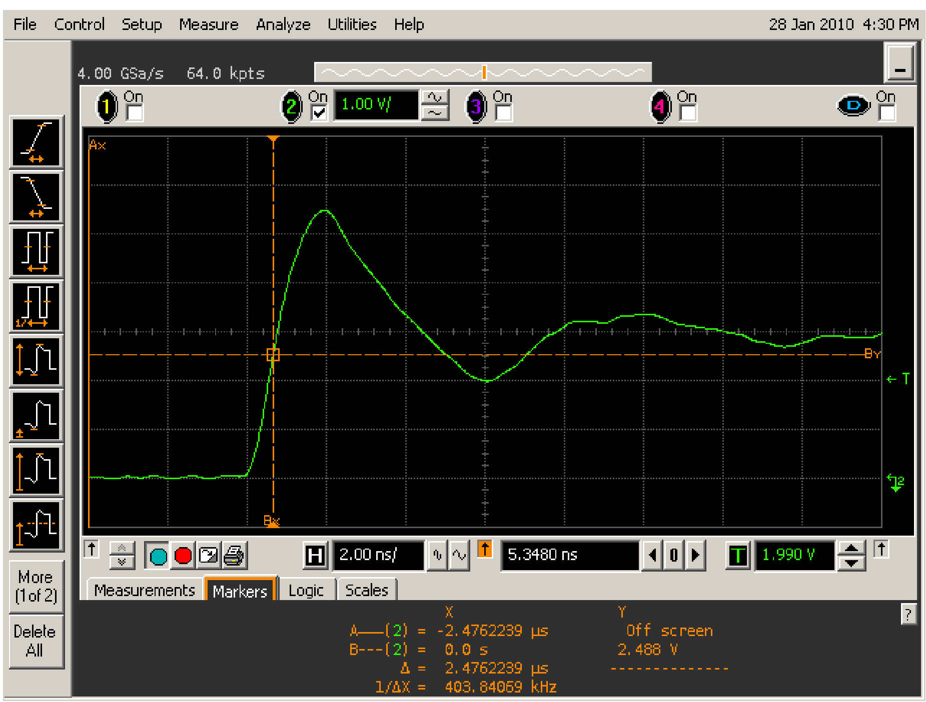

Figure 11(b) DUT 6613 post-annealing rising edge.

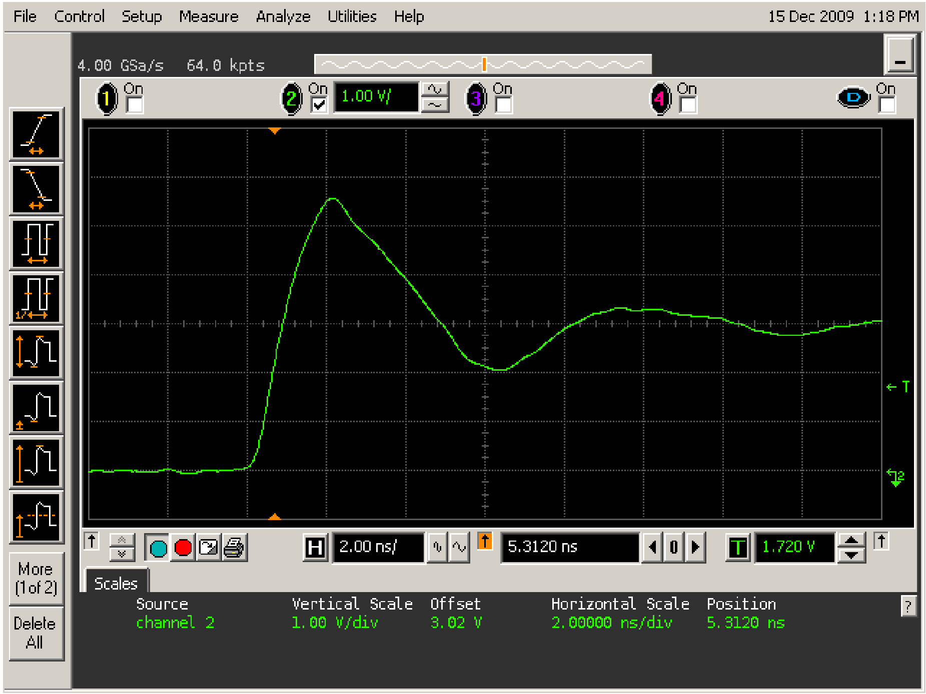

Figure 12(a) DUT 6615 pre-irradiation rising edge.

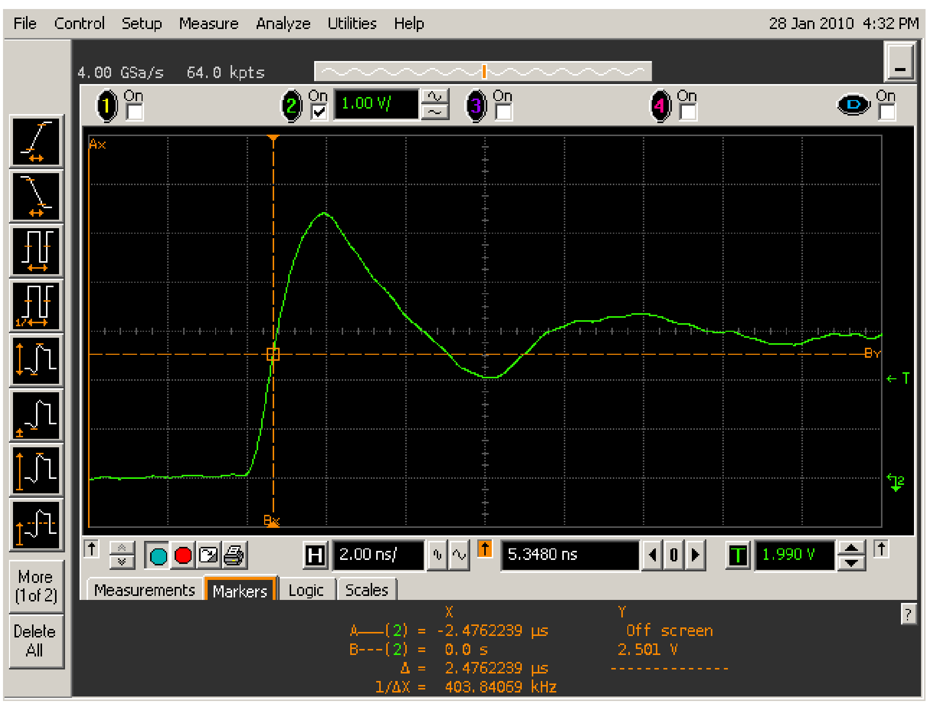

Figure 12(b) DUT 6615 post-annealing rising edge.

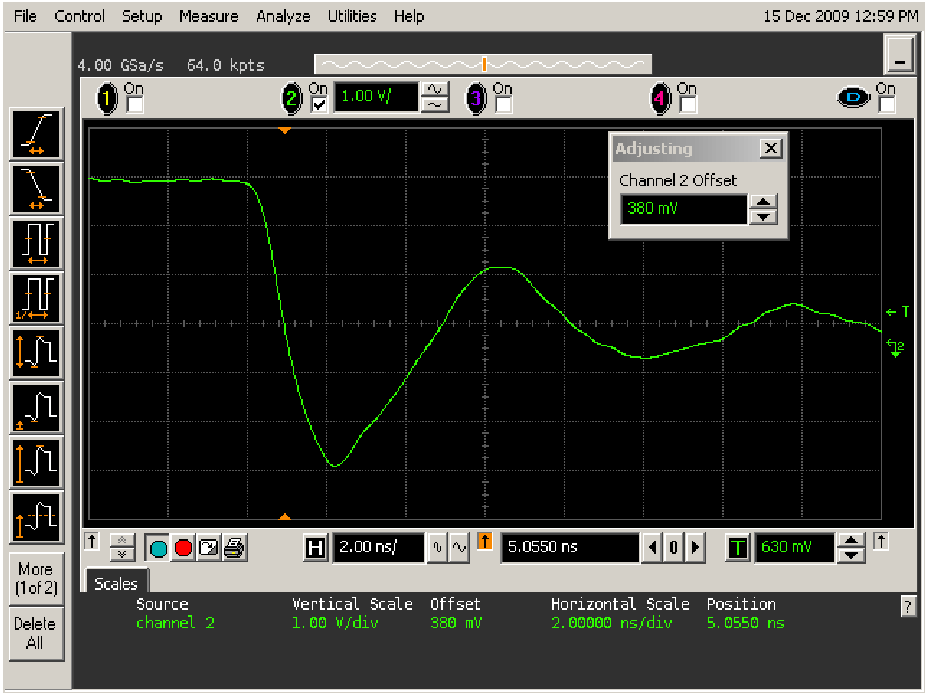

Figure 13(a) DUT 6609 pre-irradiation falling edge.

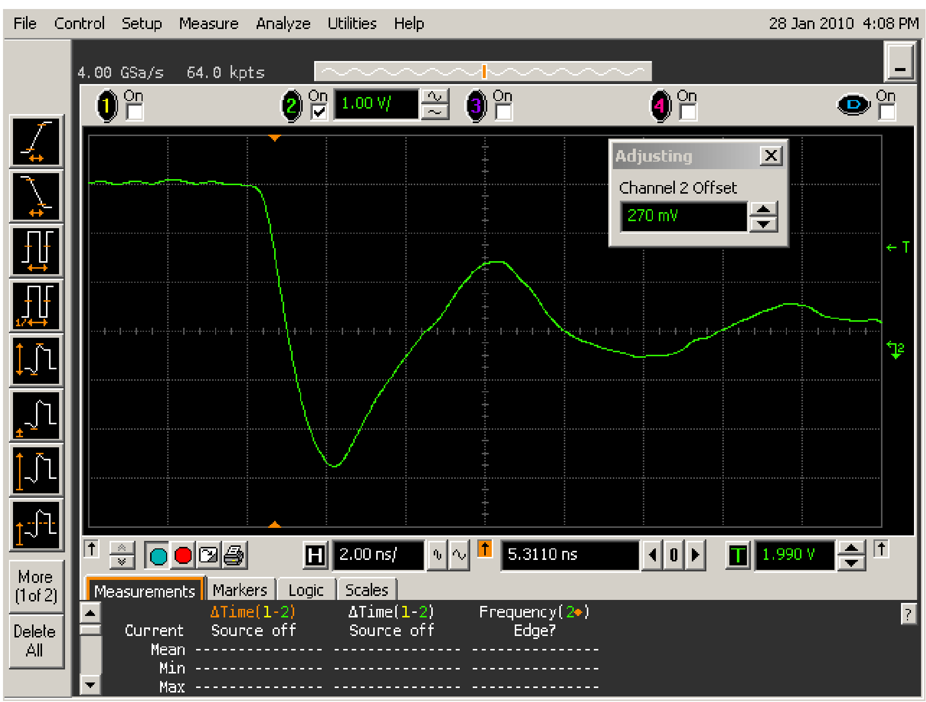

Figure 13(b) DUT 6609 post-annealing falling edge.

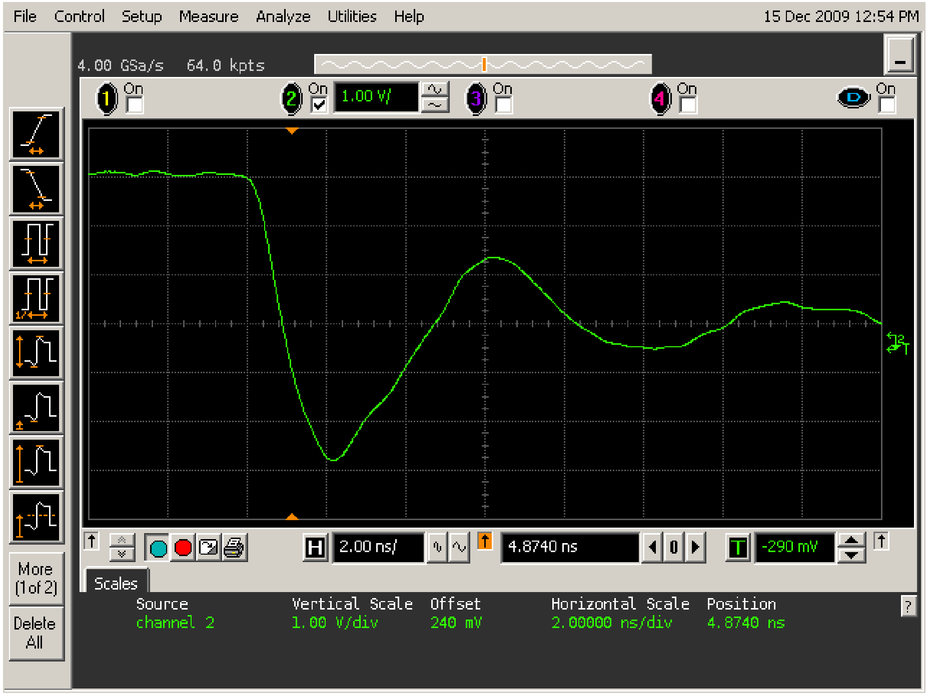

Figure 14(a) DUT 6611 pre-irradiation falling edge.

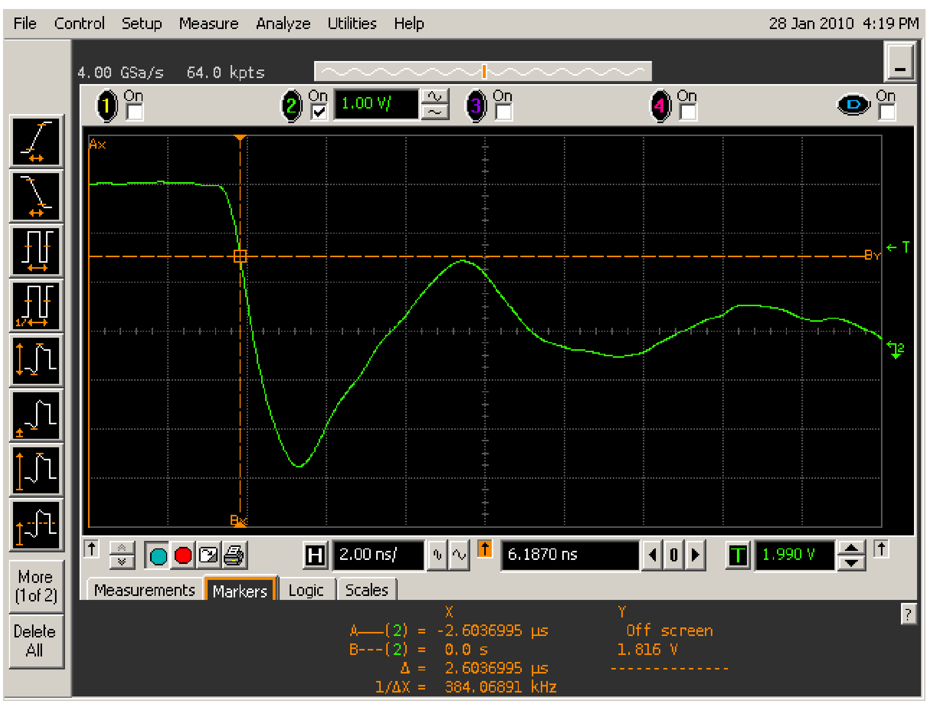

Figure 14(b) DUT 6611 post-annealing falling edge.

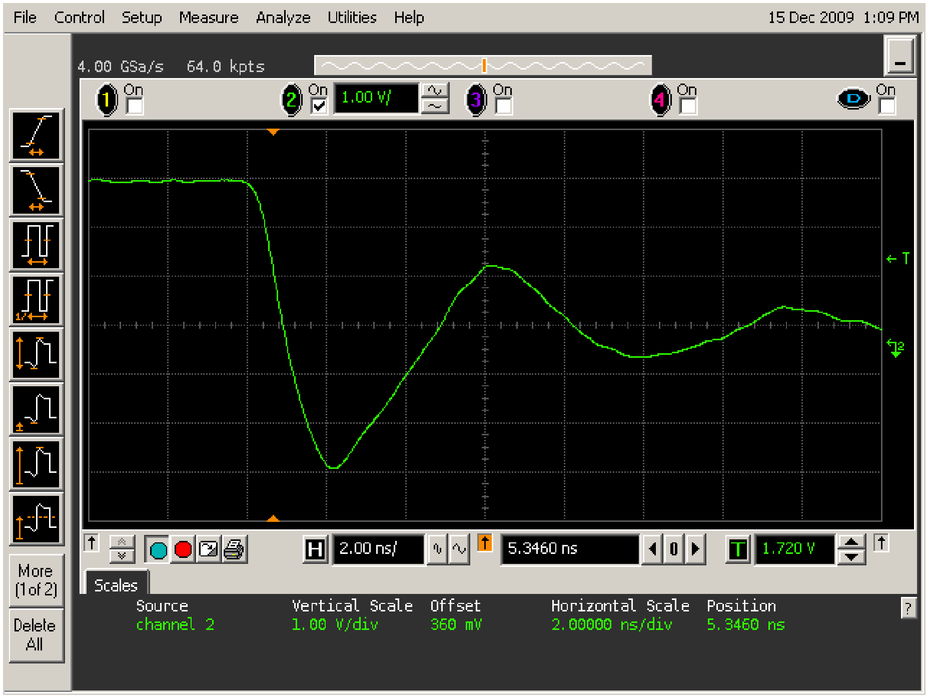

Figure 15(a) DUT 6612 pre-irradiation falling edge.

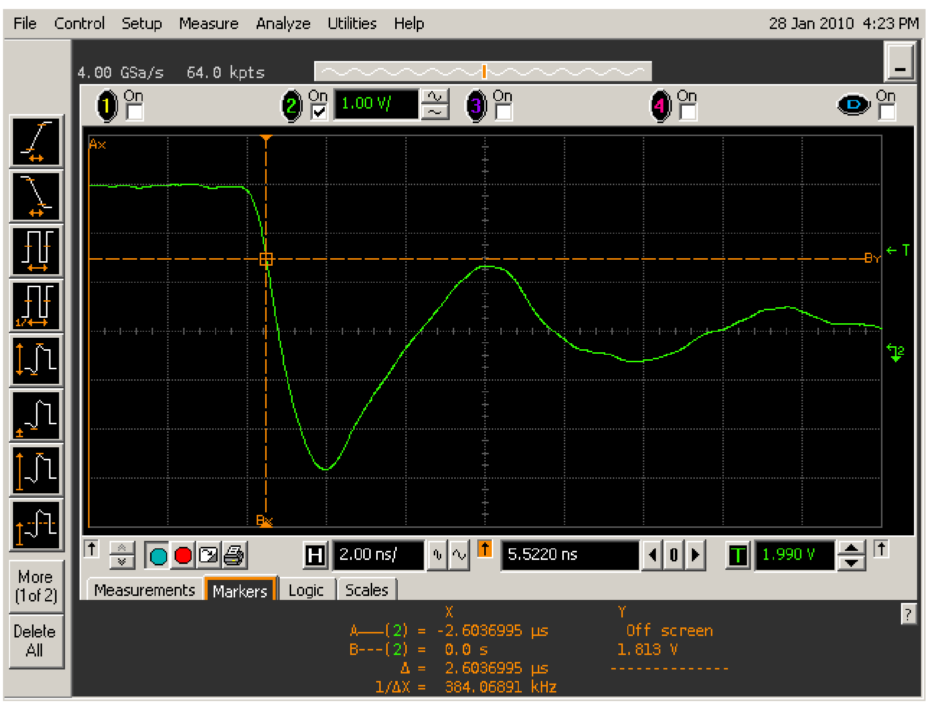

Figure 15(b) DUT 6612 post-annealing falling edge.

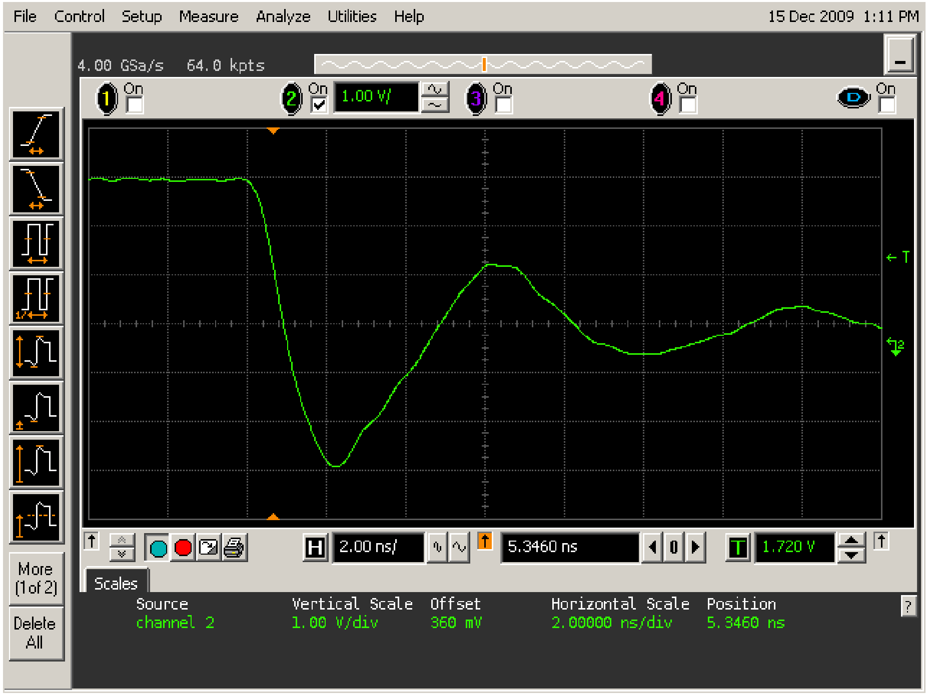

Figure 16(a) DUT 6613 pre-irradiation falling edge.

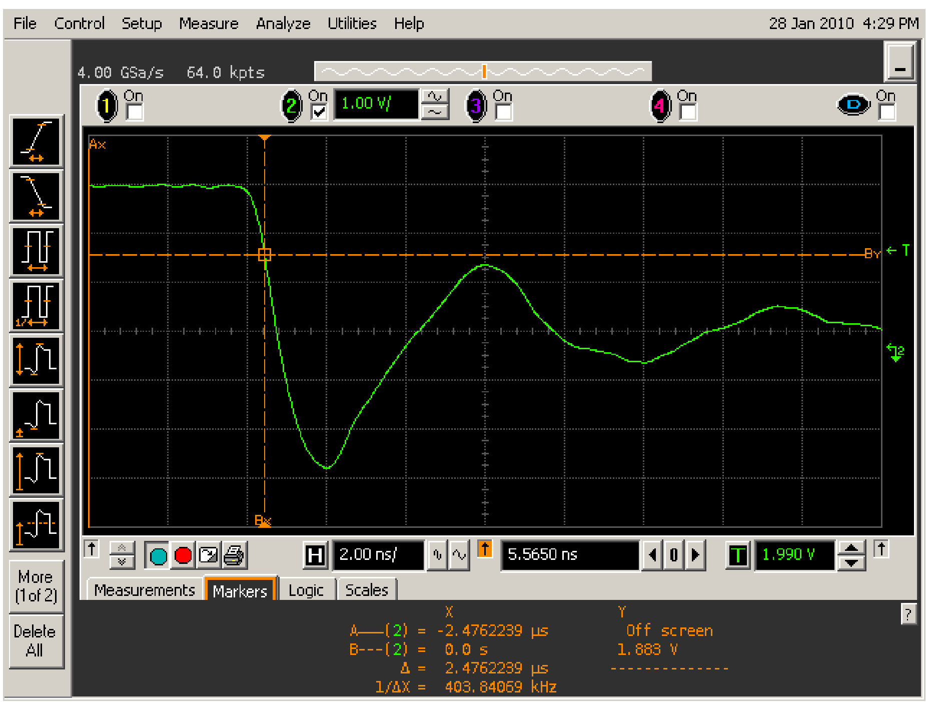

Figure 16(b) DUT 6613 post-annealing falling edge.

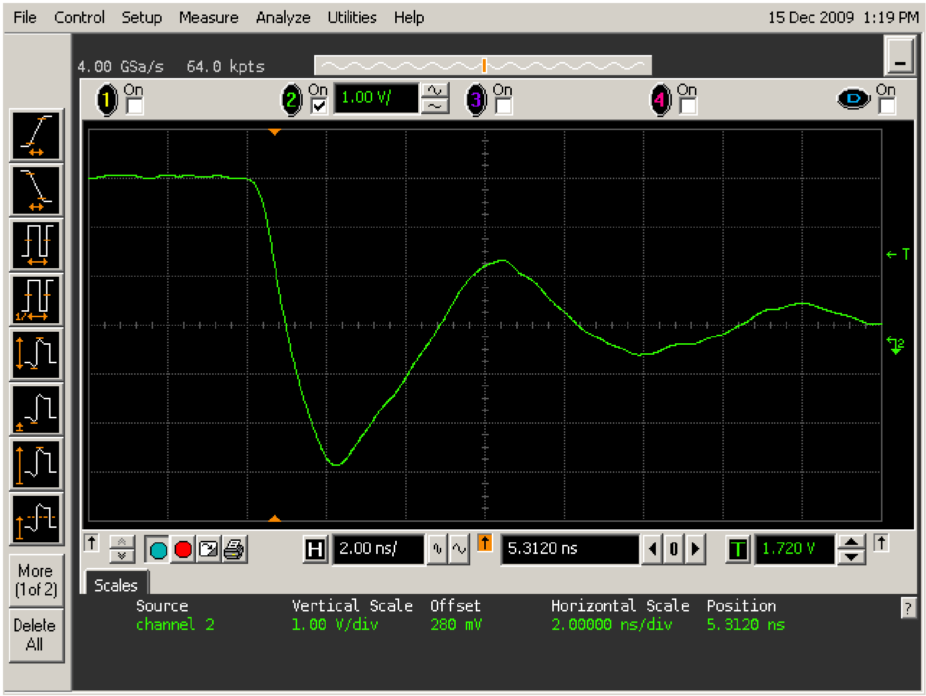

Figure 17(a) DUT 6615 pre-irradiation falling edge.

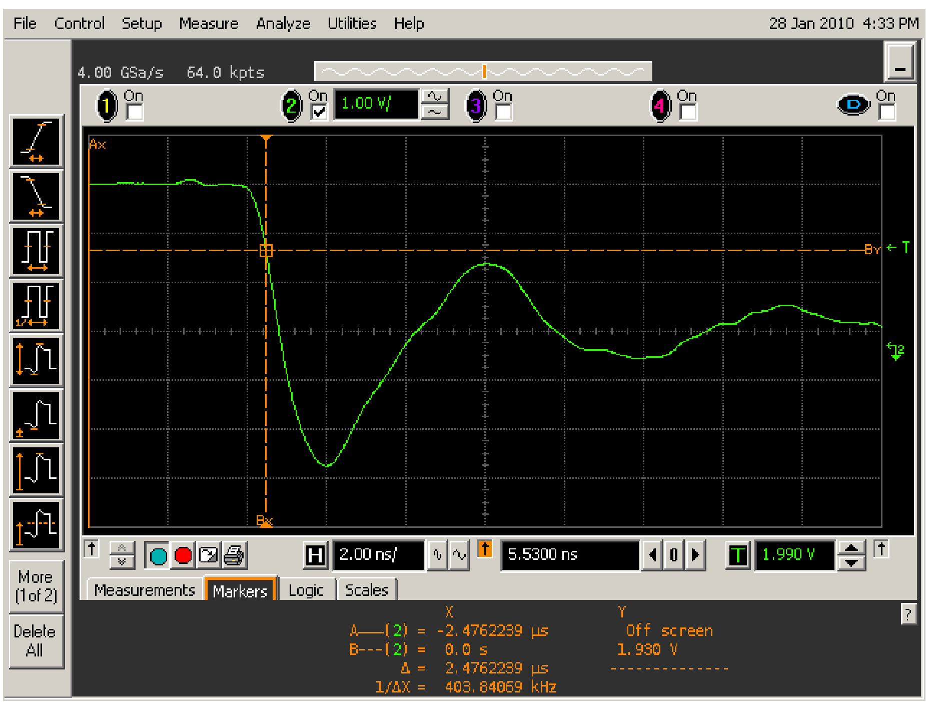

Figure 17(b) DUT 6615 post-annealing falling edge.