TOTAL IONIZING DOSE TEST REPORT

No. 08T-RTAX2000S-D32R41
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I. SUMMARY TABLE

Table 1 summarizes the TID tolerance for each tested parameters. The overall tolerance is limited by the standby power-supply current (I_{CC}). Because of logistical limitations, the room temperature annealing allowed by 1019.6 to anneal down I_{CC} is performed only for approximately 10 days, which is only enough to anneal down the I_{CC} to pass the spec for DUTs irradiated to 200 krad(SiO_2) but not for DUTs irradiated to 300 krad(SiO_2). Otherwise, every DUT passes the major specs listed in the table for 300 krad(SiO_2).

Table 1 Tolerances for each tested parameter

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 200 krad(SiO_2)
3. Input Switching Threshold (V_{IHL}/V_{ILH})	Passed 300 krad(SiO_2)
4. Output Threshold (V_{OL}/V_{OH})	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes device under test (DUT), irradiation facility and parameters, test method, test design, and electrical parameter measurements. This TID testing, in various slightly modified forms, had been used to accumulate an extensive TID database for many generations of antifuse-based FPGAs; the link to access this TID database is attached in below:

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

The part name of the DUTs is RTAX2000S; the package is CG624. UMC used 0.15 µm technologies to manufacture it. The particular lot is numbered D32R41.

The Gamma Irradiator in radiation facility of Defense Microelectronics Activity is used to irradiate DUTs with Gamma rays: number 7152 and number 7166 are irradiated to 200 krad(SiO_2); number 7087, number 7089, and number 7133 are irradiated to 300 krad(SiO_2). The dose rate is constant at 5 krad(SiO_2)/min, and the environment is kept at 25°C.

B. Test Method

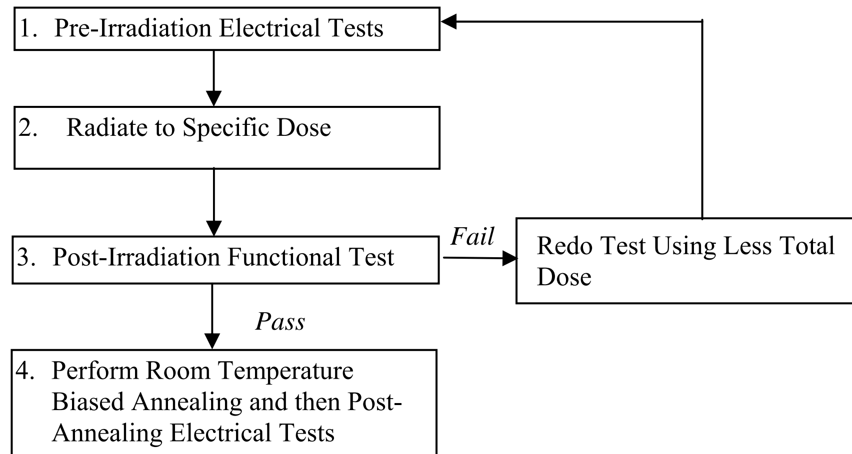

Figure 1 Parametric test flow chart

The test method is based on the military standard TM1019.6. Figure 1 shows the test flow. During irradiation, the DUT is statically biased with V_{CCI}/V_{CCA} = 3.3V/1.5V and all the inputs grounded. The accelerated annealing test in TM1019.6, section 3.12 has been done on samples of RTAXS product, and the results show that post-irradiation annealing recovers the electrical characteristics rather than adversely affects the electrical performance. This is consistent with the general belief that the dominant TID effects in deep submicron CMOS devices are due to hole-rapping-in-field-oxide induced leakage currents and these leakages decreases with annealing temperatures. For a lot testing such as the one in this report, the accelerated annealing test is omitted because it has been proven by the above information that the annealing effect is not adverse.

TM1019.6, Section 3.11 "extended room temperature anneal test" has been applied for approximately 10-days of annealing. The data measured after this annealing is termed "Post Annealing" in section III Test Results.

C. DUT Logic Design

The DUT design, named rtax2000_CG624_Top, is a high utilization and generic design. Figure 2 shows the block diagram of the design, and its Verilog file (rtax2000_CG624_Top.v) is in the aforementioned link. The functional test is performed on every sub-design with inputs and outputs; most inputs, including global clocks, are tested for threshold voltage and leakage current; the standby I_{CC} test includes measuring static IO current (I_{CCI}) and static logic array current (I_{CCA}). Except propagation delay and the transition characteristic, which are measured on bench from the output pin O_BS, all other parameter measurements are performed on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench by measuring the expected outputs from shift registers and long buffer string (sub-design 5 and 6 described in the following).

Sub-design 1 Embedded SRAM

This is to test the function of the embedded RAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

Sub-design 2 Unidirectional LVTTL Inputs and Outputs

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

Sub-design 3 Bidirectional 3.3V-LVTTL IO

This is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for testing.

Sub-design 4 3.3V-LVPECL Input

This is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst possible differential input standard. There are 7 channels.

Sub-design 5 Shift Registers

This is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and each of the other three has 2,048 bits.

Sub-design 6 Long Buffer String

This is to measure the radiation effects on the propagation delay. A clock signal feeding a toggle flip-flop generates a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge and the output switching at the end of the buffer string due to this clock edge is defined as propagation delay, which can be high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the total-dose tolerance. The total dose to cause 10% of propagation degradation is considered as the critical tolerance.

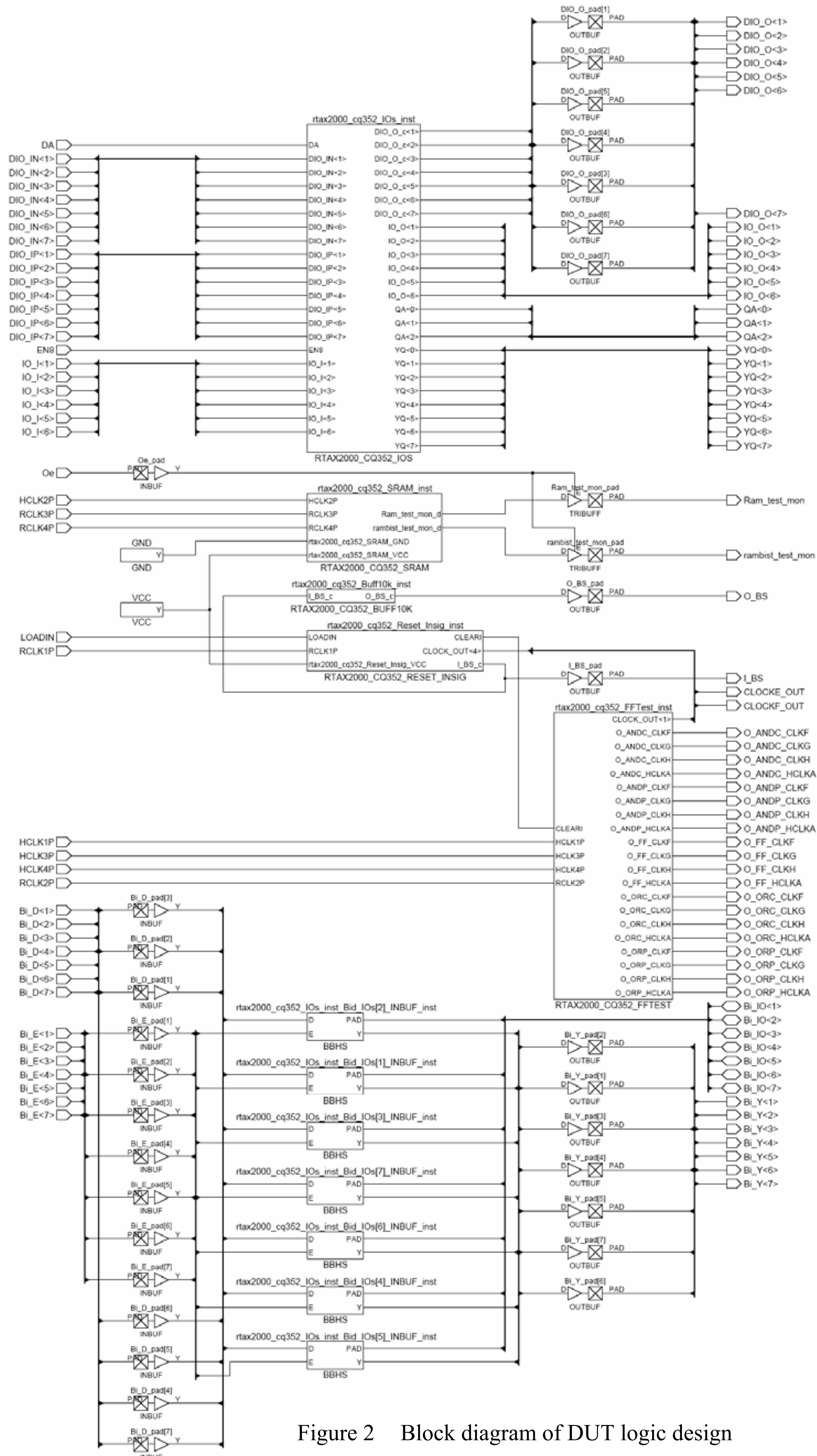

Figure 2 Block diagram of DUT logic design

III. TEST RESULTS

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing. As mentioned previously, right after the irradiation and before annealing only the functionality of shift registers and long buffer string were tested on bench.

A. *Functional Test*

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester. Every DUT also passed post-irradiation and pre-annealing functional tests of the shift registers and buffer string by using a bench setup.

B. *Standby Power Supply Current (I_{CCA} and I_{CCI})*

The logic-array power supply, V_{CCA}, is 1.5V, and the IO power supply, V_{CCI}, is 3.3V. Their standby currents, I_{CCA} and I_{CCI}, are monitored in-flux; Figure 3-8 show the plots of I_{CCA} and I_{CCI} versus total dose for the DUTs.

Referring to TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} should be defined as the addition of highest I_{CCI}, I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS spec sheet in the document posted on the Actel website; the link is attached in below:

http://www.actel.com/documents/RTAXS_DS.pdf

Therefor, the PIPL for I_{CCA} is 500 mA, and the PIPL of I_{CCI} is 35+10+3.13×7 = 66.91(mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation—right after irradiation and before annealing, and post-annealing I_{CCA} and I_{CCI} data: the post-annealing I_{CCA} of every DUT, either irradiated to 200 krad(SiO_2) or 300 krad(SiO_2) is below the PIPL; the post-annealing I_{CCI} of every DUT irradiated to 200 krad(SiO_2) is below the PIPL; but the post-annealing I_{CCI} of every DUT irradiated to 300 krad(SiO_2) exceed the PIPL.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing I_{CCA} and I_{CCI}

DUT	Total Dose krad (SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
7087	300	3	39	3	24	293	124
7089	300	5	40	4	23	287	133
7133	300	5	39	3	23	297	128
7152	200	3	5	3	24	94	39
7166	200	2	3	1	23	111	45

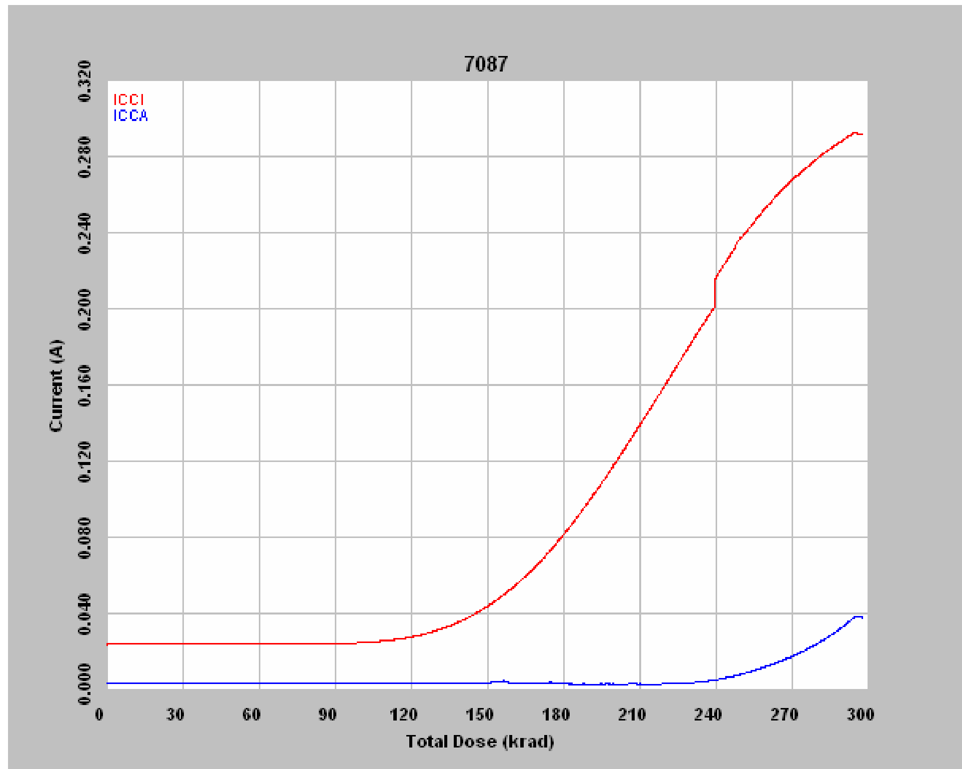

Figure 3 DUT 7087 in-flux I_{CCA} and I_{CCI}.

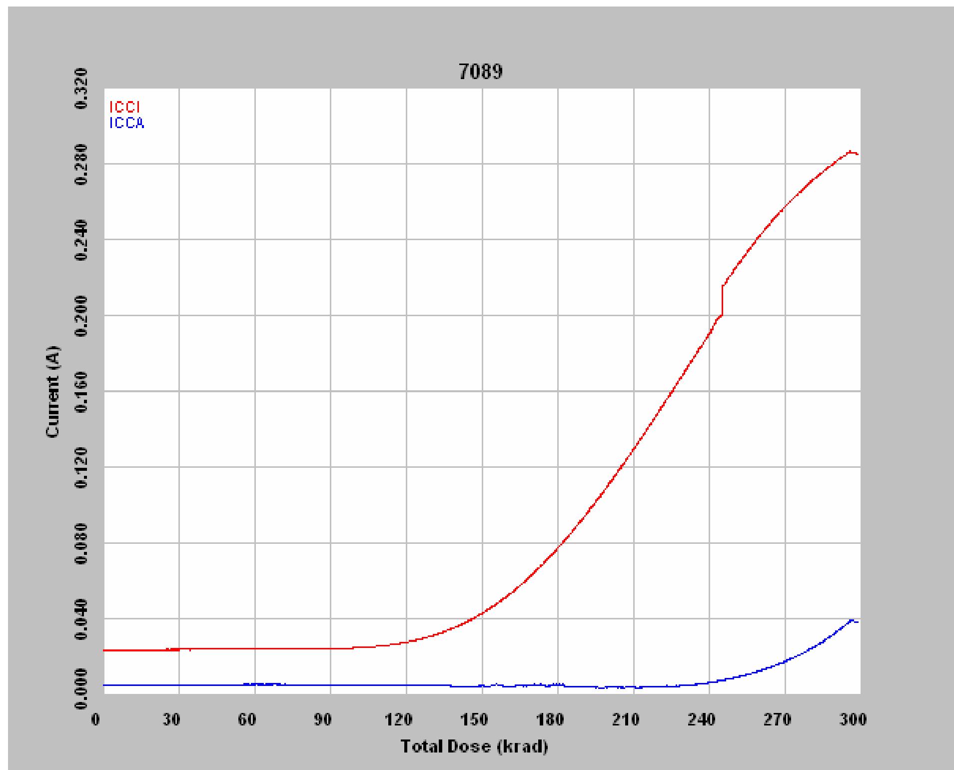

Figure 4 DUT 7089 in-flux I_{CCA} and I_{CCI}

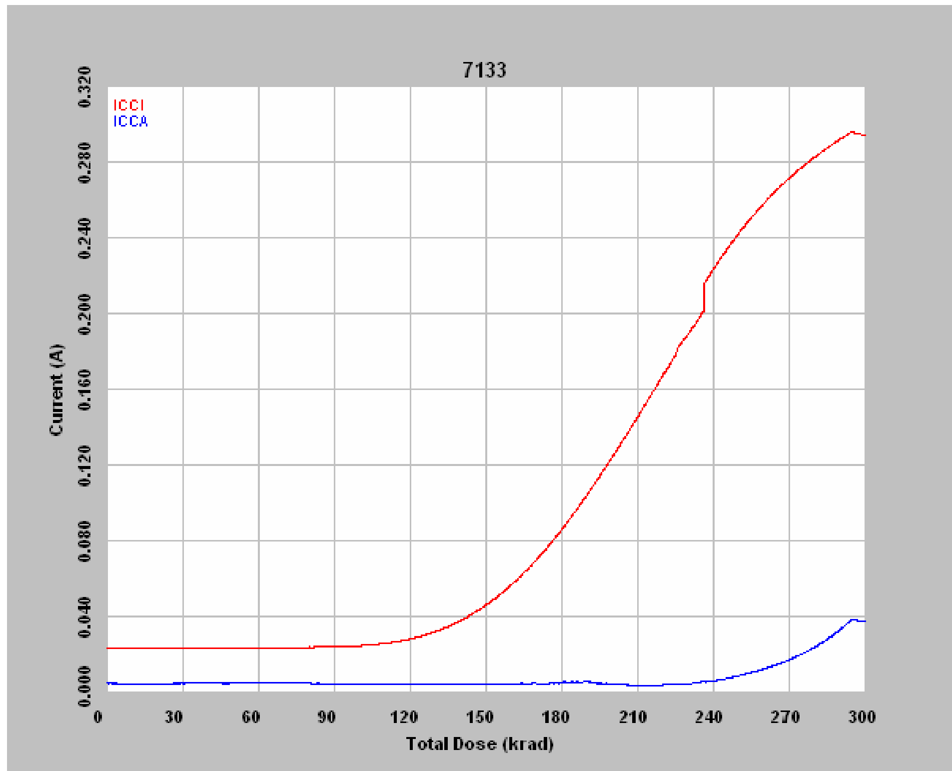

Figure 5 DUT 7133 in-flux I_{CCA} and I_{CCI}

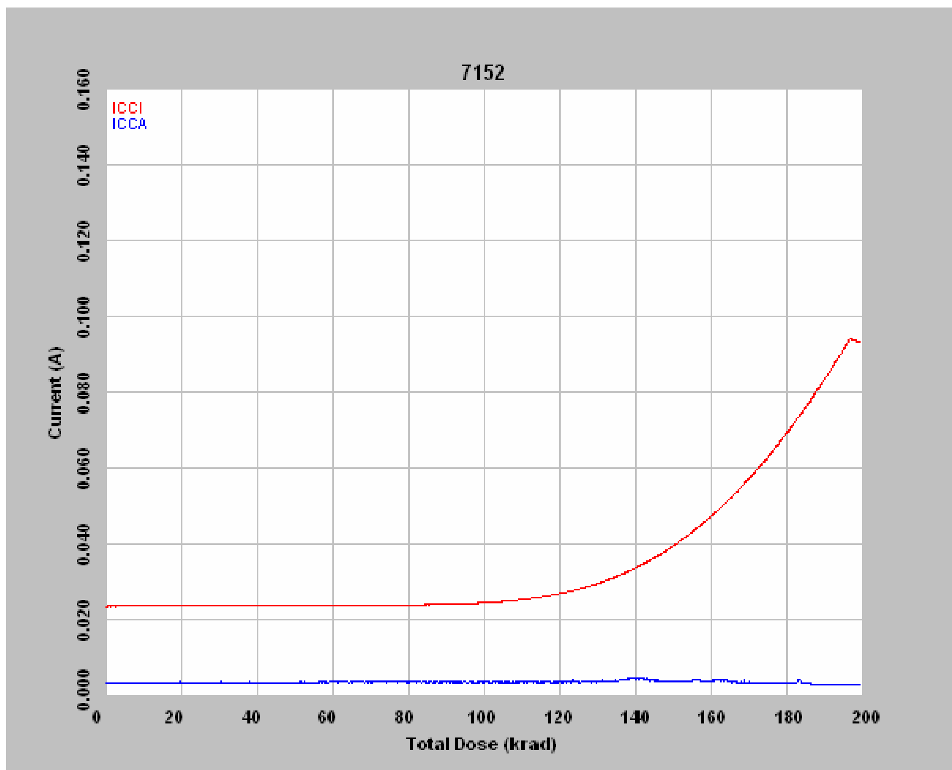

Figure 6 DUT 7152 in-flux I_{CCA} and I_{CCI}

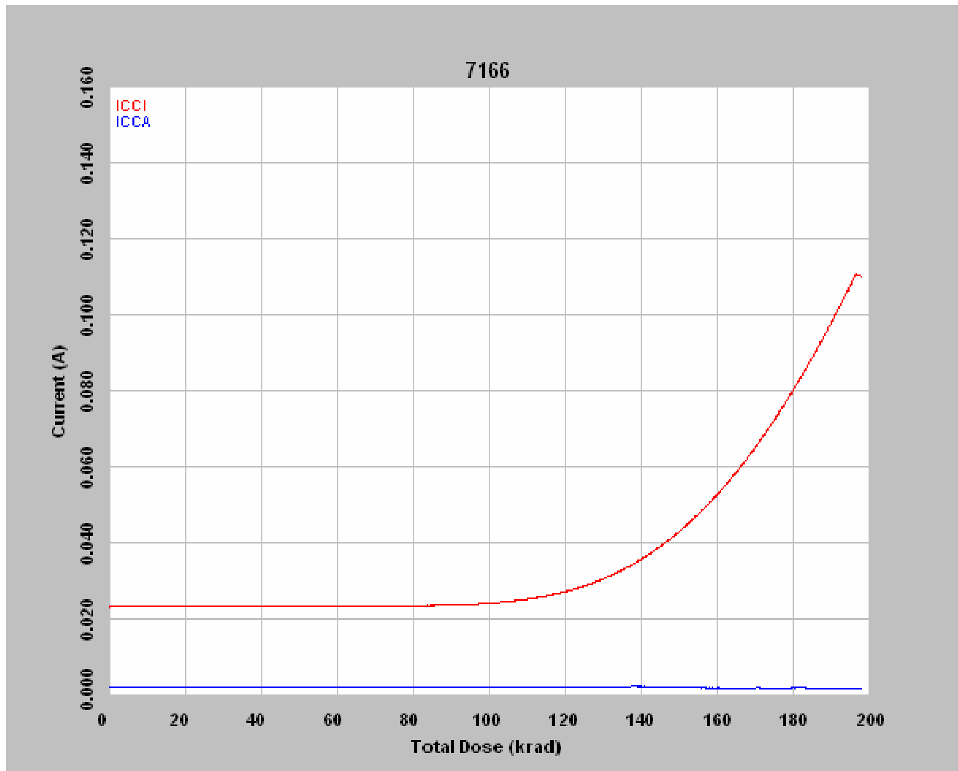

Figure 7 DUT 7166 in-flux I_{CCA} and I_{CCI}

C. Single-Ended 3.3V-LVTTL V_{IHL}/V_{ILH} and I_{IL}/I_{IH}

The input switching thresholds, or trip point, is defined as the applied input voltage at which the output of the design—often just input and output buffers—starts to switch: V_{IHL} is the input trip point when the input is going high to low; V_{ILH} is the input trip point when the input is going low to high.

Tables 3a and 3b list the pre-irradiation and post-annealing single-ended V_{IHL}. In each case, the difference between the pre-irradiation and post-annealing data is negligibly small. Tables 4a and 4b show the pre-irradiation and post-annealing single-ended V_{ILH}; again the difference between the pre-irradiation and post-annealing data is negligibly small.

I_{IL} is the current sink into an input being forced to low, and I_{IH} is the current source from an input being forced to high. The PIPL for both of them is 5µA.

Tables 5a and 5b show the pre-irradiation and the post-annealing I_{IL} data. Tables 6a and 6b show the pre-irradiation and post-annealing I_{IH} data. The post-annealing data of both I_{IL} and I_{IH} for every tested input in every DUT is below the 5µA PIPL. Some pre-irradiation I_{IL} or I_{IH} data exceeding the 5µA spec are believed due to noises in the tester because these DUT had been previously tested with "PASS" marking on every room temperature spec.

Table 3a

DUT		7087		7089		7133	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.36	1.35	1.36	1.35	1.36	1.35
bi_levels_vil	Bi_D_6	1.35	1.33	1.34	1.33	1.35	1.33
bi_levels_vil	Bi_D_5	1.36	1.34	1.36	1.34	1.36	1.35
bi_levels_vil	Bi_D_4	1.36	1.35	1.36	1.35	1.36	1.35
bi_levels_vil	Bi_D_3	1.36	1.35	1.35	1.34	1.36	1.35
bi_levels_vil	Bi_D_2	1.36	1.34	1.35	1.34	1.36	1.35
bi_levels_vil	Bi_D_1	1.35	1.34	1.35	1.34	1.36	1.34
bi_levels_vil	DA	1.36	1.35	1.36	1.35	1.37	1.35
bi_levels_vil	EN8	1.33	1.32	1.33	1.31	1.33	1.32
bi_levels_vil	IO_I_6	1.35	1.33	1.35	1.34	1.35	1.34
bi_levels_vil	IO_I_5	1.35	1.34	1.34	1.33	1.34	1.33
bi_levels_vil	IO_I_4	1.39	1.37	1.39	1.38	1.39	1.38
bi_levels_vil	IO_I_3	1.39	1.38	1.39	1.37	1.37	1.36
bi_levels_vil	IO_I_2	1.38	1.37	1.39	1.38	1.38	1.38
bi_levels_vil	IO_I_1	1.39	1.38	1.39	1.38	1.39	1.38
bi_levels_vil	RCLK1P	1.43	1.42	1.43	1.42	1.42	1.42
bi_levels_vil	RCLK2P	1.43	1.41	1.43	1.42	1.43	1.42

Table 3b

DUT		7152		7166	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.36	1.35	1.37	1.36
bi_levels_vil	Bi_D_6	1.34	1.33	1.36	1.35
bi_levels_vil	Bi_D_5	1.35	1.34	1.36	1.35
bi_levels_vil	Bi_D_4	1.35	1.35	1.37	1.36
bi_levels_vil	Bi_D_3	1.35	1.34	1.36	1.36
bi_levels_vil	Bi_D_2	1.35	1.34	1.36	1.35
bi_levels_vil	Bi_D_1	1.35	1.34	1.36	1.35
bi_levels_vil	DA	1.37	1.35	1.37	1.36
bi_levels_vil	EN8	1.33	1.33	1.34	1.33
bi_levels_vil	IO_I_6	1.35	1.34	1.35	1.34
bi_levels_vil	IO_I_5	1.35	1.33	1.34	1.34
bi_levels_vil	IO_I_4	1.39	1.38	1.40	1.39
bi_levels_vil	IO_I_3	1.39	1.37	1.37	1.36
bi_levels_vil	IO_I_2	1.39	1.38	1.39	1.38
bi_levels_vil	IO_I_1	1.39	1.38	1.39	1.38
bi_levels_vil	RCLK1P	1.43	1.42	1.43	1.42
bi_levels_vil	RCLK2P	1.43	1.42	1.43	1.42

Table 4a

DUT		7087		7089		7133	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.36	1.36	1.36	1.35	1.36	1.35
bi_levels_vih	Bi_D_6	1.37	1.36	1.37	1.36	1.37	1.36
bi_levels_vih	Bi_D_5	1.35	1.36	1.37	1.36	1.37	1.36
bi_levels_vih	Bi_D_4	1.36	1.35	1.36	1.35	1.36	1.35
bi_levels_vih	Bi_D_3	1.37	1.36	1.37	1.36	1.37	1.37
bi_levels_vih	Bi_D_2	1.37	1.36	1.37	1.36	1.38	1.37
bi_levels_vih	Bi_D_1	1.36	1.36	1.36	1.36	1.37	1.36
bi_levels_vih	DA	1.38	1.38	1.39	1.38	1.39	1.38
bi_levels_vih	EN8	1.43	1.42	1.44	1.43	1.44	1.43
bi_levels_vih	IO_I_6	1.41	1.40	1.41	1.39	1.41	1.40
bi_levels_vih	IO_I_5	1.42	1.39	1.40	1.42	1.40	1.41
bi_levels_vih	IO_I_4	1.38	1.38	1.39	1.38	1.39	1.38
bi_levels_vih	IO_I_3	1.40	1.39	1.39	1.39	1.40	1.39
bi_levels_vih	IO_I_2	1.38	1.37	1.39	1.38	1.39	1.38
bi_levels_vih	IO_I_1	1.39	1.39	1.39	1.39	1.39	1.39
bi_levels_vih	RCLK1P	1.42	1.41	1.43	1.42	1.42	1.41
bi_levels_vih	RCLK2P	1.43	1.41	1.43	1.43	1.43	1.42

Table 4b

DUT		7152		7166	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.36	1.35	1.37	1.36
bi_levels_vih	Bi_D_6	1.36	1.36	1.38	1.37
bi_levels_vih	Bi_D_5	1.36	1.35	1.37	1.37
bi_levels_vih	Bi_D_4	1.35	1.35	1.37	1.36
bi_levels_vih	Bi_D_3	1.36	1.36	1.38	1.37
bi_levels_vih	Bi_D_2	1.36	1.36	1.37	1.37
bi_levels_vih	Bi_D_1	1.36	1.36	1.37	1.37
bi_levels_vih	DA	1.39	1.38	1.39	1.39
bi_levels_vih	EN8	1.44	1.44	1.45	1.45
bi_levels_vih	IO_I_6	1.41	1.40	1.42	1.41
bi_levels_vih	IO_I_5	1.40	1.41	1.42	1.40
bi_levels_vih	IO_I_4	1.39	1.38	1.39	1.38
bi_levels_vih	IO_I_3	1.39	1.39	1.40	1.39
bi_levels_vih	IO_I_2	1.39	1.38	1.39	1.38
bi_levels_vih	IO_I_1	1.39	1.39	1.39	1.38
bi_levels_vih	RCLK1P	1.42	1.41	1.42	1.42
bi_levels_vih	RCLK2P	1.43	1.42	1.43	1.42

Table 5a

DUT		7087		7089		7133	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	-20.5 uA	-891.8 pA	-20.5 uA	-3.2 nA	-20.5 uA	-2.6 nA
IIL_Inputs_Max_	Bi_D_2	-20.5 uA	573.3 pA	-20.5 uA	-2.1 nA	-20.5 uA	-473.2 pA
IIL_Inputs_Max_	Bi_D_3	-20.1 uA	-473.2 pA	-20.5 uA	-2.8 nA	-20.5 uA	-473.2 pA
IIL_Inputs_Max_	Bi_D_4	365.9 nA	-2.7 nA	431.7 nA	-2.9 nA	324.9 nA	-149.5 pA
IIL_Inputs_Max_	Bi_D_5	502.6 nA	-149.5 pA	443.6 nA	-1.6 nA	421.6 nA	-568.1 pA
IIL_Inputs_Max_	Bi_D_6	-15.4 uA	-3.7 nA	-15.3 uA	-5.6 nA	-14.7 uA	-4.7 nA
IIL_Inputs_Max_	Bi_D_7	376.4 nA	-963.0 pA	472.4 nA	-3.9 nA	376.4 nA	-1.4 nA
IIL_Inputs_Max_	Bi_E_1	499.8 nA	1.3 nA	502.5 nA	919.4 pA	426.1 nA	-1.6 nA
IIL_Inputs_Max_	Bi_E_2	515.4 nA	-753.8 pA	500.2 nA	710.3 pA	537.2 nA	-753.8 pA
IIL_Inputs_Max_	Bi_E_3	506.0 nA	1.5 nA	499.5 nA	501.1 pA	432.0 nA	-126.3 pA
IIL_Inputs_Max_	Bi_E_4	547.9 nA	501.1 pA	515.9 nA	-335.5 pA	595.5 nA	-126.3 pA
IIL_Inputs_Max_	Bi_E_5	459.6 nA	292.0 pA	426.6 nA	-126.3 pA	428.2 nA	-963.0 pA
IIL_Inputs_Max_	Bi_E_6	515.0 nA	-1.4 nA	435.1 nA	-1.2 nA	459.0 nA	-963.0 pA
IIL_Inputs_Max_	Bi_E_7	570.4 nA	-544.7 pA	420.9 nA	501.1 pA	457.3 nA	-1.4 nA
IIL_Inputs_Max_	DA	-3.1 nA	-3.3 nA	-5.8 nA	-6.4 nA	-6.2 nA	-5.2 nA
IIL_Inputs_Max_	DIO_IN_1	-4.3 nA	-4.1 nA	704.0 pA	-3.1 nA	-6.2 nA	-4.5 nA
IIL_Inputs_Max_	DIO_IN_2	-2.2 nA	-2.4 nA	-2.2 nA	-4.1 nA	-4.3 nA	-3.9 nA
IIL_Inputs_Max_	DIO_IN_3	-3.5 nA	-3.5 nA	2.4 nA	-4.9 nA	-5.4 nA	-4.7 nA
IIL_Inputs_Max_	DIO_IN_4	-1.2 nA	-3.3 nA	5.5 nA	-4.7 nA	-4.3 nA	-4.3 nA
IIL_Inputs_Max_	DIO_IN_5	-3.1 nA	-5.4 nA	-3.7 nA	-3.7 nA	-4.3 nA	-3.5 nA
IIL_Inputs_Max_	DIO_IN_6	-1.8 nA	-3.3 nA	-4.3 nA	-4.9 nA	-4.7 nA	-4.5 nA
IIL_Inputs_Max_	DIO_IN_7	-2.8 nA	-2.4 nA	-3.1 nA	-4.7 nA	-3.9 nA	-3.9 nA
IIL_Inputs_Max_	DIO_IP_1	-4.1 nA	-4.7 nA	-4.7 nA	-3.3 nA	-5.4 nA	-6.4 nA
IIL_Inputs_Max_	DIO_IP_2	-4.1 nA	-3.5 nA	503.3 pA	-6.4 nA	-5.8 nA	-6.0 nA
IIL_Inputs_Max_	DIO_IP_3	-3.1 nA	-4.3 nA	-7.7 nA	-5.2 nA	-2.4 nA	-5.8 nA
IIL_Inputs_Max_	DIO_IP_4	-2.4 nA	-2.6 nA	-3.3 nA	-3.9 nA	-4.3 nA	-1.8 nA
IIL_Inputs_Max_	DIO_IP_5	-4.3 nA	-1.8 nA	4.9 nA	-2.8 nA	-3.9 nA	-3.1 nA
IIL_Inputs_Max_	DIO_IP_6	4.1 nA	-2.2 nA	-2.0 nA	-1.4 nA	-3.7 nA	-2.2 nA
IIL_Inputs_Max_	DIO_IP_7	-1.6 nA	-1.8 nA	-2.8 nA	-5.4 nA	-2.8 nA	-3.9 nA
IIL_Inputs_Max_	EN8	-2.4 nA	-4.5 nA	-5.6 nA	-3.1 nA	-3.5 nA	-2.4 nA
IIL_Inputs_Max_	HCLK1P	-753.8 pA	1.1 nA	-544.7 pA	82.8 pA	501.1 pA	2.4 nA
IIL_Inputs_Max_	HCLK2P	-2.6 nA	-1.4 nA	76.1 pA	-3.3 nA	-4.9 nA	-2.4 nA
IIL_Inputs_Max_	HCLK3P	-1.3 nA	364.0 pA	-2.6 nA	573.3 pA	-2.1 nA	364.0 pA
IIL_Inputs_Max_	HCLK4P	-1.2 nA	-3.9 nA	-2.9 nA	-2.2 nA	269.1 pA	-568.1 pA
IIL_Inputs_Max_	IO_I_1	-6.0 nA	-2.4 nA	-7.3 nA	-2.9 nA	-3.7 nA	-4.3 nA
IIL_Inputs_Max_	IO_I_2	-682.5 pA	-891.8 pA	-2.4 nA	-3.4 nA	-3.6 nA	-1.9 nA
IIL_Inputs_Max_	IO_I_3	-3.3 nA	-4.1 nA	-11.0 nA	-1.8 nA	-4.5 nA	-2.9 nA
IIL_Inputs_Max_	IO_I_4	-3.6 nA	-891.8 pA	-6.5 nA	-2.4 nA	-8.8 nA	-1.3 nA
IIL_Inputs_Max_	IO_I_5	-1.6 nA	-4.7 nA	-4.3 nA	-4.3 nA	-5.8 nA	-4.9 nA
IIL_Inputs_Max_	IO_I_6	-2.8 nA	-2.0 nA	-4.5 nA	-3.3 nA	-2.4 nA	-2.6 nA
IIL_Inputs_Max_	LOADIN	-3.2 nA	-10.1 nA	-12.4 nA	-11.2 nA	-11.2 nA	-11.4 nA
IIL_Inputs_Max_	RCLK1P	455.6 nA	-1.6 nA	484.7 nA	-3.9 nA	398.0 nA	-3.9 nA
IIL_Inputs_Max_	RCLK2P	479.0 nA	897.1 pA	459.3 nA	1.1 nA	420.1 nA	897.1 pA
IIL_Inputs_Max_	RCLK3P	-1.1 nA	1.2 nA	-263.9 pA	-1.7 nA	-2.1 nA	-682.5 pA
IIL_Inputs_Max_	RCLK4P	-1.8 nA	-753.8 pA	-544.7 pA	501.1 pA	-2.0 nA	919.4 pA

Table 5b

DUT		7152		7166	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	331.8 nA	-3.4 nA	-8.4 nA	-5.1 nA
IIL_Inputs_Max_	Bi_D_2	-20.5 uA	-1.1 nA	-3.4 nA	-2.4 nA
IIL_Inputs_Max_	Bi_D_3	398.1 nA	-2.4 nA	-2.8 nA	-263.9 pA
IIL_Inputs_Max_	Bi_D_4	-11.4 uA	-1.6 nA	-5.0 nA	59.8 pA
IIL_Inputs_Max_	Bi_D_5	-4.9 nA	-777.4 pA	-1.2 nA	478.4 pA
IIL_Inputs_Max_	Bi_D_6	-10.5 nA	-6.4 nA	-9.3 nA	-4.5 nA
IIL_Inputs_Max_	Bi_D_7	406.7 nA	-544.7 pA	-2.2 nA	-753.8 pA
IIL_Inputs_Max_	Bi_E_1	-20.5 uA	-335.5 pA	-2.4 nA	919.4 pA
IIL_Inputs_Max_	Bi_E_2	485.7 nA	-1.4 nA	292.0 pA	-753.8 pA
IIL_Inputs_Max_	Bi_E_3	-7.0 nA	-753.8 pA	-753.8 pA	-1.6 nA
IIL_Inputs_Max_	Bi_E_4	-5.2 nA	-1.2 nA	-126.3 pA	82.8 pA
IIL_Inputs_Max_	Bi_E_5	897.1 pA	919.4 pA	-544.7 pA	-963.0 pA
IIL_Inputs_Max_	Bi_E_6	-20.5 uA	-1.4 nA	-1.4 nA	-963.0 pA
IIL_Inputs_Max_	Bi_E_7	591.4 nA	2.0 nA	-753.8 pA	1.5 nA
IIL_Inputs_Max_	DA	-2.9 nA	-6.8 nA	-7.7 nA	-5.2 nA
IIL_Inputs_Max_	DIO_IN_1	-3.3 nA	-5.4 nA	2.6 nA	-6.4 nA
IIL_Inputs_Max_	DIO_IN_2	444.4 nA	-5.6 nA	2.0 nA	-2.6 nA
IIL_Inputs_Max_	DIO_IN_3	-682.5 pA	-4.1 nA	-4.7 nA	-4.5 nA
IIL_Inputs_Max_	DIO_IN_4	510.8 nA	-3.9 nA	-4.7 nA	-3.5 nA
IIL_Inputs_Max_	DIO_IN_5	-4.7 nA	-3.1 nA	-6.0 nA	-3.5 nA
IIL_Inputs_Max_	DIO_IN_6	-3.1 nA	-2.4 nA	-5.4 nA	-3.7 nA
IIL_Inputs_Max_	DIO_IN_7	-7.0 nA	-5.8 nA	-2.2 nA	-3.7 nA
IIL_Inputs_Max_	DIO_IP_1	617.5 nA	-3.7 nA	-5.8 nA	-4.5 nA
IIL_Inputs_Max_	DIO_IP_2	-3.9 nA	-5.6 nA	-1.8 nA	-3.1 nA
IIL_Inputs_Max_	DIO_IP_3	-3.1 nA	-5.2 nA	-2.6 nA	-5.2 nA
IIL_Inputs_Max_	DIO_IP_4	-1.7 nA	-2.4 nA	-4.7 nA	-2.8 nA
IIL_Inputs_Max_	DIO_IP_5	474.9 nA	-2.6 nA	-5.4 nA	-3.3 nA
IIL_Inputs_Max_	DIO_IP_6	-6.0 nA	-2.6 nA	-3.5 nA	-5.2 nA
IIL_Inputs_Max_	DIO_IP_7	-3.5 nA	-4.3 nA	-4.1 nA	-3.9 nA
IIL_Inputs_Max_	EN8	-1.3 nA	-4.9 nA	-6.4 nA	-1.2 nA
IIL_Inputs_Max_	HCLK1P	456.7 nA	919.4 pA	-1.2 nA	-2.6 nA
IIL_Inputs_Max_	HCLK2P	-6.4 nA	-5.6 nA	-6.4 nA	-2.0 nA
IIL_Inputs_Max_	HCLK3P	-5.4 nA	991.9 pA	154.7 pA	-473.2 pA
IIL_Inputs_Max_	HCLK4P	520.9 nA	897.1 pA	-777.4 pA	-1.6 nA
IIL_Inputs_Max_	IO_I_1	-3.5 nA	-6.8 nA	-2.9 nA	-4.9 nA
IIL_Inputs_Max_	IO_I_2	-125.0 pA	782.6 pA	-2.4 nA	-1.1 nA
IIL_Inputs_Max_	IO_I_3	-1.8 nA	-5.2 nA	-5.4 nA	-3.7 nA
IIL_Inputs_Max_	IO_I_4	-4.3 nA	991.9 pA	-2.4 nA	-473.2 pA
IIL_Inputs_Max_	IO_I_5	-2.0 nA	-5.4 nA	-2.6 nA	-1.6 nA
IIL_Inputs_Max_	IO_I_6	-544.7 pA	-753.2 pA	-1.8 nA	-4.1 nA
IIL_Inputs_Max_	LOADIN	491.4 nA	-10.3 nA	-11.6 nA	-10.1 nA
IIL_Inputs_Max_	RCLK1P	-3.1 nA	-6.0 nA	-8.1 nA	-4.3 nA
IIL_Inputs_Max_	RCLK2P	-4.7 nA	1.1 nA	-986.7 pA	1.1 nA
IIL_Inputs_Max_	RCLK3P	-2.6 nA	1.2 nA	-1.3 nA	-2.1 nA
IIL_Inputs_Max_	RCLK4P	-1.4 nA	-753.8 pA	-1.2 nA	1.8 nA

Table 6a

DUT		7087		7089		7133	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	20.7 uA	4.1 nA	20.7 uA	5.2 nA	20.7 uA	3.5 nA
IIH_Inputs_Max_	Bi_D_2	20.7 uA	3.1 nA	20.7 uA	3.1 nA	20.7 uA	5.2 nA
IIH_Inputs_Max_	Bi_D_3	20.7 uA	4.3 nA	20.7 uA	2.9 nA	20.7 uA	2.7 nA
IIH_Inputs_Max_	Bi_D_4	574.6 nA	4.9 nA	623.2 nA	2.8 nA	535.3 nA	897.1 pA
IIH_Inputs_Max_	Bi_D_5	566.0 nA	1.1 nA	563.1 nA	3.4 nA	565.6 nA	1.7 nA
IIH_Inputs_Max_	Bi_D_6	1.0 uA	913.4 pA	1.2 uA	3.6 nA	939.3 nA	913.4 pA
IIH_Inputs_Max_	Bi_D_7	735.3 nA	2.4 nA	918.9 nA	3.8 nA	838.2 nA	2.0 nA
IIH_Inputs_Max_	Bi_E_1	555.0 nA	2.4 nA	632.4 nA	710.3 pA	573.6 nA	2.8 nA
IIH_Inputs_Max_	Bi_E_2	439.7 nA	1.5 nA	362.3 nA	1.8 nA	390.2 nA	501.1 pA
IIH_Inputs_Max_	Bi_E_3	320.7 nA	2.2 nA	289.8 nA	919.4 pA	237.9 nA	1.1 nA
IIH_Inputs_Max_	Bi_E_4	795.3 nA	1.1 nA	812.7 nA	3.0 nA	818.9 nA	501.1 pA
IIH_Inputs_Max_	Bi_E_5	247.1 nA	2.2 nA	267.2 nA	1.3 nA	324.9 nA	1.3 nA
IIH_Inputs_Max_	Bi_E_6	324.9 nA	2.0 nA	301.7 nA	-126.3 pA	265.1 nA	501.1 pA
IIH_Inputs_Max_	Bi_E_7	2.2 nA	2.4 nA	426.1 nA	2.4 nA	-126.3 pA	501.1 pA
IIH_Inputs_Max_	DA	1.3 nA	3.0 nA	922.1 pA	2.4 nA	1.3 nA	503.3 pA
IIH_Inputs_Max_	DIO_IN_1	-4.5 nA	-2.2 nA	-1.4 nA	704.0 pA	913.4 pA	-342.6 pA
IIH_Inputs_Max_	DIO_IN_2	293.9 pA	1.3 nA	-125.0 pA	-962.6 pA	84.4 pA	922.1 pA
IIH_Inputs_Max_	DIO_IN_3	1.8 nA	1.8 nA	293.9 pA	-753.2 pA	1.1 nA	84.4 pA
IIH_Inputs_Max_	DIO_IN_4	-1.6 nA	-2.0 nA	3.6 nA	-551.9 pA	-133.2 pA	-551.9 pA
IIH_Inputs_Max_	DIO_IN_5	2.4 nA	-962.6 pA	2.8 nA	503.3 pA	-2.0 nA	-334.4 pA
IIH_Inputs_Max_	DIO_IN_6	-125.0 pA	-125.0 pA	2.2 nA	-3.3 nA	-1.4 nA	712.7 pA
IIH_Inputs_Max_	DIO_IN_7	712.7 pA	293.9 pA	2.0 nA	-1.6 nA	-1.2 nA	-1.6 nA
IIH_Inputs_Max_	DIO_IP_1	2.6 nA	-1.2 nA	-133.2 pA	-551.9 pA	-2.9 nA	-2.4 nA
IIH_Inputs_Max_	DIO_IP_2	-334.4 pA	-543.8 pA	10.6 nA	-3.5 nA	-2.4 nA	293.9 pA
IIH_Inputs_Max_	DIO_IP_3	4.3 nA	-1.6 nA	5.5 nA	-1.6 nA	-2.6 nA	-342.6 pA
IIH_Inputs_Max_	DIO_IP_4	1.6 nA	-962.6 pA	-125.0 pA	-3.3 nA	-2.4 nA	-2.0 nA
IIH_Inputs_Max_	DIO_IP_5	-1.6 nA	-543.8 pA	-2.6 nA	712.7 pA	-543.8 pA	-1.2 nA
IIH_Inputs_Max_	DIO_IP_6	13.5 nA	-125.0 pA	13.9 nA	503.3 pA	-962.6 pA	-753.2 pA
IIH_Inputs_Max_	DIO_IP_7	1.6 nA	1.1 nA	1.6 nA	-1.6 nA	922.1 pA	-962.6 pA
IIH_Inputs_Max_	EN8	-543.8 pA	1.1 nA	2.0 nA	84.4 pA	-543.8 pA	1.6 nA
IIH_Inputs_Max_	HCLK1P	-963.0 pA	1.8 nA	-544.7 pA	-544.7 pA	-544.7 pA	2.6 nA
IIH_Inputs_Max_	HCLK2P	-3.9 nA	-1.4 nA	-2.2 nA	-2.6 nA	-970.5 pA	-3.1 nA
IIH_Inputs_Max_	HCLK3P	782.6 pA	1.2 nA	573.3 pA	-682.5 pA	991.9 pA	2.7 nA
IIH_Inputs_Max_	HCLK4P	-568.1 pA	1.9 nA	-149.5 pA	-2.7 nA	-568.1 pA	1.3 nA
IIH_Inputs_Max_	IO_I_1	-6.4 nA	-3.9 nA	-1.8 nA	-1.8 nA	-3.9 nA	-1.2 nA
IIH_Inputs_Max_	IO_I_2	-682.5 pA	3.7 nA	782.6 pA	991.9 pA	2.5 nA	2.2 nA
IIH_Inputs_Max_	IO_I_3	-2.9 nA	-5.2 nA	-1.6 nA	-3.1 nA	-3.5 nA	-2.4 nA
IIH_Inputs_Max_	IO_I_4	4.8 nA	1.6 nA	9.2 nA	3.1 nA	4.6 nA	2.0 nA
IIH_Inputs_Max_	IO_I_5	6.8 nA	-1.8 nA	-6.2 nA	-2.4 nA	-342.6 pA	-2.4 nA
IIH_Inputs_Max_	IO_I_6	712.7 pA	-334.4 pA	3.9 nA	293.9 pA	-962.6 pA	2.0 nA
IIH_Inputs_Max_	LOADIN	-3.2 nA	-1.7 nA	-5.5 nA	-2.4 nA	-3.0 nA	-2.0 nA
IIH_Inputs_Max_	RCLK1P	764.5 nA	-342.6 pA	744.6 nA	-2.2 nA	673.9 nA	285.4 pA
IIH_Inputs_Max_	RCLK2P	322.0 nA	1.7 nA	260.0 nA	687.7 pA	241.8 nA	1.9 nA
IIH_Inputs_Max_	RCLK3P	1.4 nA	2.0 nA	-891.8 pA	991.9 pA	-2.4 nA	573.3 pA
IIH_Inputs_Max_	RCLK4P	82.8 pA	501.1 pA	-753.8 pA	2.8 nA	-1.4 nA	710.3 pA

Table 6b

DUT		7152		7166	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	20.7 uA	6.2 nA	4.1 nA	6.6 nA
IIH_Inputs_Max_	Bi_D_2	20.7 uA	6.6 nA	2.5 nA	4.6 nA
IIH_Inputs_Max_	Bi_D_3	20.7 uA	364.0 pA	2.0 nA	3.1 nA
IIH_Inputs_Max_	Bi_D_4	568.5 nA	5.3 nA	897.1 pA	3.0 nA
IIH_Inputs_Max_	Bi_D_5	609.6 nA	2.2 nA	3.2 nA	2.8 nA
IIH_Inputs_Max_	Bi_D_6	874.2 nA	494.7 pA	10.8 nA	4.1 nA
IIH_Inputs_Max_	Bi_D_7	757.6 nA	3.0 nA	3.8 nA	3.0 nA
IIH_Inputs_Max_	Bi_E_1	710.4 nA	2.2 nA	-335.5 pA	3.0 nA
IIH_Inputs_Max_	Bi_E_2	409.2 nA	710.3 pA	710.3 pA	3.2 nA
IIH_Inputs_Max_	Bi_E_3	334.9 nA	3.6 nA	-963.0 pA	1.8 nA
IIH_Inputs_Max_	Bi_E_4	789.2 nA	919.4 pA	710.3 pA	3.0 nA
IIH_Inputs_Max_	Bi_E_5	367.2 nA	2.0 nA	919.4 pA	710.3 pA
IIH_Inputs_Max_	Bi_E_6	296.9 nA	1.8 nA	501.1 pA	1.5 nA
IIH_Inputs_Max_	Bi_E_7	538.0 nA	3.0 nA	1.1 nA	1.5 nA
IIH_Inputs_Max_	DA	2.0 nA	922.1 pA	-334.4 pA	922.1 pA
IIH_Inputs_Max_	DIO_IN_1	-2.0 nA	76.1 pA	2.6 nA	-1.6 nA
IIH_Inputs_Max_	DIO_IN_2	2.4 nA	84.4 pA	84.4 pA	1.6 nA
IIH_Inputs_Max_	DIO_IN_3	-962.6 pA	-2.2 nA	-125.0 pA	-543.8 pA
IIH_Inputs_Max_	DIO_IN_4	-4.7 nA	-2.2 nA	-5.8 nA	-5.2 nA
IIH_Inputs_Max_	DIO_IN_5	293.9 pA	-962.6 pA	922.1 pA	-962.6 pA
IIH_Inputs_Max_	DIO_IN_6	84.4 pA	-125.0 pA	1.1 nA	712.7 pA
IIH_Inputs_Max_	DIO_IN_7	-543.8 pA	-2.0 nA	84.4 pA	293.9 pA
IIH_Inputs_Max_	DIO_IP_1	-2.0 nA	-1.2 nA	-2.2 nA	-3.1 nA
IIH_Inputs_Max_	DIO_IP_2	-2.0 nA	712.7 pA	-2.6 nA	-543.8 pA
IIH_Inputs_Max_	DIO_IP_3	-2.2 nA	-3.9 nA	-10.2 nA	-3.1 nA
IIH_Inputs_Max_	DIO_IP_4	-1.2 nA	-753.2 pA	-1.6 nA	-1.2 nA
IIH_Inputs_Max_	DIO_IP_5	-334.4 pA	-2.4 nA	-1.4 nA	-1.6 nA
IIH_Inputs_Max_	DIO_IP_6	-2.6 nA	-3.1 nA	-753.2 pA	-1.2 nA
IIH_Inputs_Max_	DIO_IP_7	84.4 pA	-1.8 nA	-125.0 pA	2.0 nA
IIH_Inputs_Max_	EN8	-962.6 pA	-125.0 pA	-1.6 nA	-1.6 nA
IIH_Inputs_Max_	HCLK1P	-1.6 nA	-544.7 pA	1.5 nA	2.0 nA
IIH_Inputs_Max_	HCLK2P	-2.6 nA	-2.6 nA	-2.4 nA	-3.3 nA
IIH_Inputs_Max_	HCLK3P	1.8 nA	573.3 pA	-263.9 pA	573.3 pA
IIH_Inputs_Max_	HCLK4P	-1.2 nA	897.1 pA	1.5 nA	-1.2 nA
IIH_Inputs_Max_	IO_I_1	-1.4 nA	-2.2 nA	-11.4 nA	-2.2 nA
IIH_Inputs_Max_	IO_I_2	364.0 pA	1.6 nA	-1.9 nA	991.9 pA
IIH_Inputs_Max_	IO_I_3	-551.9 pA	-970.5 pA	-1.8 nA	-3.3 nA
IIH_Inputs_Max_	IO_I_4	15.6 nA	3.3 nA	-54.6 pA	991.9 pA
IIH_Inputs_Max_	IO_I_5	-4.9 nA	-2.4 nA	-5.8 nA	-1.2 nA
IIH_Inputs_Max_	IO_I_6	84.4 pA	-1.4 nA	-962.6 pA	503.3 pA
IIH_Inputs_Max_	LOADIN	-4.3 nA	-4.7 nA	-2.6 nA	-3.2 nA
IIH_Inputs_Max_	RCLK1P	830.4 nA	-2.4 nA	-2.9 nA	-3.1 nA
IIH_Inputs_Max_	RCLK2P	291.2 nA	-1.6 nA	-2.0 nA	687.7 pA
IIH_Inputs_Max_	RCLK3P	364.0 pA	1.8 nA	-1.1 nA	1.4 nA
IIH_Inputs_Max_	RCLK4P	919.4 pA	82.8 pA	919.4 pA	2.2 nA

D. Differential Input 3.3V-LVPECL Threshold Voltage (V_{IL}/V_{IH})

The LVPECL V_{IL}/V_{IH} is measured as the minimum differential voltage applied between P (positive) and N (negative) to generate a stable output Low/High respectively. For V_{IL} the differential is $V_N - V_P$, and for V_{IH} the differential is $V_P - V_N$. The applied common voltage ($\frac{V_P + V_N}{2}$) is 1.8V. Tables 7a and 7b show the pre-irradiation and post-annealing tested data for V_{IL} of seven LVPECL inputs, and tables 8a and 8b show their pre-irradiation and post-annealing tested data for V_{IH}. In every case, pre-irradiation or post-annealing, the tested data passed the spec of 0.3V.

Table 7a

DUT		**7087**		**7089**		**7133**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	110	80	120	85	110	80
bi_levels_vil	DIO_IP_6	110	80	105	70	105	75
bi_levels_vil	DIO_IP_5	110	85	110	75	125	95
bi_levels_vil	DIO_IP_4	95	65	75	40	85	55
bi_levels_vil	DIO_IP_3	75	55	75	45	70	45
bi_levels_vil	DIO_IP_2	85	60	80	50	85	60
bi_levels_vil	DIO_IP_1	55	25	60	30	60	30

Table 7b

DUT		**7152**		**7166**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	105	90	100	90
bi_levels_vil	DIO_IP_6	105	90	105	100
bi_levels_vil	DIO_IP_5	110	95	115	100
bi_levels_vil	DIO_IP_4	85	70	80	65
bi_levels_vil	DIO_IP_3	75	65	75	70
bi_levels_vil	DIO_IP_2	80	70	85	75
bi_levels_vil	DIO_IP_1	60	45	55	45

Table 8a

DUT		7087		7089		7133	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	105	75	115	80	105	75
bi_levels_vih	DIO_IP_6	105	75	100	65	100	70
bi_levels_vih	DIO_IP_5	105	80	105	70	120	90
bi_levels_vih	DIO_IP_4	90	60	70	35	80	50
bi_levels_vih	DIO_IP_3	70	50	70	45	65	40
bi_levels_vih	DIO_IP_2	80	55	75	45	80	55
bi_levels_vih	DIO_IP_1	65	35	70	40	65	40

Table 8b

DUT		7152		7166	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	100	85	95	85
bi_levels_vih	DIO_IP_6	100	85	105	95
bi_levels_vih	DIO_IP_5	105	90	110	95
bi_levels_vih	DIO_IP_4	85	65	75	60
bi_levels_vih	DIO_IP_3	75	65	75	65
bi_levels_vih	DIO_IP_2	80	65	80	70
bi_levels_vih	DIO_IP_1	70	55	65	55

E. 3.3V-LVTTL Output-Drive Voltage (V_{OL}/V_{OH})

The output drive voltage V_{OL}/V_{OH} is measured at an output pin when it is at Low/High state and sinking/sourcing 24 mA current respectively. The spec for V_{OL}/V_{OH} is < 0.4V/ >2.4V respectively. Table 9a and 9b show the pre-irradiation and post-annealing tested data for V_{OL}; in every case the V_{OL} data passes the spec. Table 10a and 10b show the pre-irradiation and post-annealing tested data for V_{OH}; in every case the V_{OH} data passes the spec.

Table 9a

DUT		7087		7089		7133	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	35	30	30	30	30
bi_levels_vol	Bi_IO_5	35	30	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35	35	35
bi_levels_vol	Bi_IO_3	30	35	35	30	35	35
bi_levels_vol	Bi_IO_2	30	30	30	30	35	30
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	30	25	30	25	30	30
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	25	25	20	25	20	25
bi_levels_vol	QA_2	20	20	0	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	20	0	20	20	20	0

Table 9b

DUT		7152		7166	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35
bi_levels_vol	Bi_IO_3	30	30	35	30
bi_levels_vol	Bi_IO_2	30	30	35	30
bi_levels_vol	Bi_IO_1	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25
bi_levels_vol	Bi_Y_1	30	25	30	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20
bi_levels_vol	CLOCKF_OUT	20	25	25	25
bi_levels_vol	QA_2	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20
bi_levels_vol	QA_0	20	0	20	0

Table 10a

DUT		7087		7089		7133	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_6	2.965	2.970	2.965	2.965	2.965	2.970
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_6	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_5	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_4	2.980	2.980	2.980	2.980	2.980	2.980
bi_levels_voh	Bi_Y_3	2.980	2.980	2.980	2.980	2.980	2.985
bi_levels_voh	Bi_Y_2	2.980	2.980	2.980	2.980	2.980	2.980
bi_levels_voh	Bi_Y_1	2.980	2.980	2.980	2.980	2.980	2.980
bi_levels_voh	CLOCKE_OUT	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	CLOCKF_OUT	2.970	2.975	2.975	2.975	2.970	2.970
bi_levels_voh	QA_2	2.985	2.980	2.980	2.975	2.980	2.975
bi_levels_voh	QA_1	2.985	2.980	2.980	2.980	2.980	2.980
bi_levels_voh	QA_0	2.985	2.980	2.985	2.980	2.985	2.980

Table 10b

DUT		7152		7166	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.970	2.970	2.970	2.975
bi_levels_voh	Bi_IO_6	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_IO_5	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_IO_4	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_IO_3	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_IO_2	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_IO_1	2.965	2.970	2.965	2.970
bi_levels_voh	Bi_Y_7	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_6	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_5	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_4	2.980	2.985	2.980	2.985
bi_levels_voh	Bi_Y_3	2.980	2.985	2.985	2.985
bi_levels_voh	Bi_Y_2	2.980	2.985	2.980	2.985
bi_levels_voh	Bi_Y_1	2.980	2.985	2.980	2.985
bi_levels_voh	CLOCKE_OUT	2.970	2.975	2.970	2.975
bi_levels_voh	CLOCKF_OUT	2.970	2.975	2.970	2.975
bi_levels_voh	QA_2	2.980	2.980	2.980	2.980
bi_levels_voh	QA_1	2.980	2.980	2.980	2.980
bi_levels_voh	QA_0	2.985	2.985	2.985	2.980

F. Propagation Delay

The propagation delay spec for TID testing is defined as ±10% degradation. Table 11 lists the pre-irradiation and post-annealing propagation delays. Due to tester issues, there are only two sets of good data from two DUTs for 300 krad(SiO_2). Both cases pass the aforementioned spec.

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose krad(SiO_2)	Pre-Irradiation (μs)	Post-Annealing (μs)	Degradation (%)
7087	300	2.419	2.373	-1.91
7133	300	2.363	2.266	-4.03