TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX32SU-D19S61
March 8, 2005
J.J. Wang
(650) 318-4576
jih-jong.wang@actel.com

I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 62.3 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 11 days room temperature annealing: average I_{CCA} = 56.8 mA, and average I_{CCI} = 71.6 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 60 krad (Si); two DUTs out of five show switching from 5V-PCI to 5V-CMOS after 100 krad(Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion.
6. Transition Time	Passed 60 krad (Si); after 100-krad irradiation the same two DUTs showing the input-threshold switching show visible transition time degradation.

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. In this test, the threshold of most of the available inputs is measured.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 52446, 52462 and 52673 are irradiated to 60 krad; DUT 52552, 52557, 52642, 52661 and 52683 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D19S61
Quantity Tested	8
Serial Number	60 krad: 52446, 52462, 52673 100 krad: 52552, 52557, 52642, 52661, 52683
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

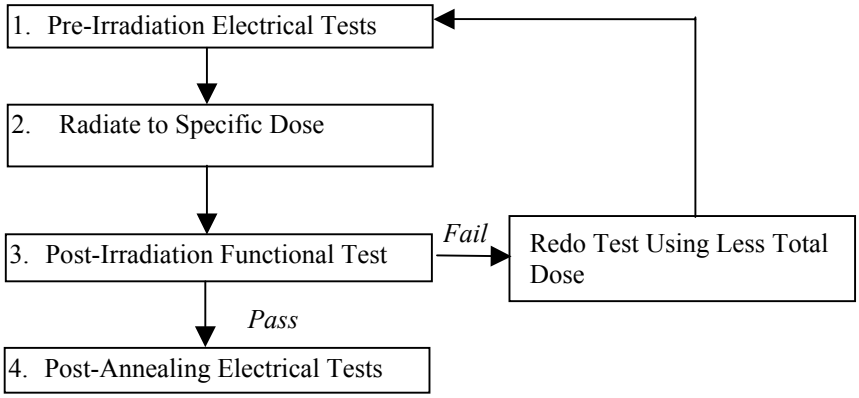


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. The 60-krad group is annealed for 3 days, and the 100-krad group is annealed for 11 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. For DUT irradiated to total dose of 100 krad, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is due to the temporary degradation of the charge pump; the degradation is caused by the radiation-induced leakage current overloading the output of the charge pump. After the pump degrading to a certain voltage, the array logic changes to another state and causes the I_{CCA} transition. In the mean time the logic outputs are disabled. However, the temporary degradation of the charge pump is only a testing artifact because the logic outputs recover within few hours during room temperature annealing.

By technicality, TM1019 doesn't allow further irradiation after disabling of the logic outputs. However, in this case, because the logic state of the DUT is still well defined, further irradiation is still valid. Every DUT was irradiated to 100 krad; after few hours of room temperature annealing, the logic outputs in every DUT were recovered.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
52446	60 krad	12.8	10	28.6	16
52462	60 krad	17.3	10	32	18
52673	60 krad	14.3	11	33.9	18
52552	100 krad	NA	77	NA	79
52557	100 krad	NA	71	NA	70
52642	100 krad	NA	44	NA	56
52661	100 krad	NA	39	NA	86
52683	100 krad	NA	53	NA	67

The 60 krad group shows the post-annealed I_{CC} passing the 25 mA spec. For the 100 krad group, a semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 52557, the tolerance is extracted as 62.3 krad for 10 years mission.

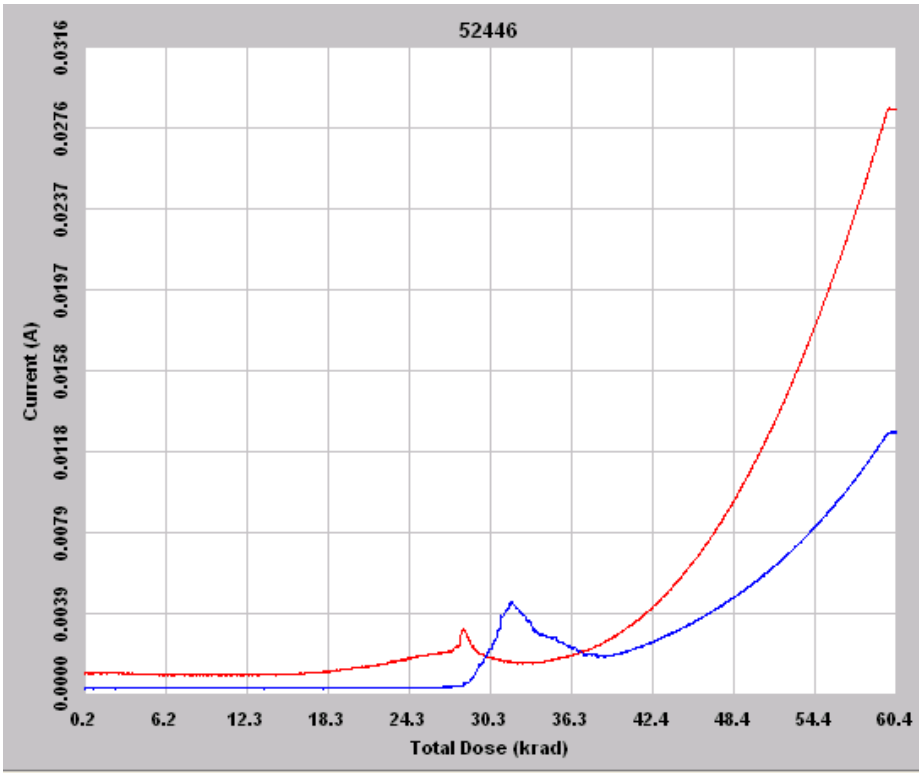


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 52446, 60-krad total dose. The transient peaks in ICCA and ICCI are testing artifacts due to accidental floating nodes in the device.

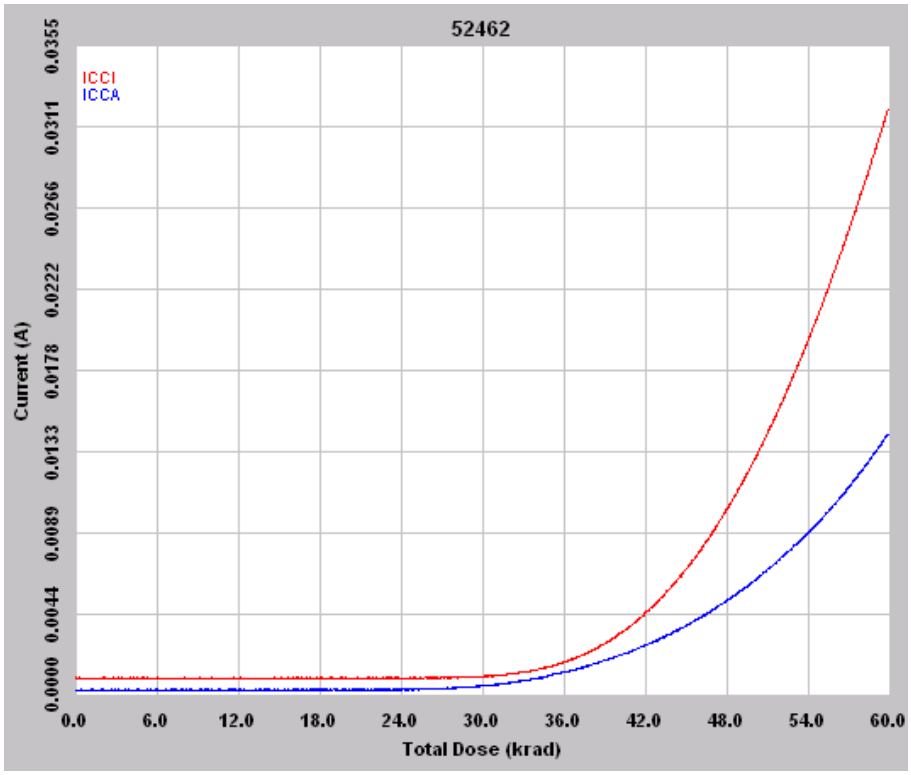


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 52462, 60-krad total dose

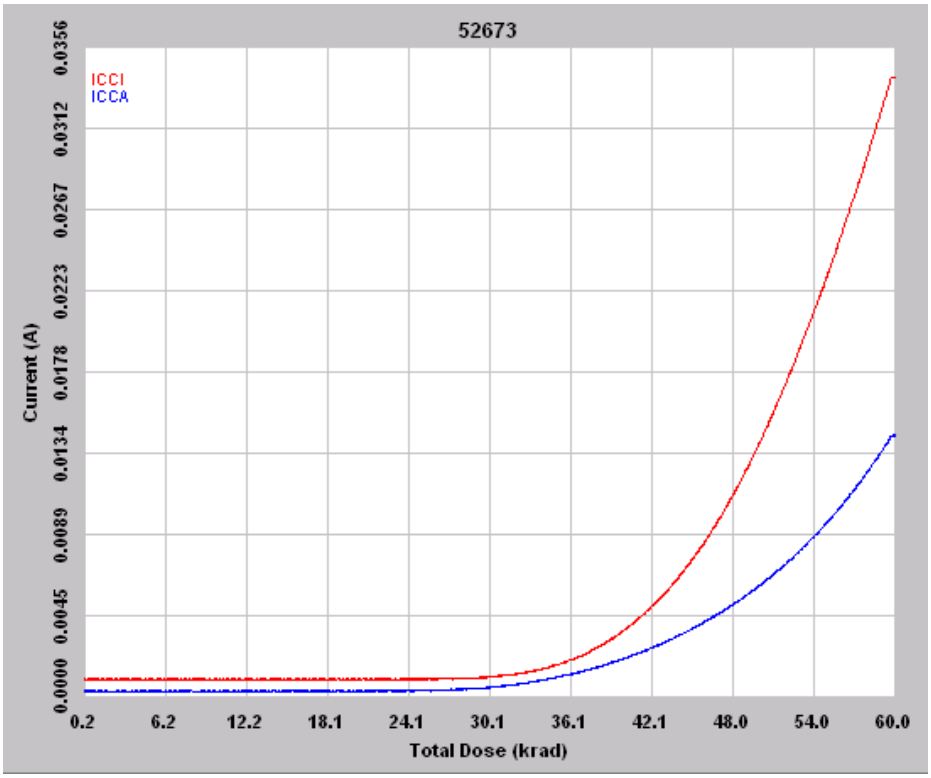


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 52462, 60-krad total dose

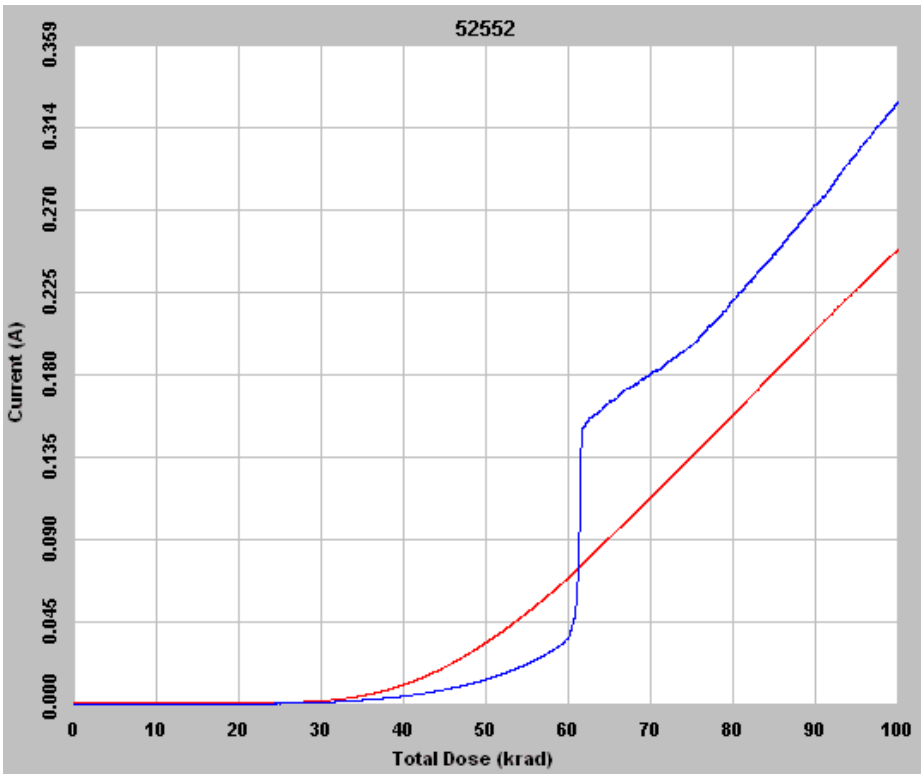


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 52552, I_{CCA} shows a transition near 62 krad that indicates the temporary disable of the charge pump.

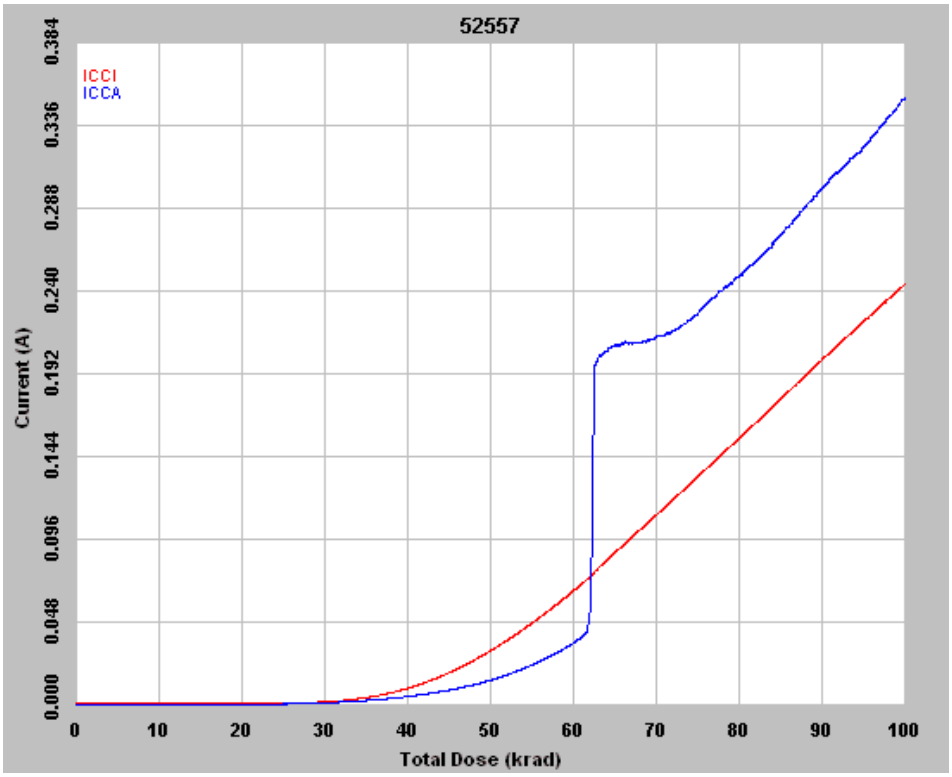


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 52557, I_{CCA} shows a transition near 62.5 krad that indicates the temporary disable of the charge pump.

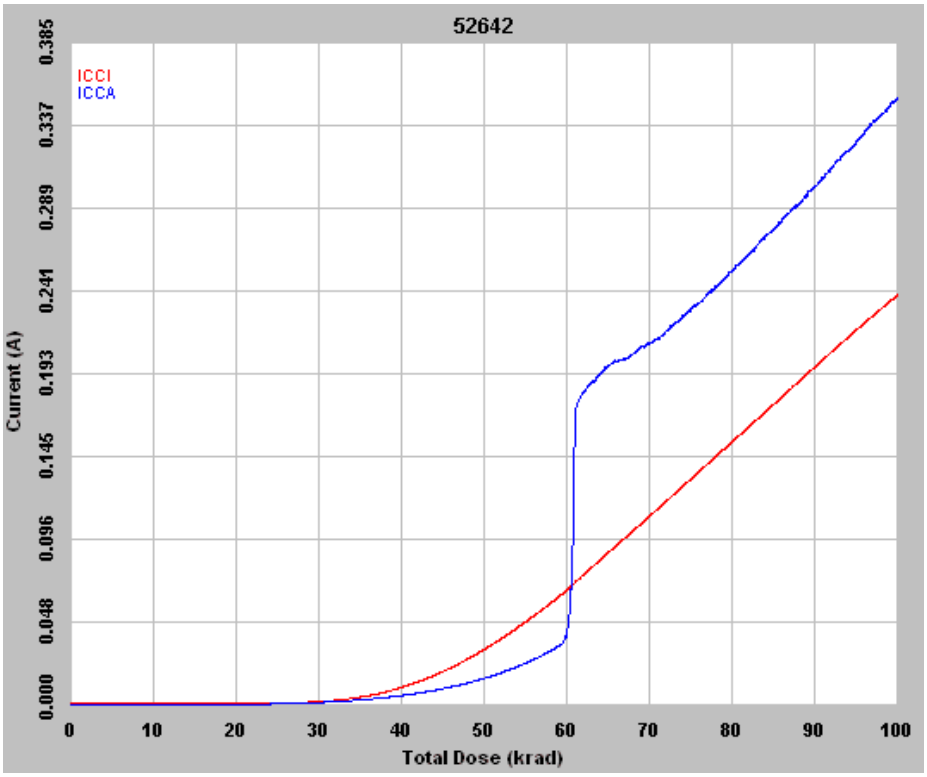


Figure 7 In flux I_{CCA} and I_{CCI} of DUT 52642, I_{CCA} shows a transition near 61 krad that indicates the temporary disable of the charge pump.

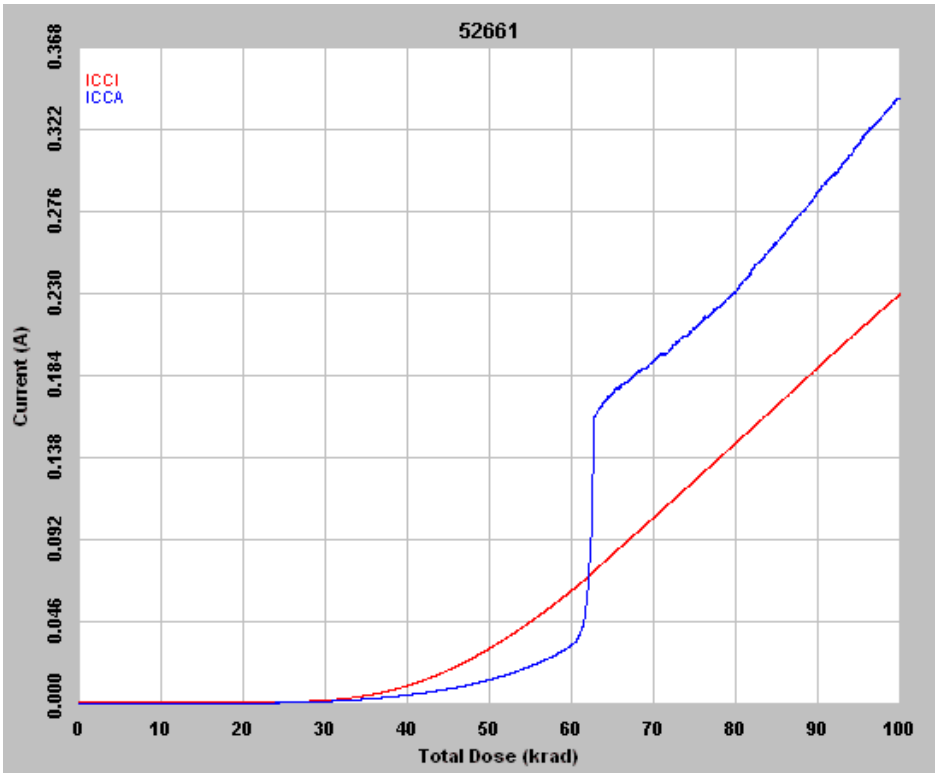


Figure 8 In flux I_{CCA} and I_{CCI} of DUT 52661, I_{CCA} shows a transition near 62.5 krad that indicates the temporary disable of the charge pump.

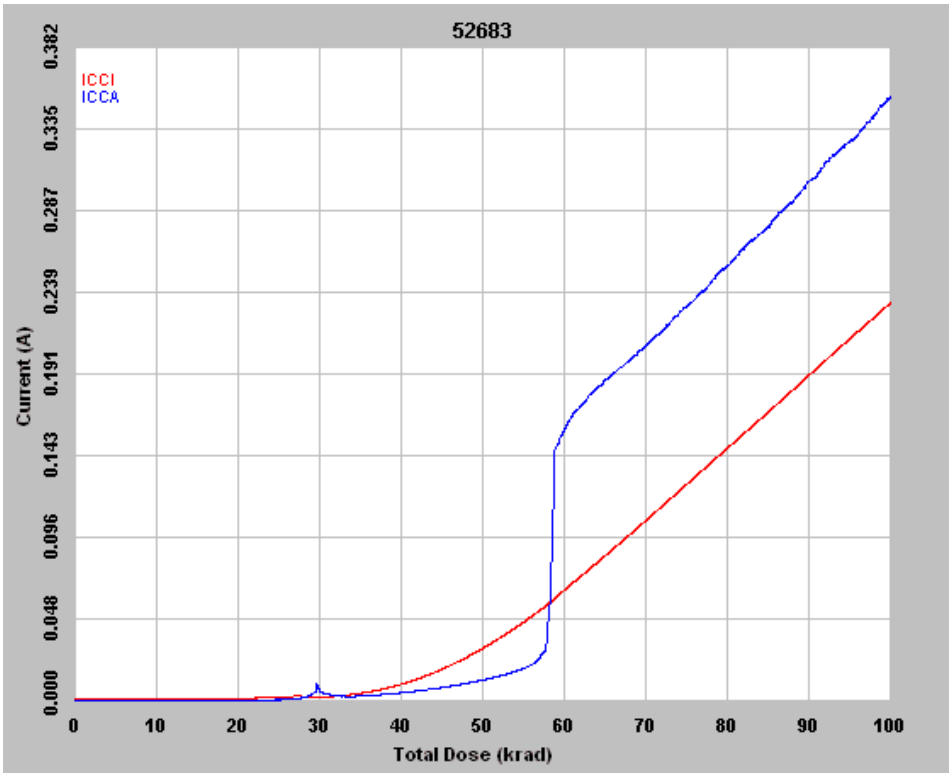


Figure 9 In flux I_{CCA} and I_{CCI} of DUT 52683, I_{CCA} shows a transition near 58 krad that indicates the temporary disable of the charge pump.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. DUT 52557 shows that the measured input changes from 5V-PCI to 5V-CMOS after 100-krad irradiation. Note that 5V-PCI has trip point near 1.5 V, and 5V-CMOS has trip point near 2.5 V.

The root cause is the same as that of the radiation-induced I_{CC}; the radiation-induced parasitic leakage turns off one of the pull-down NMOSFET, which is programmed to be turned on for 5V-PCI. The turning off of this NMOSFET switches the input from 5V-PCI to 5V-CMOS. Annealing at elevated temperature to reduce ICC can also recover the input from 5V-CMOS back to 5V-PCI. Further investigation indicates that this is the worst case scenario; the 5V-PCI input is the most sensitive to radiation effect.

Additional input pins in the test design are measured to detect this abnormality; Tables 5a, 5b and 5c list the results. In summary, for 100-krad group two DUTs, 52552 and 52557, out of five show radiation-induced input threshold switching. For DUT 52552 three pins out of twelve show switching; for DUT 52557 one pin out of twelve shows switching. For 60-krad group, there is no DUT showing switching.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Total Dose	Pre-Irradiation		Post-Annealing	
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
52446	60 krad	1.24	1.51	1.38	1.45
52462	60 krad	1.25	1.52	1.22	1.53
52673	60 krad	1.25	1.51	1.24	1.48
52552	100 krad	1.25	1.52	1.23	1.49
52557	100 krad	1.24	1.51	2.41	2.67
52642	100 krad	1.23	1.50	1.24	1.56
52661	100 krad	1.25	1.51	1.26	1.48
52683	100 krad	1.26	1.52	1.41	1.57

Table 5a Additional Post-Annealing Input Thresholds

In/Out Pin:	DAH/QA0H		ENCNTR/YO0		ENCNTRH/YO0H		IDII0/IDIO0	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
52446	1.43	1.46	1.38	1.44	1.39	1.46	n/a	n/a
52462	1.39	1.5	1.41	1.47	1.41	1.49	1.21	1.56
52673	1.39	1.49	1.31	1.54	1.38	1.46	1.38	1.48
52552	2.59	2.63	1.42	1.48	2.57	2.64	1.4	1.55
52557	1.47	1.51	1.44	1.47	1.45	1.49	1.43	1.51
52642	1.39	1.53	1.35	1.49	1.38	1.5	1.4	1.53
52661	1.41	1.48	1.38	1.48	1.35	1.49	1.36	1.55
52683	1.42	1.52	1.43	1.49	1.42	1.49	1.41	1.49

Table 5b Additional Post-Annealing Input Thresholds

In/Out Pin:	IDII1/IDIO1		IDII2/IDIO2		IDII3/IDIO3		IDII4/IDIO4	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
52446	1.39	1.45	1.38	1.46	1.38	1.45	1.39	1.45
52462	1.4	1.52	1.39	1.55	NA	NA	1.38	1.44
52673	1.37	1.47	1.37	1.47	1.32	1.46	1.36	1.45
52552	1.37	1.49	1.43	1.49	1.41	1.49	2.61	2.66
52557	1.47	1.51	1.45	1.51	1.42	1.48	1.42	1.48
52642	1.39	1.49	n/a	n/a	1.4	1.62	1.51	1.63
52661	1.38	1.45	1.43	1.51	1.31	1.56	1.4	1.48
52683	1.44	1.47	1.44	1.48	1.42	1.47	1.43	1.47

Table 5c Additional Post-Annealing Input Thresholds

In/Out Pin:	IDII5/IDIO5		IDII6/IDIO6		IDII7/IDIO7	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
52446	1.38	1.45	1.38	1.46	1.4	1.45
52462	1.38	1.45	1.22	1.58	1.41	1.49
52673	1.34	1.46	1.38	1.48	1.37	1.44
52552	1.41	1.47	1.38	1.54	1.36	1.46
52557	1.44	1.51	1.48	1.54	1.45	1.48
52642	1.37	1.49	1.37	1.57	1.37	1.48
52661	1.36	1.43	1.13	1.64	1.39	1.49
52683	1.42	1.49	1.43	1.5	1.42	1.48

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 6 and 7. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 6 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
52446	0.009	0.009	0.103	0.104	0.172	0.173	0.434	0.437	0.893	0.899
52462	0.009	0.009	0.103	0.103	0.171	0.172	0.432	0.435	0.890	0.895
52673	0.009	0.009	0.102	0.104	0.171	0.173	0.432	0.438	0.889	0.900
52552	0.009	0.009	0.102	0.105	0.171	0.174	0.431	0.440	0.887	0.906
52557	0.009	0.009	0.101	0.103	0.168	0.171	0.425	0.432	0.875	0.891
52642	0.009	0.009	0.101	0.102	0.169	0.170	0.425	0.429	0.876	0.883
52661	0.008	0.009	0.101	0.104	0.169	0.174	0.426	0.438	0.878	0.902
52683	0.009	0.009	0.102	0.104	0.171	0.174	0.431	0.439	0.886	0.902

Table 7 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
52446	4.99	4.99	4.87	4.86	4.65	4.65	4.06	4.07	2.76	2.77
52462	4.99	4.98	4.86	4.86	4.64	4.65	4.04	4.06	2.68	2.71
52673	4.99	4.99	4.86	4.86	4.64	4.64	4.05	4.05	2.72	2.70
52552	4.98	4.98	4.86	4.86	4.66	4.64	4.07	4.06	2.77	2.72
52557	4.98	4.98	4.86	4.86	4.65	4.64	4.07	4.05	2.78	2.66
52642	4.98	4.98	4.86	4.86	4.65	4.64	4.07	4.06	2.77	2.71
52661	4.98	4.98	4.86	4.86	4.65	4.63	4.05	4.03	2.70	2.58
52683	4.98	4.99	4.86	4.86	4.64	4.65	4.06	4.06	2.75	2.69

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. In every case, the DUT passed the 10% degradation criterion.

Table 8 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation	Post-Annealing	Degradation
52446	529.49	532.68	0.61%
52462	519.29	521.67	0.47%
52673	523.57	524.07	0.11%
52552	514.89	540.74	5.04%
52557	516.93	541.84	4.86%
52642	510.12	534.59	4.83%
52661	513.32	534.52	4.17%
52683	501.49	520.65	3.86%

F. Transition Time

Figures 10 to 41 show the pre- and post-annealing transition rising and falling edges. Only the falling edge of DUT 52553 and 52557 shows visible degradation. These two DUTs also are the only ones showing input threshold switching.

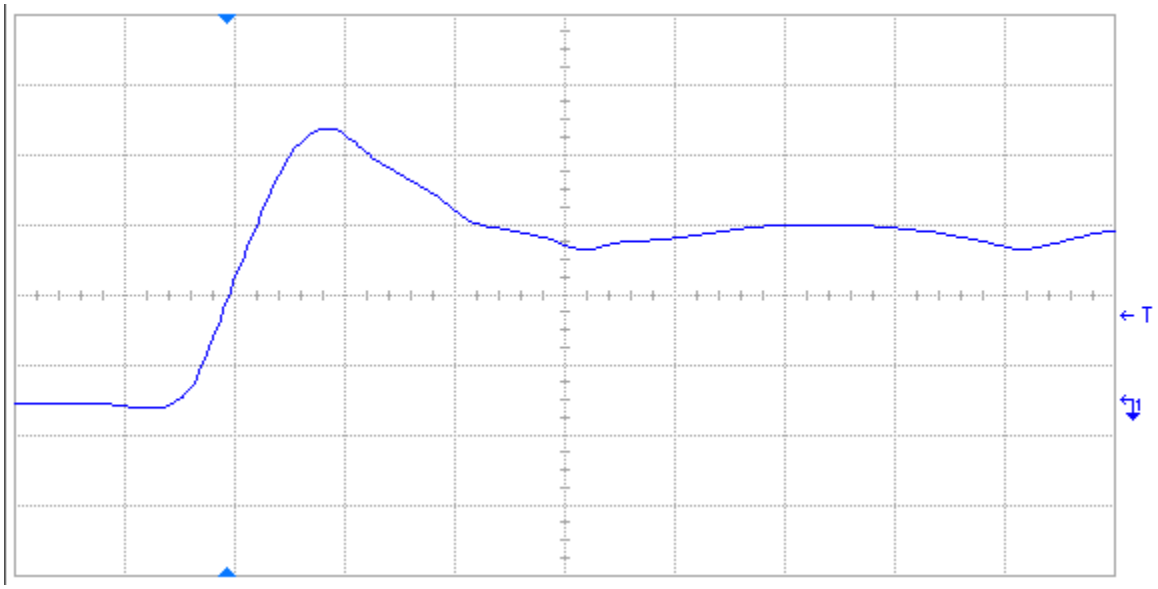


Figure 10 Pre-annealing rising edge of DUT 52446, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

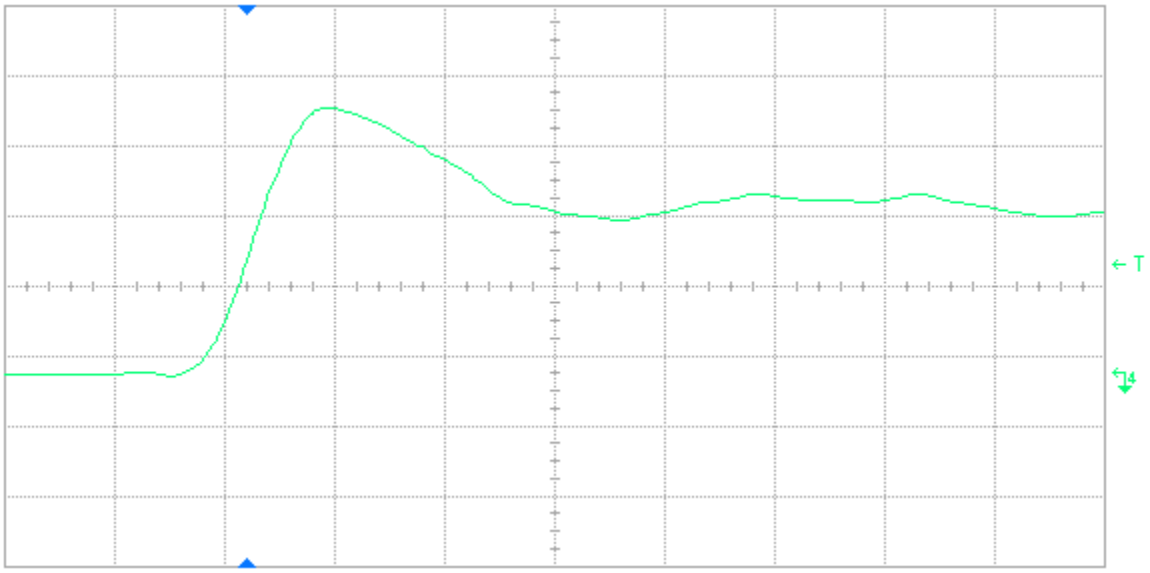


Figure 11 Post-annealing rising edge of DUT 52446, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

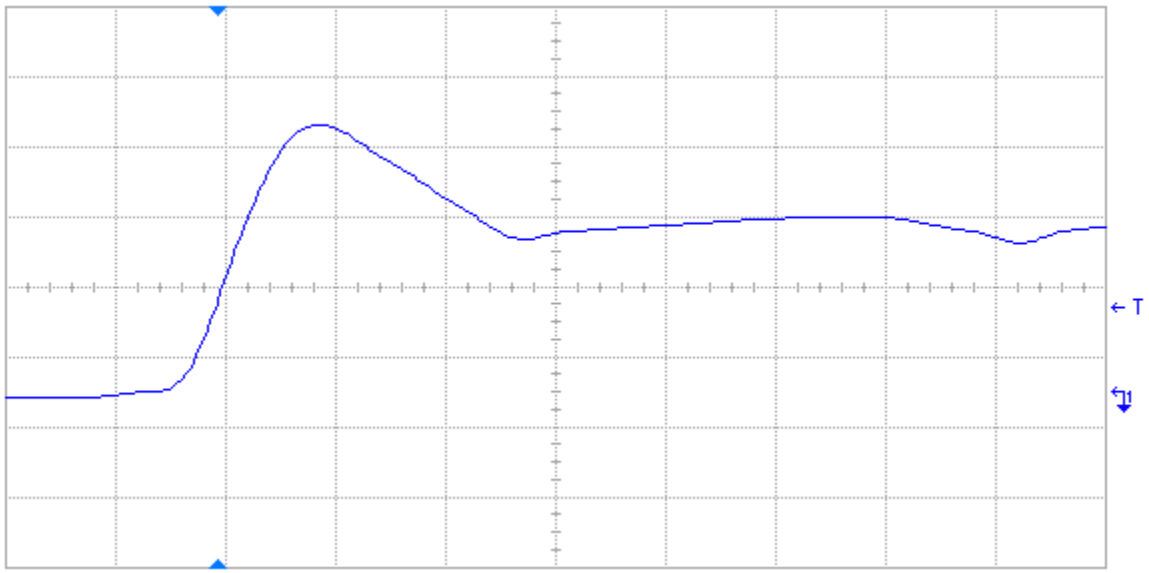


Figure 12 Pre-annealing rising edge of DUT 52462, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

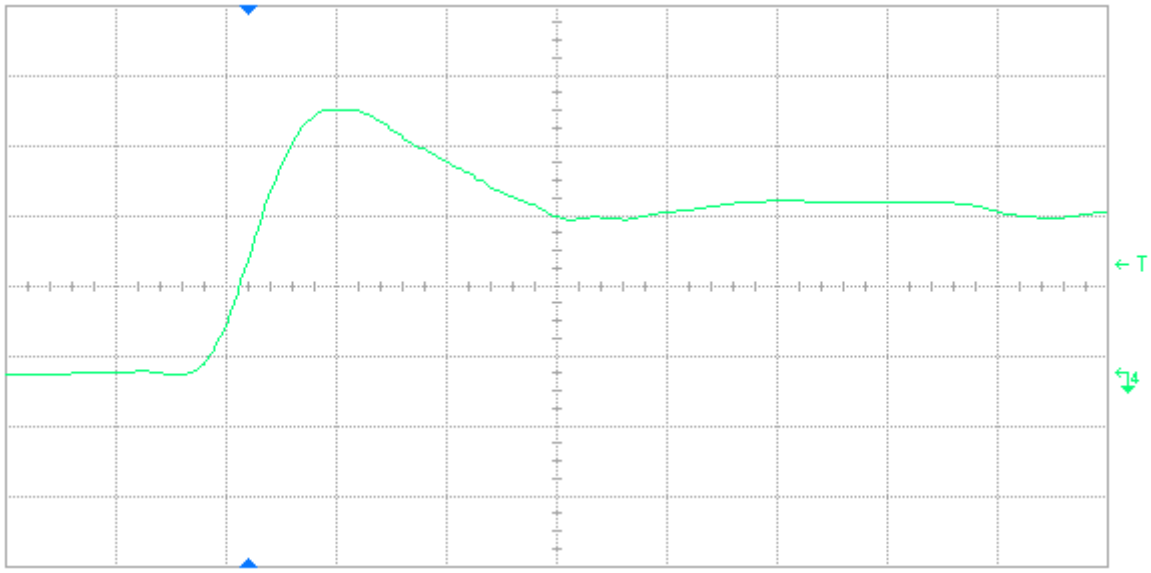


Figure 13 Post-annealing rising edge of DUT 52462, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

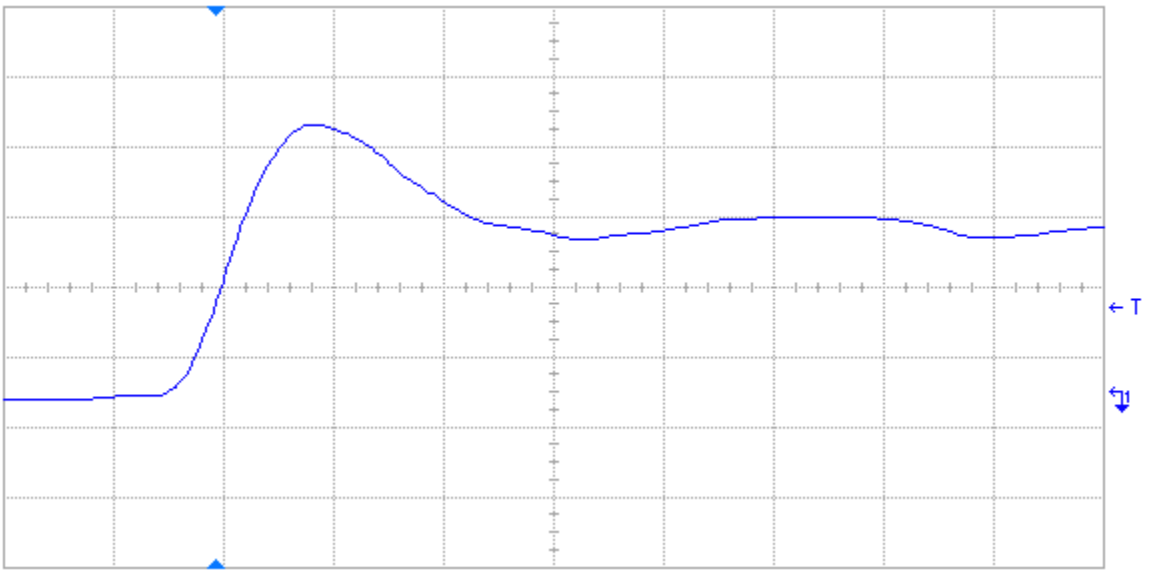


Figure 14 Pre-annealing rising edge of DUT 52673, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

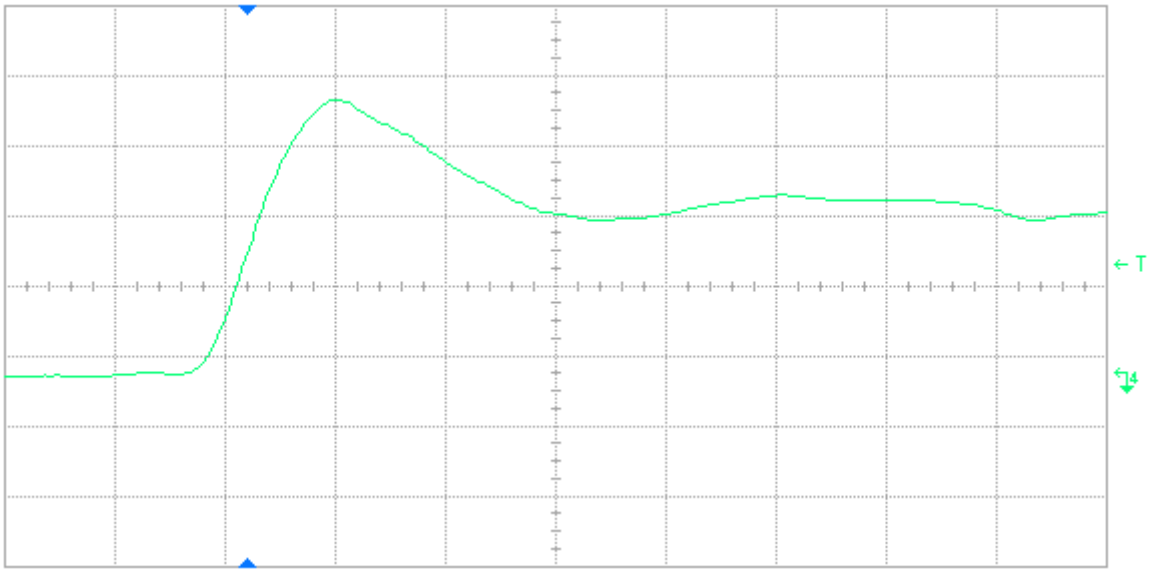


Figure 15 Post-annealing rising edge of DUT 52673, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

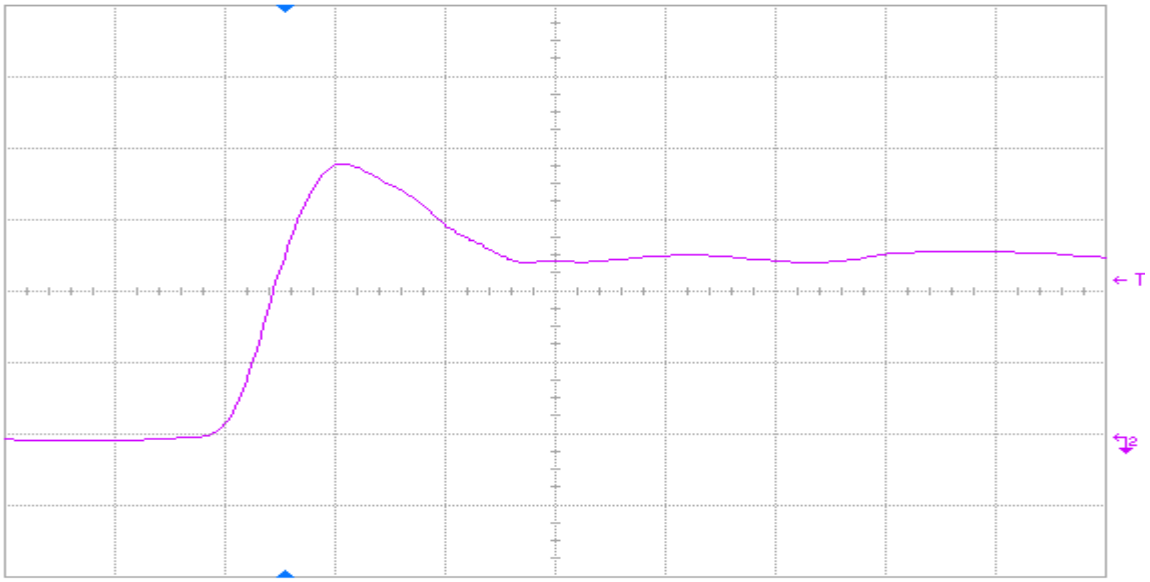


Figure 16 Pre-annealing rising edge of DUT 52552, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

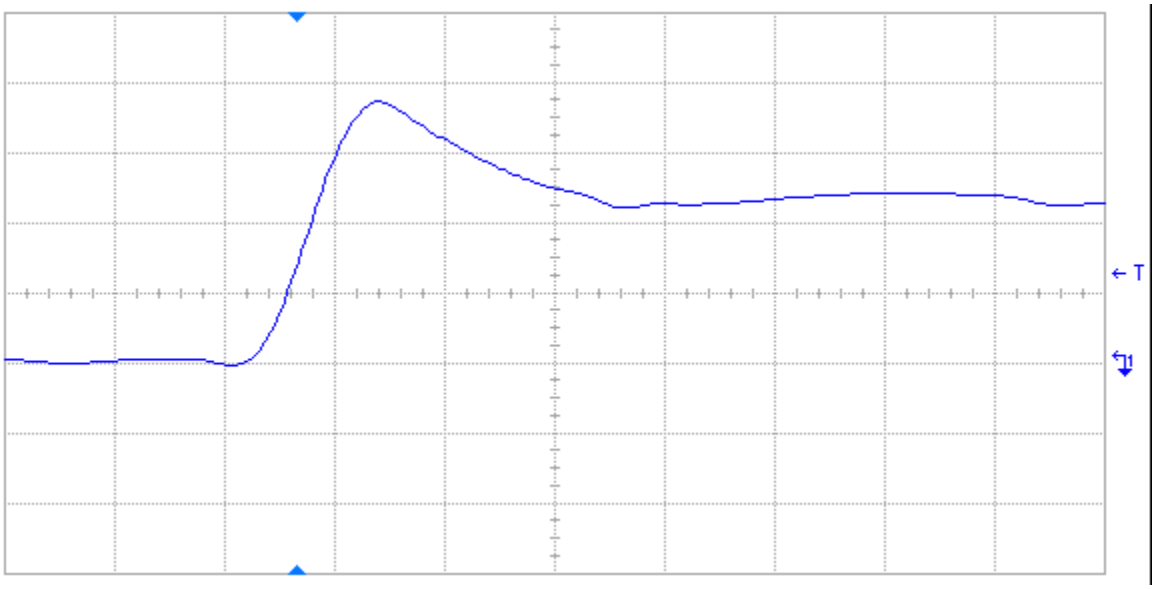


Figure 17 Post-annealing rising edge of DUT 52552, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

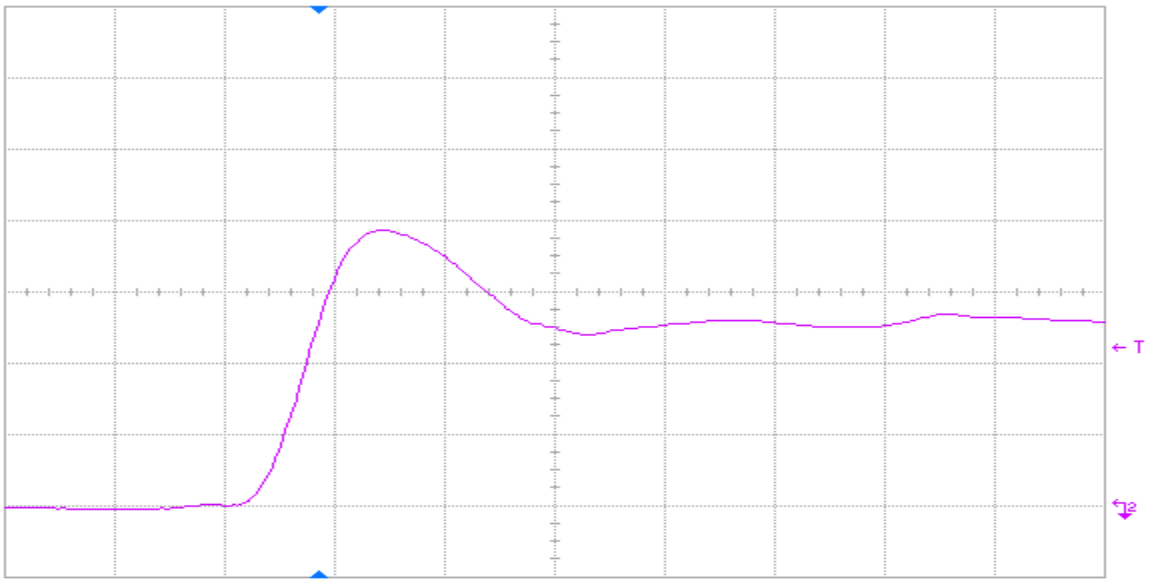


Figure 18 Pre-annealing rising edge of DUT 52557, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

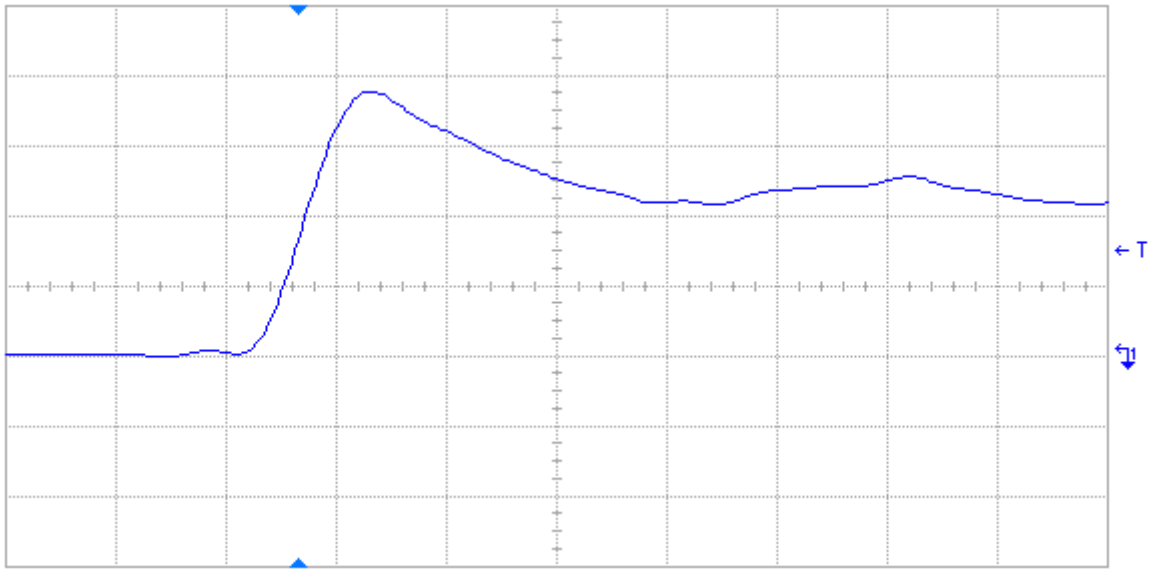


Figure 19 Post-annealing rising edge of DUT 52557, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

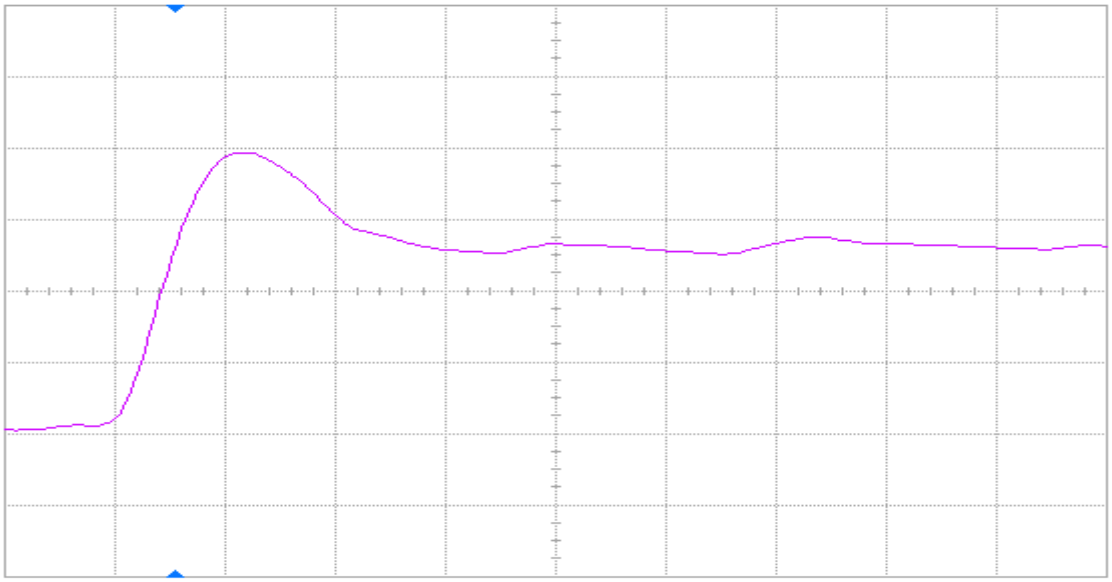


Figure 20 Pre-annealing rising edge of DUT 52642, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

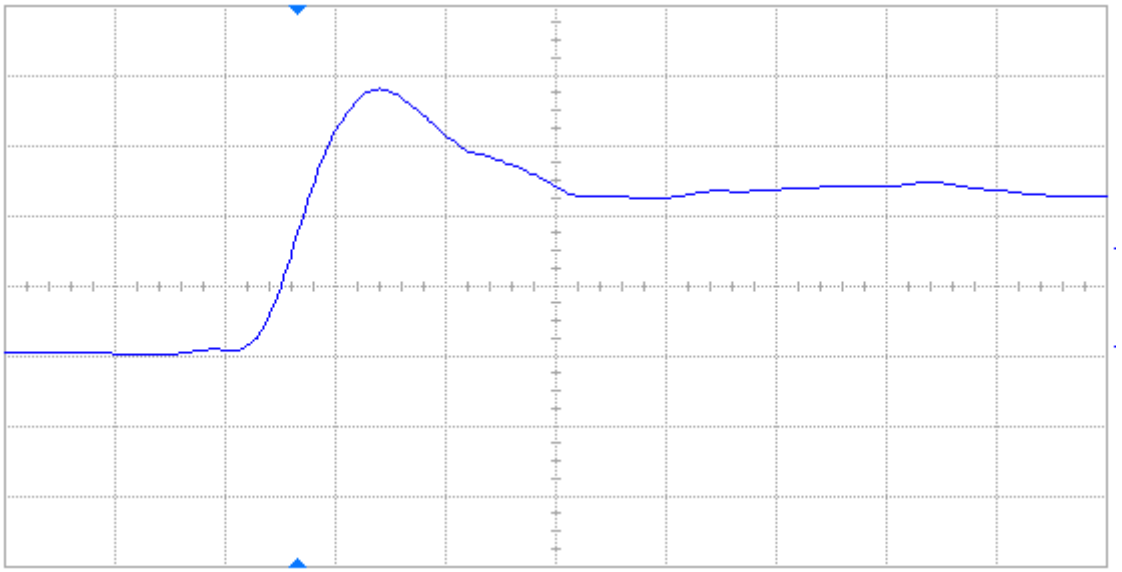


Figure 21 Post-annealing rising edge of DUT 52642, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

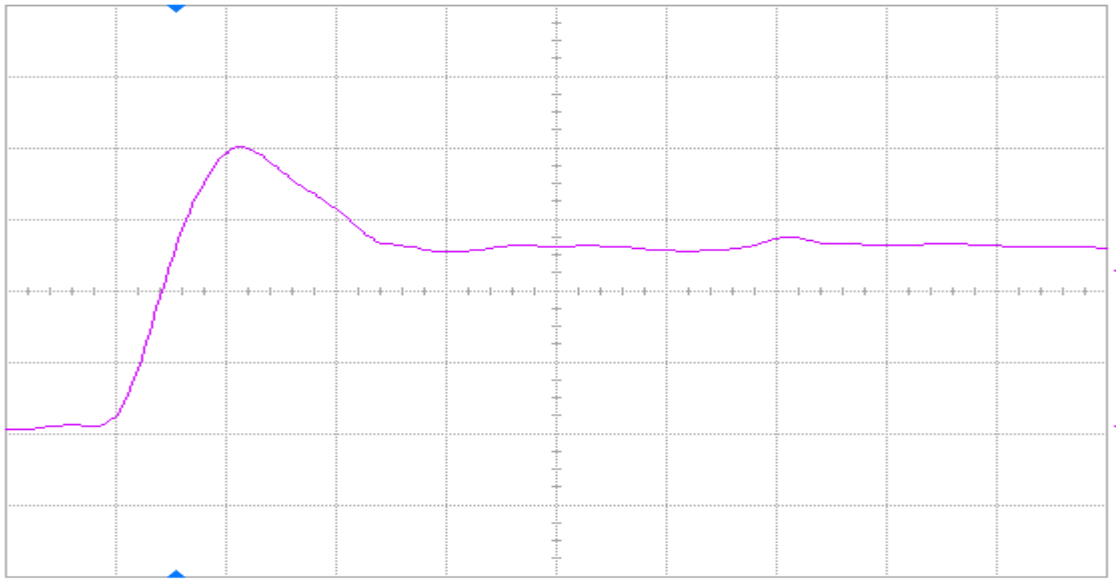


Figure 22 Pre-annealing rising edge of DUT 52661, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

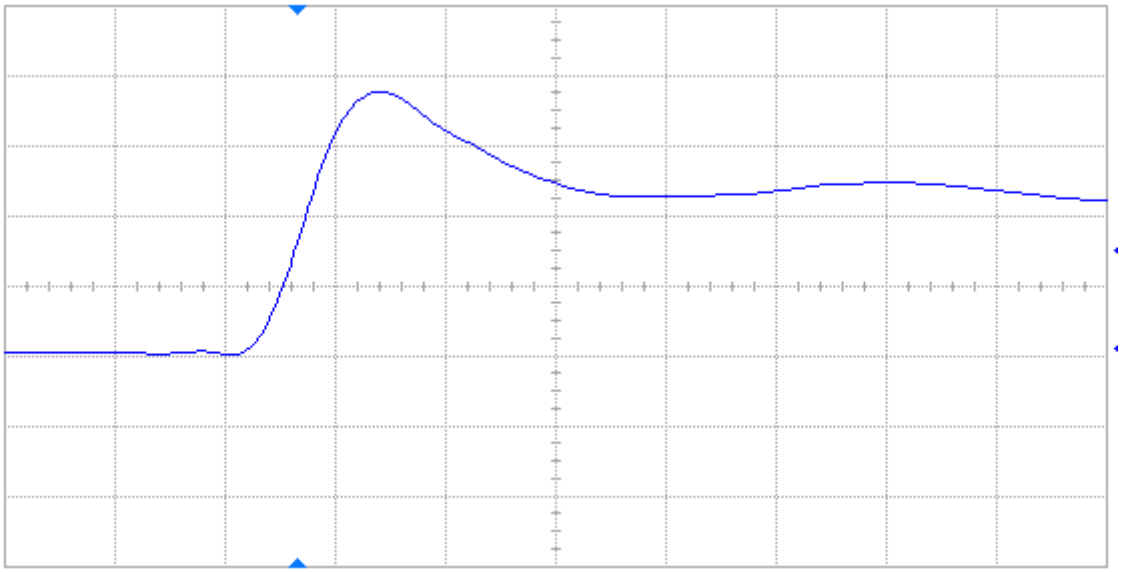


Figure 23 Post-annealing rising edge of DUT 52661, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

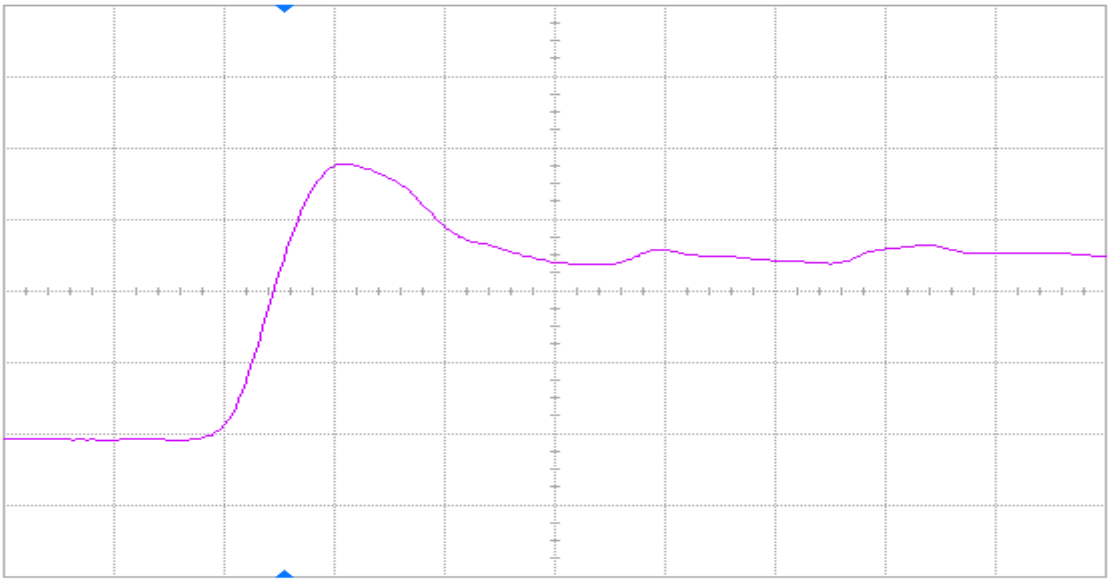


Figure 24 Pre-annealing rising edge of DUT 52683, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

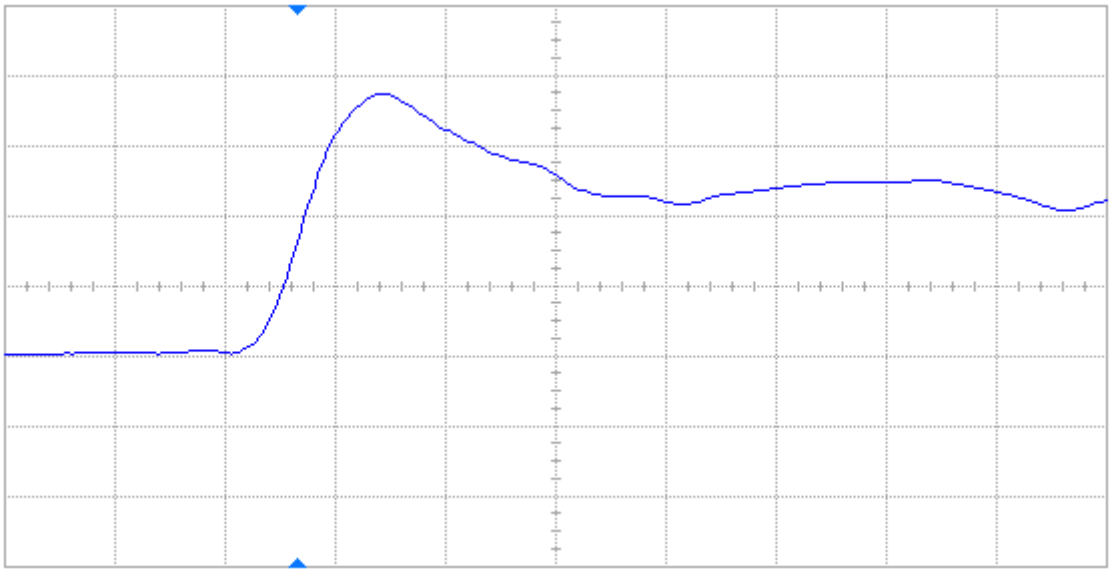


Figure 25 Post-annealing rising edge of DUT 52683, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

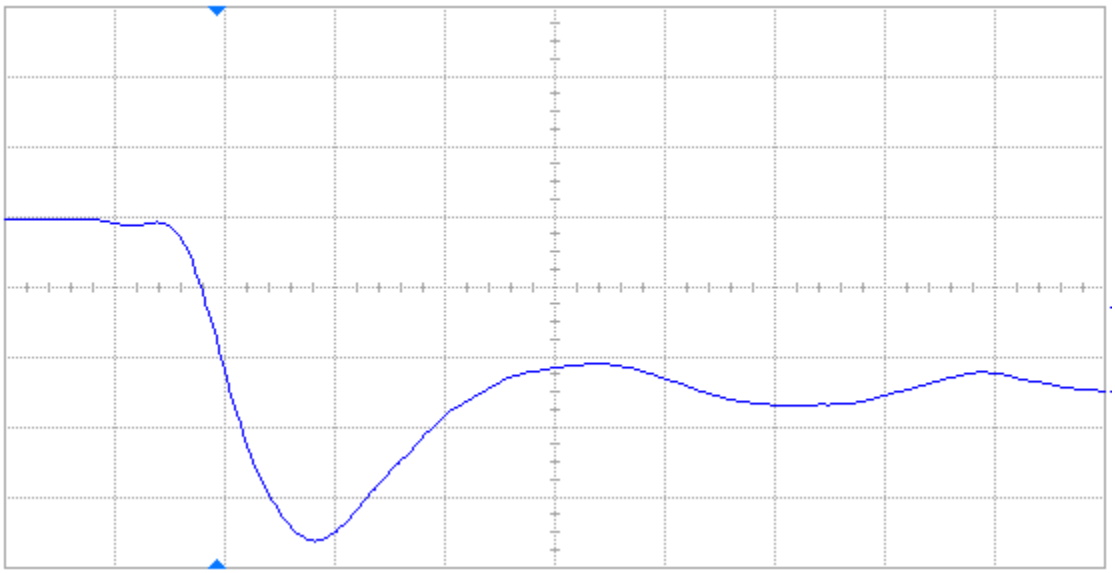


Figure 26 Pre-annealing falling edge of DUT 52446, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

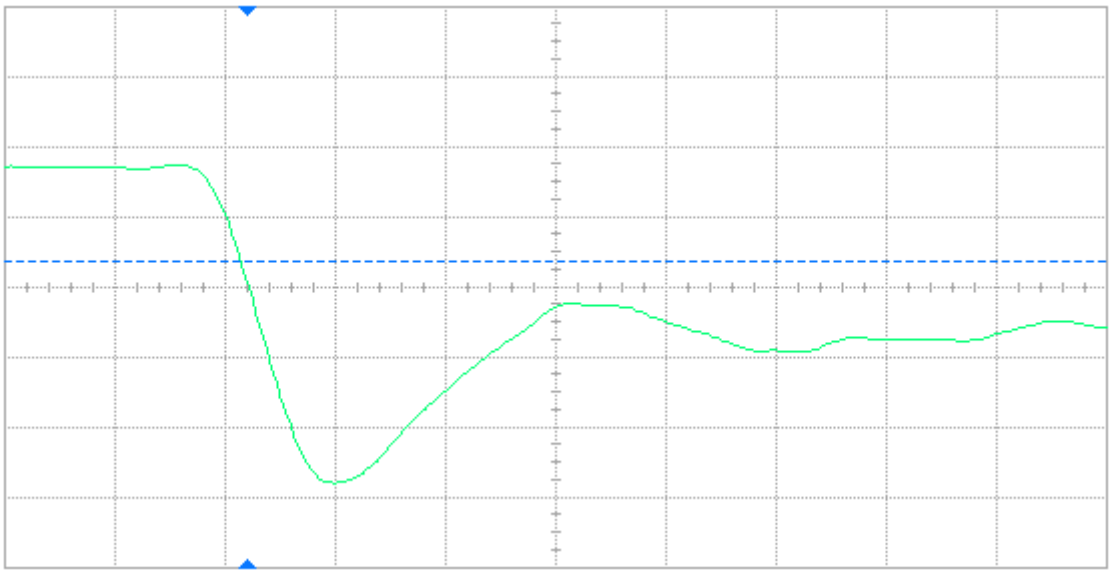


Figure 27 Post-annealing falling edge of DUT 52446, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

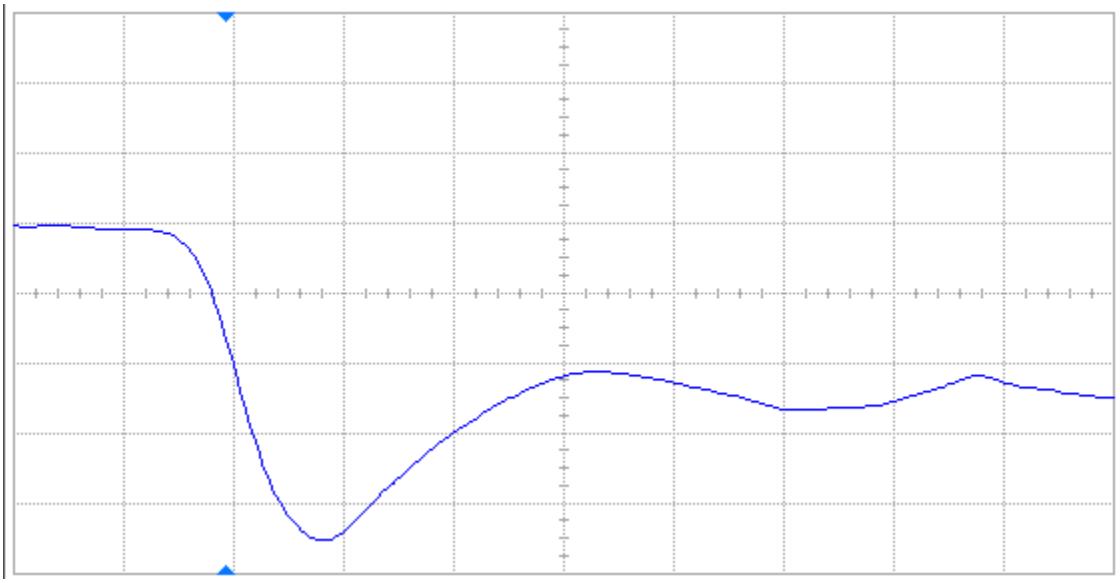


Figure 28 Pre-annealing falling edge of DUT 52462, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

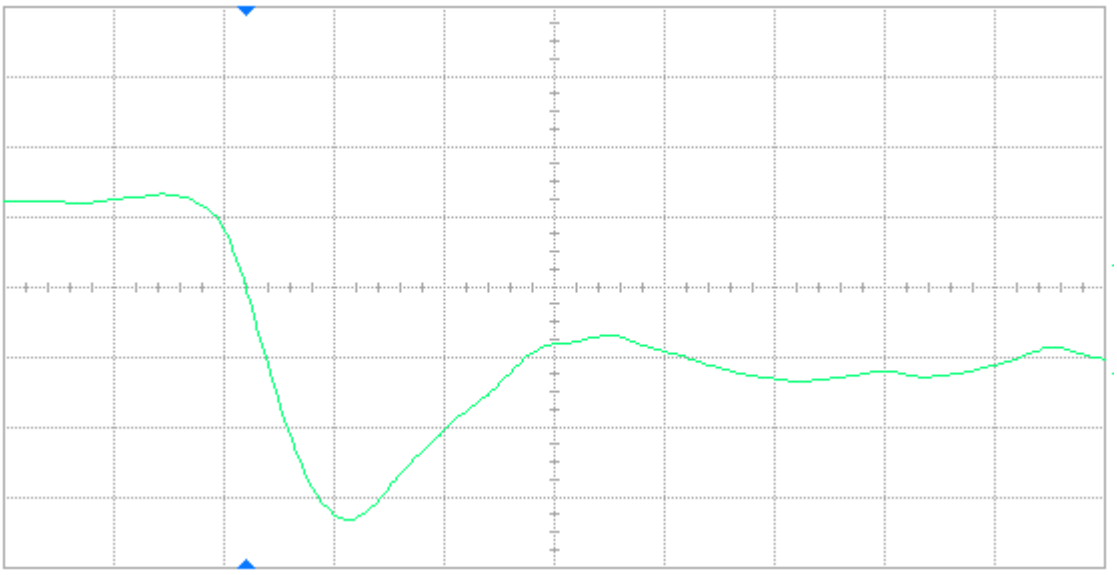


Figure 29 Post-annealing falling edge of DUT 52462, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

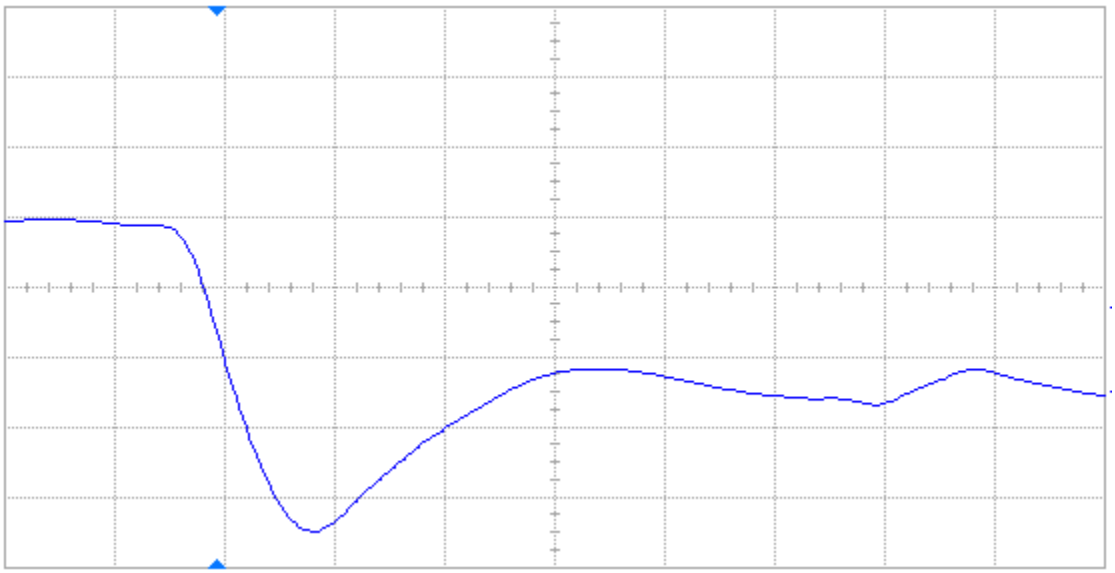


Figure 30 Pre-annealing falling edge of DUT 52673, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

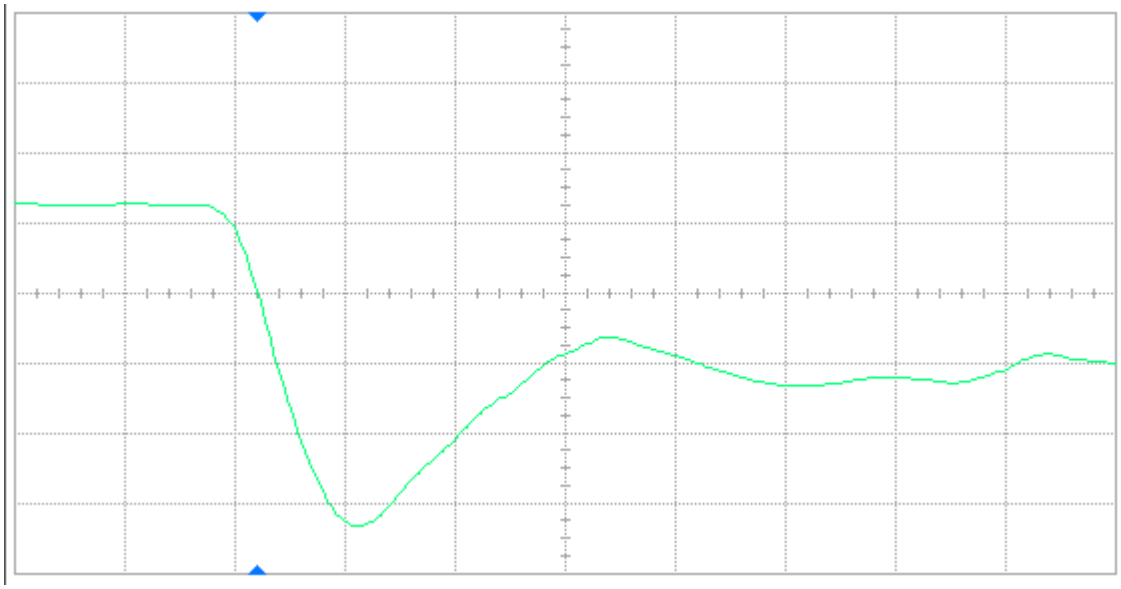


Figure 31 Post-annealing falling edge of DUT 52673, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

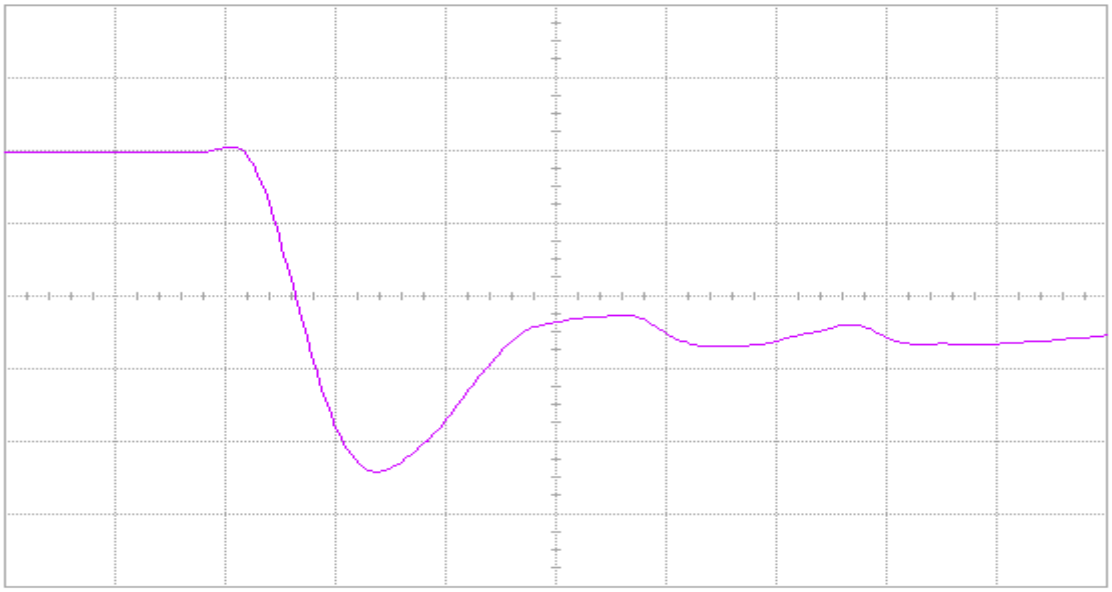


Figure 32 Pre-annealing falling edge of DUT 52552, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

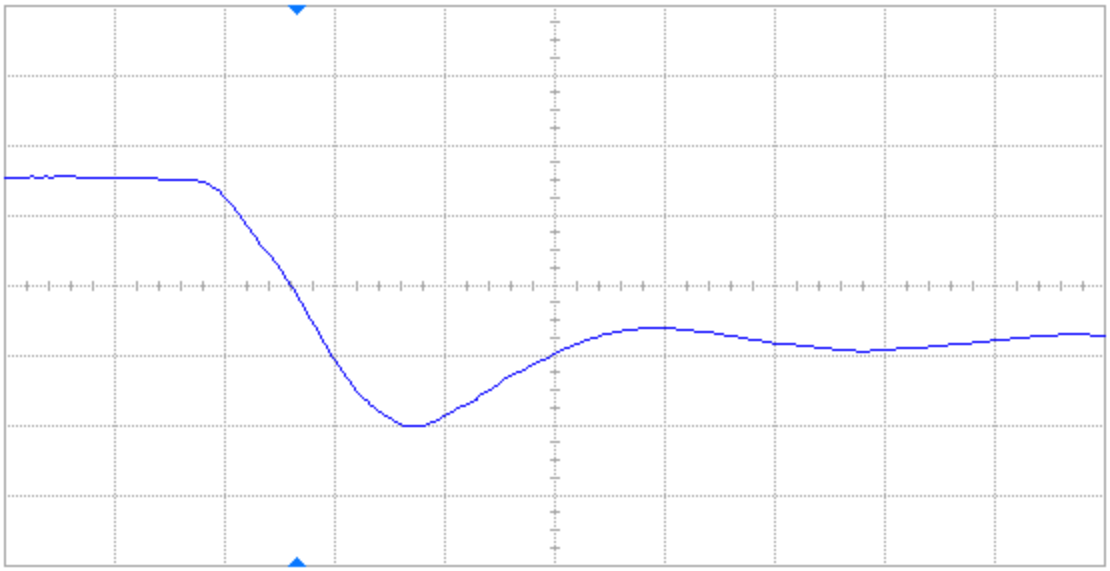


Figure 33 Post-annealing falling edge of DUT 52552, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

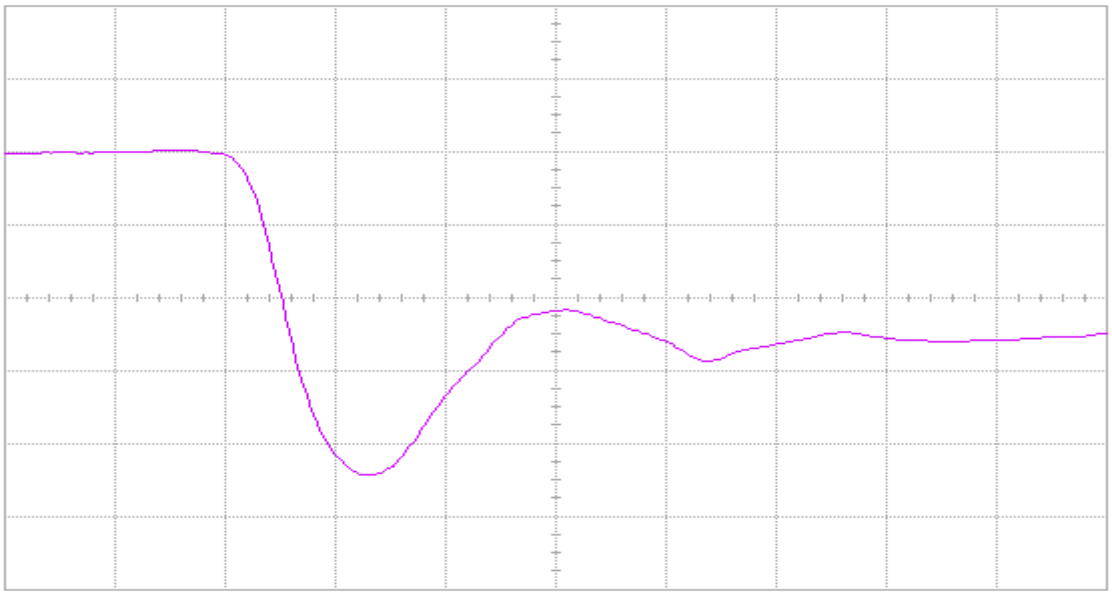


Figure 34 Pre-annealing falling edge of DUT 52557, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

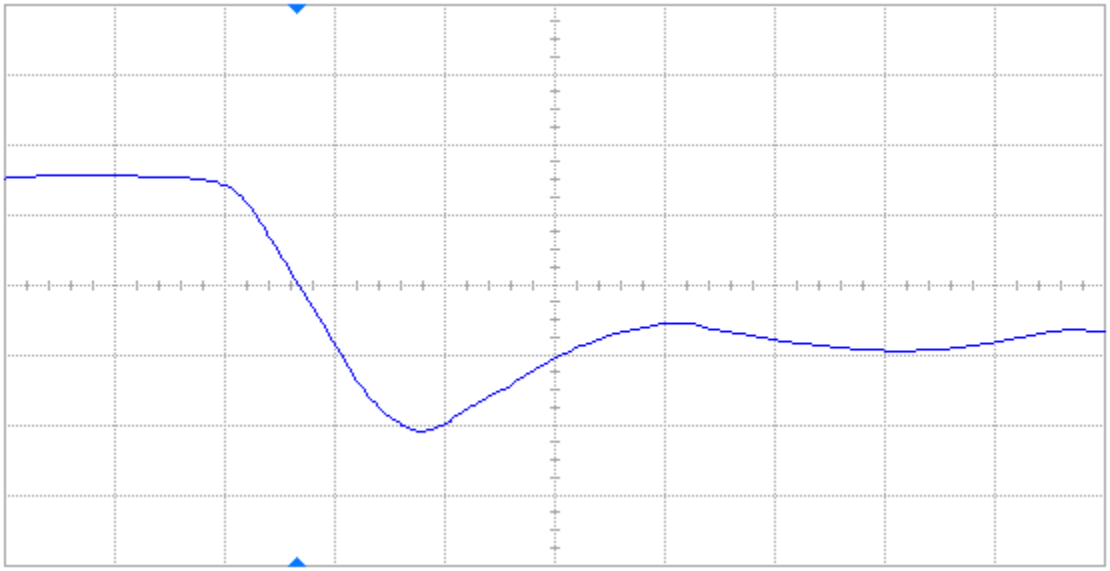


Figure 35 Post-annealing falling edge of DUT 52557, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

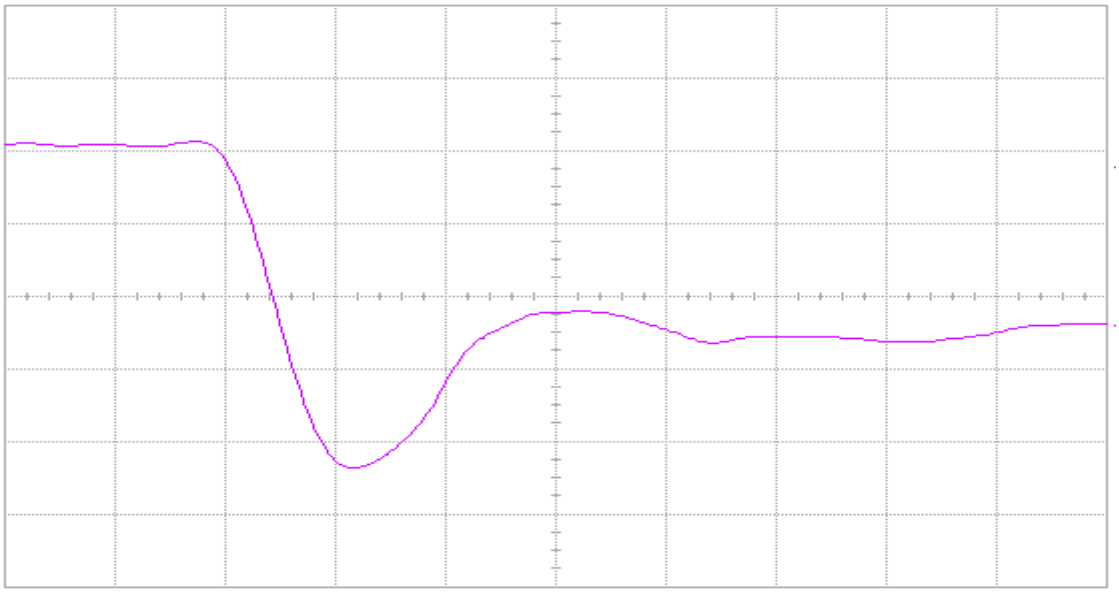


Figure 36 Pre-annealing falling edge of DUT 52642, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

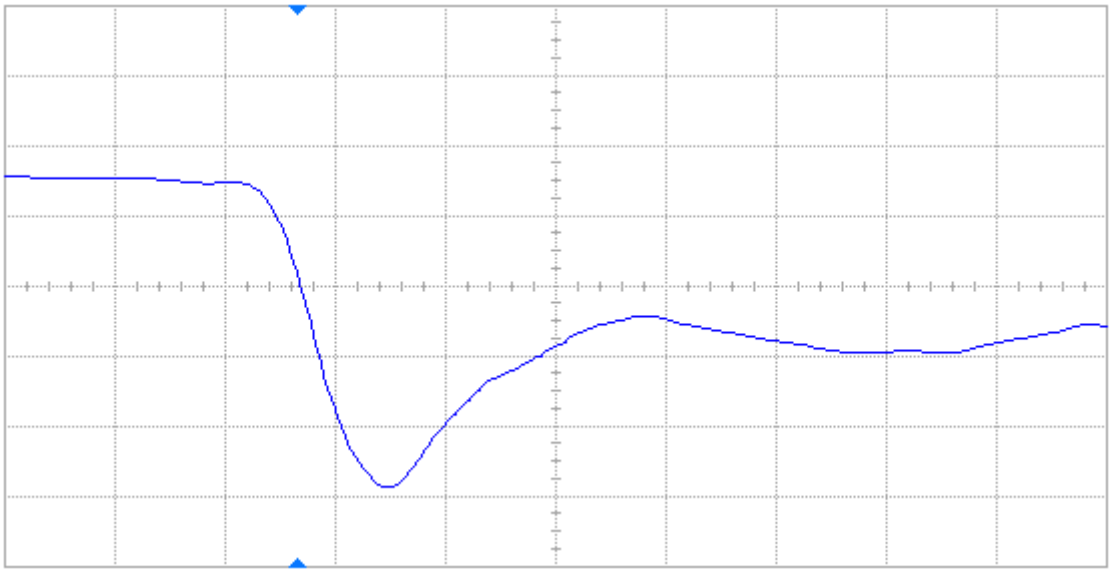


Figure 37 Post-annealing falling edge of DUT 52642, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

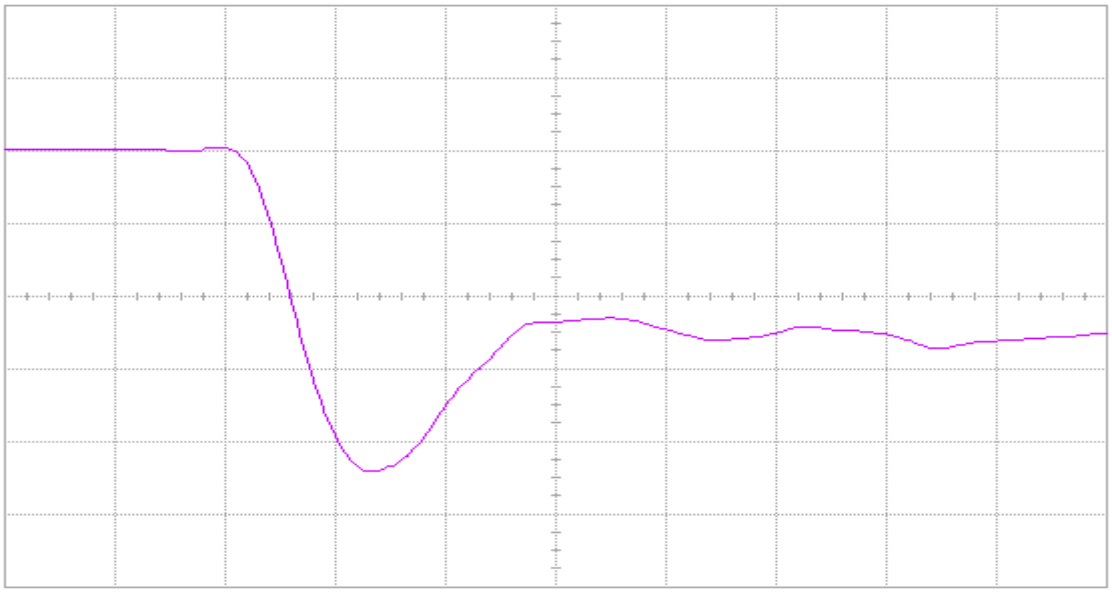


Figure 38 Pre-annealing falling edge of DUT 52661, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

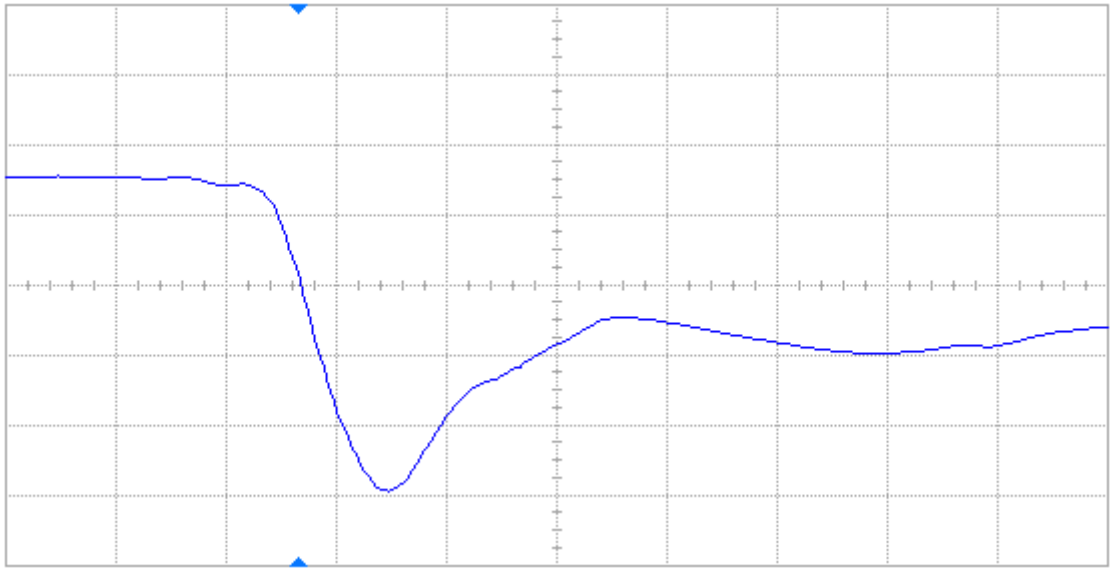


Figure 39 Post-annealing falling edge of DUT 52661, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

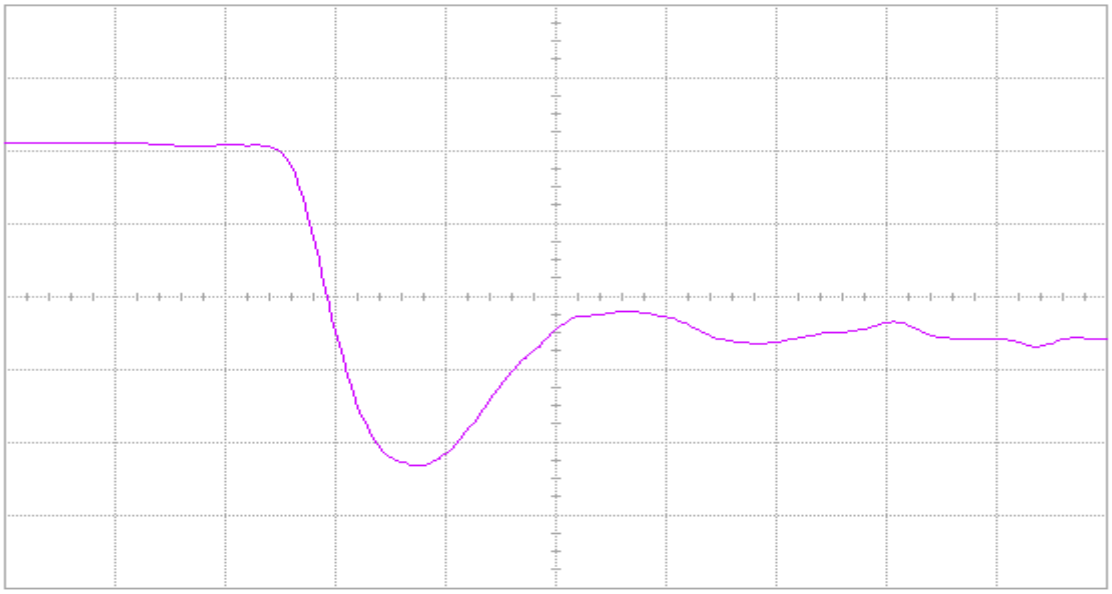


Figure 40 Pre-annealing falling edge of DUT 52683, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

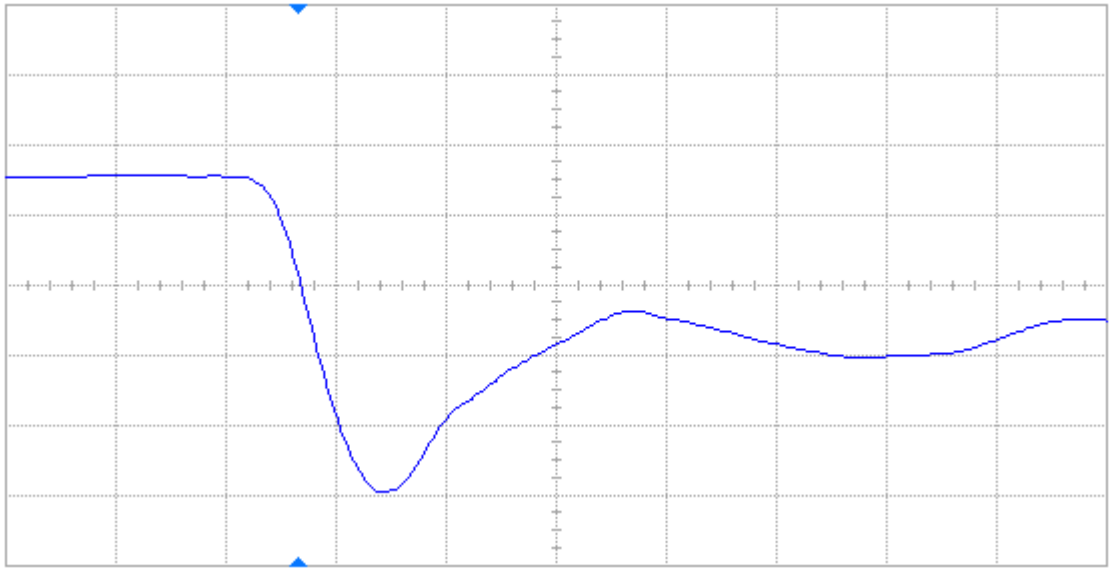
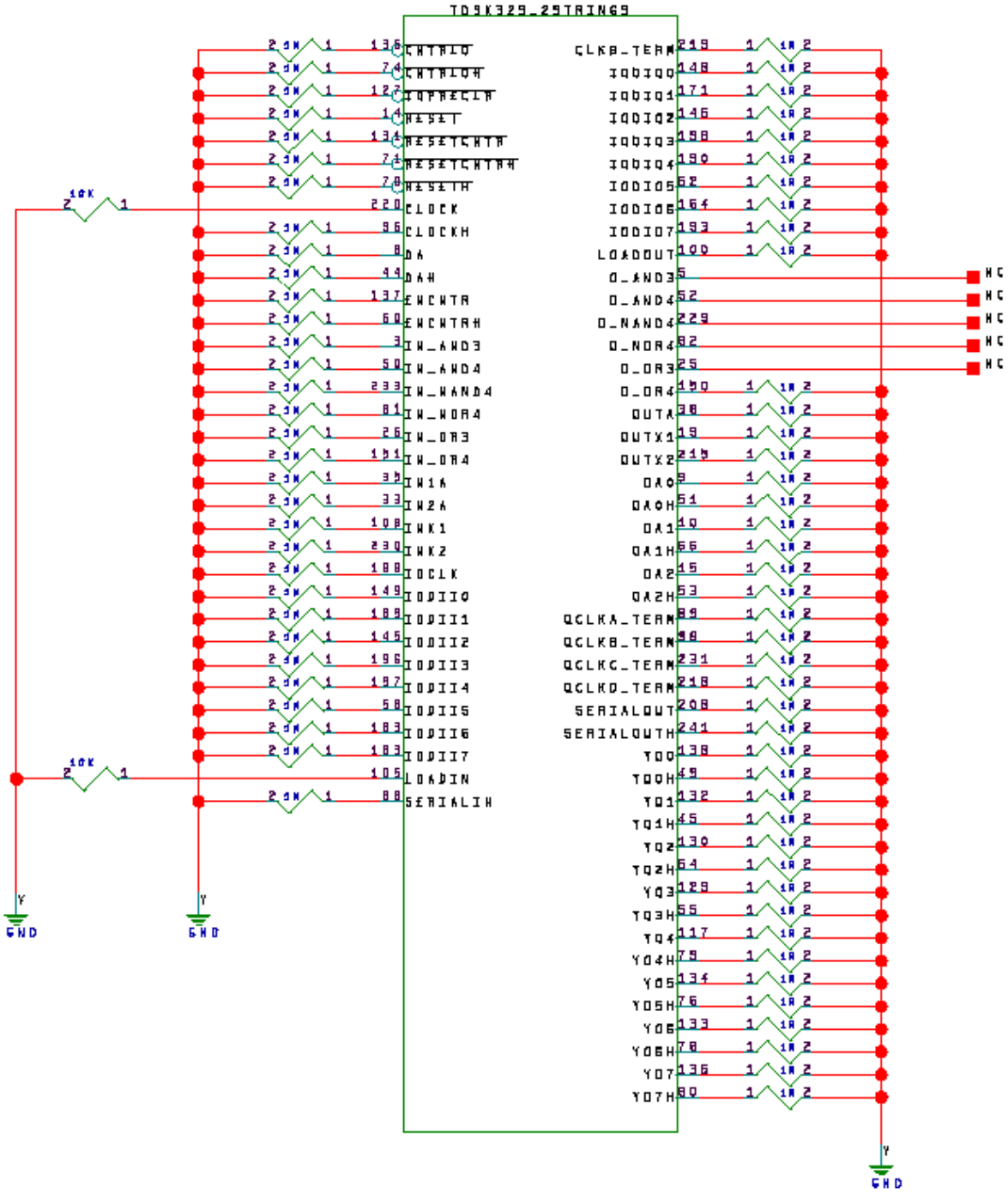
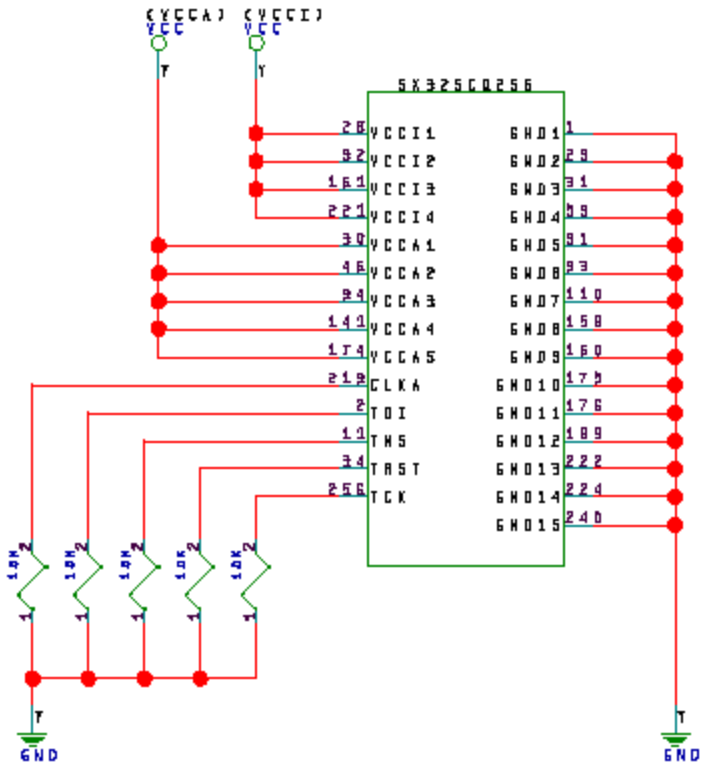


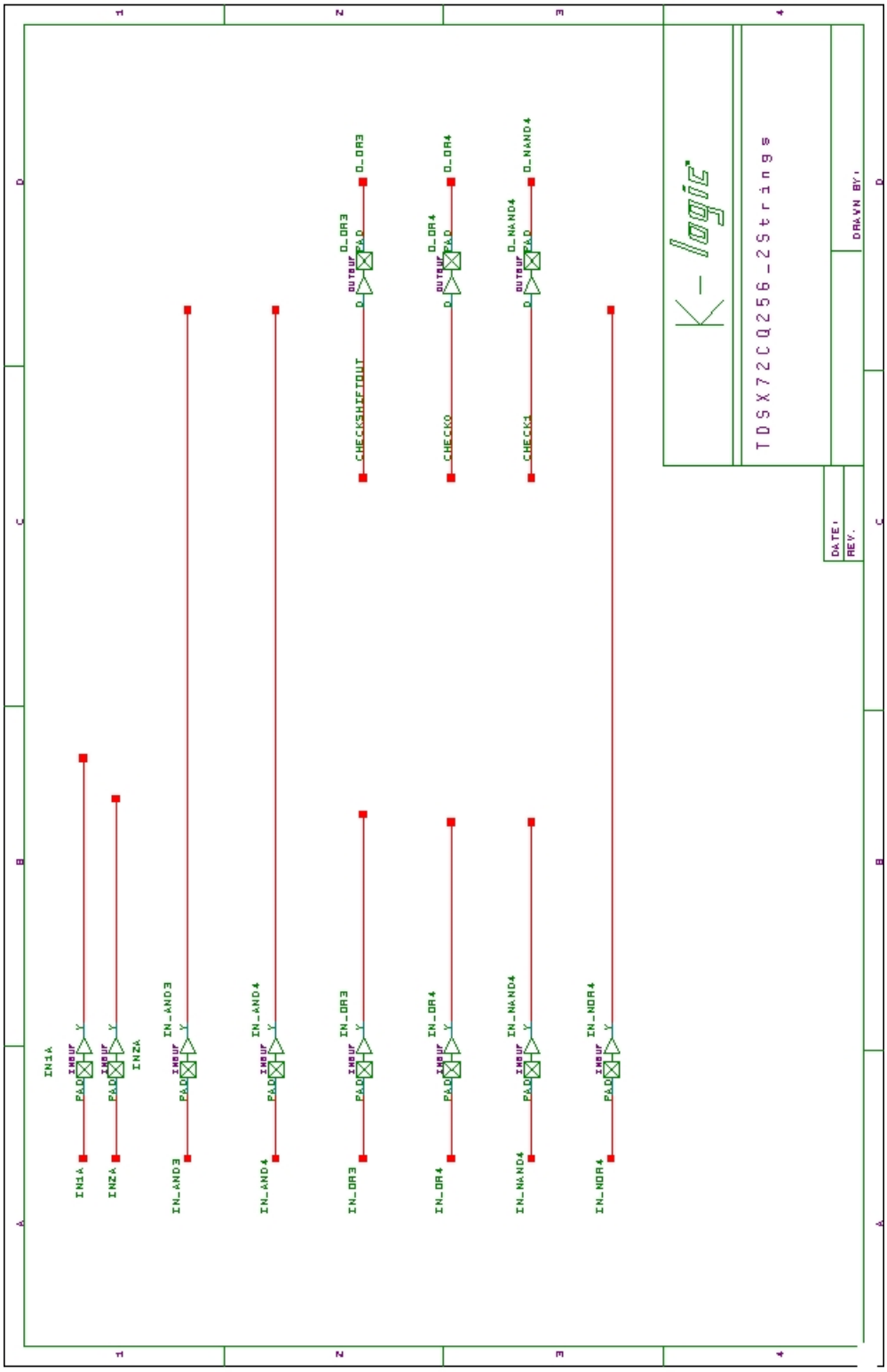
Figure 41 Post-annealing falling edge of DUT 52683, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

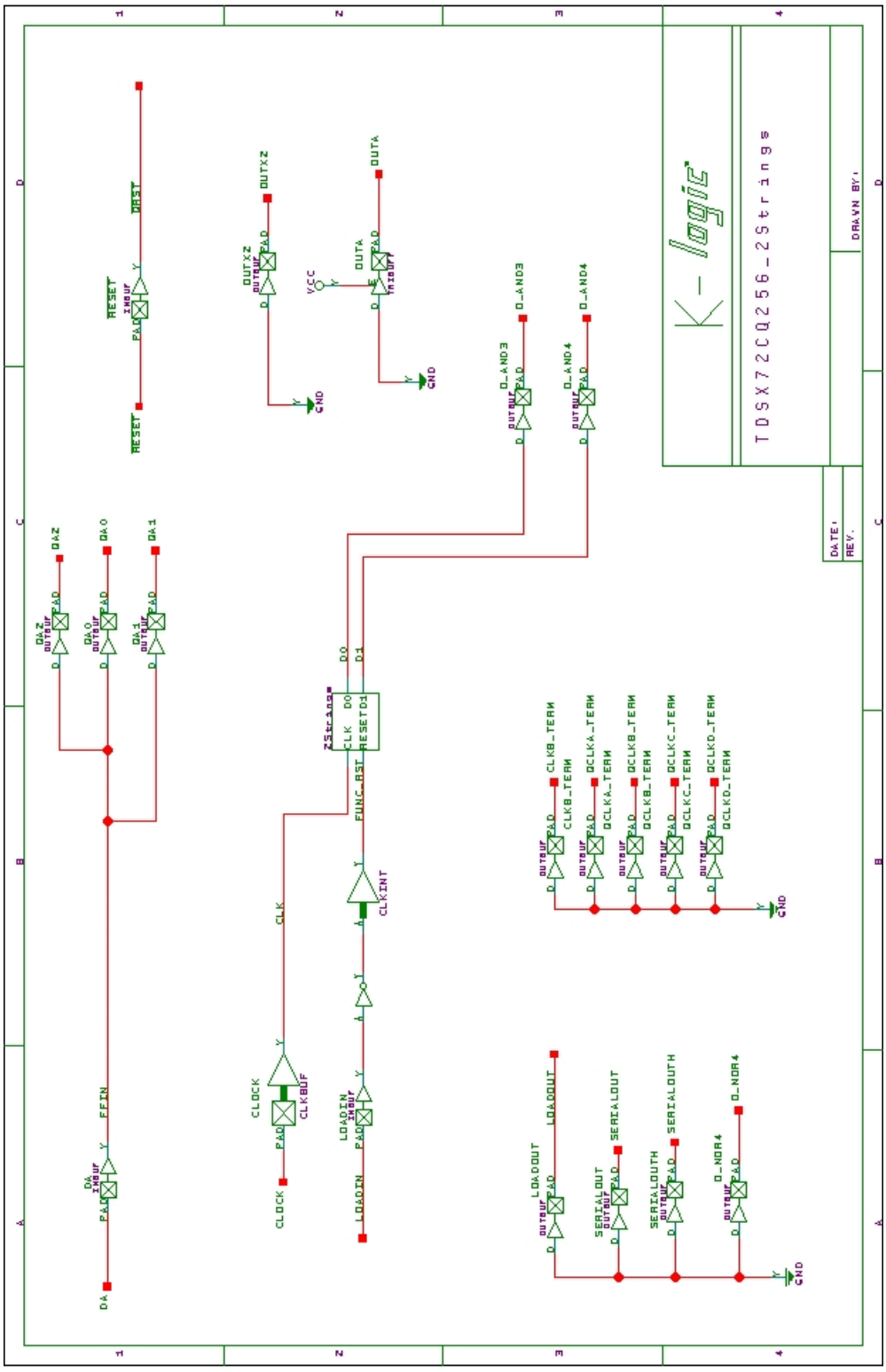
Appendix A DUT Bias

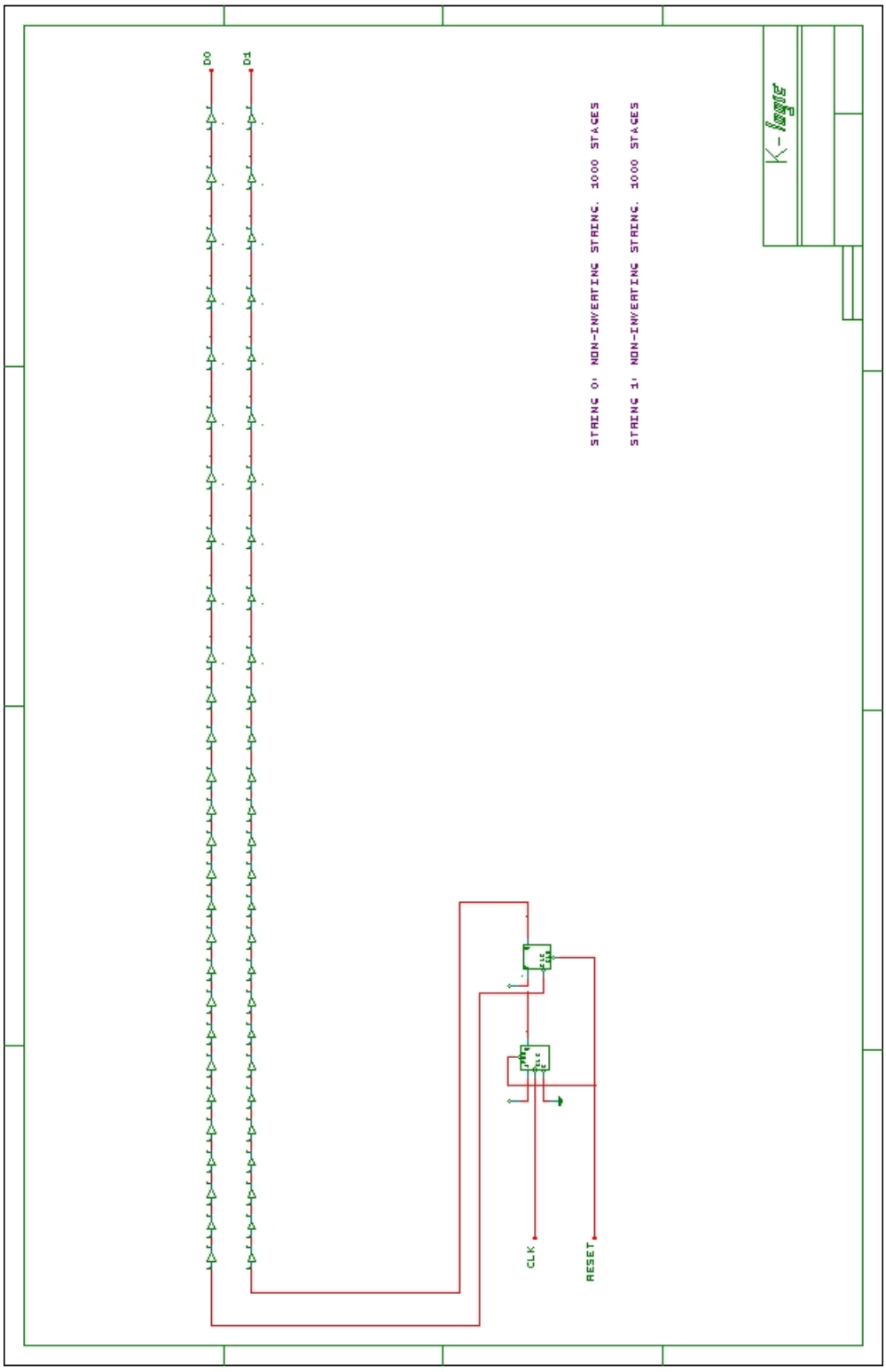


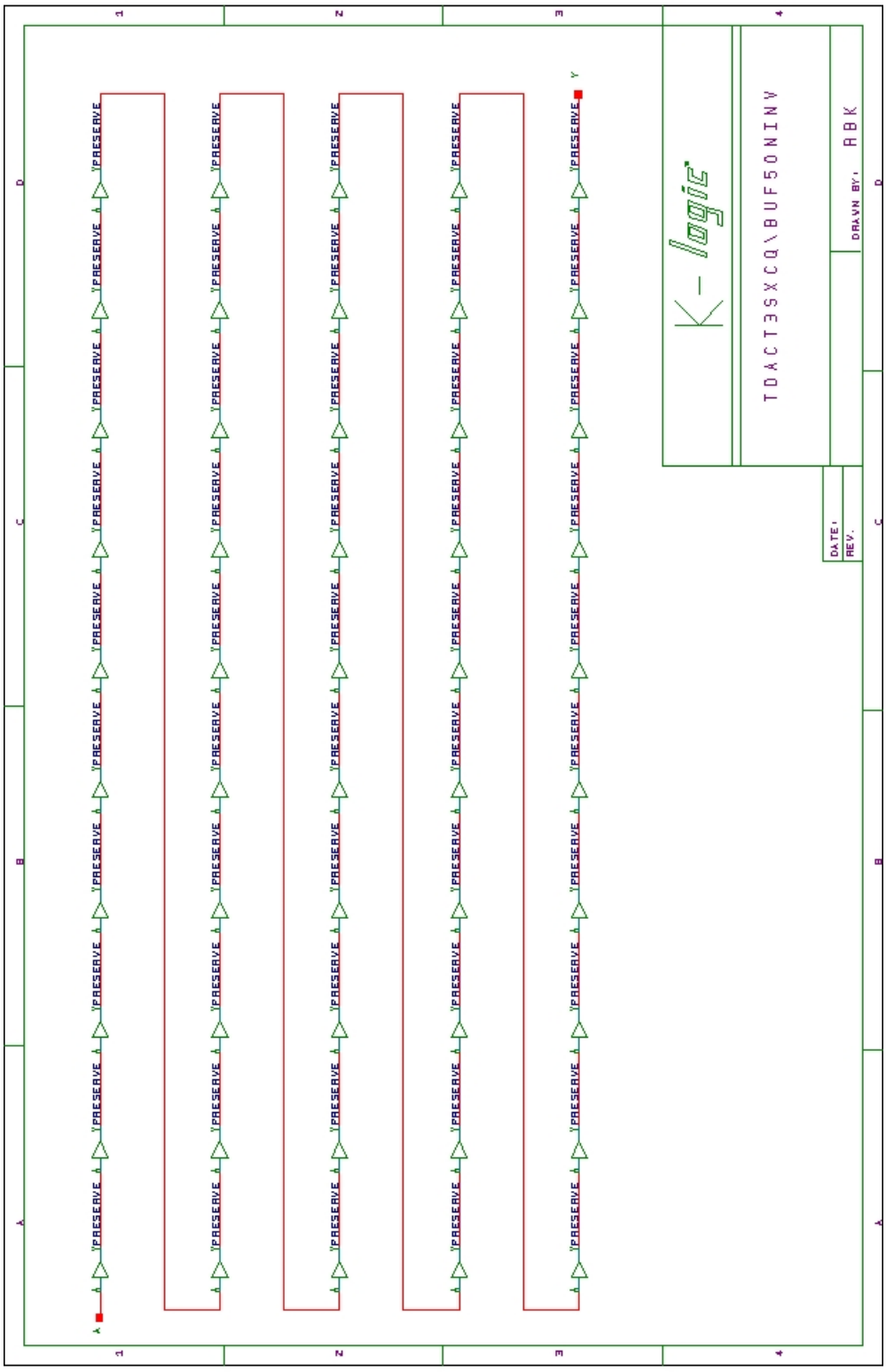

(VCCA)
VCC
(VCCI)
VCC
5X325CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
CLKA
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
10K
10K
10K
10K
10K
GND
GND

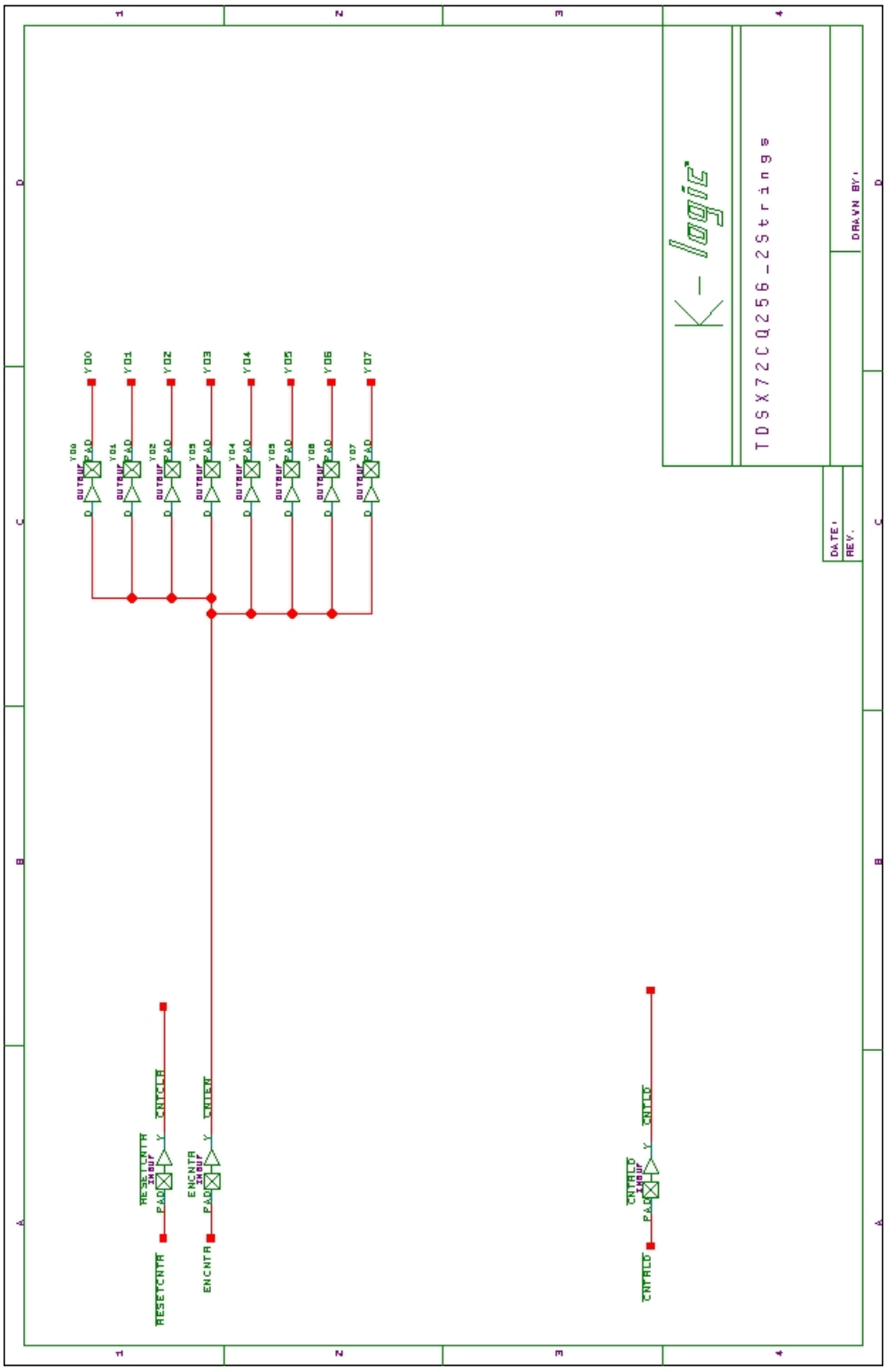
APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

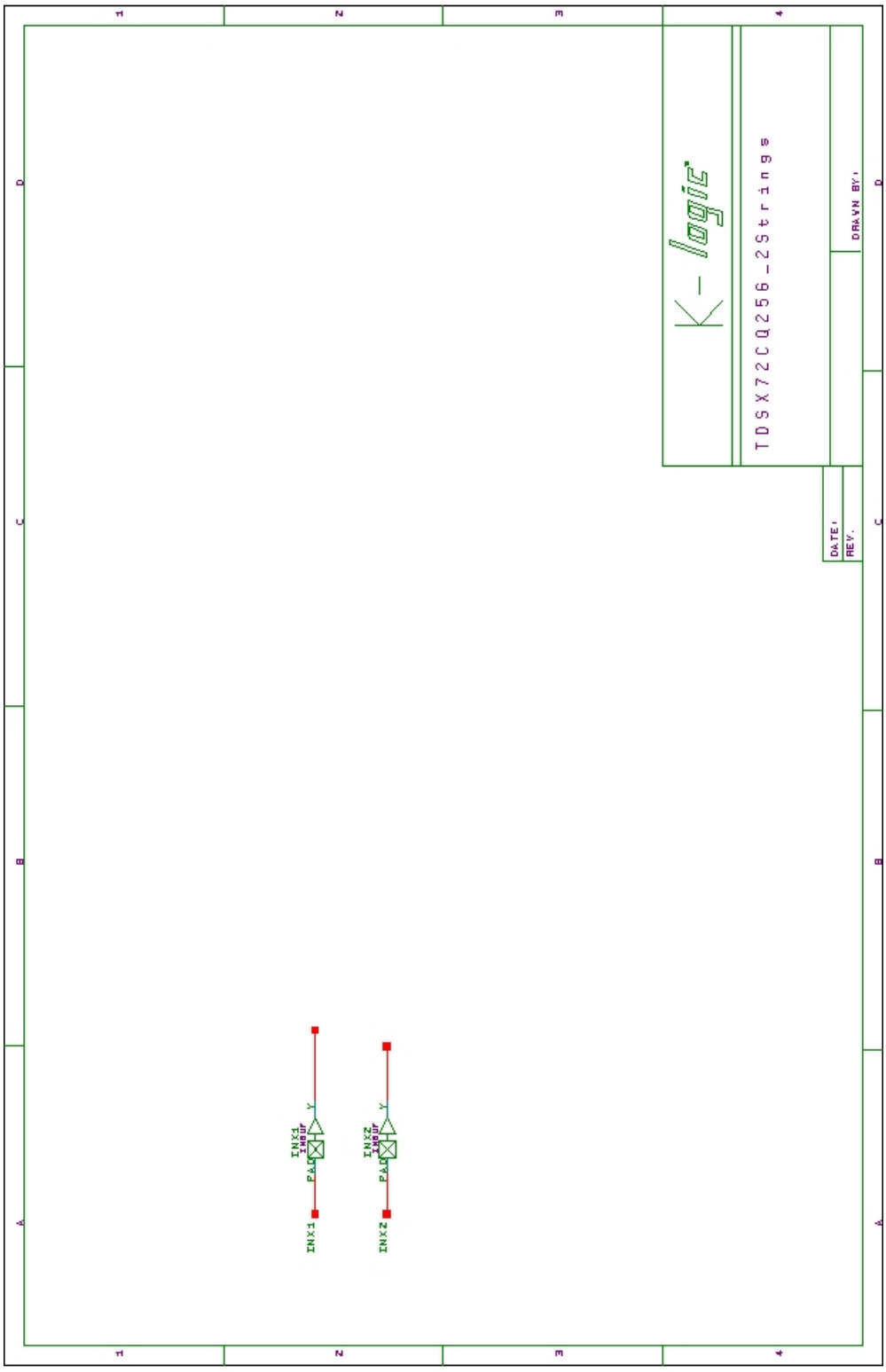


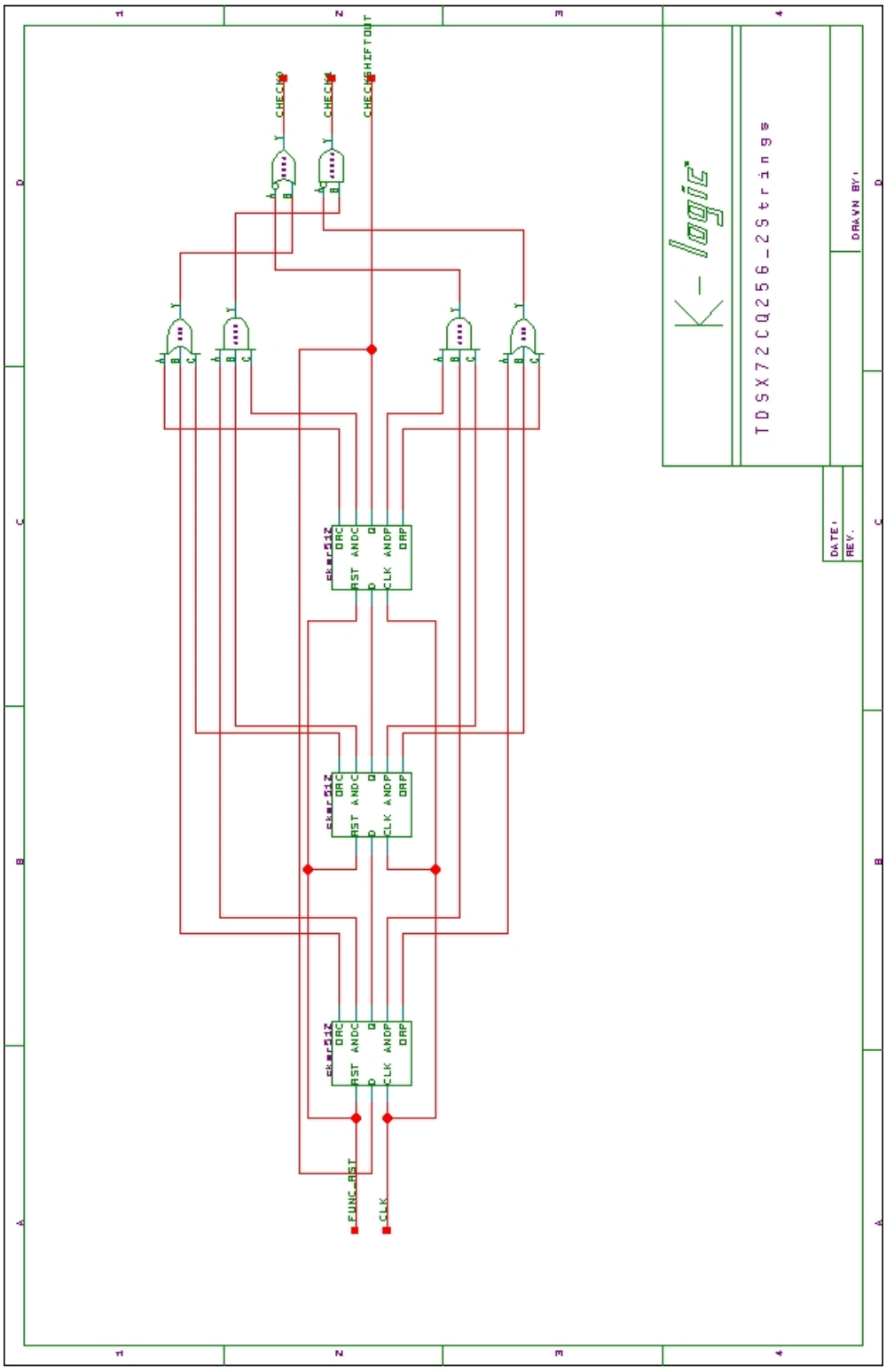

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
CLKA_TERM
CLKC_TERM
CLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

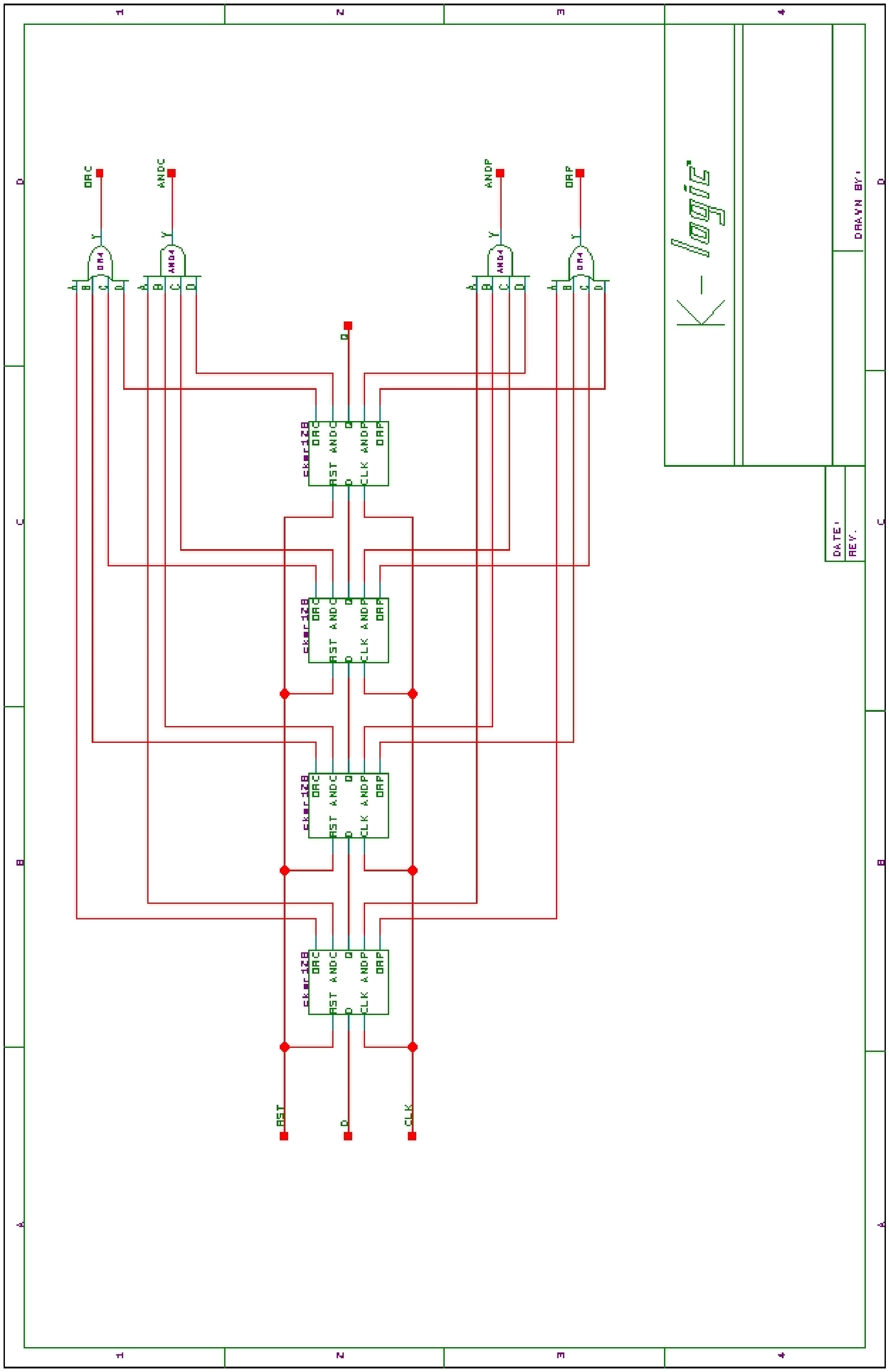

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-ism
CLK
RESET

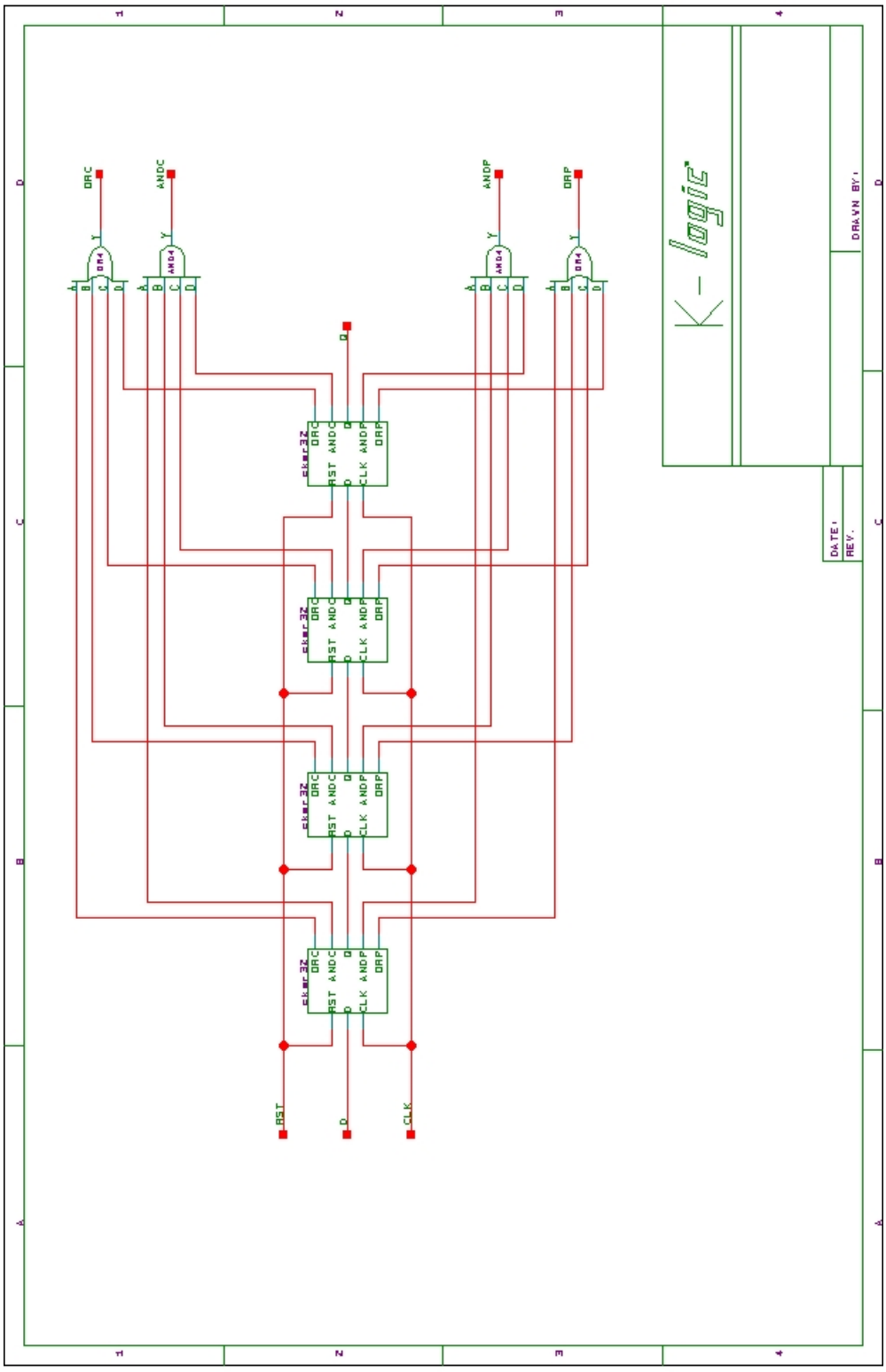

K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
Y
PRESERVE

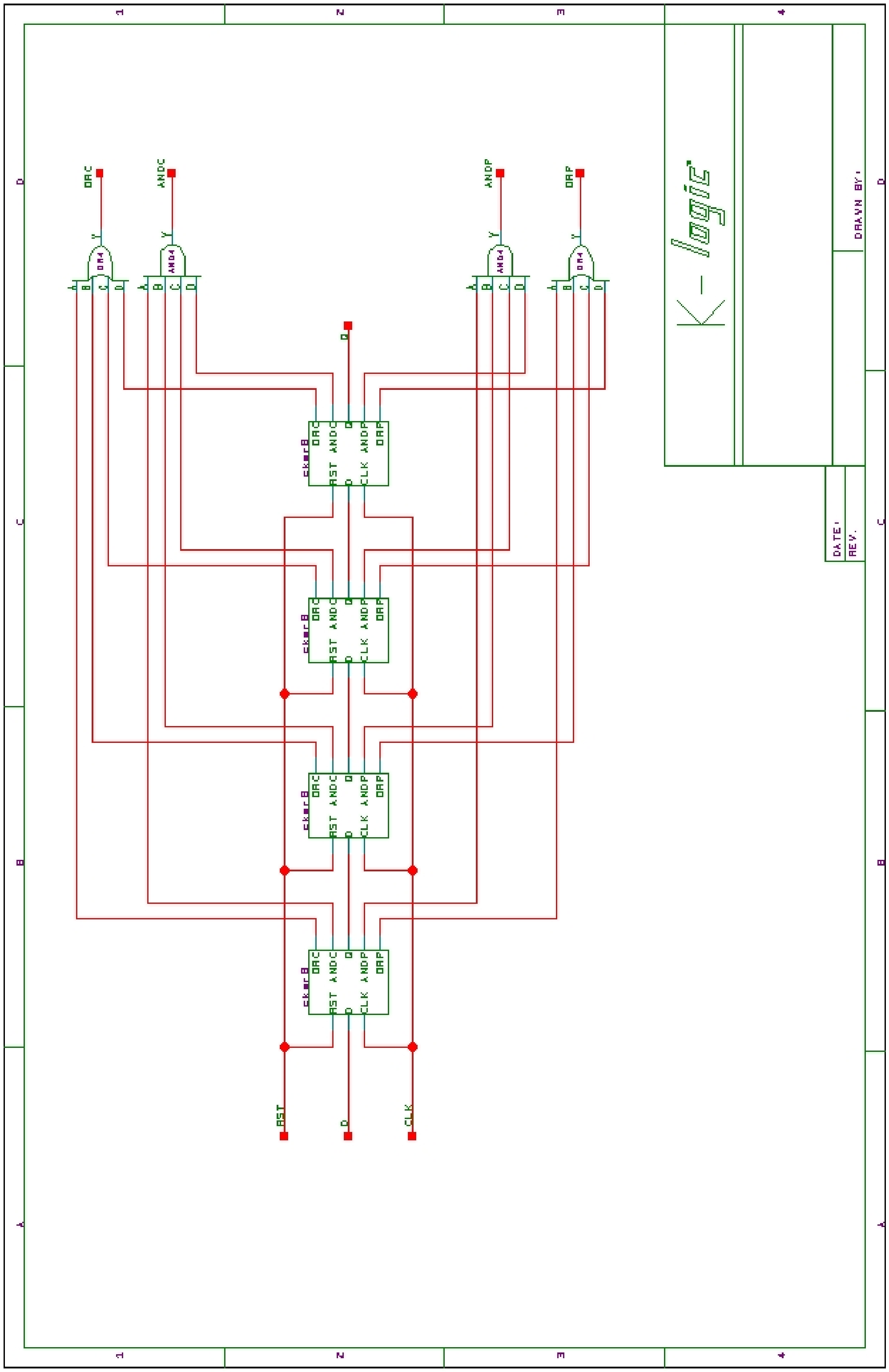

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRLD
CNTCLR
CNTEN
INBUF

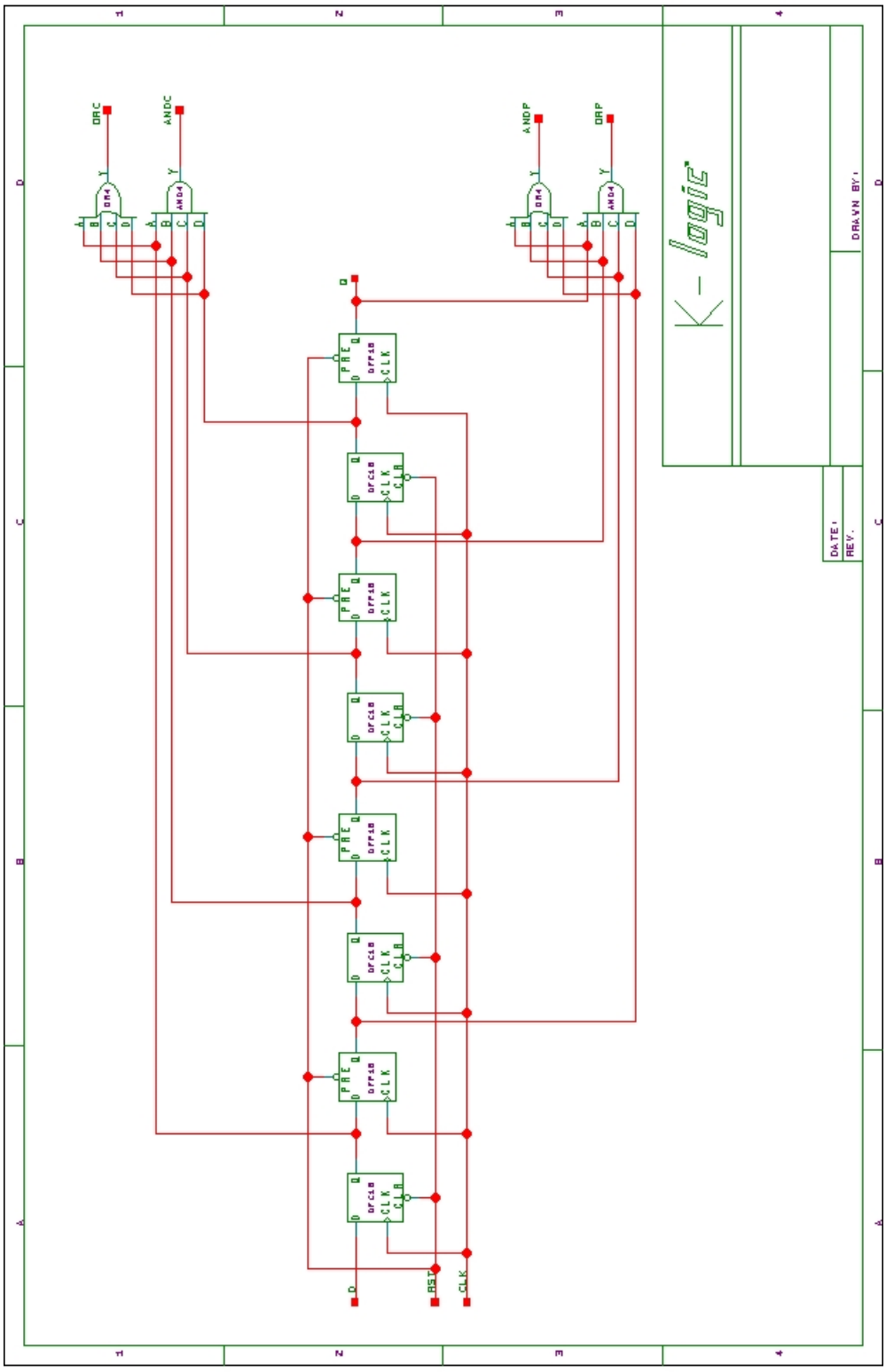

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

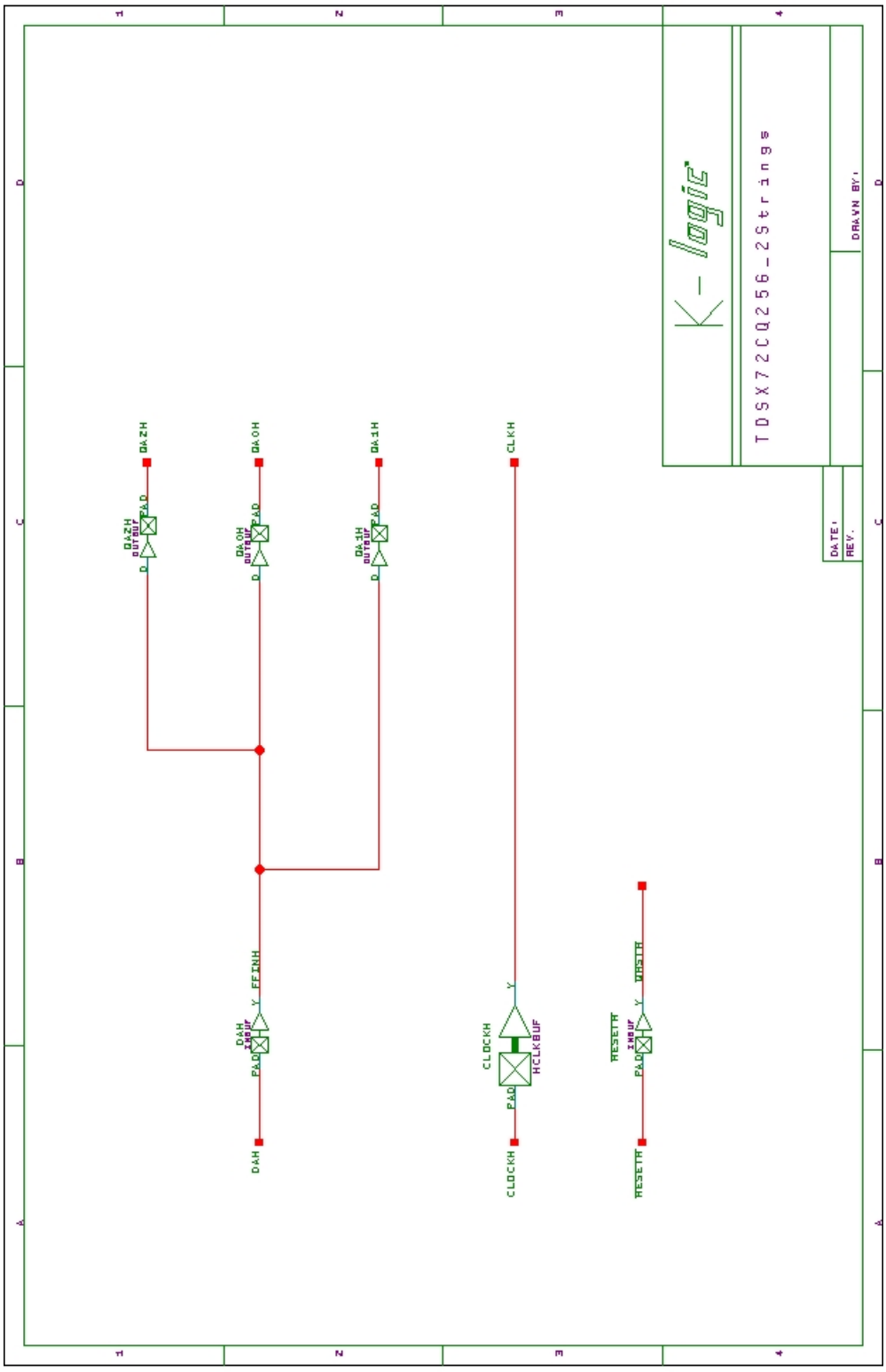

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECK
SHIFTOUT
FUNC_RST
CLK

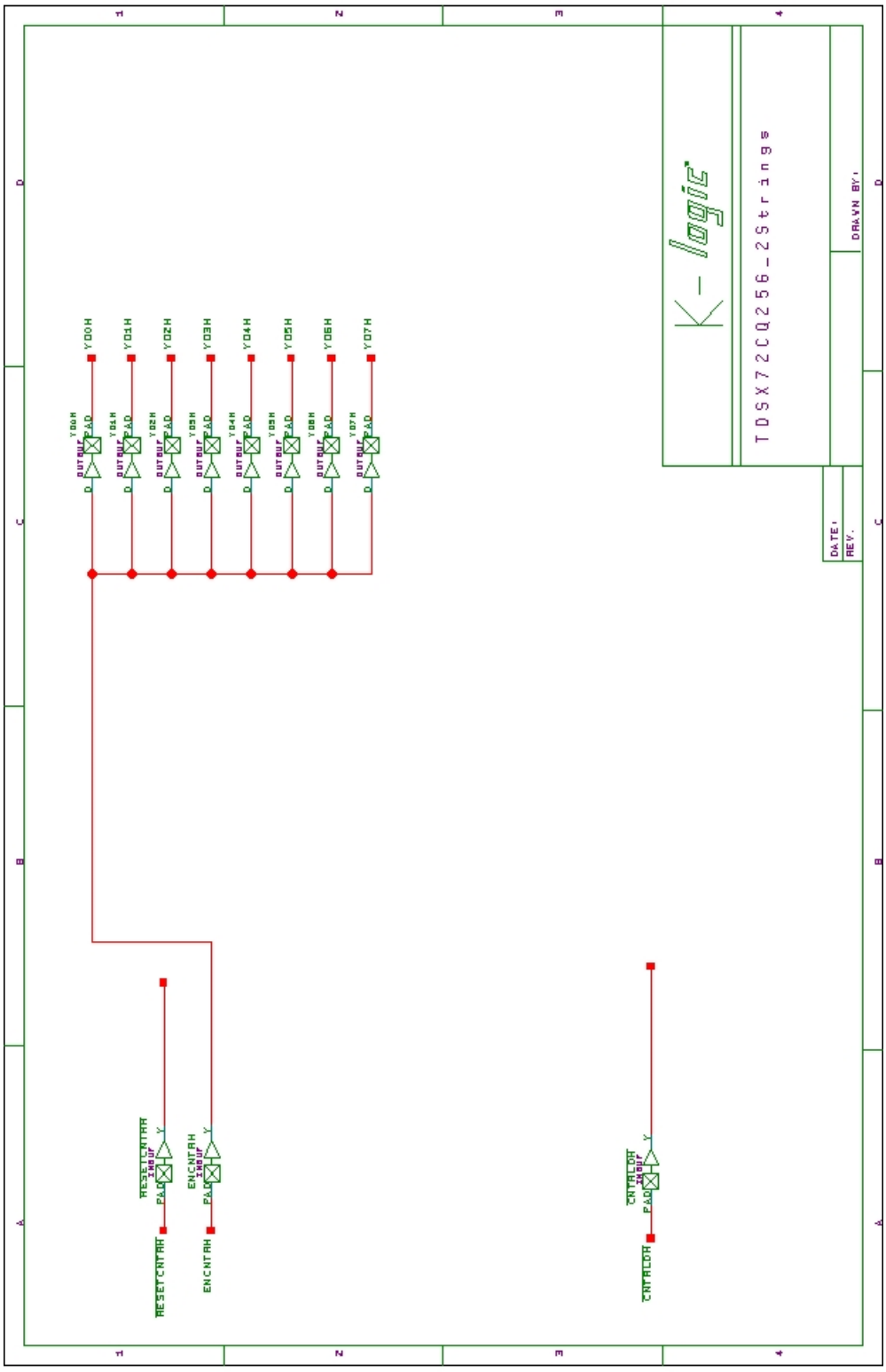

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr128
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

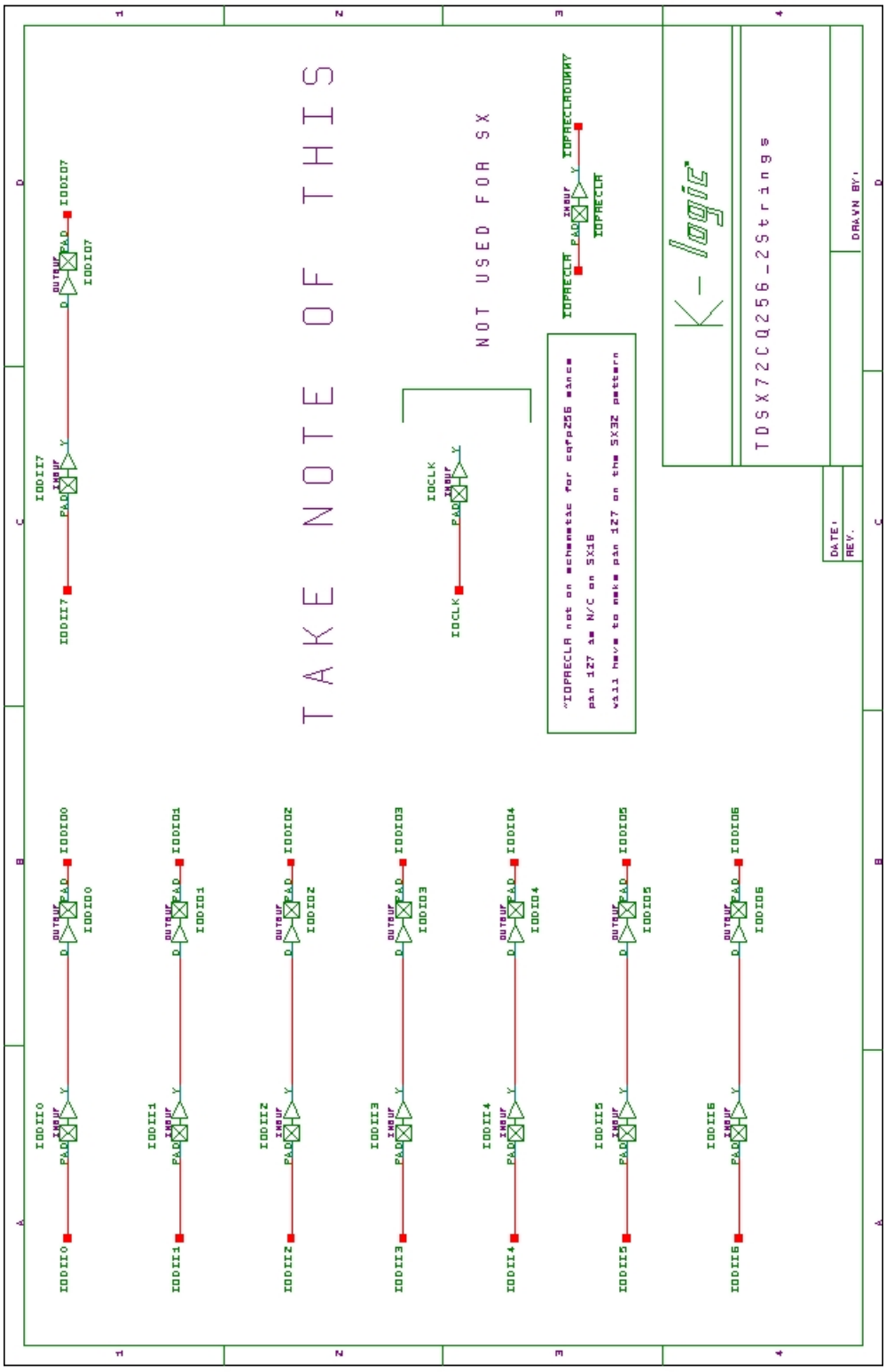

DRC
ANDC
ANDP
DRP
K- logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

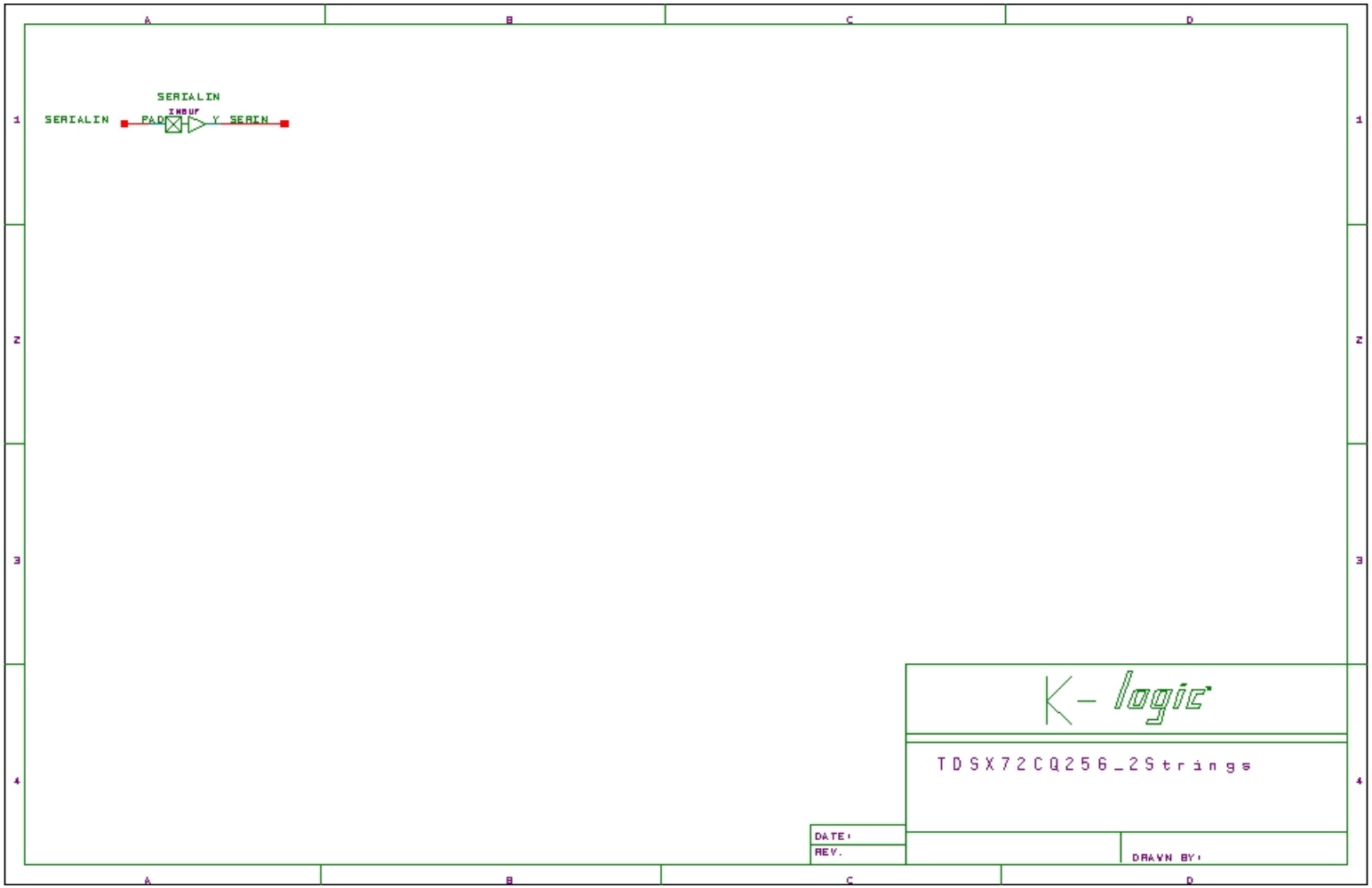

ORC
ANDC
ANDP
ORP
OR4
AND4
ckmrB
RST
D
CLK
Q
DATE:
REV.
DRAWN BY:
K-logic

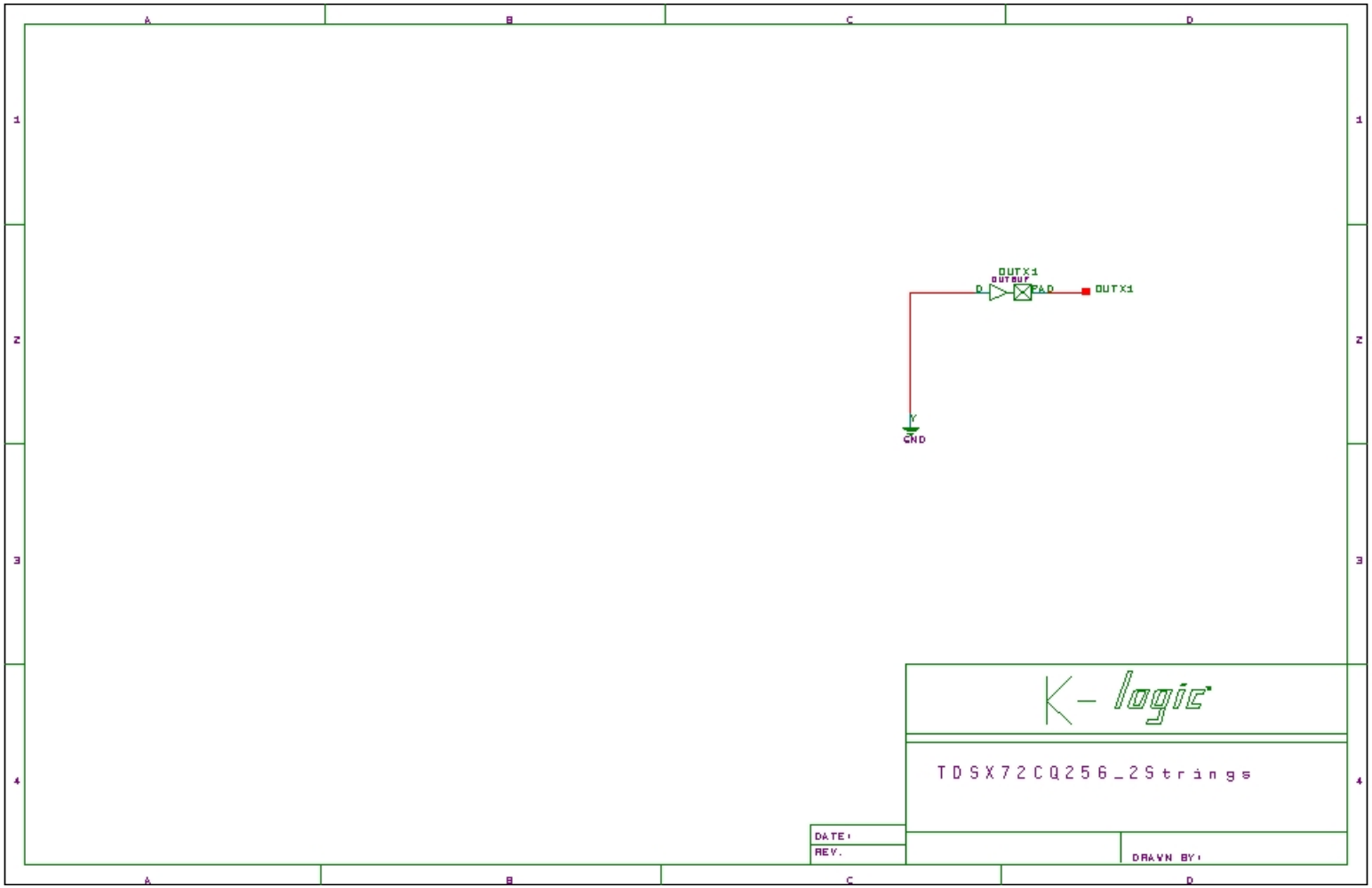

K- logic
DRAWN BY:
DATE:
REV.
ORC
ANDC
ANDF
ORF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH INBUF
Y FFINH
PAD
DAH
CLOCKH HCLKBUF
Y
PAD
CLOCKH
RESETH INBUF
Y RRSTH
PAD
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IODII7
IODCLK
IODPRECLR
IODPRECLRQUANY
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODIO7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
INBUF
OUTBUF
PAD


A
B
C
D
1
2
3
4
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


A
B
C
D
1
2
3
4
OUTX1
OUTBUF
D
PAD
OUTX1
Y
GND
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY: