Actel

TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX32SU-D1JW21
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 91 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 5 days room temperature annealing: average I_{CCA} = 136.4 mA, and average I_{CCI} = 123.2 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion.
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. In this test, the threshold of most of the available inputs is measured.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 67663 and 67714 are irradiated to 60 krad; DUT 67741, 67771 and 67774 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D1JW21
Quantity Tested	5
Serial Number	60 krad: 67663, 67714 100 krad: 67741, 67771, 67774
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

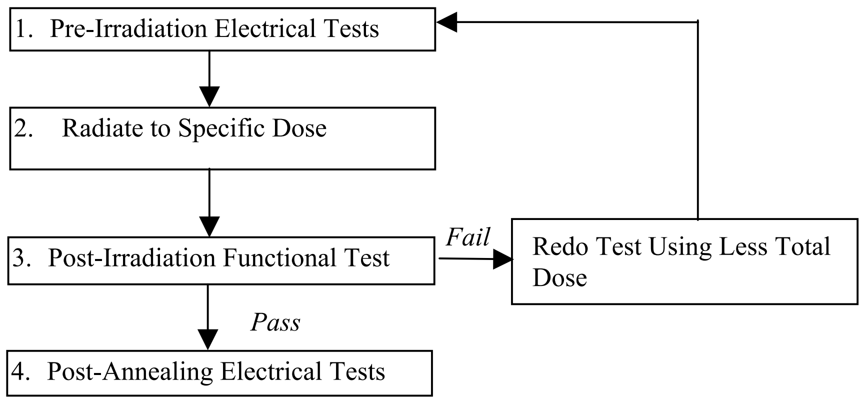


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs in both the 60-krad group and 100-krad group are biased annealed for 5 days after the 100 irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is due to the temporary degradation of the charge pump because the radiation-induced leakage current overloads the output of the charge pump. After the pump degrading to a certain voltage, the array logic changes to another state and logic outputs are disabled; this causes the I_{CCA} transition. However, the temporary degradation of the charge pump is only a testing artifact because the logic outputs recover after few hours of room temperature annealing.

By technicality, TM1019 doesn't allow further irradiation after disabling of the logic outputs. However, in this case, because the logic state of the DUT is still well defined, further irradiation is still valid. Every DUT was irradiated to 100 krad; after few hours of room temperature annealing, the logic outputs in every DUT were recovered.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
67663	60 krad	12.1	8	28	11
67714	60 krad	9.4	5	19.3	7
67741	100 krad	256	68	192	66
67771	100 krad	199	62	151	58
67774	100 krad	190	68	154.4	64

The 60-krad group shows the post-annealed I_{CC} passing the 25 mA spec. For the 100-krad group, a semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 52557, the tolerance is extracted as 91 krad for 10 years mission

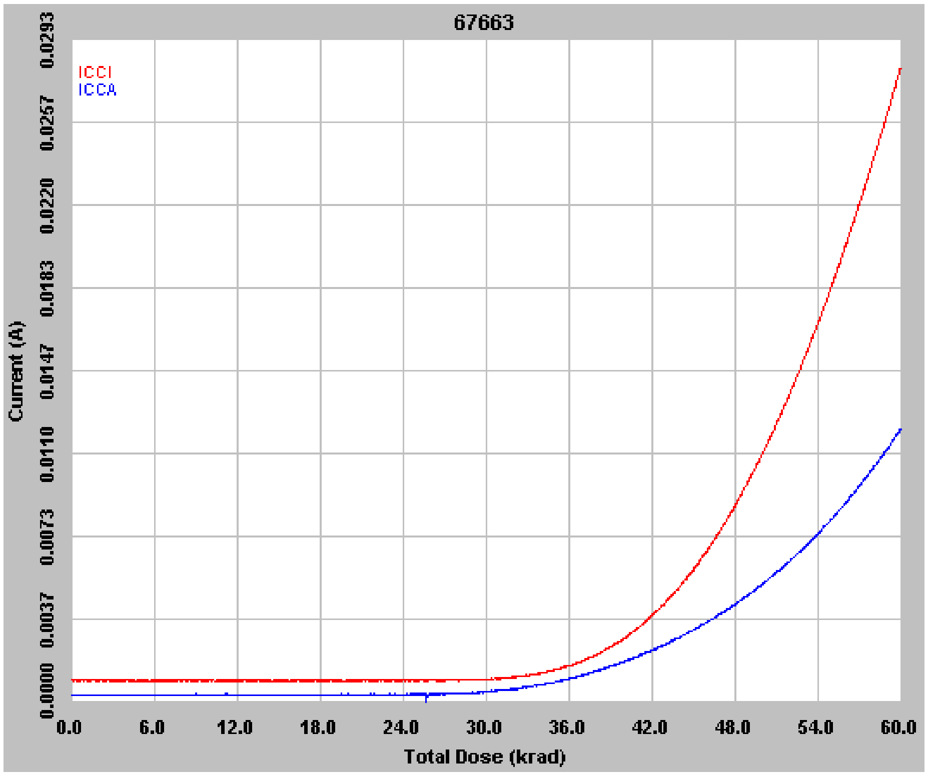


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 67663, 60-krad total dose

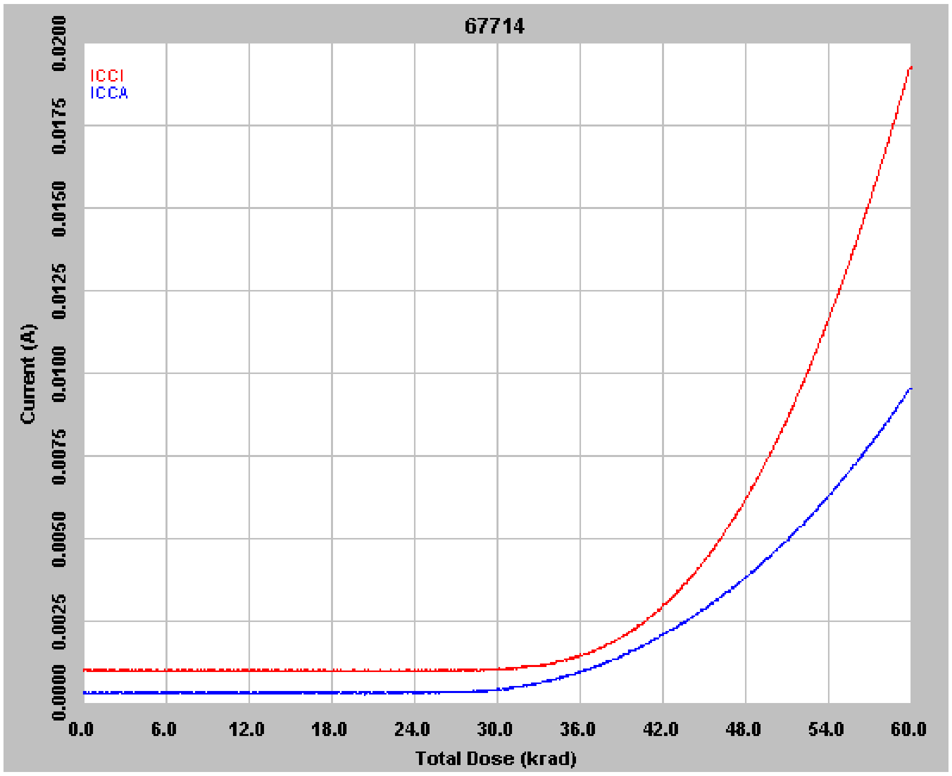


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 67714, 60-krad total dose

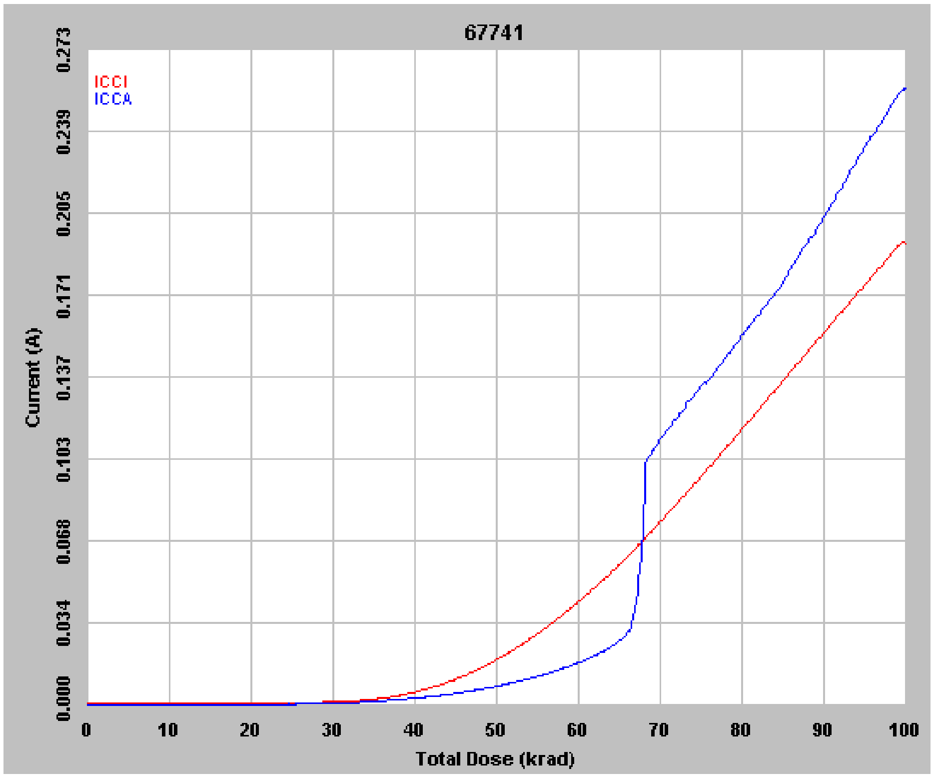


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 67741, I_{CCA} shows a transition near 67 krad that indicates the temporary disabling of the outputs

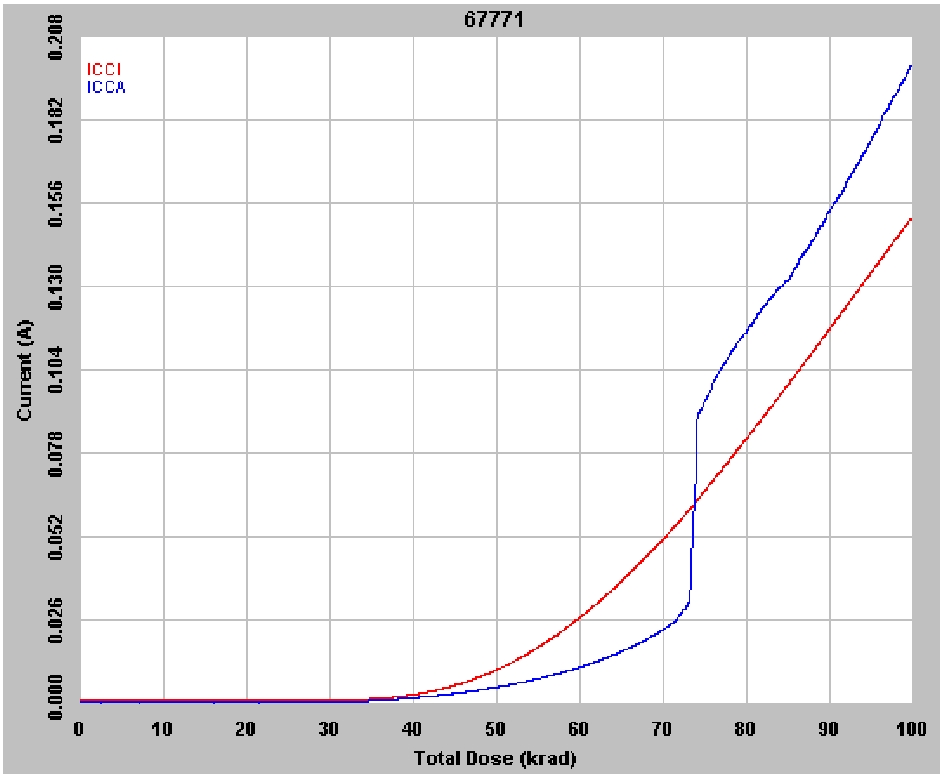


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 67771, I_{CCA} shows a transition near 74 krad that indicates the temporary disabling of the outputs.

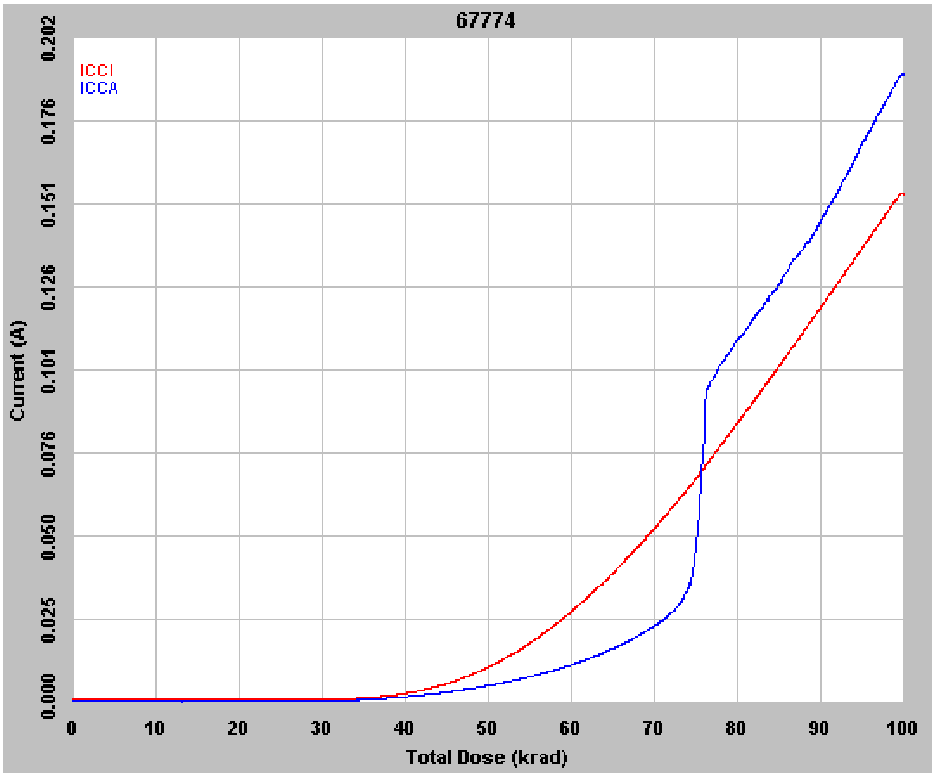


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 67774, I_{CCA} shows a transition near 75 krad that indicates the temporary disabling of the outputs.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Tables 4 and 5 list the pre-irradiation and post-annealing input thresholds. All data are within the spec limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds (DA/QA0)

DUT	Total Dose	Pre-Irradiation		Post-Annealing	
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
67663	60 krad	1.23	1.46	1.23	1.47
67714	60 krad	1.23	1.52	1.22	1.46
67741	100 krad	1.23	1.46	1.36	1.48
67771	100 krad	1.23	1.46	1.37	1.47
67774	100 krad	1.22	1.47	1.35	1.46

Table 5a Additional Post-Annealing Input Thresholds

In/Out Pin:	DAH/QA0H		ENCNTR/YO0		ENCNTRH/YO0H		IDII0/IDIO0	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
67663	1.38	1.51	1.35	1.48	1.36	1.49	1.36	1.47
67714	1.37	1.46	1.38	1.47	1.38	1.47	1.37	1.47
67741	1.4	1.47	1.41	1.5	1.4	1.44	1.34	1.54
67771	1.39	1.5	1.37	1.57	1.37	1.46	1.38	1.48
67774	1.37	1.45	1.37	1.46	1.34	1.45	1.37	1.46

Table 5b Additional Post-Annealing Input Thresholds

In/Out Pin:	IDII1/IDIO1		IDII2/IDIO2		IDII3/IDIO3		IDII4/IDIO4	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
67663	1.34	1.46	1.36	1.52	1.31	1.49	1.32	1.46
67714	1.37	1.47	1.38	1.47	1.36	1.47	1.37	1.47
67741	1.44	1.53	1.44	1.54	1.36	1.55	1.39	1.48
67771	1.38	1.45	1.38	1.48	1.38	1.47	1.38	1.45
67774	1.38	1.46	1.39	1.58	1.35	1.44	1.37	1.44

Table 5c Additional Post-Annealing Input Thresholds

In/Out Pin:	IDII5/IDIO5		IDII6/IDIO6		IDII7/IDIO7	
DUT	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
67663	1.27	1.47	1.35	1.52	1.34	1.48
67714	1.37	1.46	1.38	1.47	1.36	1.46
67741	1.44	1.54	1.45	1.54	1.38	1.49
67771	1.35	1.47	1.38	1.49	1.33	1.45
67774	1.35	1.44	1.37	1.49	1.35	1.42

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 6 and 7. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 6 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
67663	0.009	0.009	0.104	0.104	0.173	0.174	0.438	0.439	0.901	0.903
67714	0.009	0.009	0.103	0.102	0.171	0.171	0.432	0.432	0.888	0.890
67741	0.009	0.009	0.103	0.105	0.171	0.176	0.432	0.444	0.889	0.917
67771	0.009	0.009	0.104	0.109	0.174	0.181	0.439	0.456	0.903	0.938
67774	0.009	0.010	0.103	0.108	0.173	0.178	0.436	0.454	0.897	0.934

Table 7 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
67663	4.99	4.98	4.86	4.85	4.64	4.63	4.06	4.03	2.73	2.65
67714	4.98	4.99	4.86	4.86	4.65	4.65	4.07	4.06	2.77	2.71
67741	4.99	4.98	4.86	4.86	4.65	4.64	4.06	4.02	2.72	2.55
67771	4.99	4.98	4.86	4.85	4.64	4.62	4.05	4.00	2.70	2.68
67774	4.99	4.98	4.86	4.85	4.65	4.62	4.06	3.98	2.71	2.45

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. In every case the DUT passes the 10% degradation criterion. The negative degradations for 60-krad group are due to testing noise.

Table 8 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation	Post-Annealing	Degradation
67663	514.50	512.08	-0.47%
67714	509.85	497.33	-2.48%
67741	515.79	538.56	4.44%
67771	517.45	534.03	3.23%
67774	522.43	542.35	3.84%

F. Transition Time

Figures 7 to 26 show the post-annealing transition rising and falling edges. These waveforms show no observable radiation induced degradations.

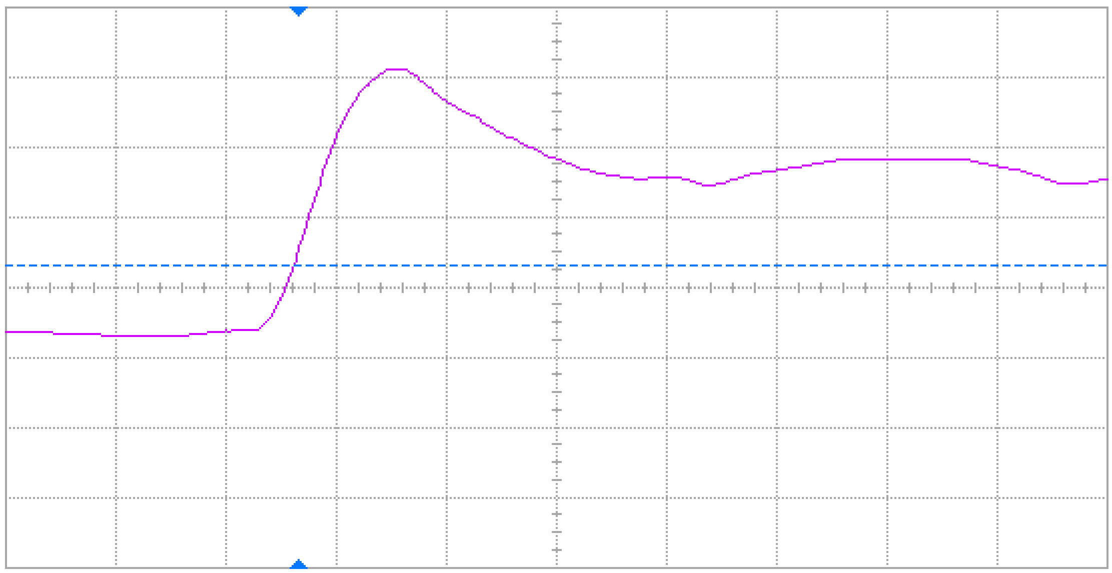


Figure 7 Pre-annealing rising edge of DUT 67663, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

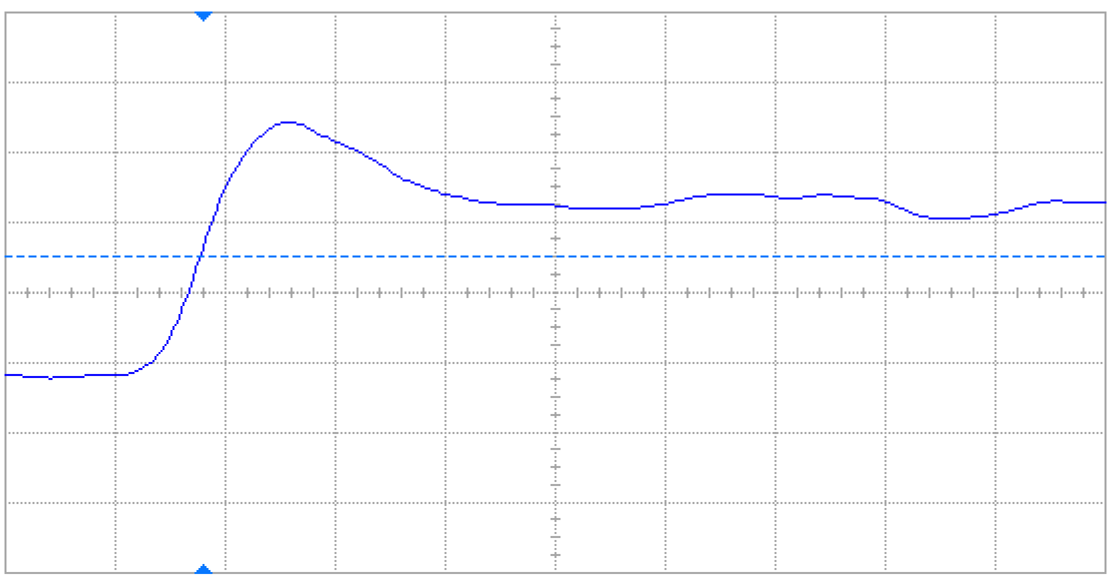


Figure 8 Post-annealing rising edge of DUT 67663, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

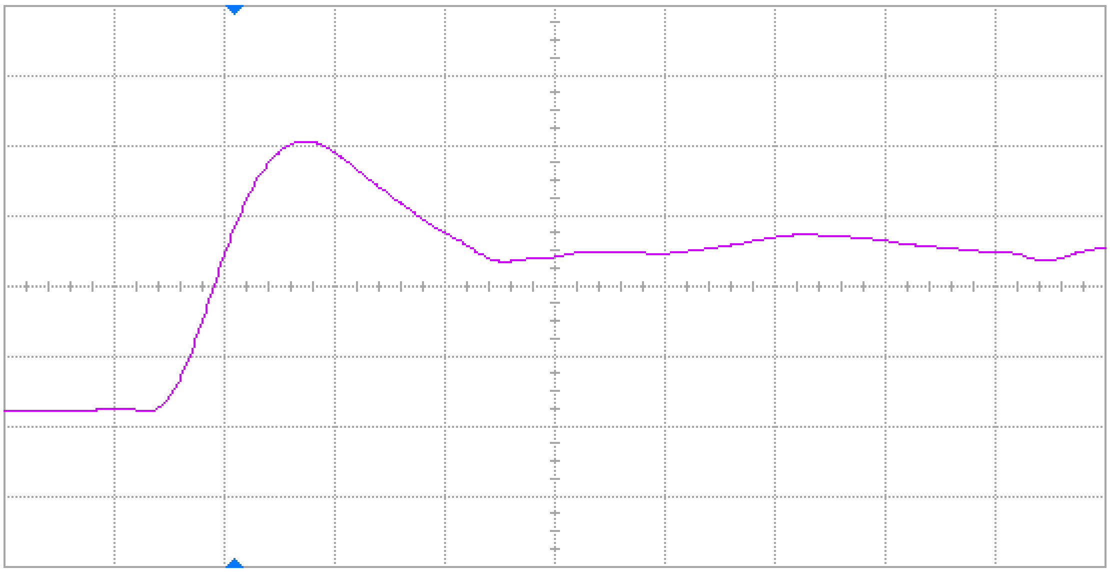


Figure 9 Pre-annealing rising edge of DUT 67714, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

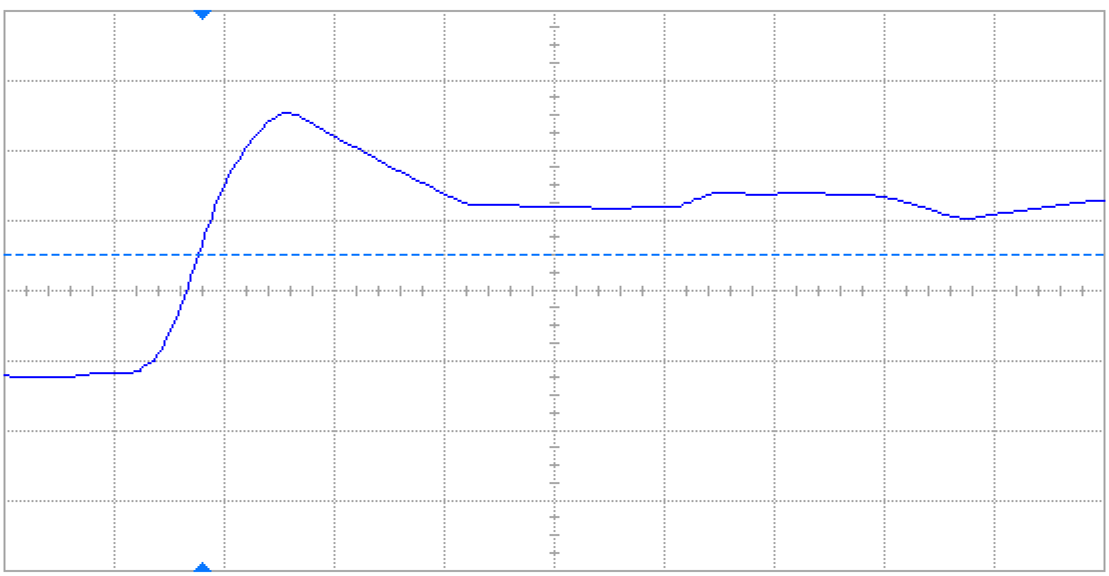


Figure 10 Post-annealing rising edge of DUT 67714, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

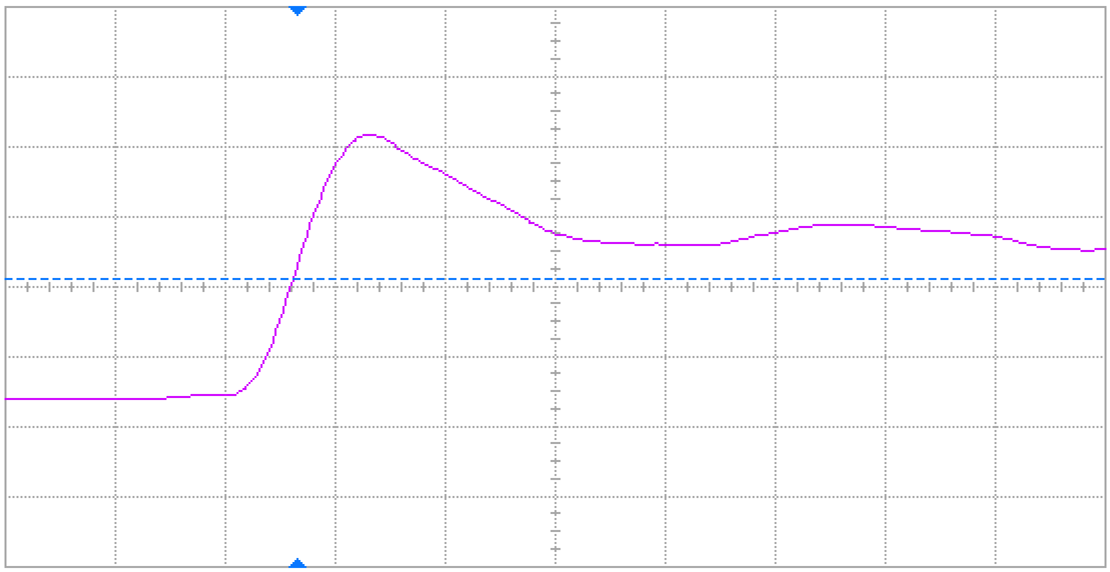


Figure 11 Pre-annealing rising edge of DUT 67741, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

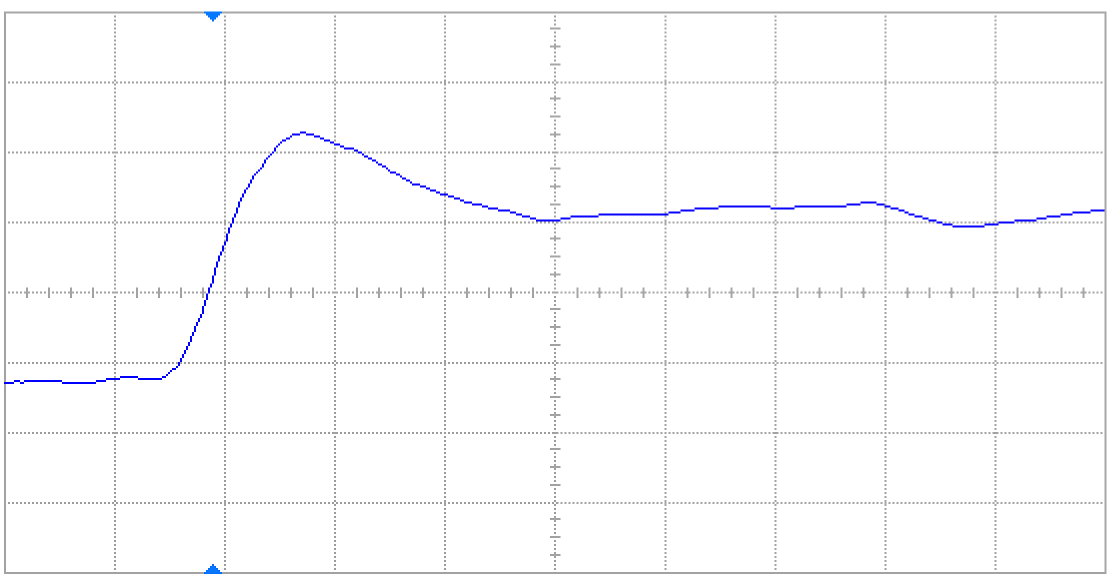


Figure 12 Post-annealing rising edge of DUT 67741, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

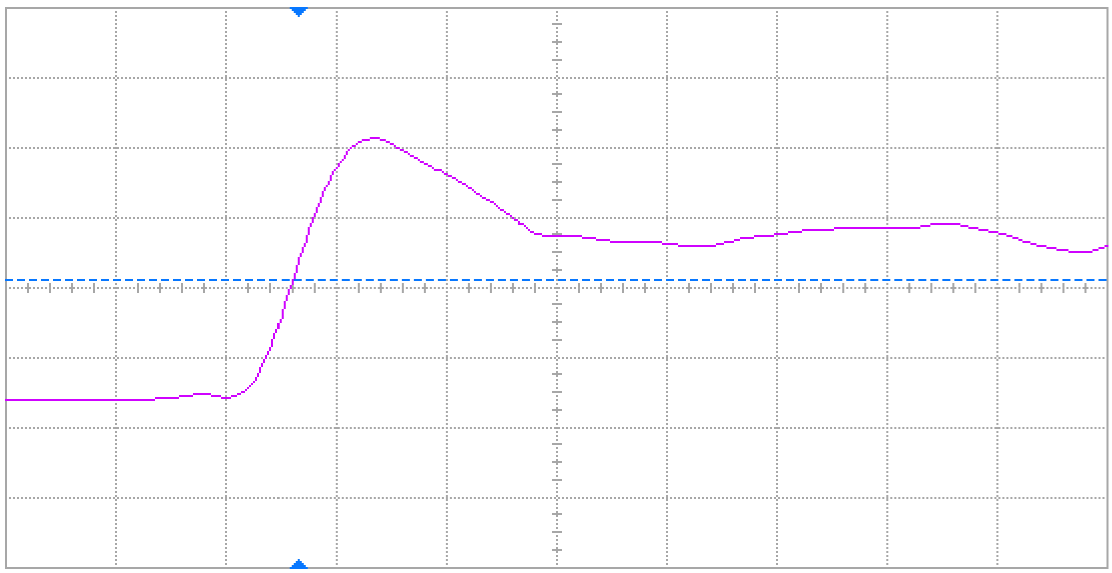


Figure 13 Pre-annealing rising edge of DUT 67771, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

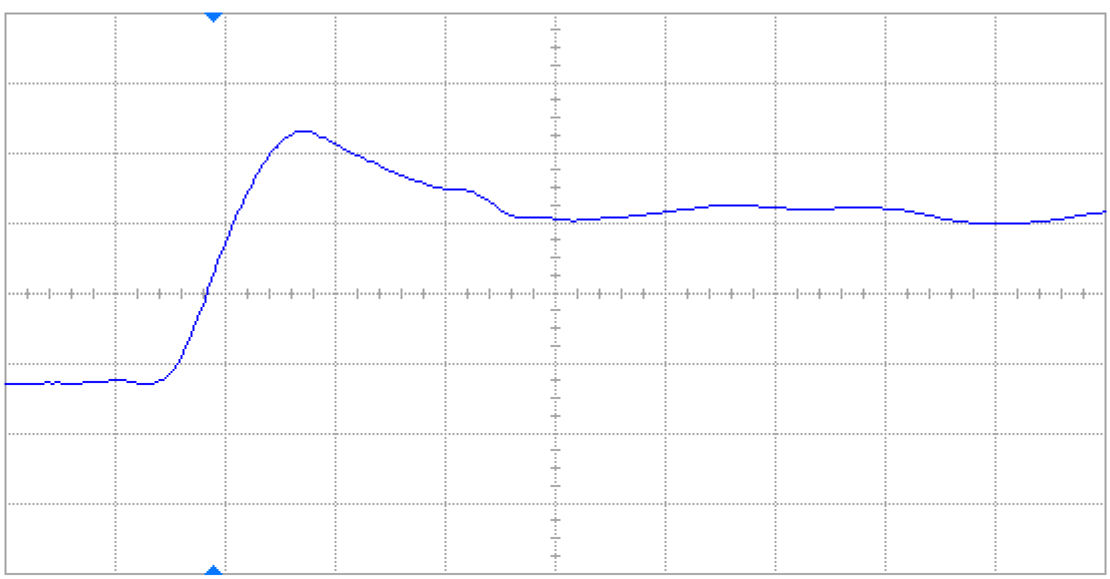


Figure 14 Post-annealing rising edge of DUT 67771, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

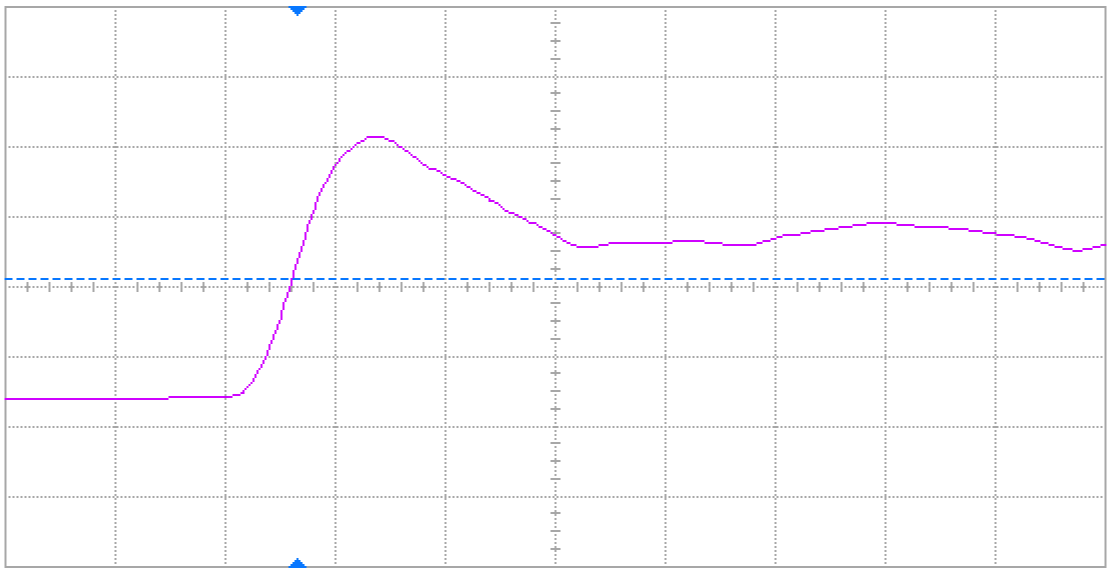


Figure 15 Pre-annealing rising edge of DUT 67774, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

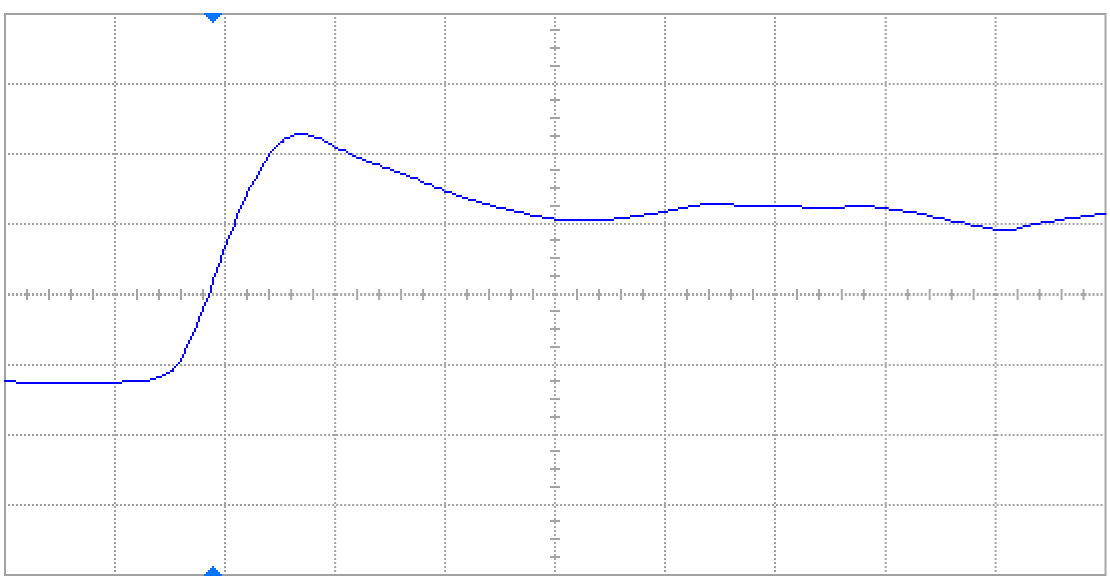


Figure 16 Post-annealing rising edge of DUT 67774, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

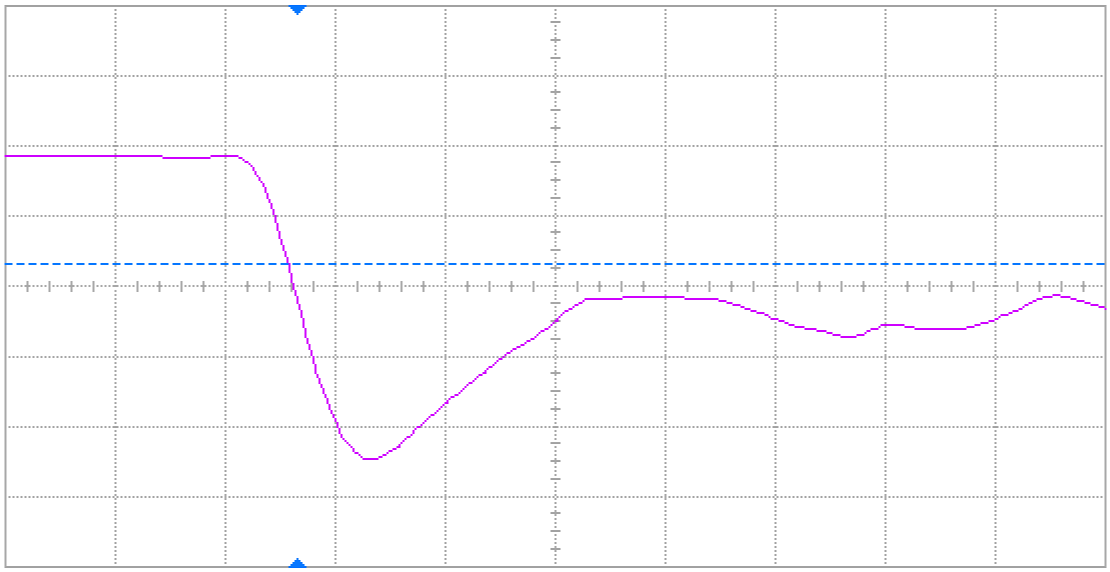


Figure 17 Pre-annealing falling edge of DUT 67663, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

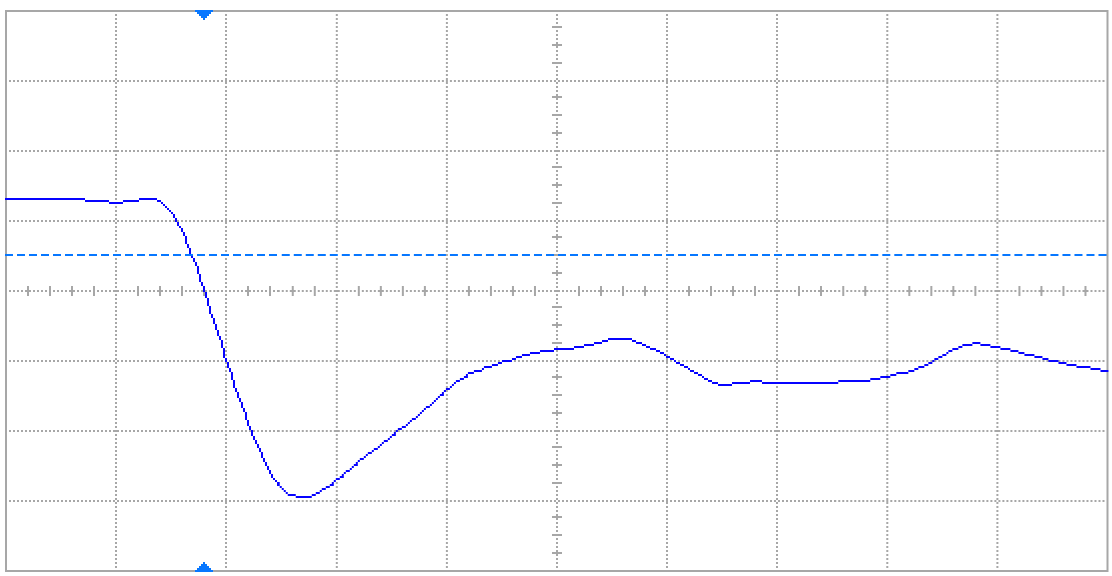


Figure 18 Post-annealing falling edge of DUT 67663, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

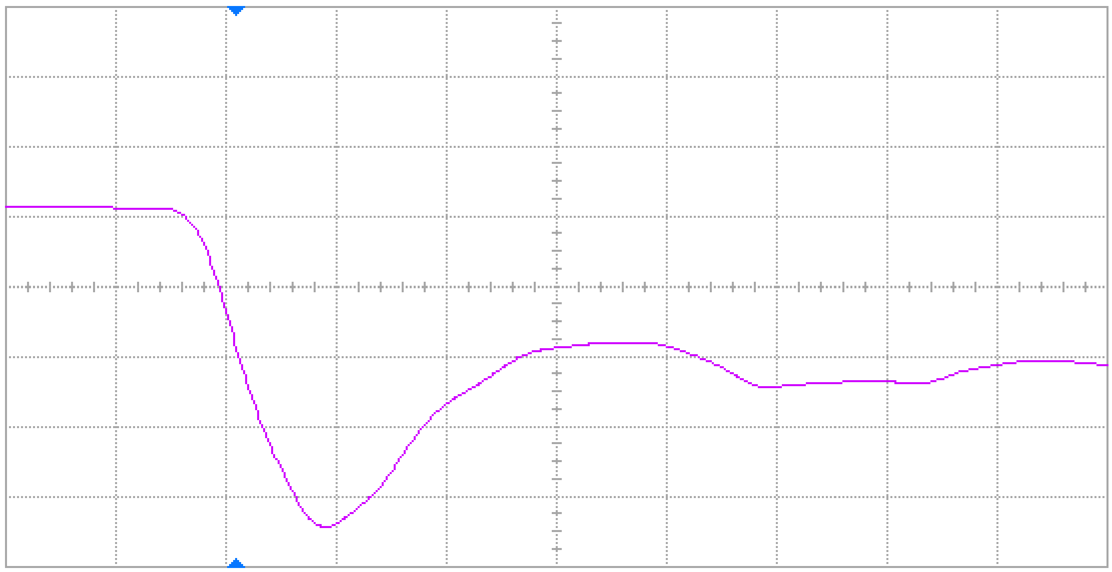


Figure 19 Pre-annealing falling edge of DUT 67714, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

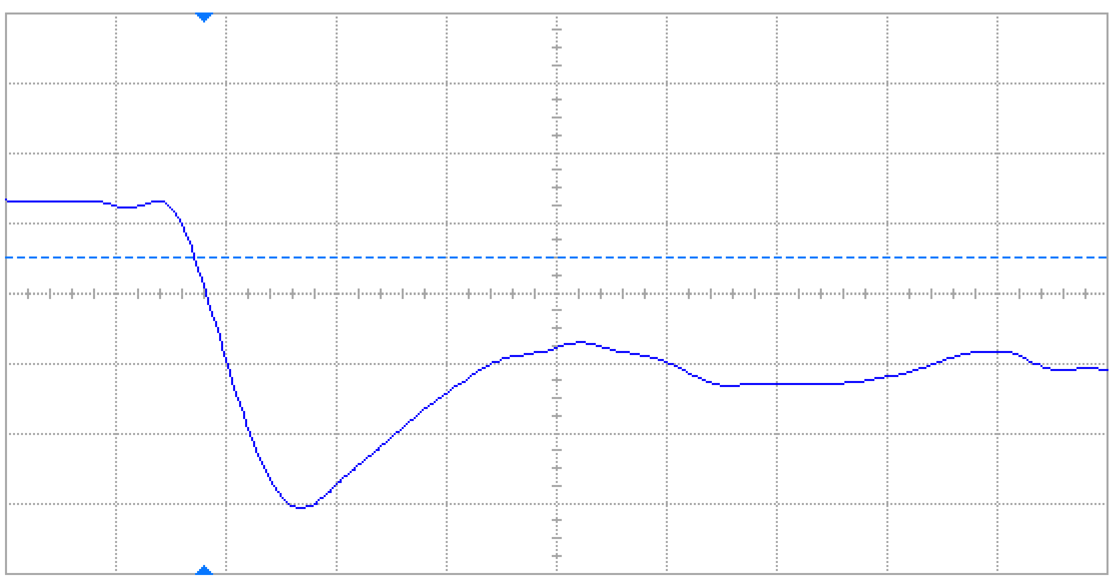


Figure 20 Post-annealing falling edge of DUT 67714, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

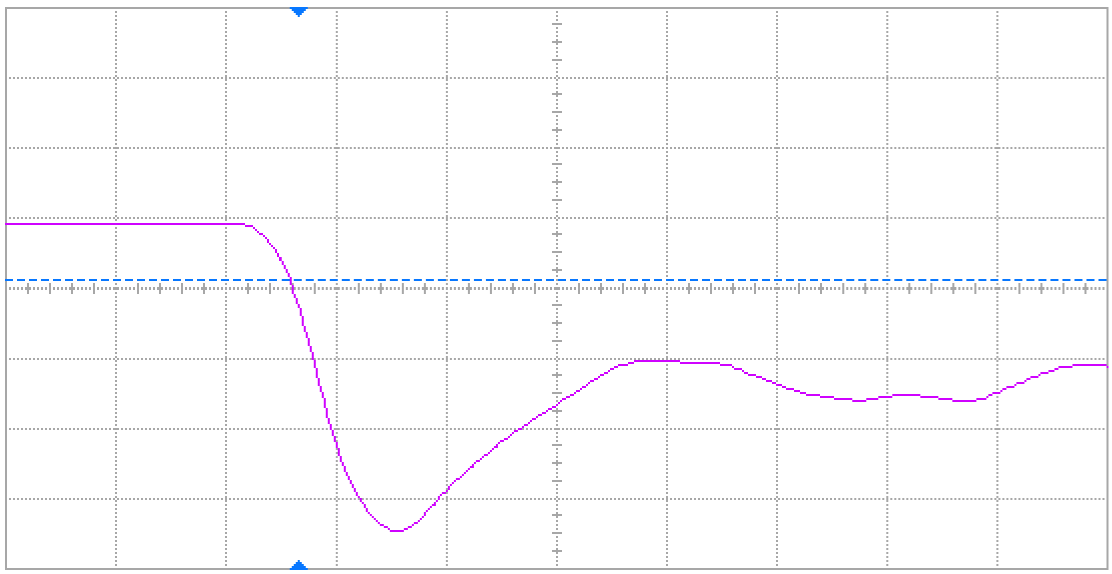


Figure 21 Pre-annealing falling edge of DUT 67741, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

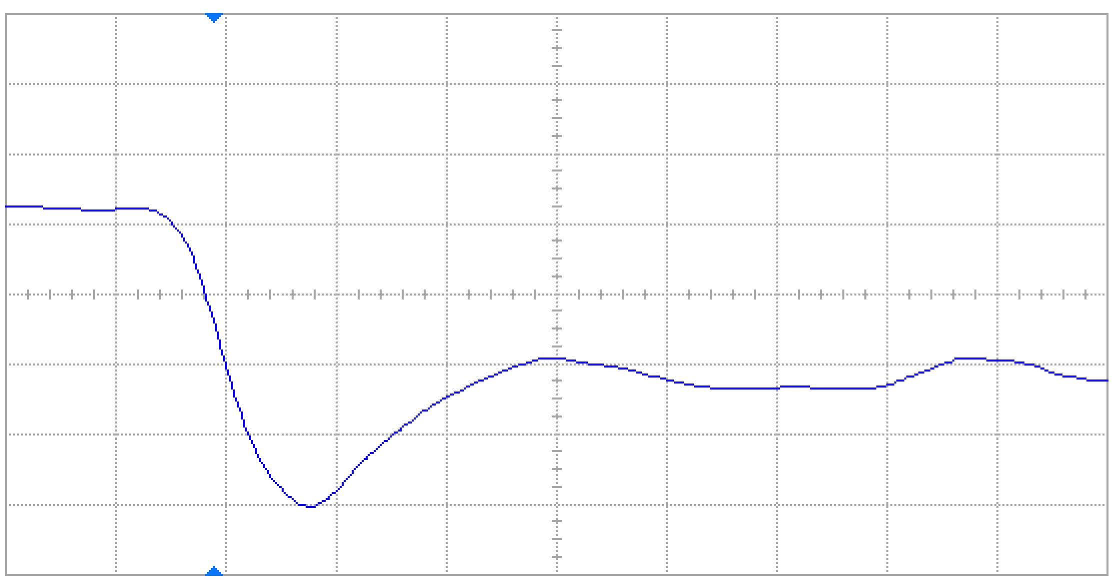


Figure 22 Post-annealing falling edge of DUT 67741, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

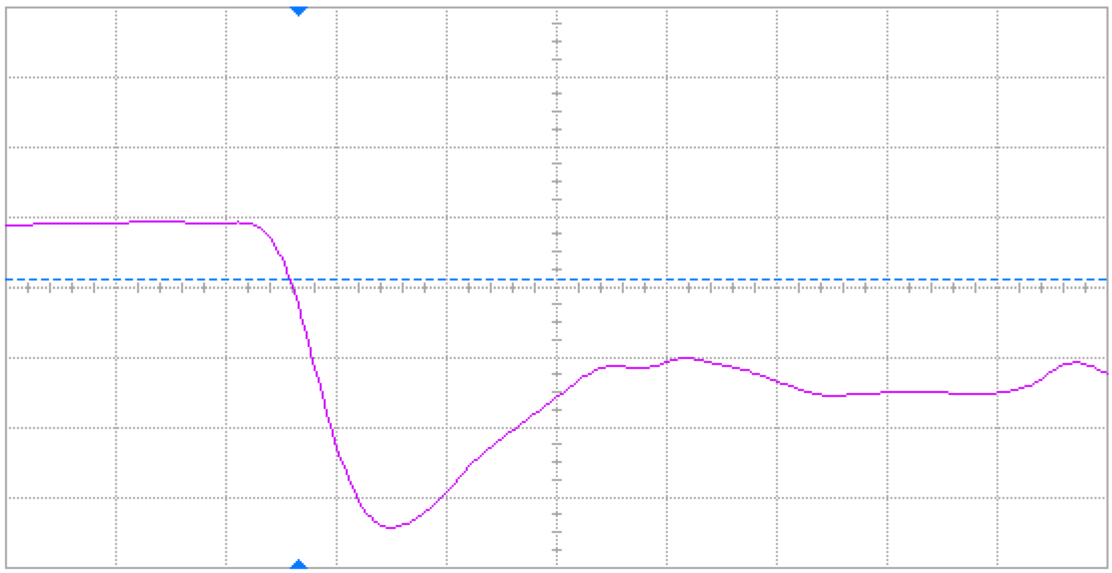


Figure 23 Pre-annealing falling edge of DUT 67771, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

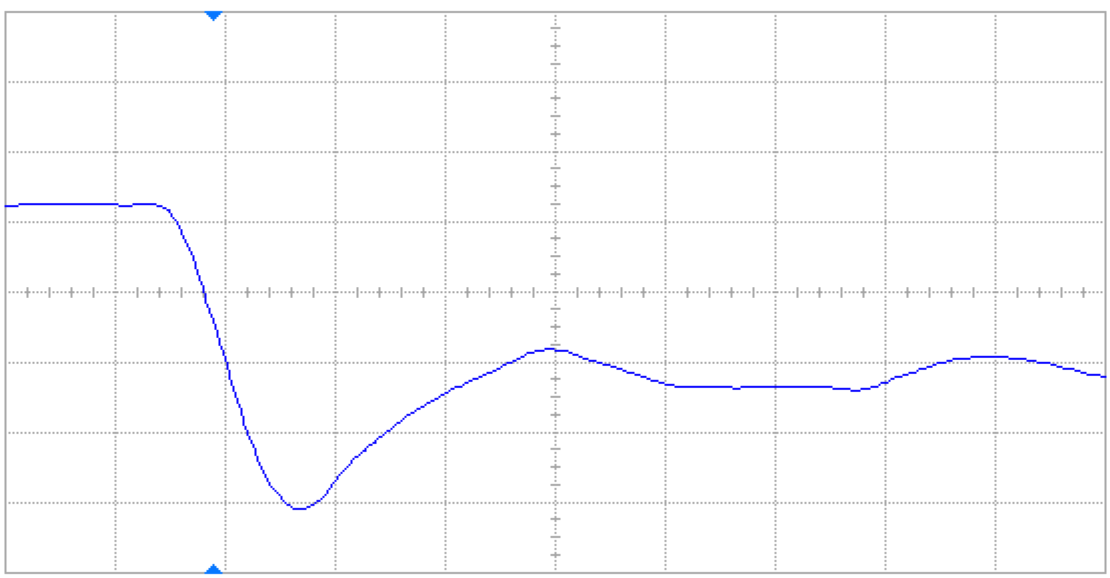


Figure 24 Post-annealing falling edge of DUT 67771, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

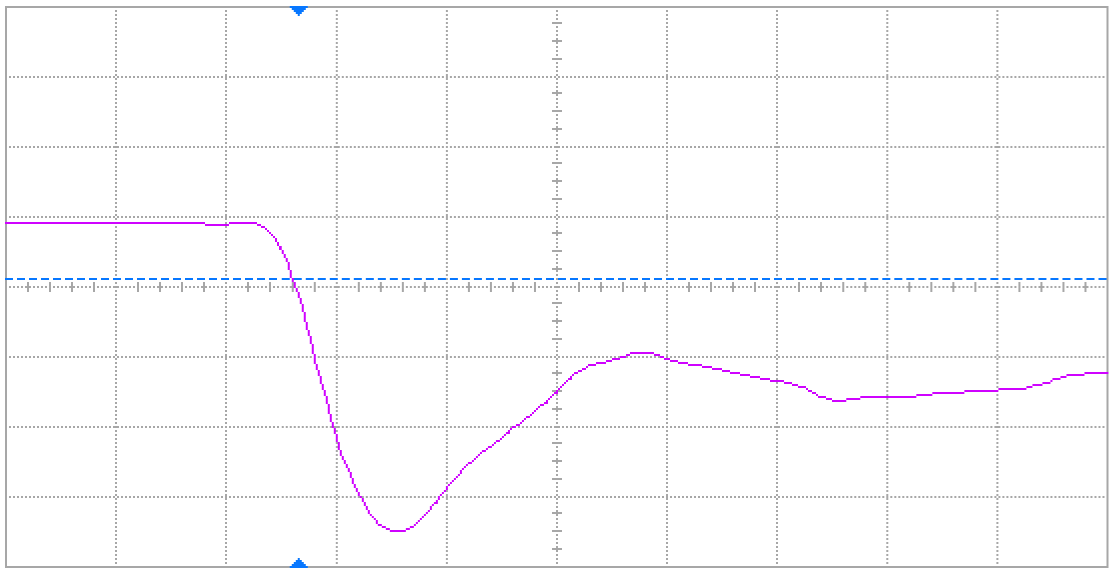


Figure 25 Pre-annealing falling edge of DUT 67774, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

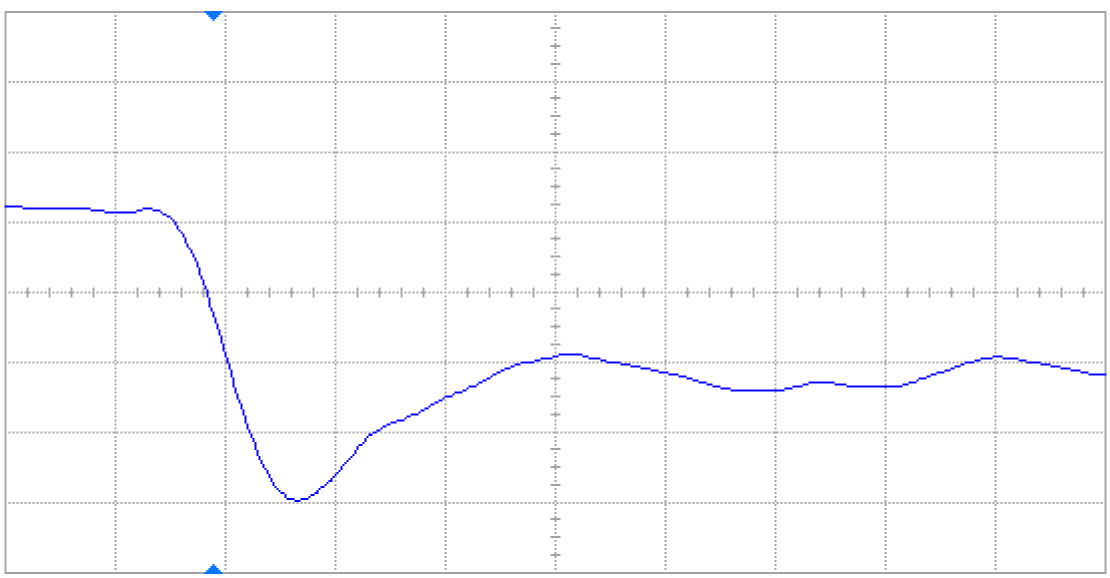
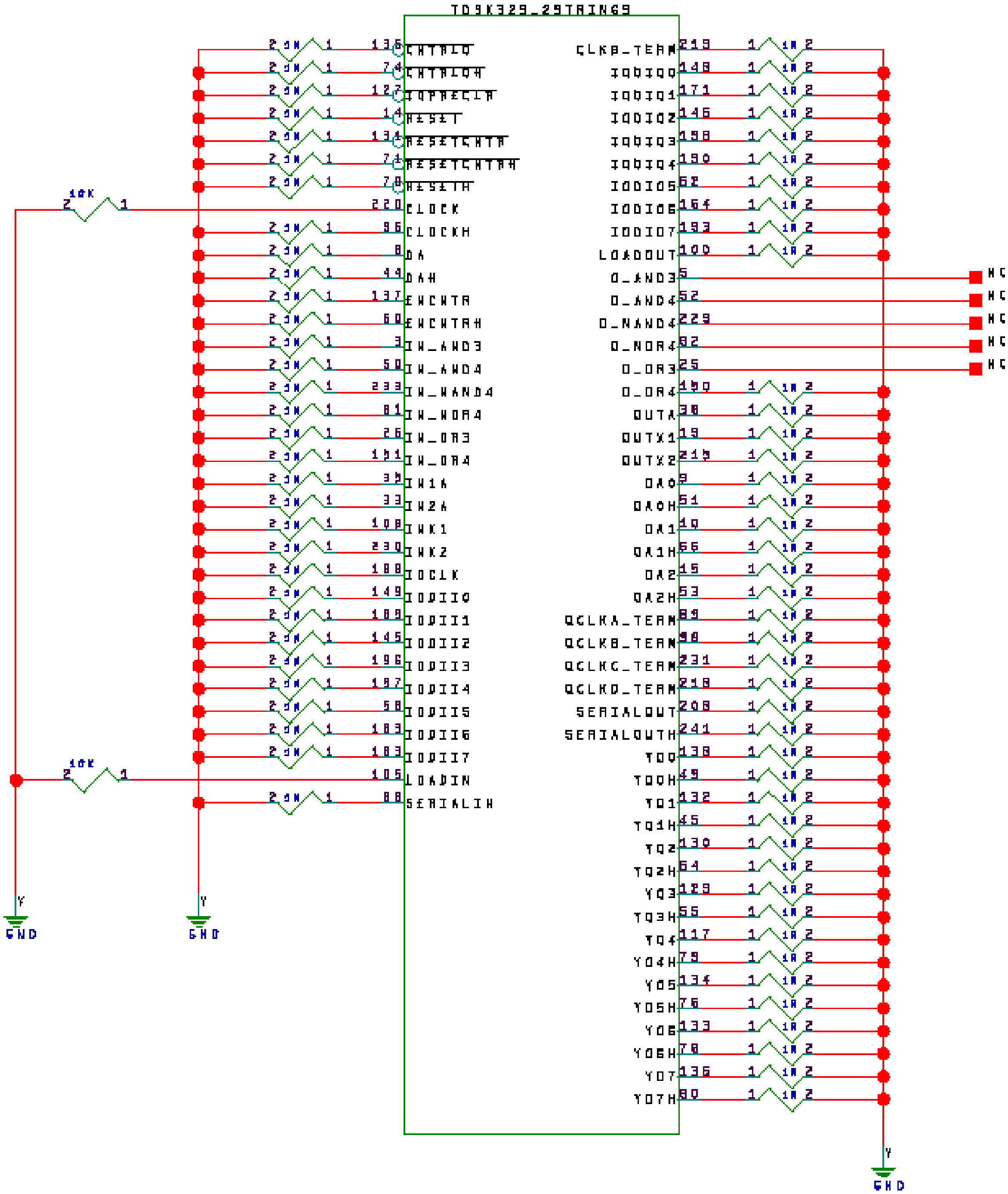
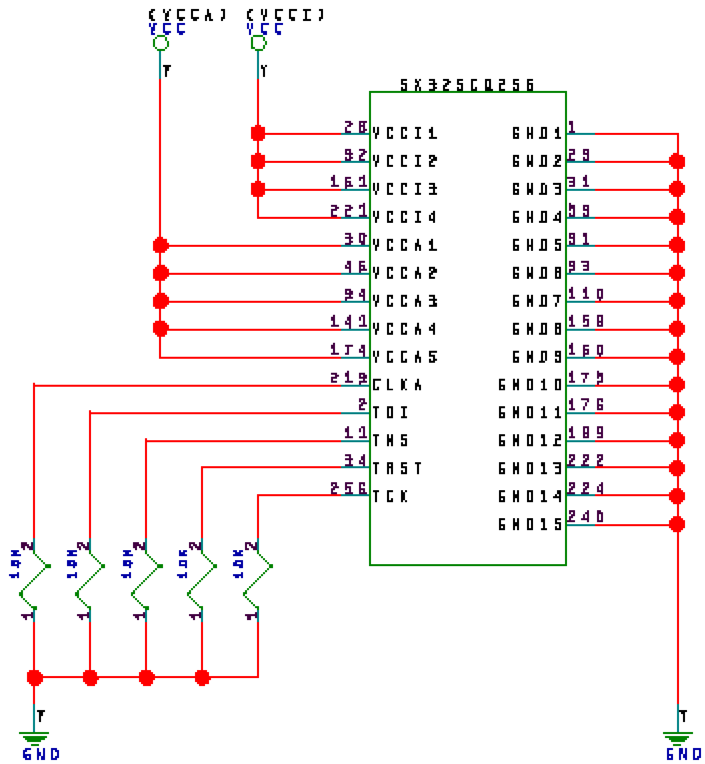


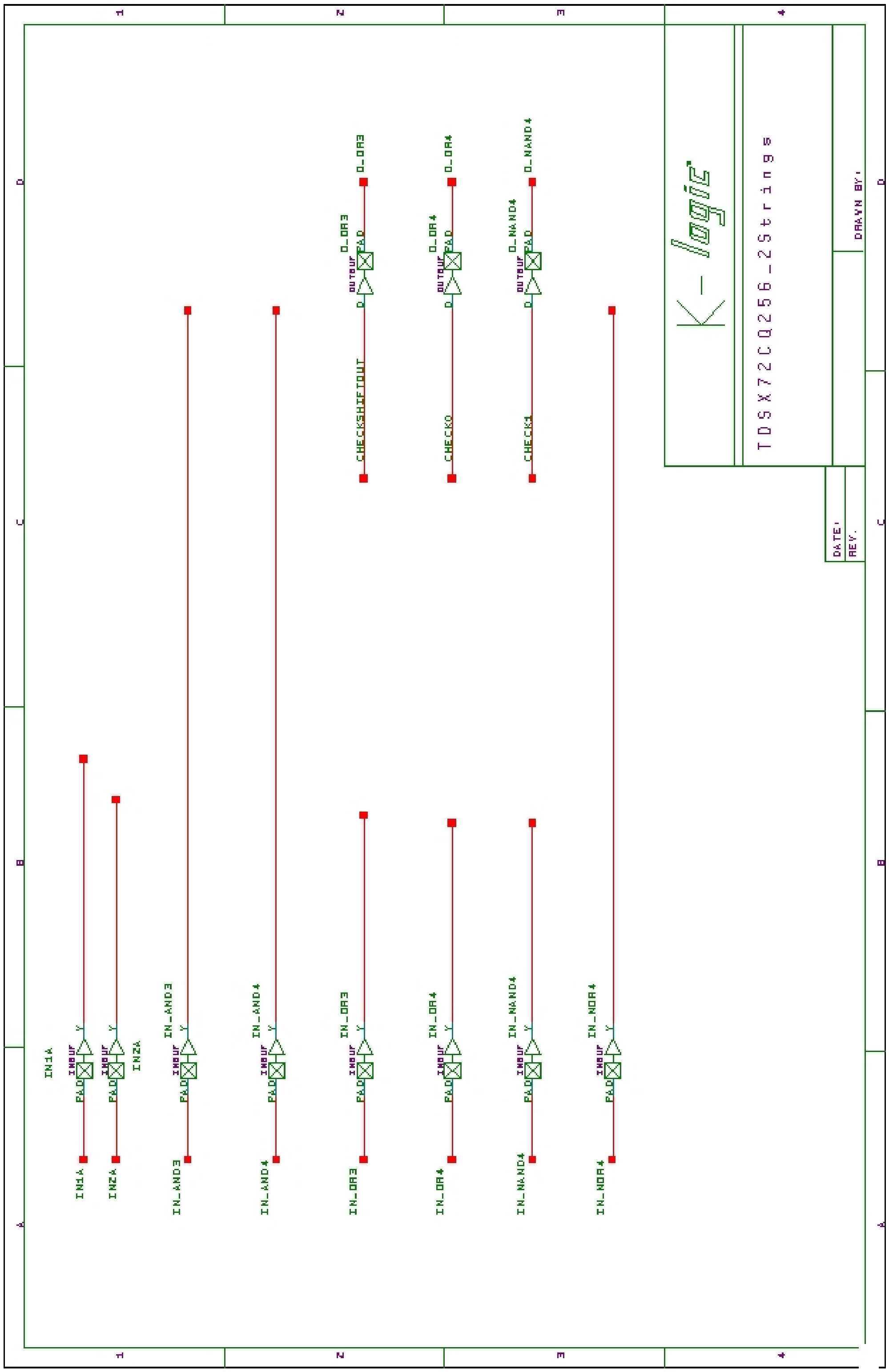
Figure 26 Post-annealing falling edge of DUT 67774, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

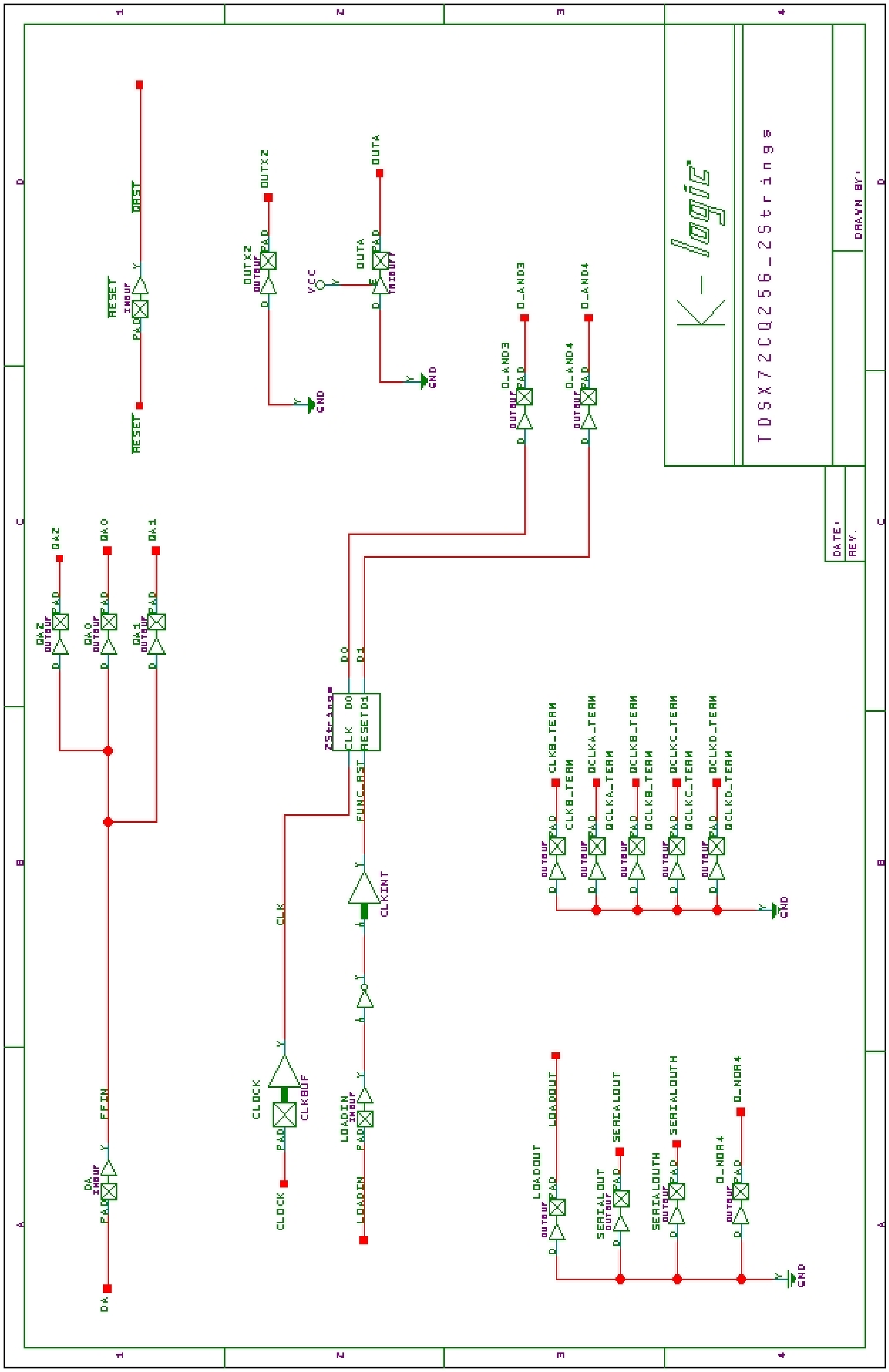
Appendix A DUT Bias

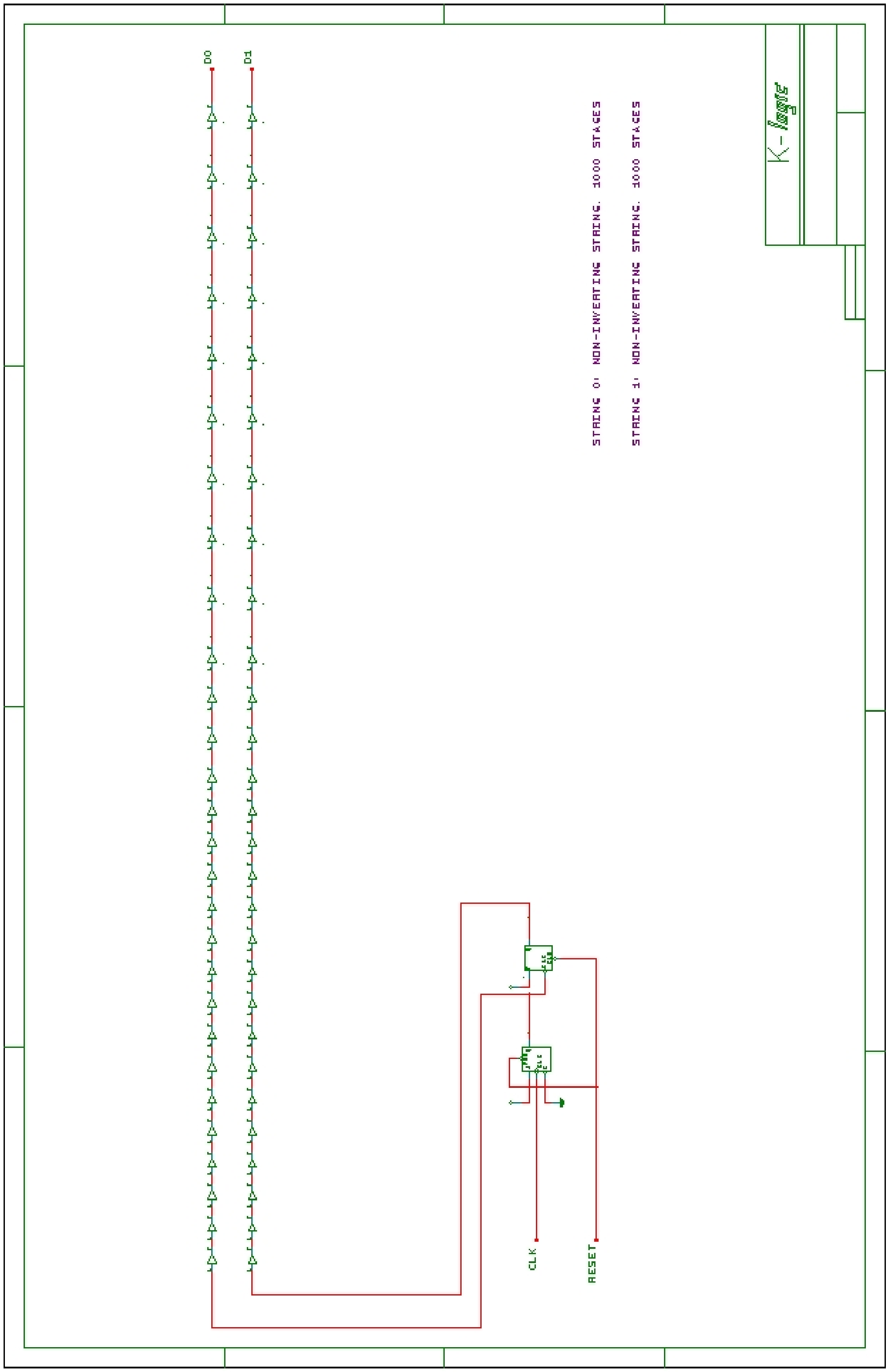


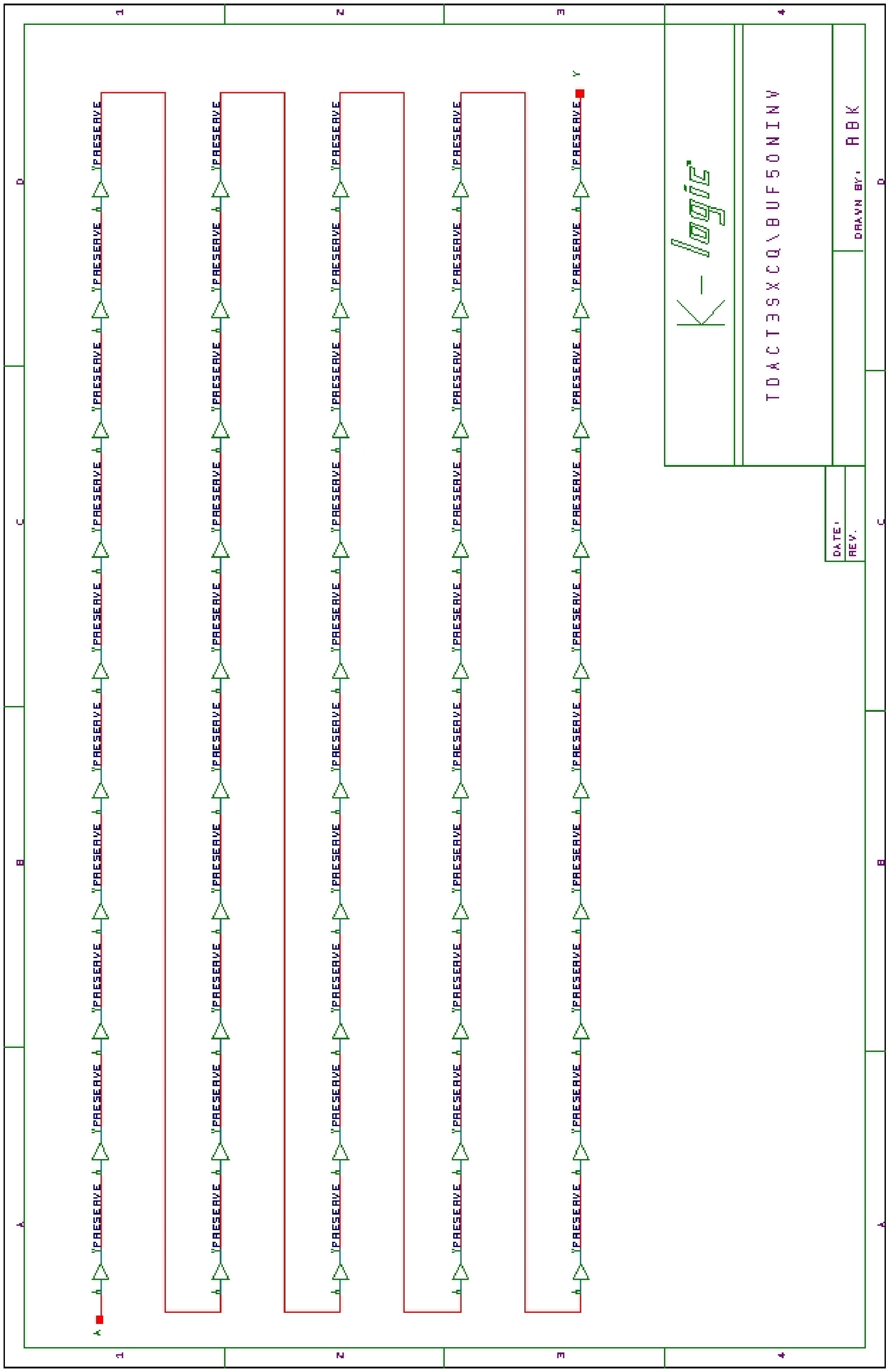


APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

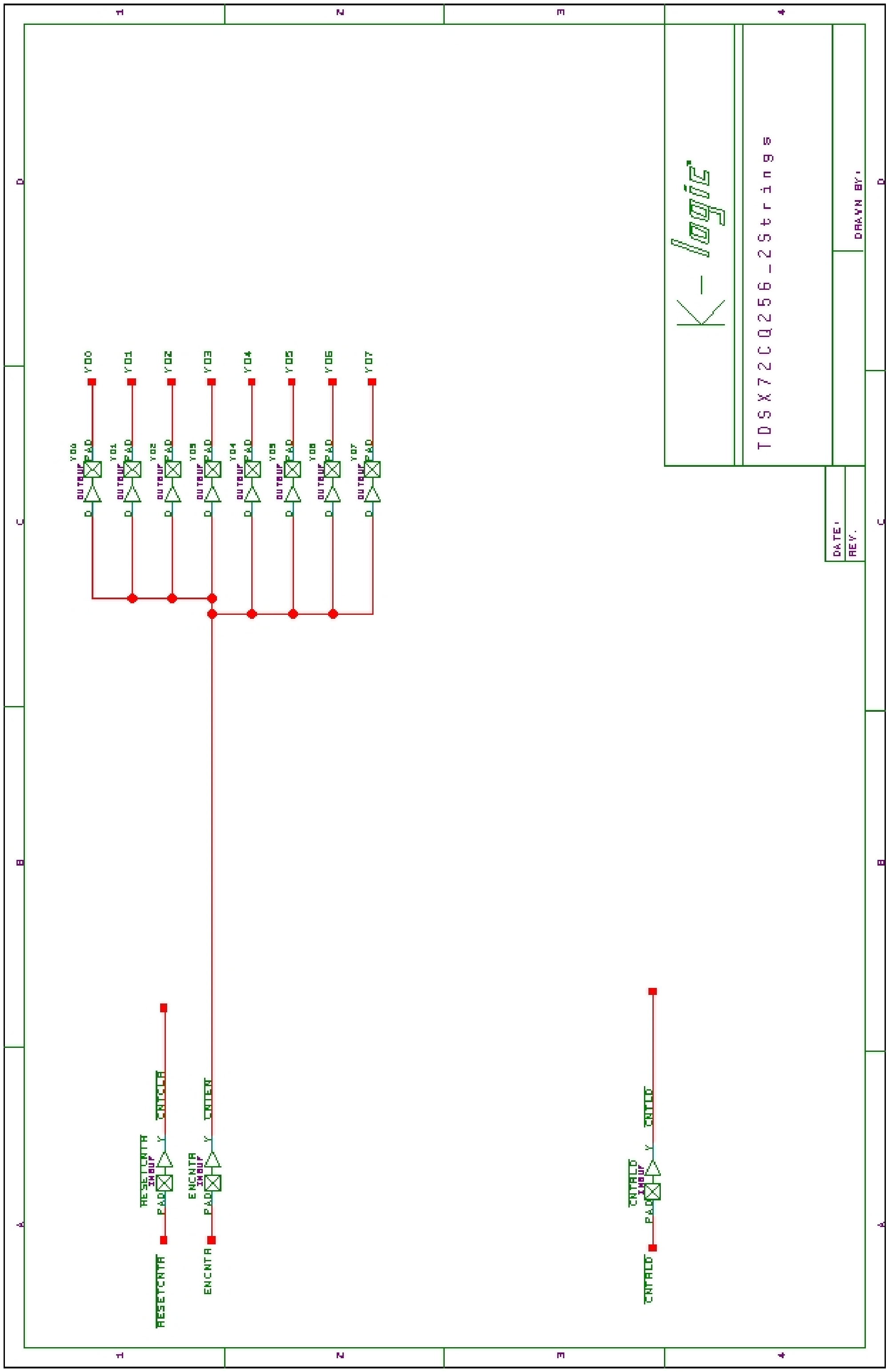


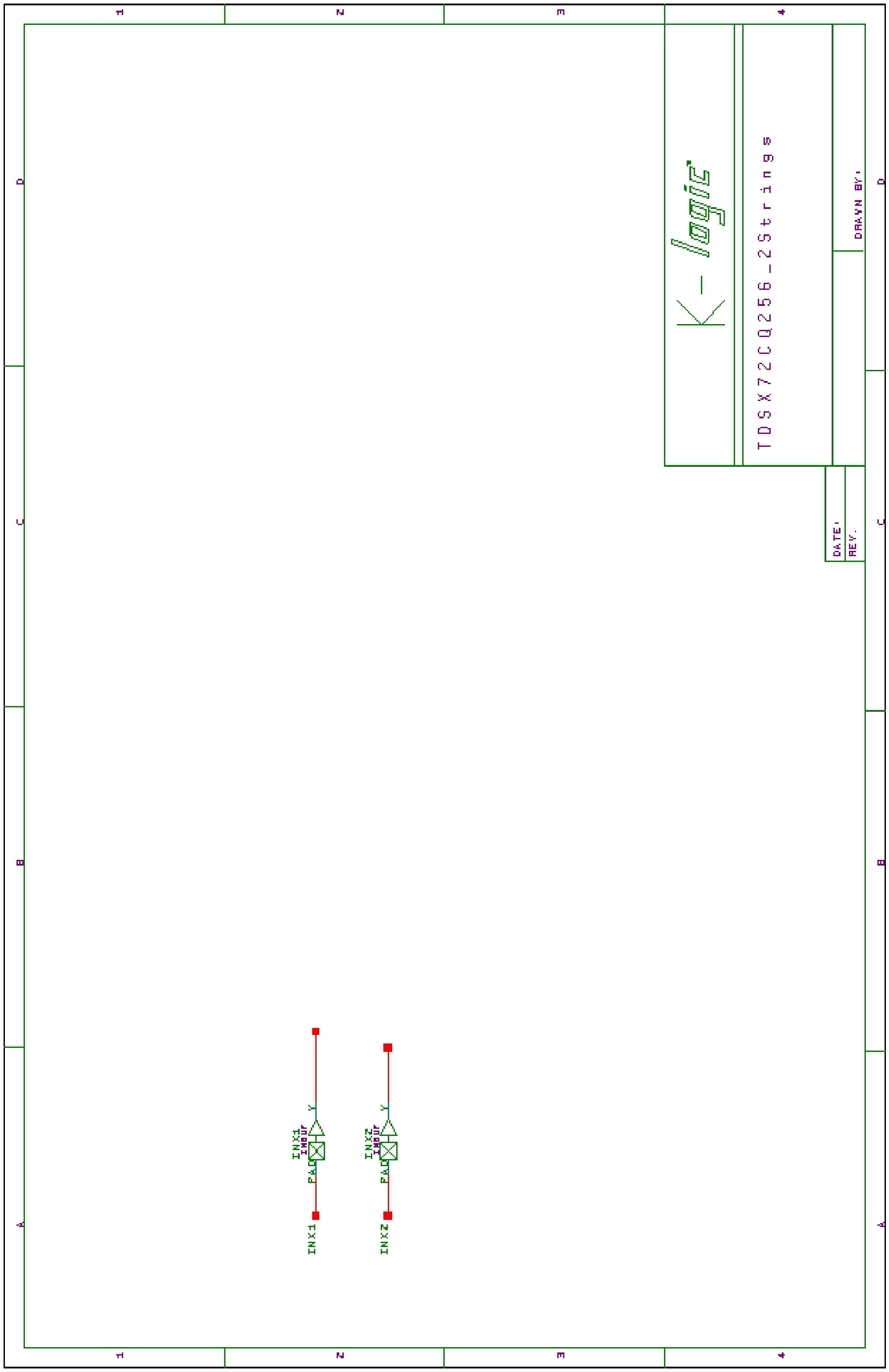

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

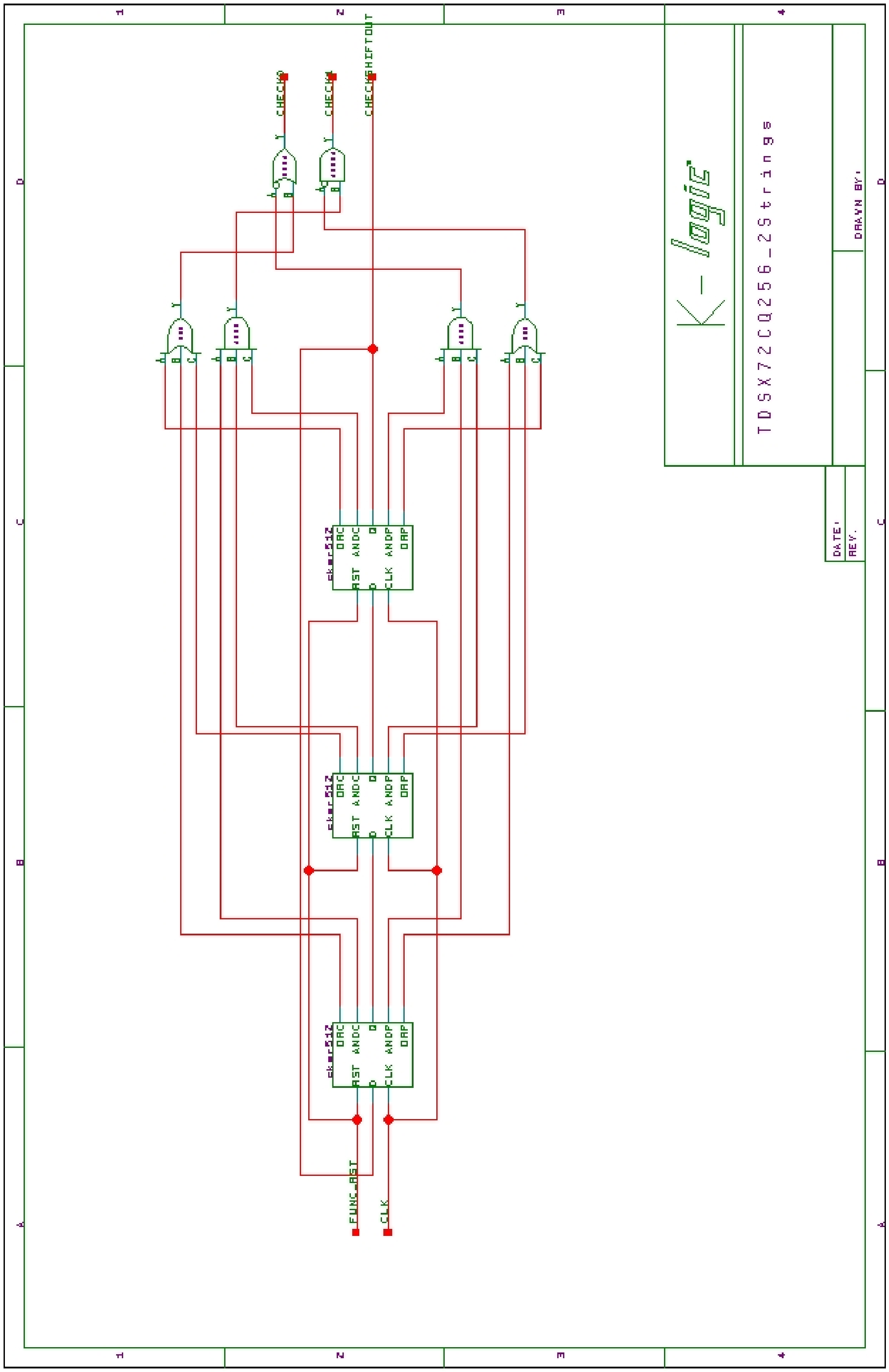

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET

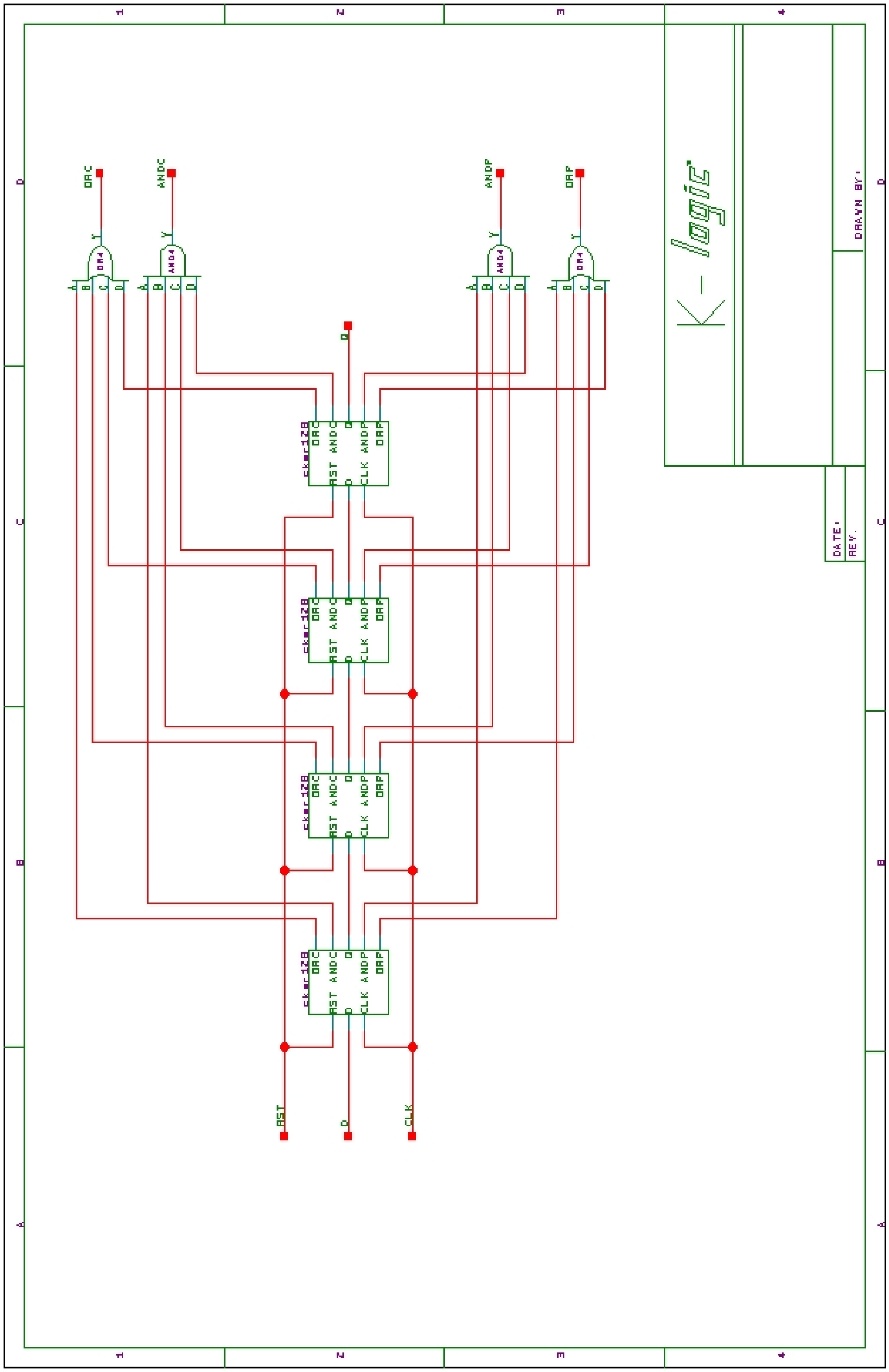


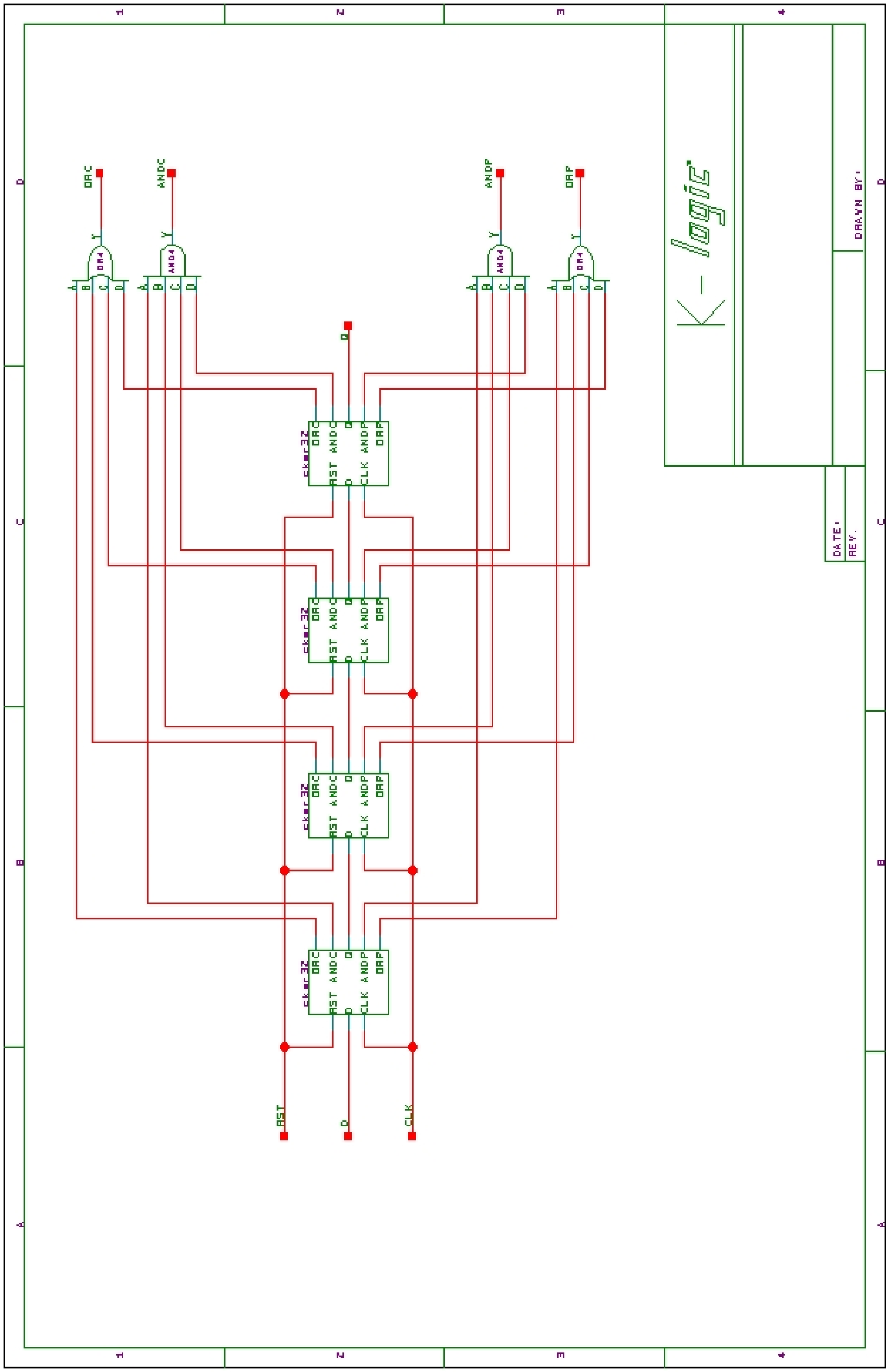
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.

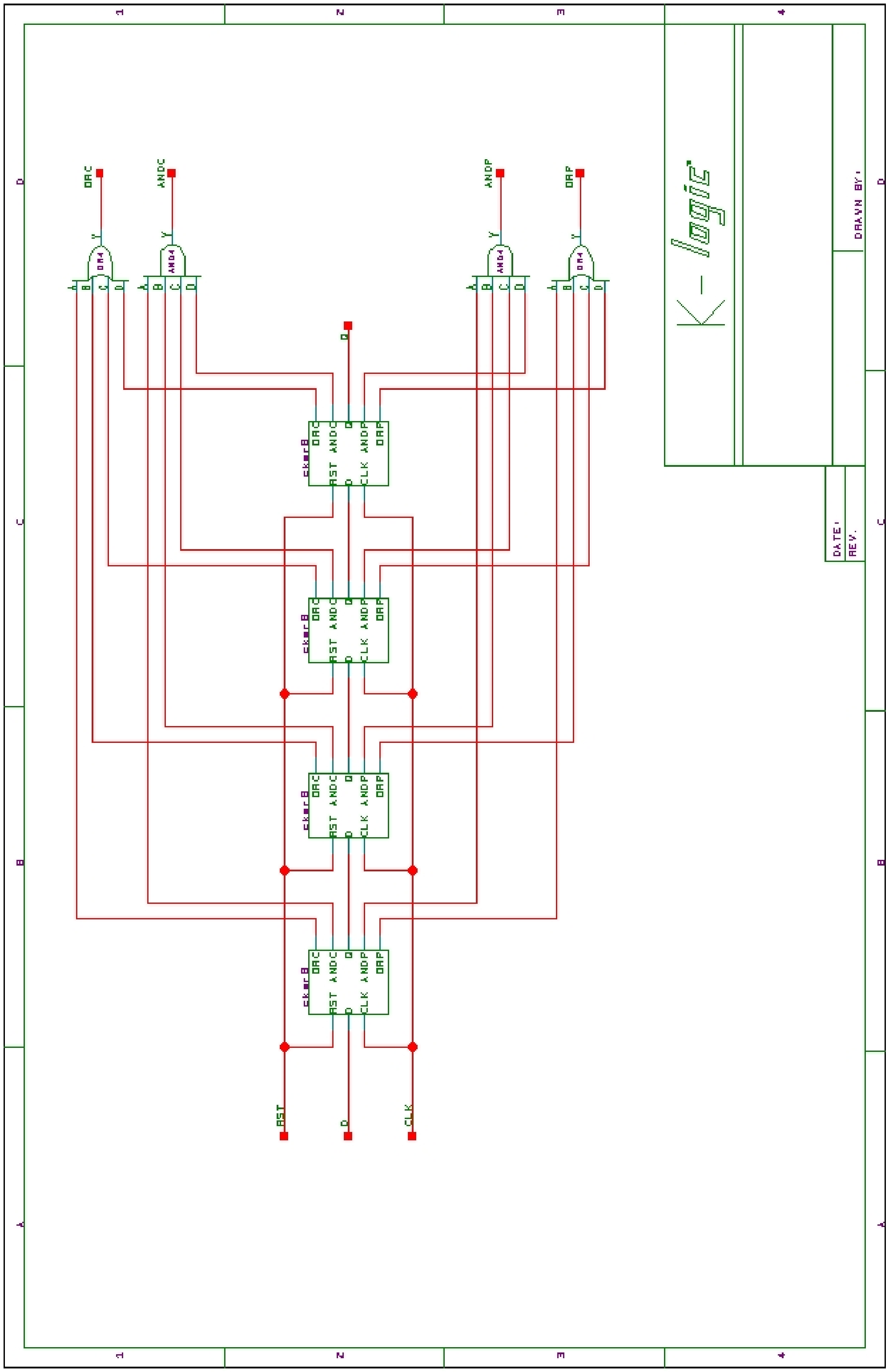

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
INBUF
RESETCNTA
CNTCLR
ENCNTA
CNTEN
CNTALD
CNTLD

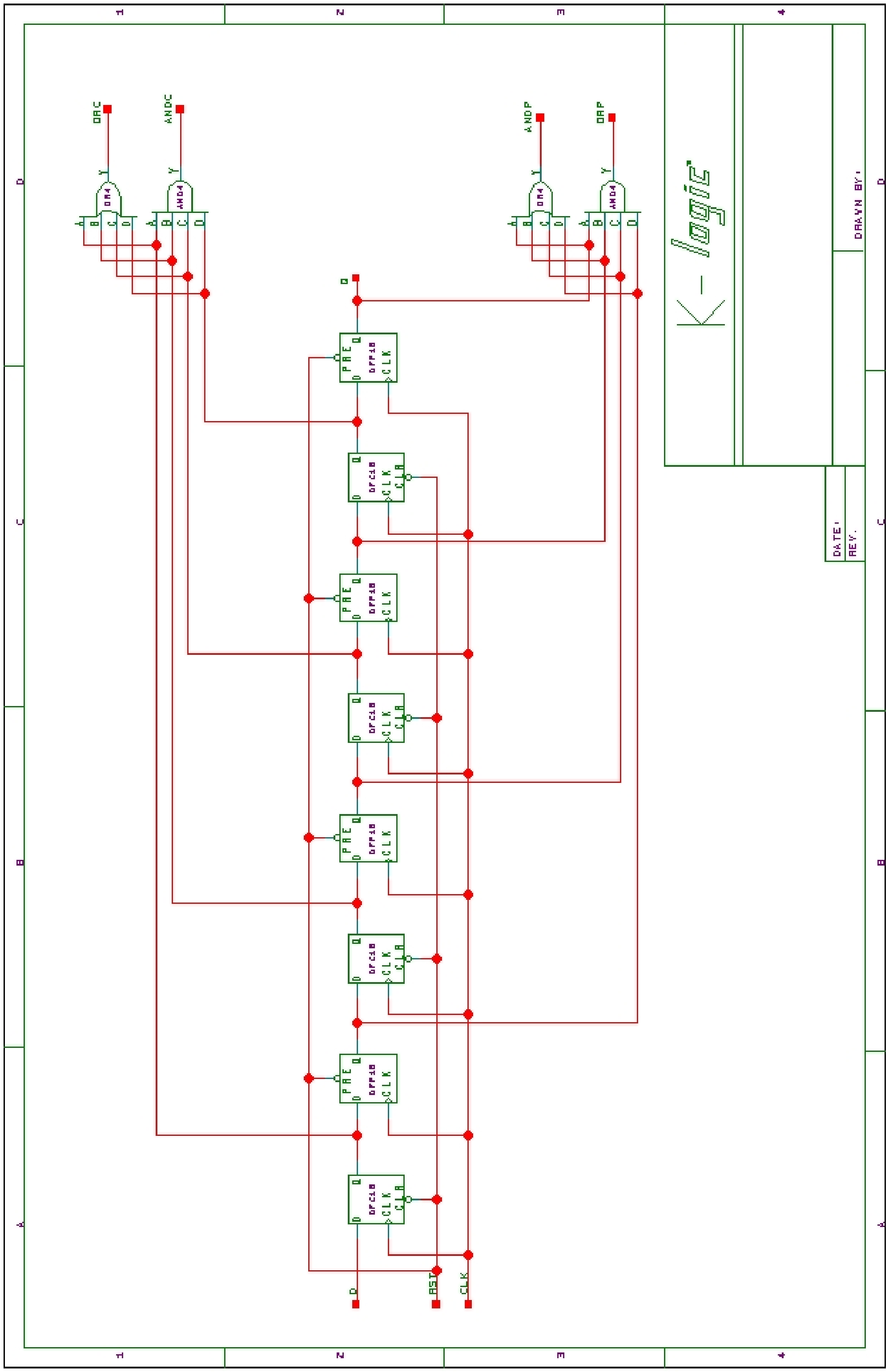

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INBUF
PAD
Y
INX2

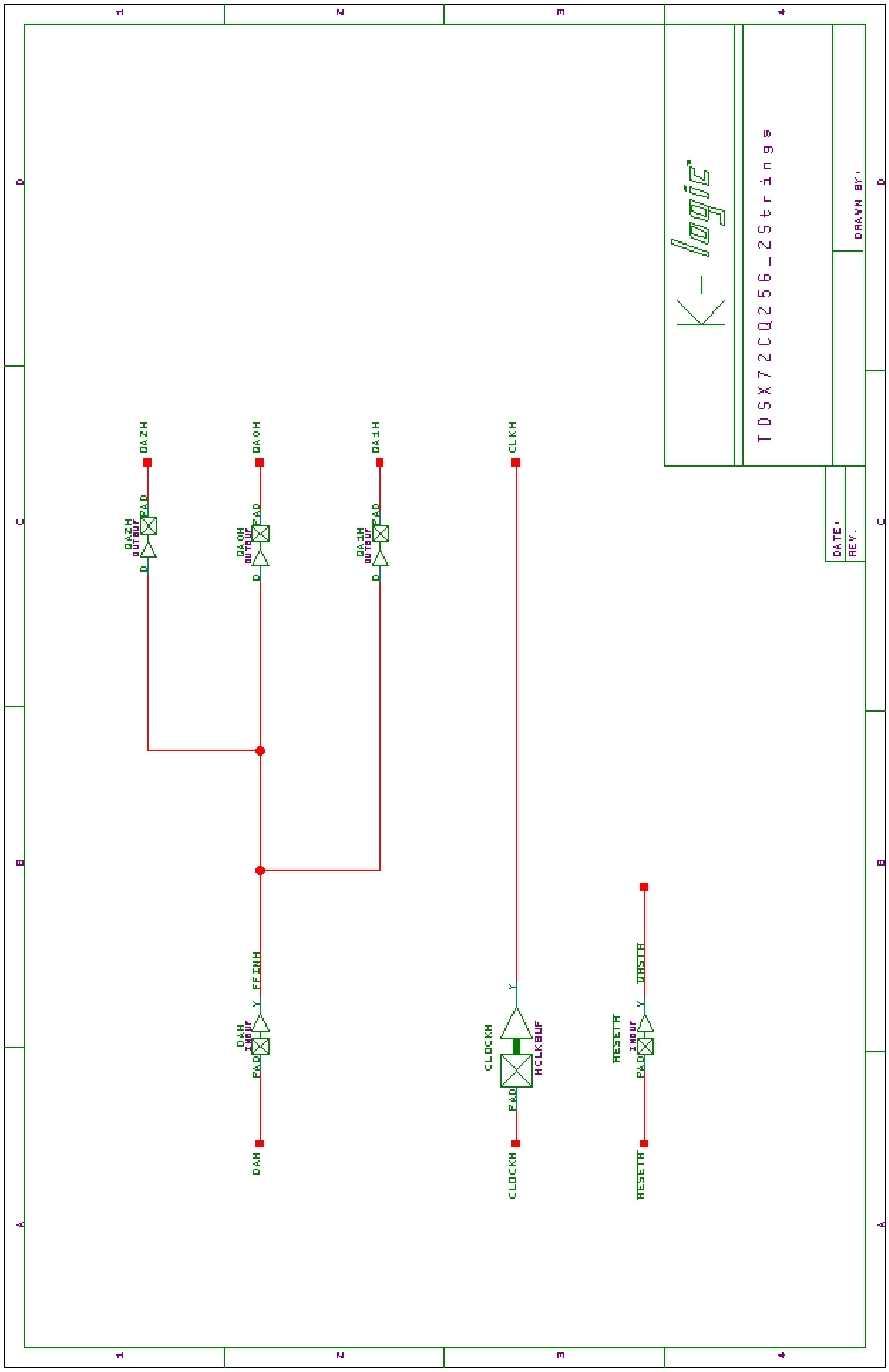

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

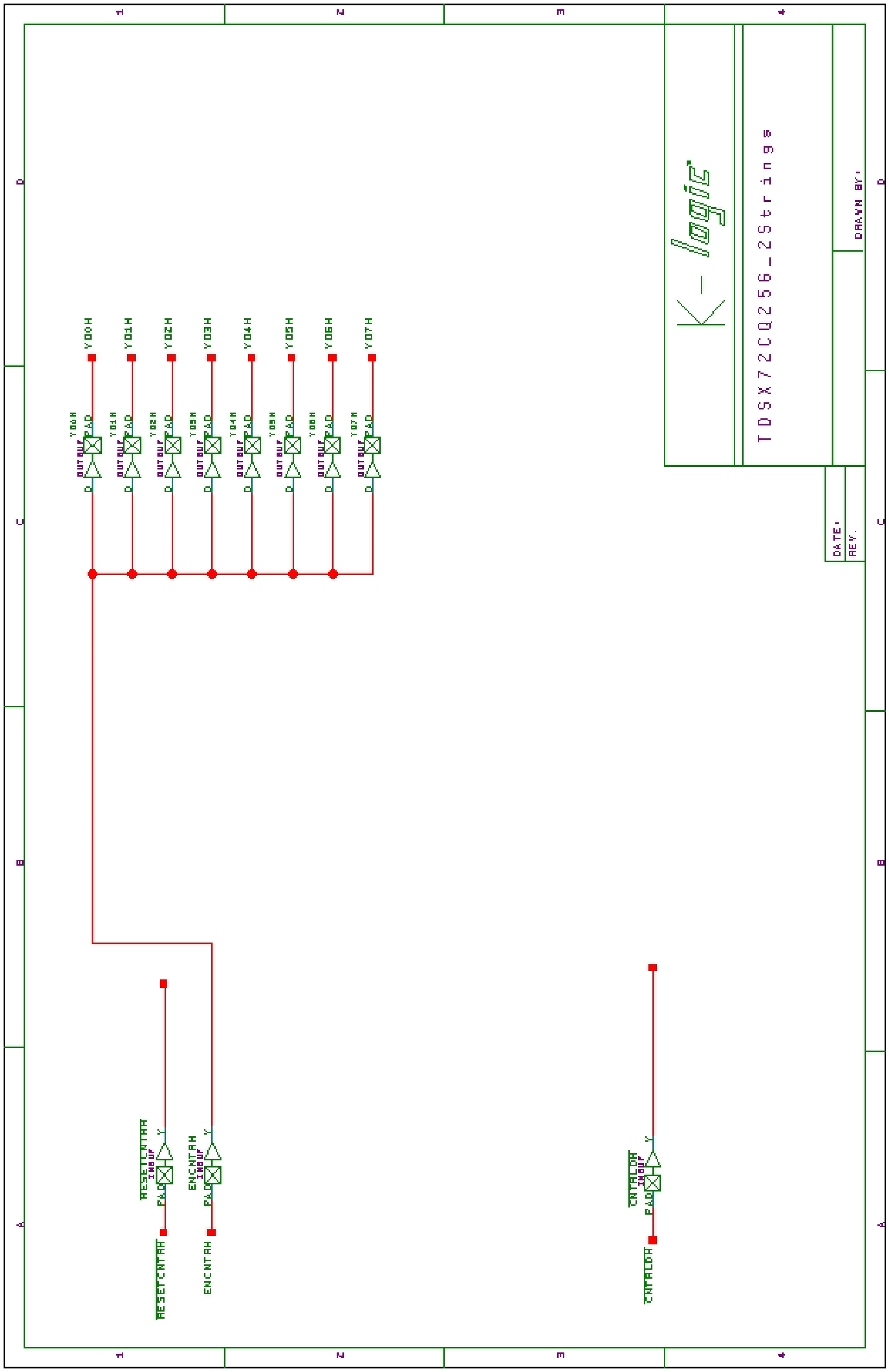

ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

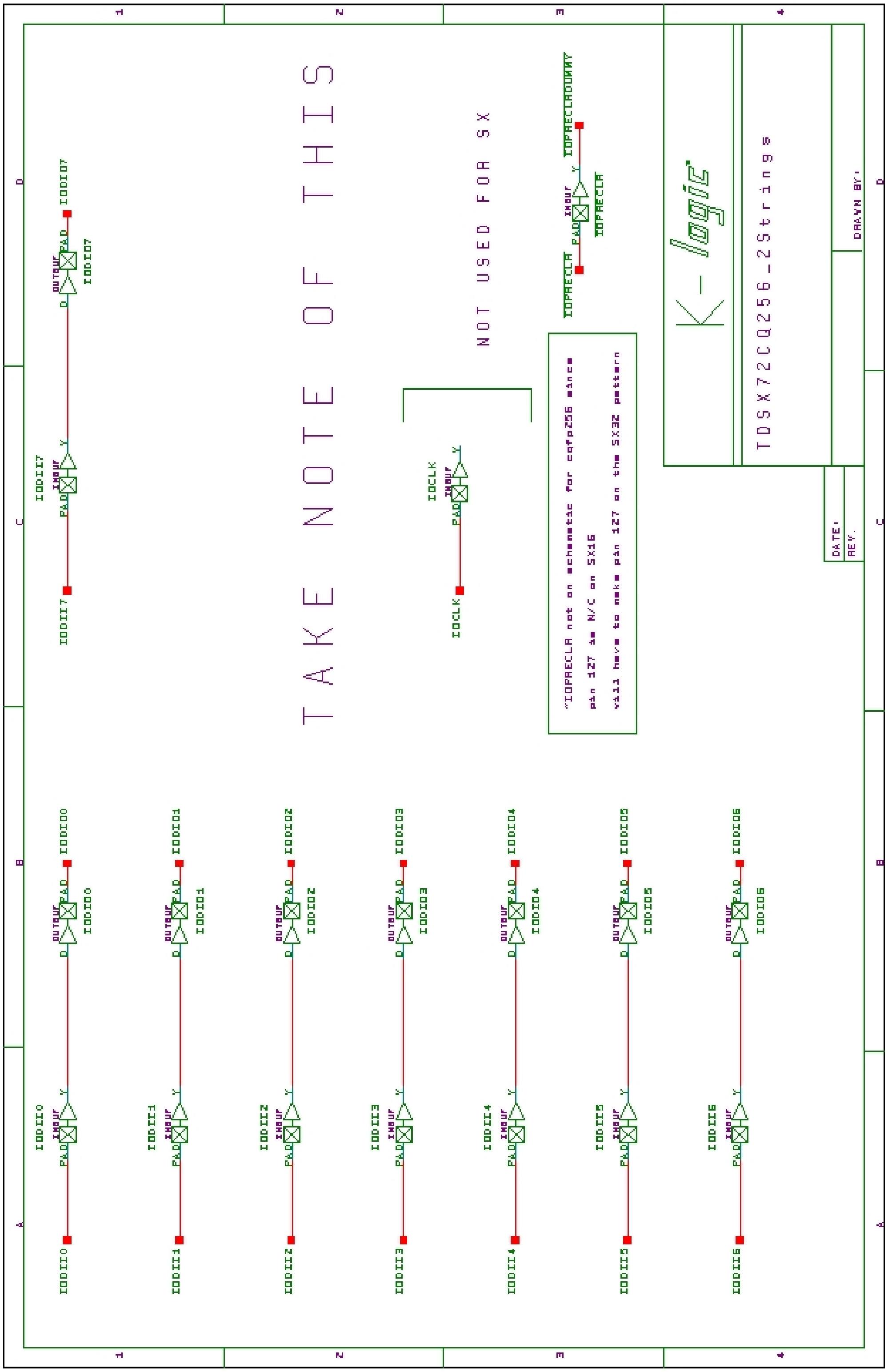

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr32
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

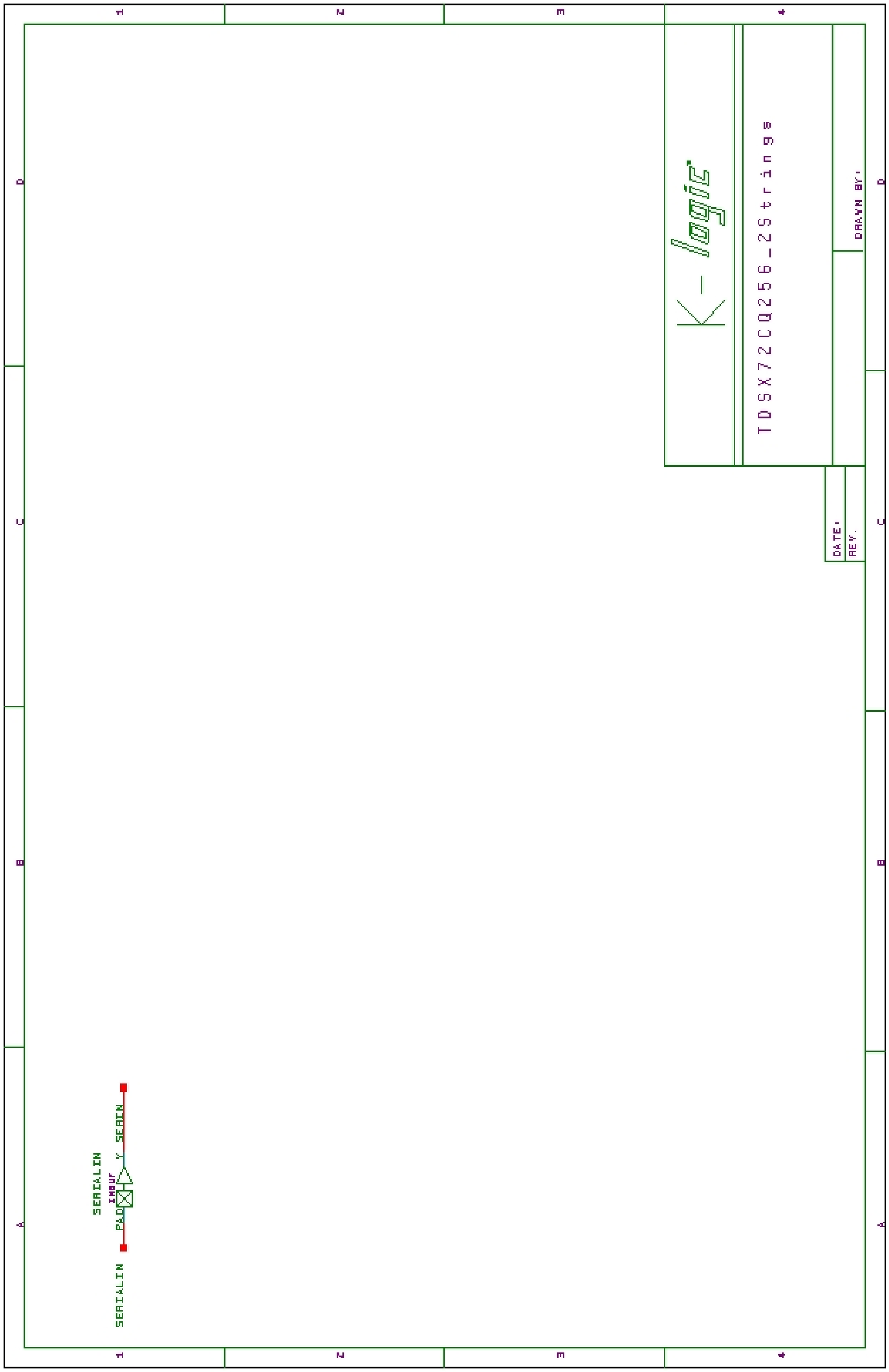

ORC
ANDC
ANDP
ORP
Q
ckmrB
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
RST
CLK
K – logic
DRAWN BY:
DATE:
REV.

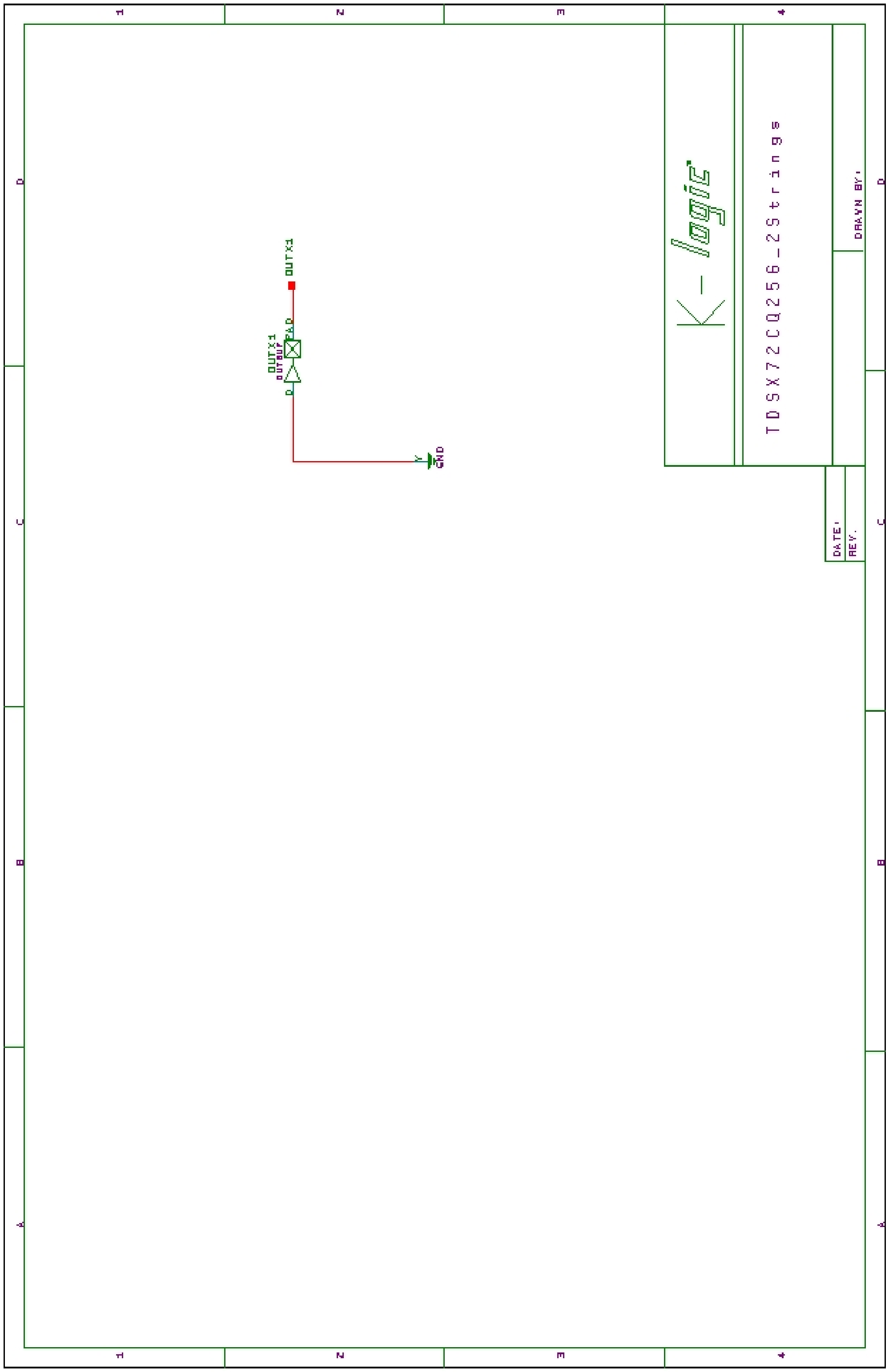

DA2H
DA0H
DA1H
CLKH
OUTBUF
PAD
D
DAH
INBUF
FFINH
CLOCKH
HCLKBUF
RESETH
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALDH
INBUF


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
IOCLK
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODII7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
IODIO7
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.



K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
SERIALIN
PAD
INBUF
Y
SERIN


K-logic
TDSX72CQ256_2Strings
OUTX1
OUTBUF
PAD
D
GND
DRAWN BY:
DATE:
REV.