TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX32SU-D1HLK1
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 79 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 5 days room temperature annealing: average I_{CCA} = 74.69 mA, and average I_{CCI} = 55 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/ and http://www.actel.com) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. In this test, the threshold of most of the available inputs is measured.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 74821, 74858 and 74862 are irradiated to 60 krad; DUT 74871, 74912 and 74953 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D1HLK1
Quantity Tested	6
Serial Number	60 krad: 74821, 74858, 74862 100 krad: 74871, 74912, 74953
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

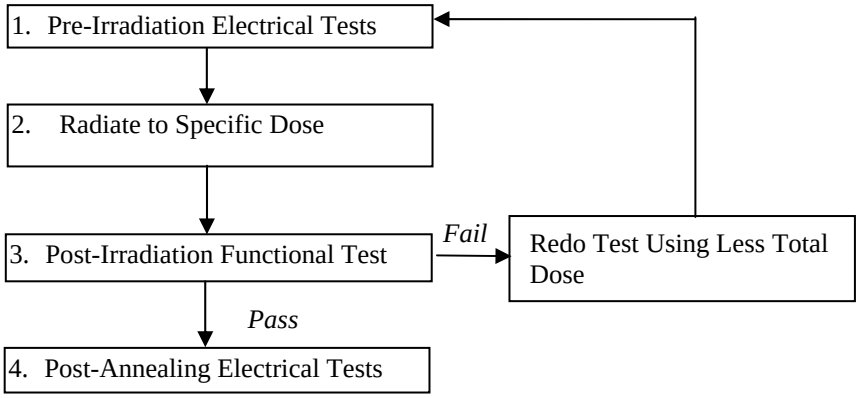


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs in both the 60-krad group and 100-krad group are bias-annealed for 5 days after the irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is probably due to the state changes during irradiation. However, this transition does not affect the functionality since each DUT passed the gross functionality test right after the irradiation.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
74821	60 krad	20	8	46	33
74858	60 krad	18	8	43	21
74862	60 krad	20	16	49	25
74871	100 krad	322	61	217	55
74912	100 krad	289	79	227	59
74953	100 krad	307	84	233	51

The 60 krad group shows the post-annealed I_{CC} passing the 25 mA spec. For the 100-krad group, a semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 74953, the tolerance is extracted as 79 krad for 10-year mission.

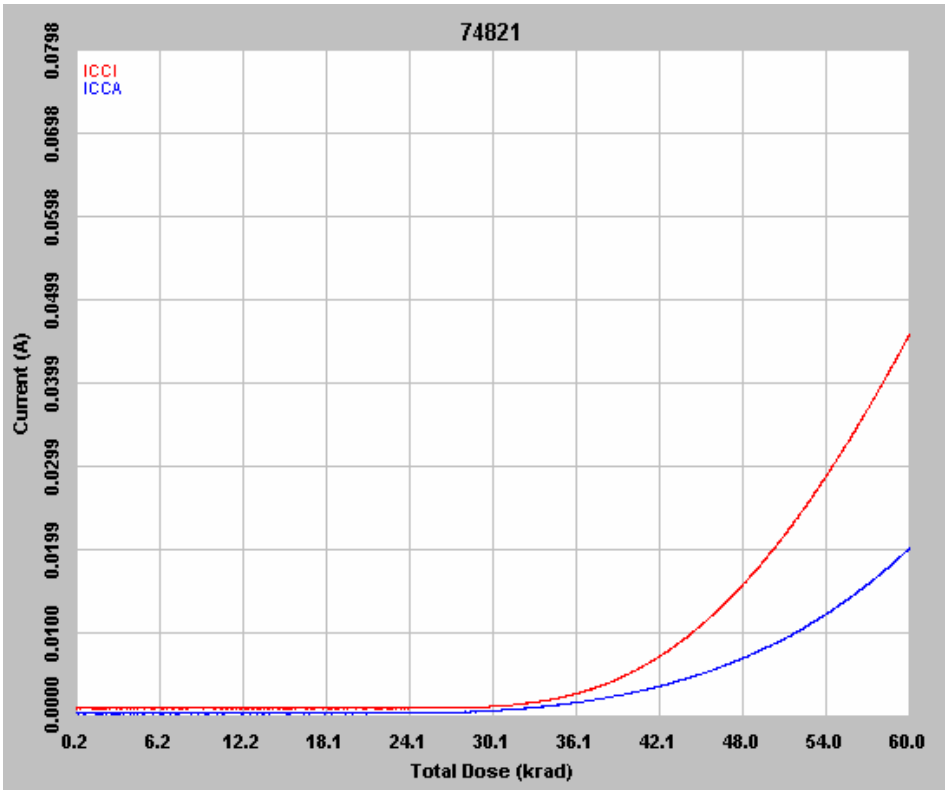


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 74821, 60 krad total dose

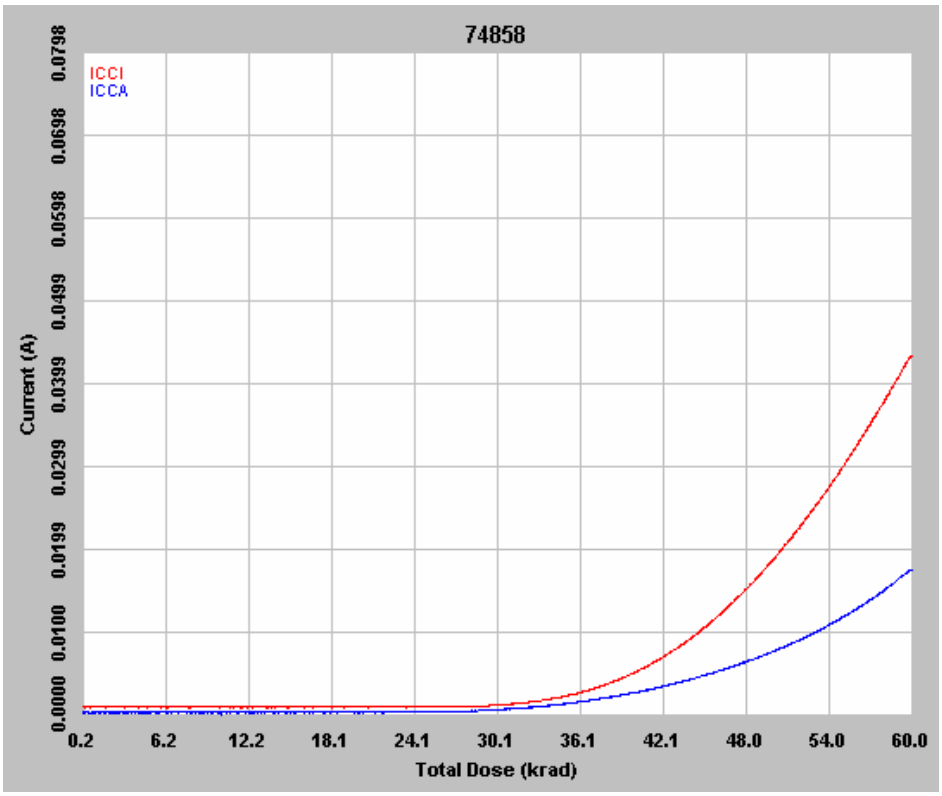


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 74858, 60 krad total dose

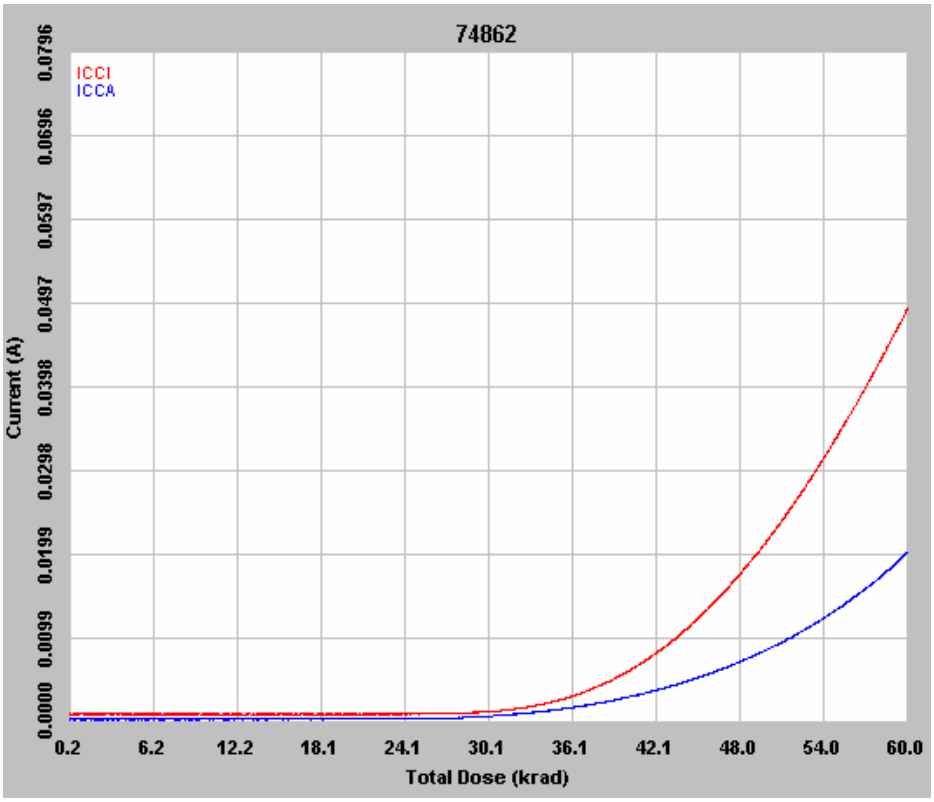


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 74862, 60 krad total dose

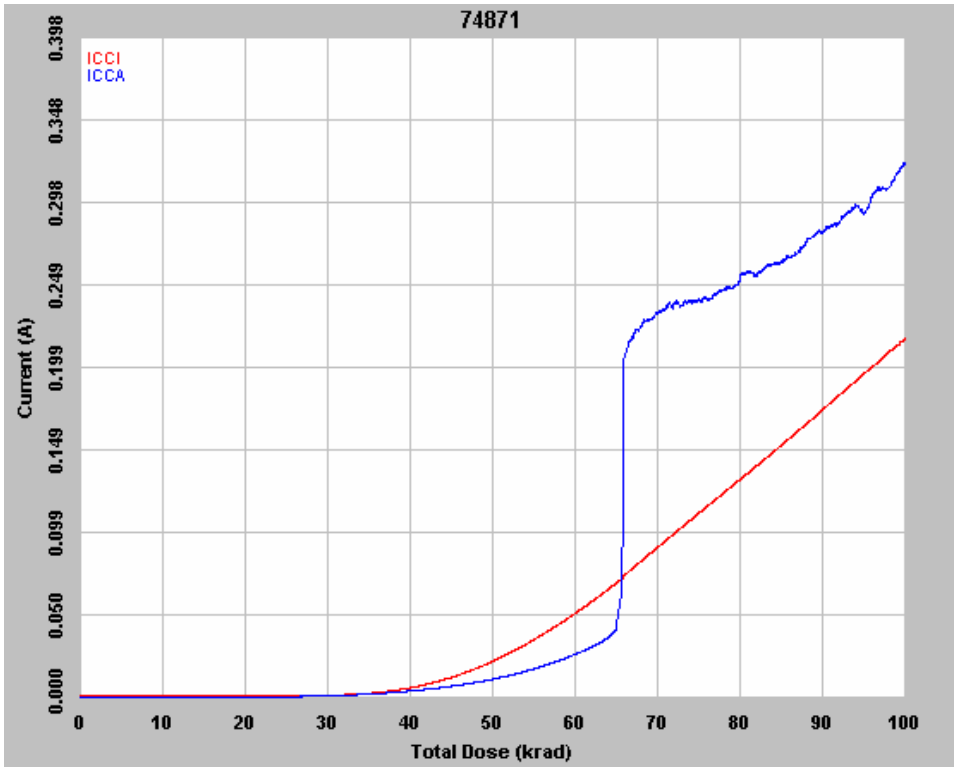


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 74871, I_{CCA} shows a transition near 66 krad

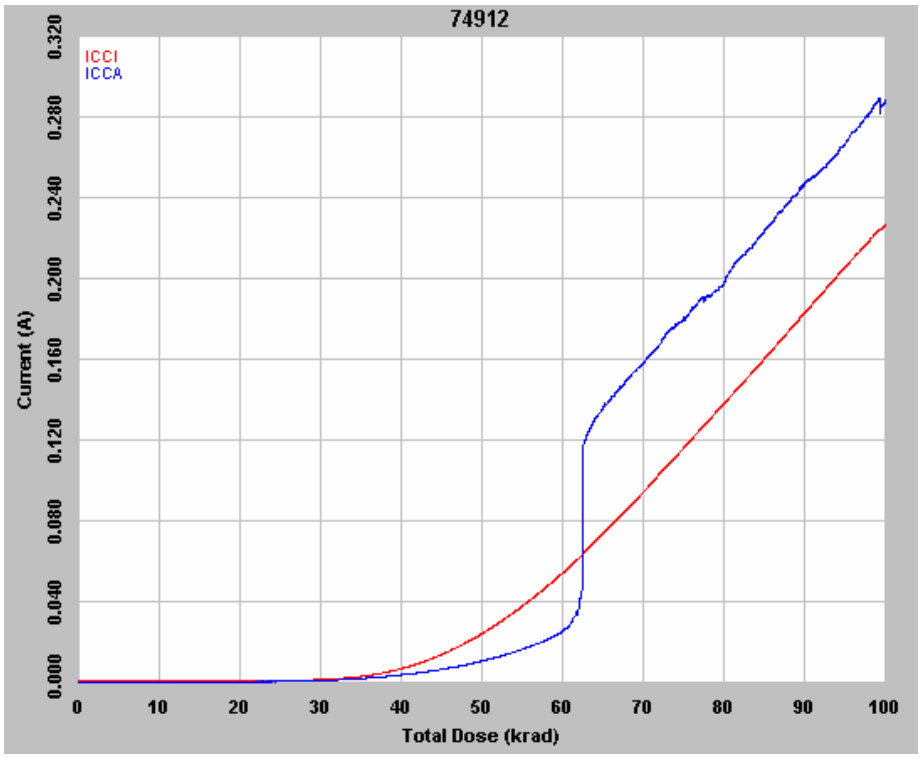


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 74912, I_{CCA} shows a transition near 62 krad.

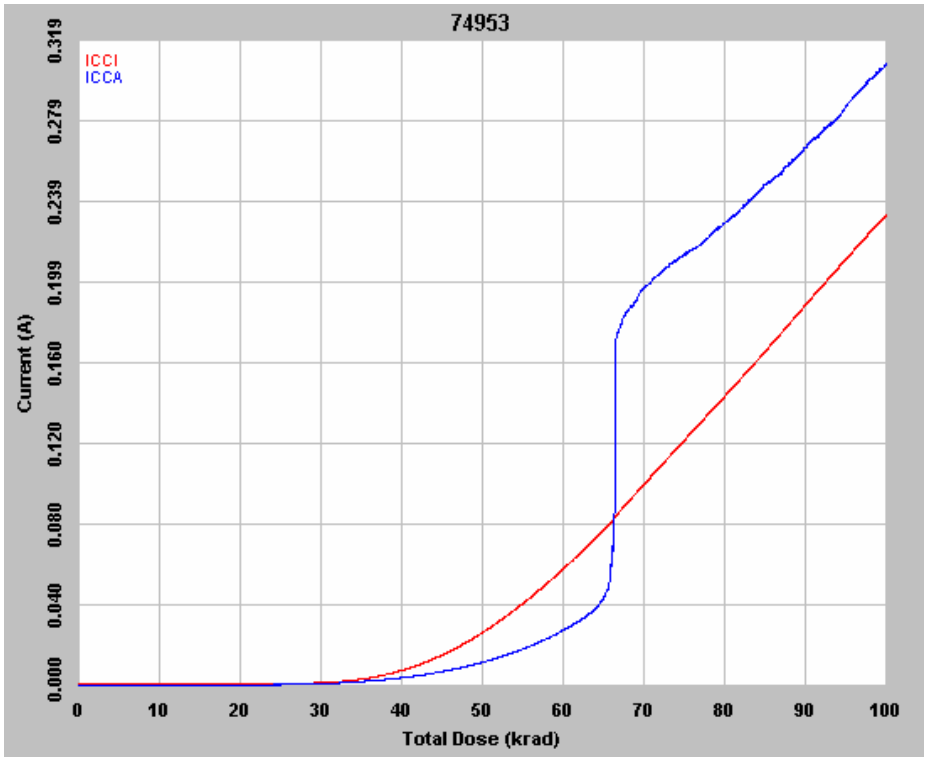


Figure 7 In flux I_{CCA} and I_{CCI} of DUT 74953, I_{CCA} shows a transition near 67 krad.

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA / QA0				DAH / QA0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.37	1.39	1.42	1.47	1.35	1.41	1.46	1.48
74858	60 krad	1.34	1.21	1.46	1.52	1.34	1.30	1.46	1.51
74862	60 krad	1.35	1.36	1.45	1.57	1.34	1.39	1.45	1.53
74871	100 krad	1.35	1.33	1.45	1.43	1.34	1.39	1.45	1.46
74912	100 krad	1.33	1.30	1.45	1.48	1.35	1.39	1.45	1.47
74953	100 krad	1.34	1.37	1.45	1.44	1.35	1.37	1.44	1.48

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR / YO0				ENCNTRH / YO0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.34	1.40	1.44	1.48	1.36	1.37	1.43	1.46
74858	60 krad	1.33	1.37	1.45	1.44	1.36	1.38	1.45	1.45
74862	60 krad	1.33	1.21	1.46	1.56	1.35	1.39	1.45	1.48
74871	100 krad	1.36	1.39	1.46	1.46	1.34	1.35	1.47	1.43
74912	100 krad	1.36	1.40	1.46	1.47	1.34	1.37	1.47	1.44
74953	100 krad	1.35	1.36	1.46	1.40	1.36	1.34	1.46	1.44

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0 / IDIO0				IDII1/ IDIO1			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.33	1.46	1.45	1.54	1.34	1.20	1.45	1.52
74858	60 krad	1.36	1.40	1.46	1.52	1.34	1.30	1.46	1.48
74862	60 krad	1.33	1.30	1.46	1.46	1.35	1.39	1.45	1.46
74871	100 krad	1.33	1.41	1.46	1.48	1.36	1.41	1.45	1.48
74912	100 krad	1.35	1.43	1.46	1.54	1.33	1.31	1.46	1.53
74953	100 krad	1.36	1.36	1.45	1.42	1.35	1.36	1.46	1.43

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2 / IDIO2				IDII3 / IDIO3			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.34	1.38	1.46	1.61	1.32	1.31	1.46	1.50
74858	60 krad	1.35	1.40	1.45	1.45	1.35	1.40	1.44	1.47
74862	60 krad	1.35	1.38	1.45	1.48	1.35	1.33	1.45	1.45
74871	100 krad	1.36	1.38	1.45	1.47	1.35	1.34	1.46	1.43
74912	100 krad	1.35	1.24	1.47	1.52	1.34	1.29	1.44	1.57
74953	100 krad	1.35	1.35	1.45	1.42	1.34	1.37	1.44	1.41

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4 / IDIO4				IDII5 / IDIO5			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.36	1.31	1.45	1.42	1.32	1.38	1.45	1.48
74858	60 krad	1.36	1.39	1.45	1.47	1.35	1.38	1.41	1.47
74862	60 krad	1.29	1.34	1.43	1.49	1.35	1.38	1.43	1.47
74871	100 krad	1.34	1.35	1.45	1.39	1.35	1.35	1.42	1.42
74912	100 krad	1.34	1.40	1.44	1.48	1.49	1.50	1.50	1.52
74953	100 krad	1.36	1.36	1.46	1.42	1.34	1.36	1.43	1.45

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6 / IDIO6				IDII7 / IDIO7			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
74821	60 krad	1.33	1.39	1.47	1.59	1.34	1.42	1.45	1.46
74858	60 krad	1.34	1.39	1.46	1.46	1.34	1.37	1.47	1.43
74862	60 krad	1.36	1.40	1.47	1.46	1.34	1.34	1.46	1.44
74871	100 krad	1.33	1.39	1.46	1.47	1.34	1.37	1.47	1.42
74912	100 krad	1.36	1.43	1.46	1.48	1.34	1.40	1.47	1.46
74953	100 krad	1.36	1.35	1.46	1.42	1.34	1.23	1.46	1.41

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
74821	60 krad	0.009	0.009	0.105	0.104	0.174	0.174	0.439	0.440	0.902	0.904
74858	60 krad	0.009	0.009	0.104	0.104	0.173	0.173	0.437	0.437	0.899	0.898
74862	60 krad	0.009	0.009	0.101	0.102	0.169	0.170	0.427	0.427	0.877	0.879
74871	100 krad	0.009	0.009	0.103	0.105	0.171	0.175	0.433	0.440	0.889	0.905
74912	100 krad	0.009	0.009	0.103	0.104	0.171	0.174	0.432	0.439	0.887	0.902
74953	100 krad	0.009	0.009	0.102	0.104	0.171	0.173	0.431	0.437	0.886	0.899

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
74821	60 krad	4.99	4.98	4.87	4.86	4.65	4.64	4.06	4.04	2.70	2.63
74858	60 krad	4.99	4.98	4.87	4.86	4.65	4.64	4.06	4.04	2.71	2.65
74862	60 krad	4.99	4.98	4.86	4.86	4.65	4.64	4.06	4.05	2.71	2.66
74871	100 krad	4.99	4.98	4.87	4.86	4.65	4.64	4.08	4.05	2.80	2.65
74912	100 krad	4.99	4.98	4.86	4.86	4.65	4.64	4.07	4.04	2.76	2.64
74953	100 krad	4.98	4.98	4.88	4.85	4.67	4.63	4.08	4.03	2.74	2.58

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. In every case the DUT passes the 10% degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation	Post-Annealing	Degradation
74821	60 krad	500.485	505.545	1.03%
74858	60 krad	494.075	502.415	1.71%
74862	60 krad	499.365	505.075	1.16%
74871	100 krad	479.76	489.88	2.14%
74912	100 krad	479.86	493.075	2.77%
74953	100 krad	493.4	505.44	2.47%

F. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

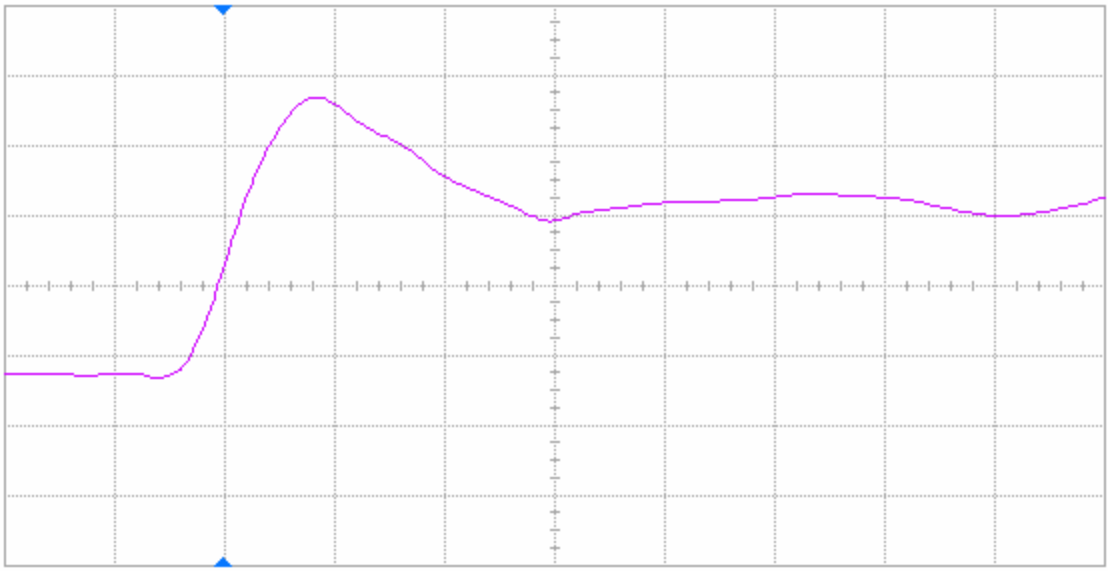


Figure 8(a) DUT 74821 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

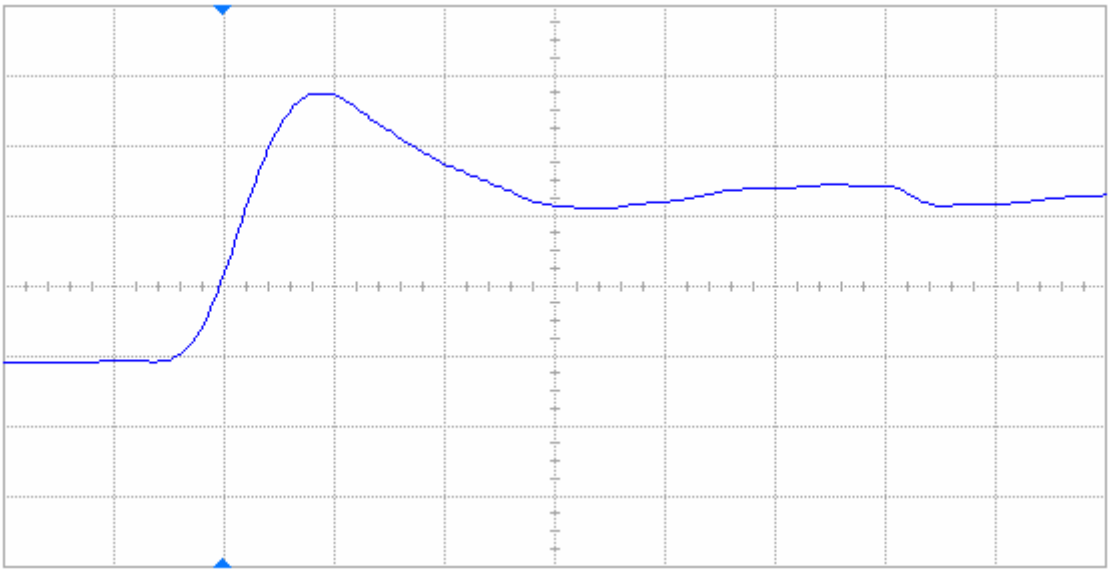


Figure 8(b) DUT 74821 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

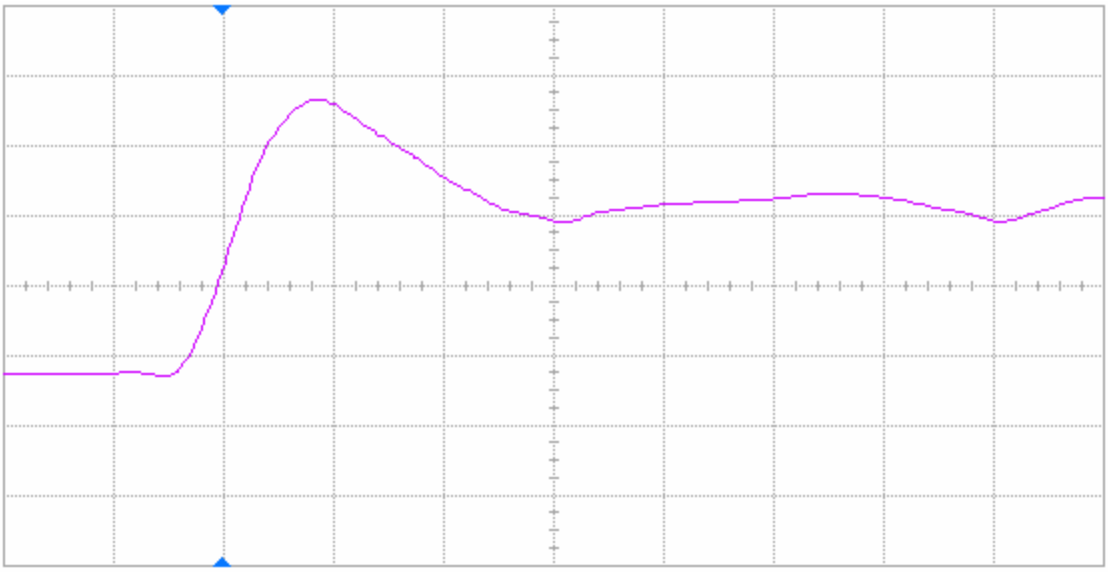


Figure 9(a) DUT 74858 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

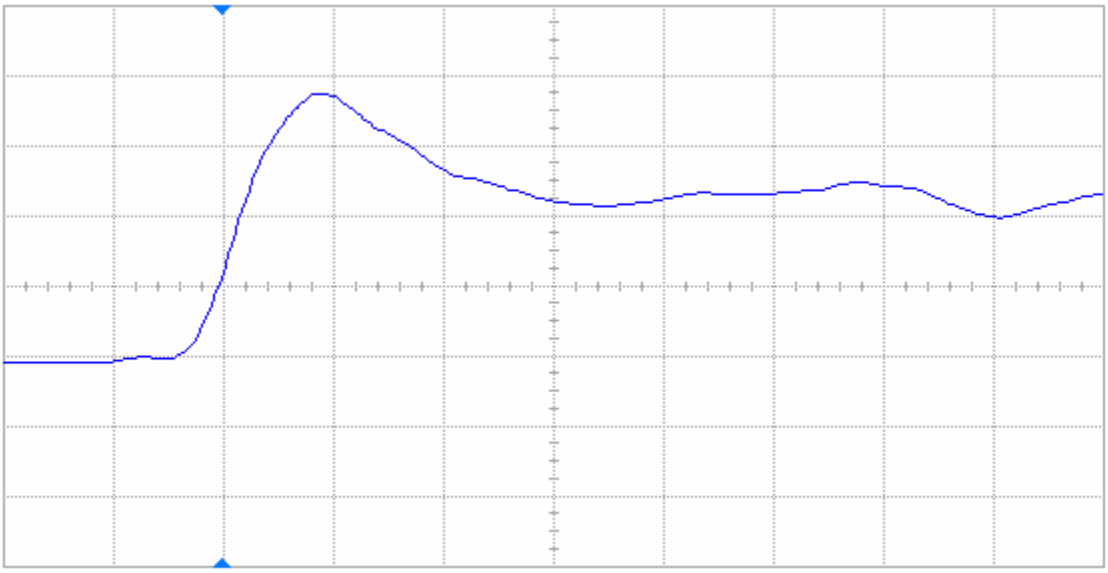


Figure 9(b) DUT 74858 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

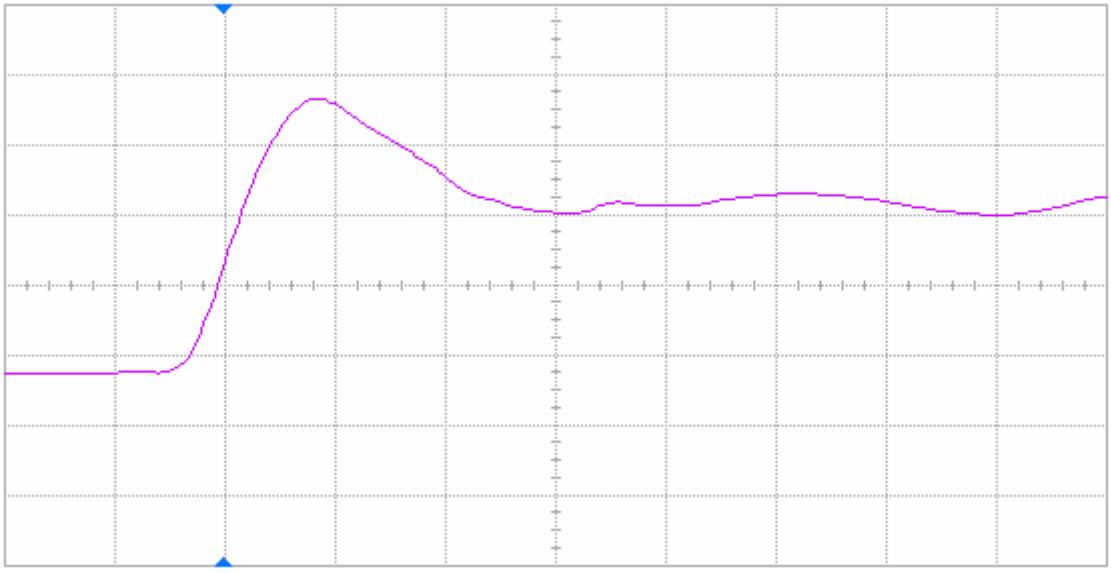


Figure 10(a) DUT 74862 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

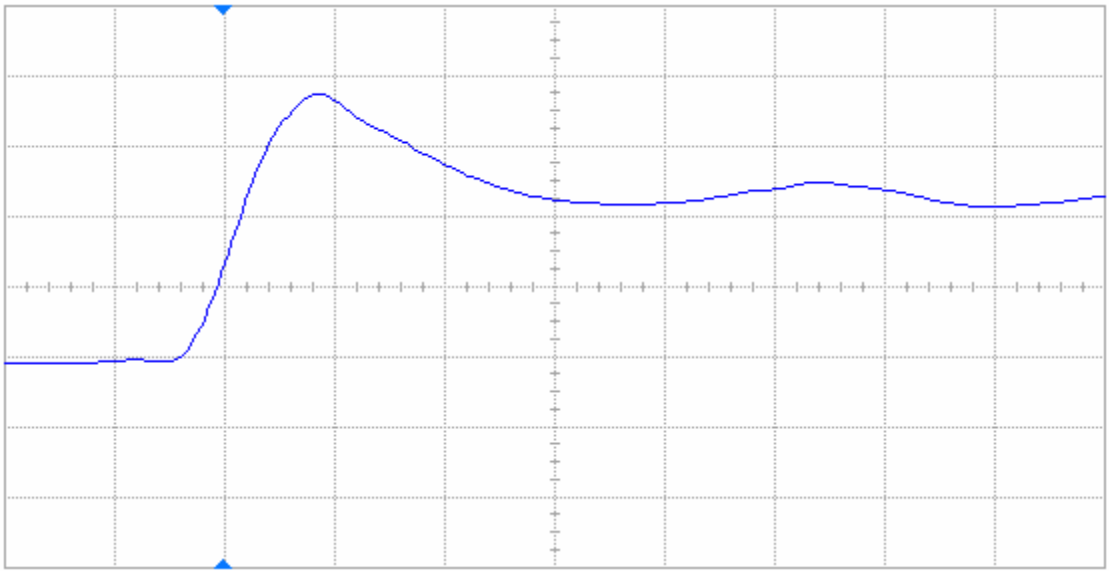


Figure 10(b) DUT 74862 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

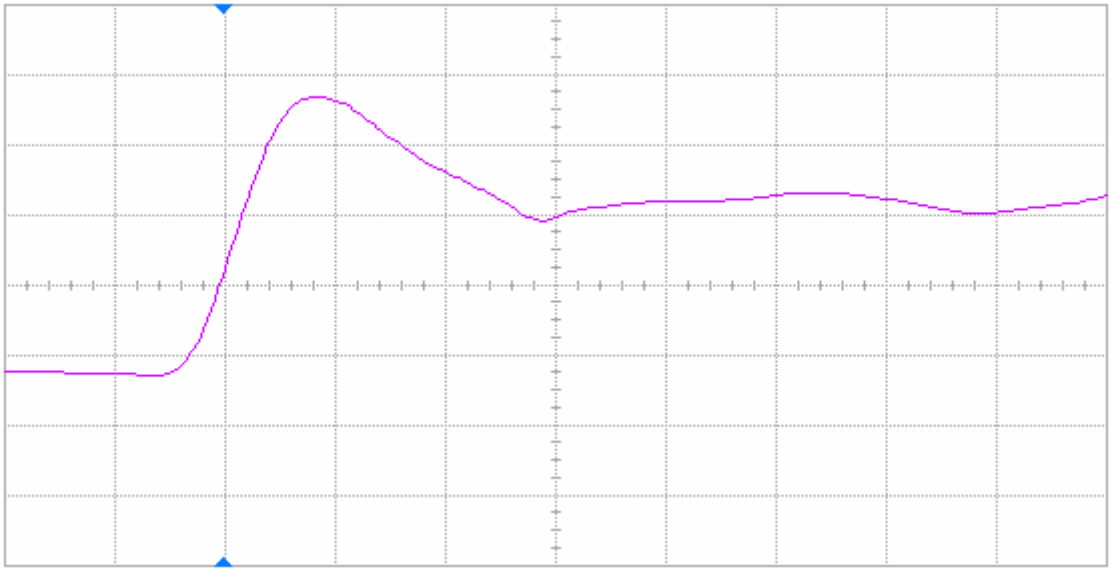


Figure 11(a) DUT 74871 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

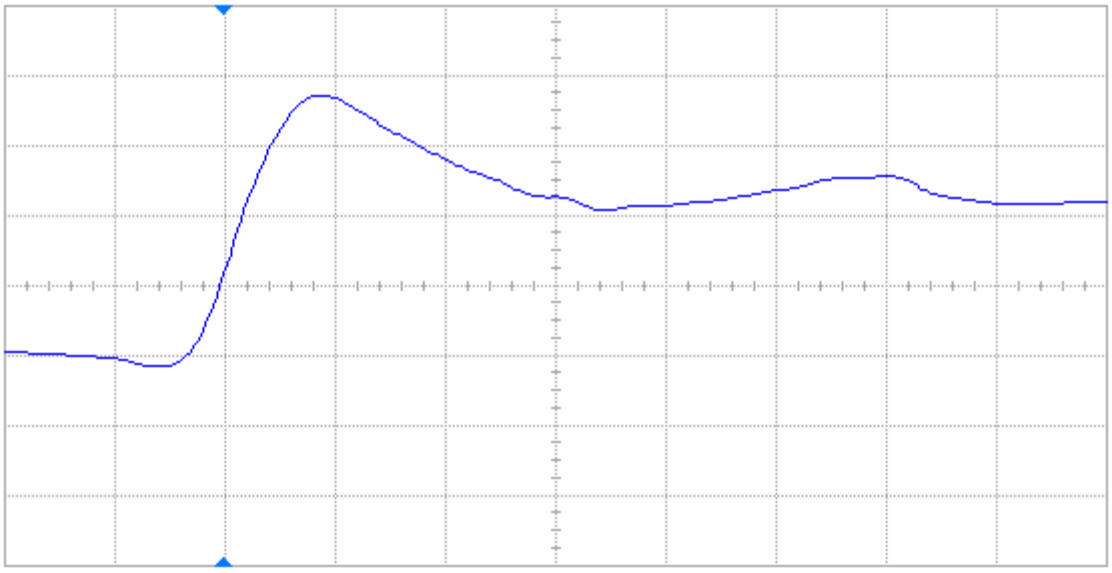


Figure 11(b) DUT 74871 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

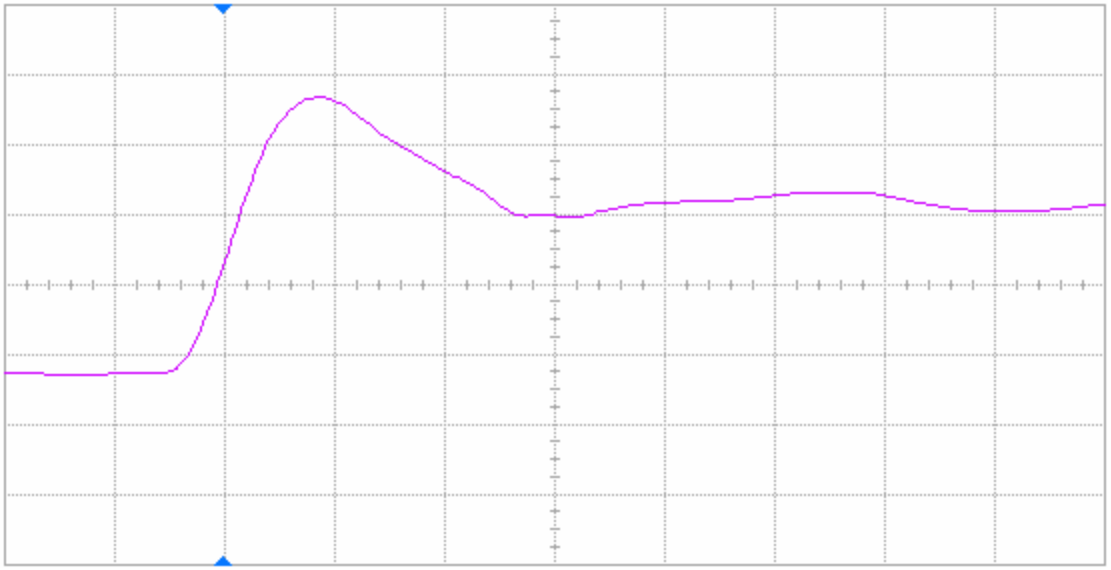


Figure 12(a) DUT 74912 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

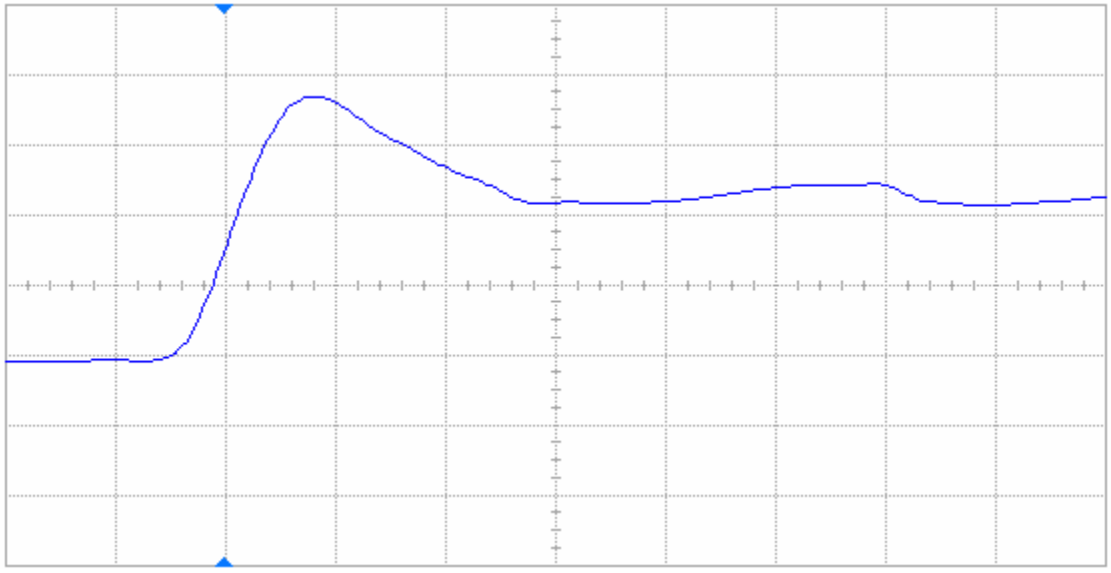


Figure 12(b) DUT 74912 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

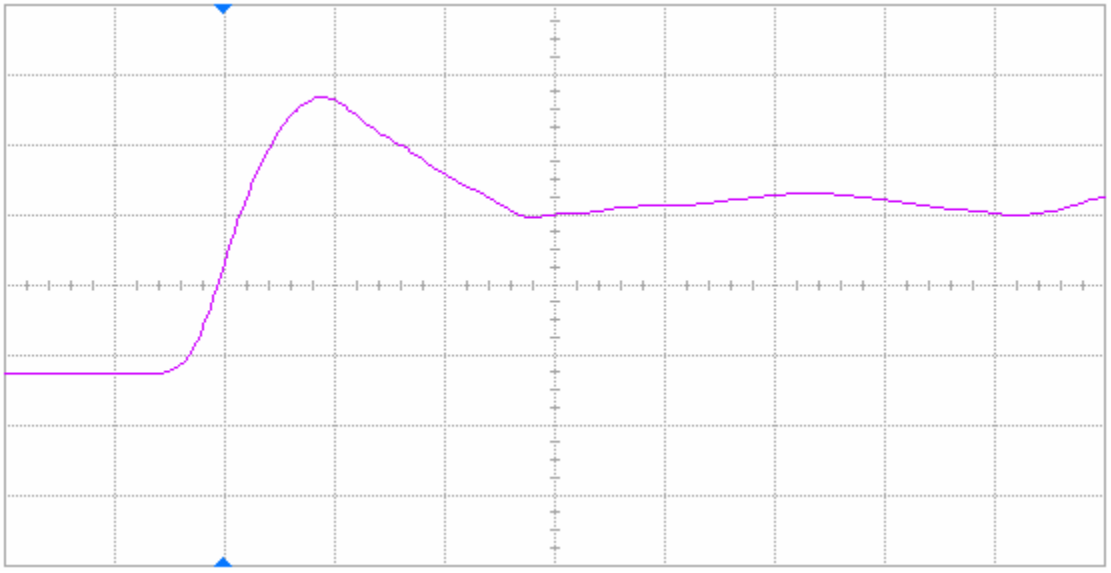


Figure 13(a) DUT 74953 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

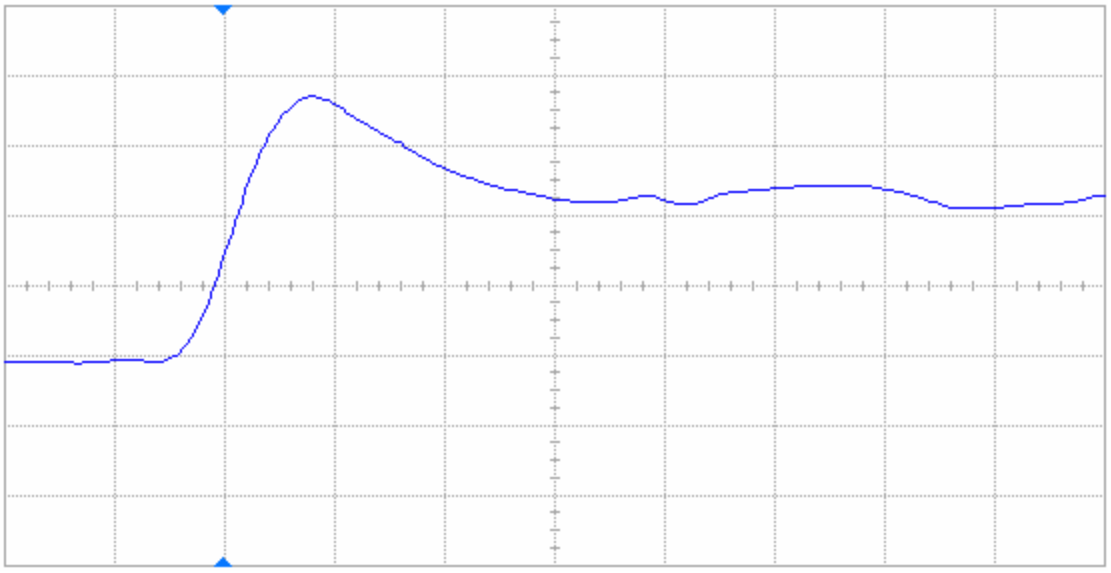


Figure 13(b) DUT 74953 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

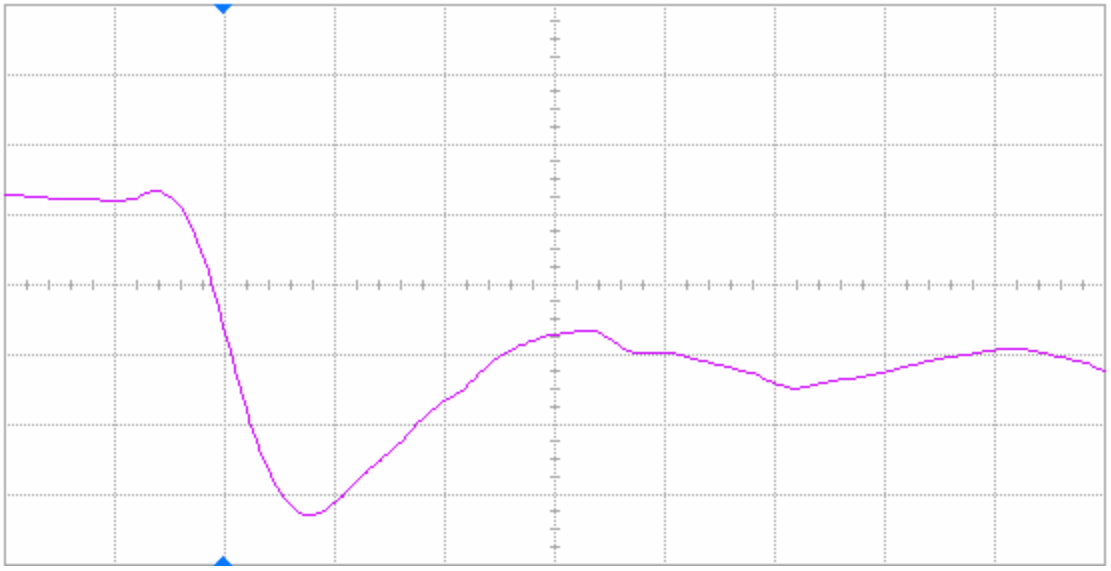


Figure 14(a) DUT 74821 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

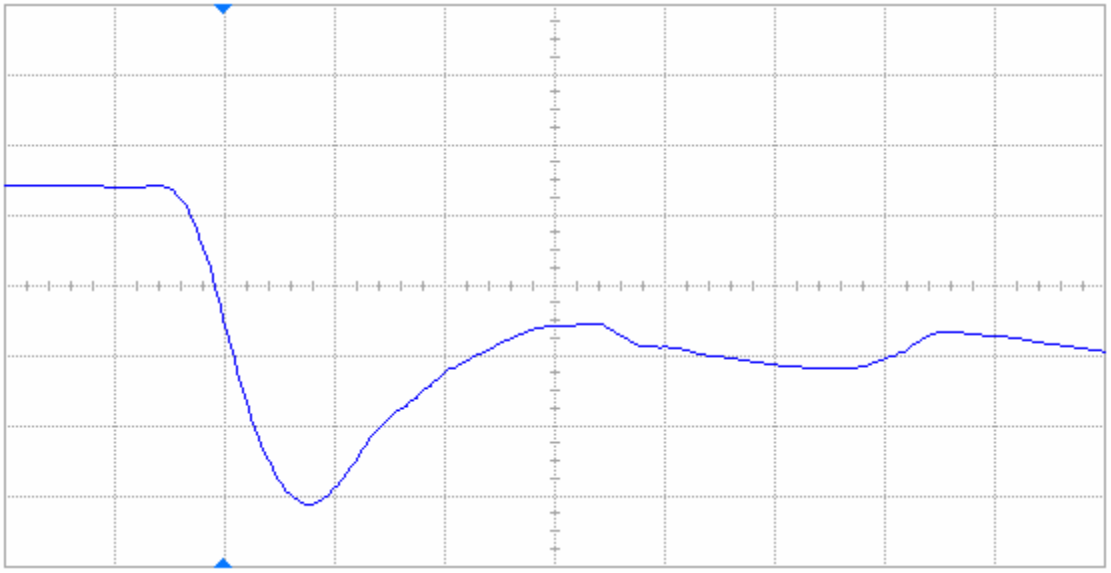


Figure 14(b) DUT 74821 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

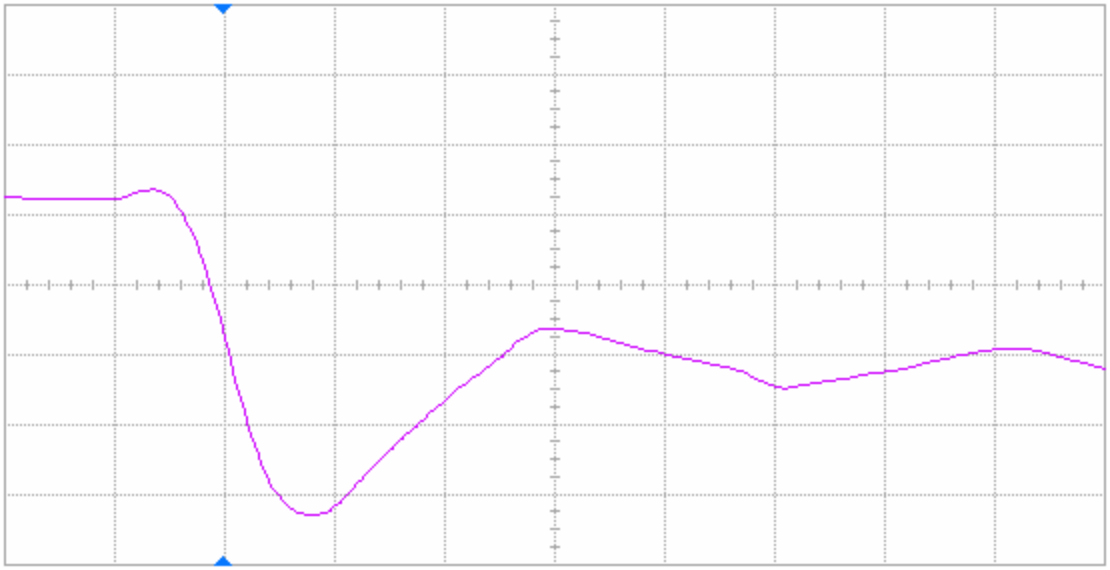


Figure 15(a) DUT 74858 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

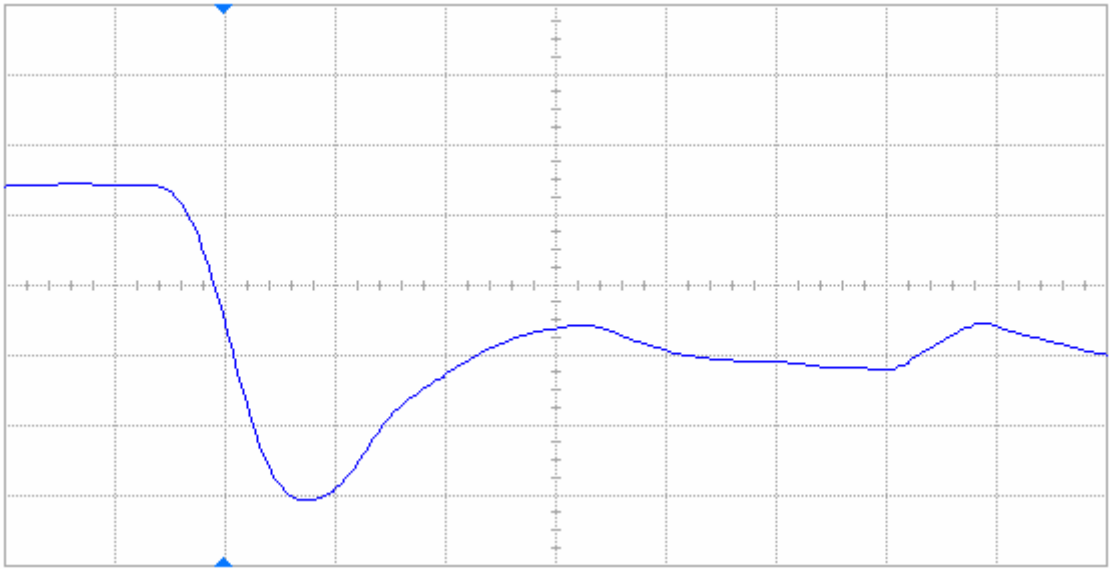


Figure 15(b) DUT 74858 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

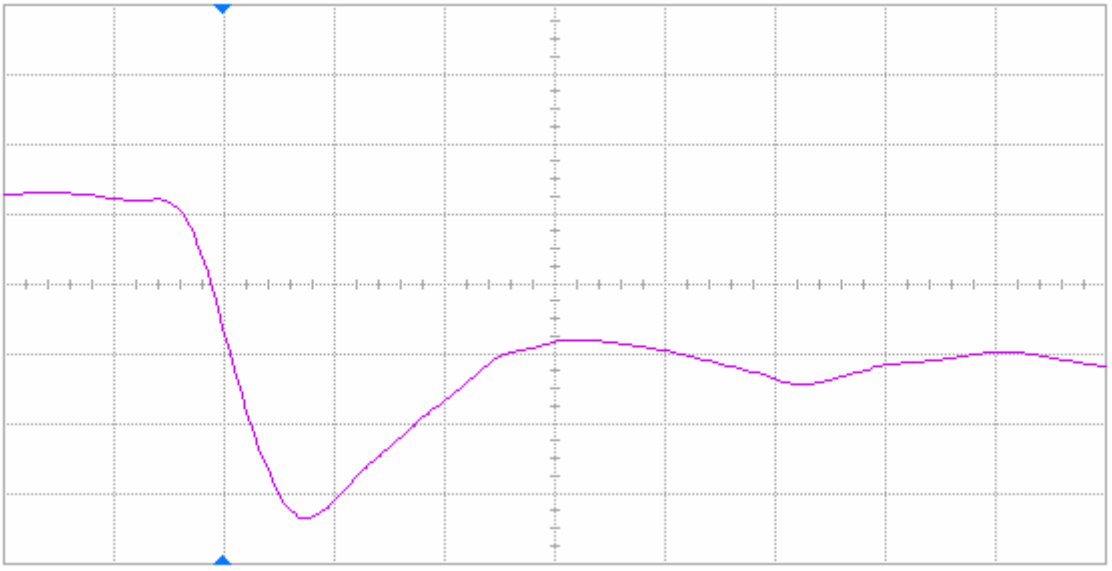


Figure 16(a) DUT 74862 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

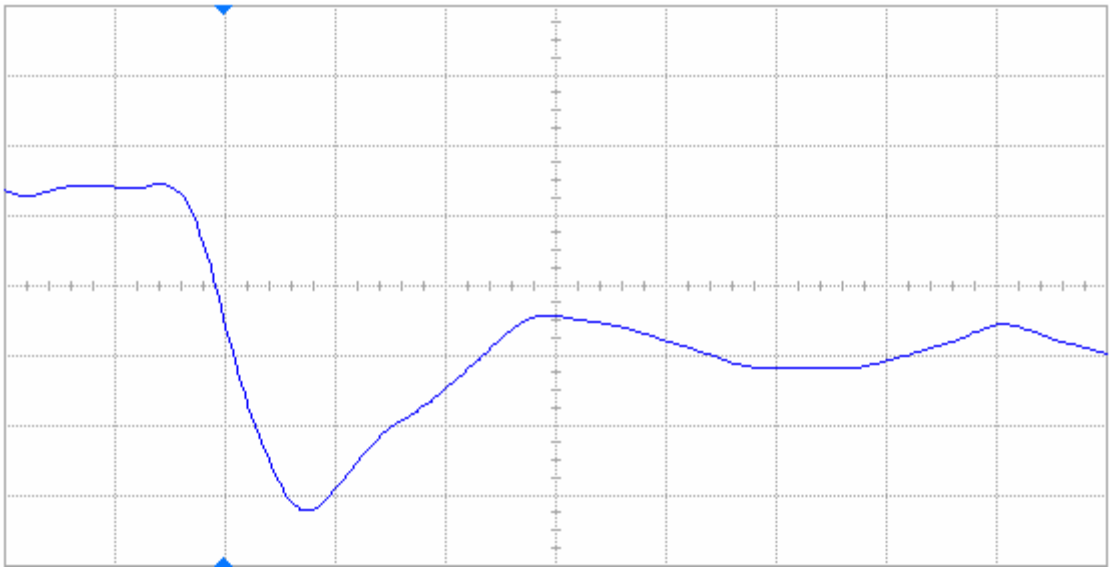


Figure 16(b) DUT 74862 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

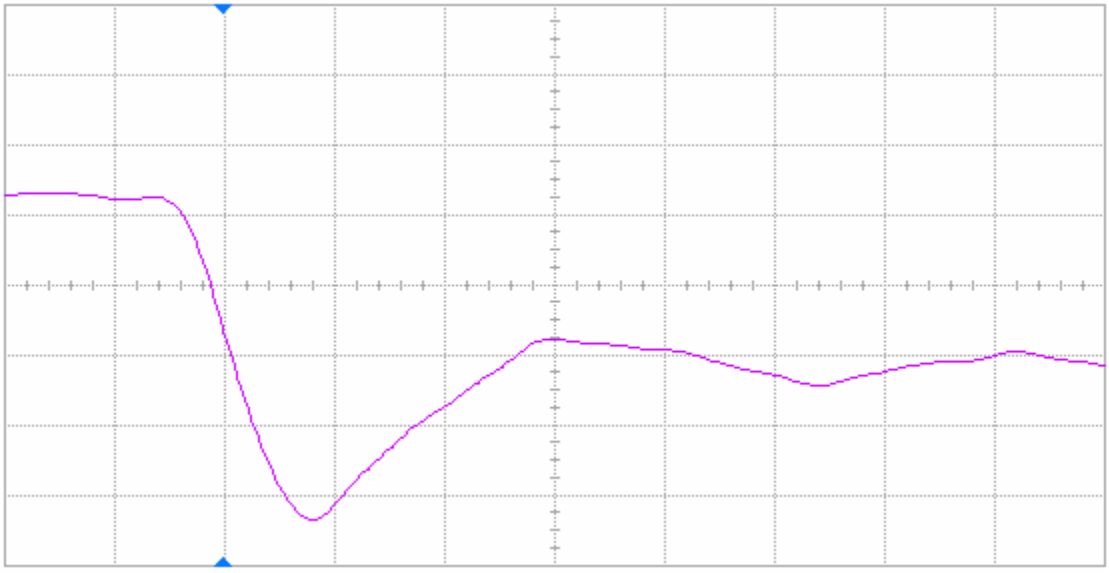


Figure 17(a) DUT 74871 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

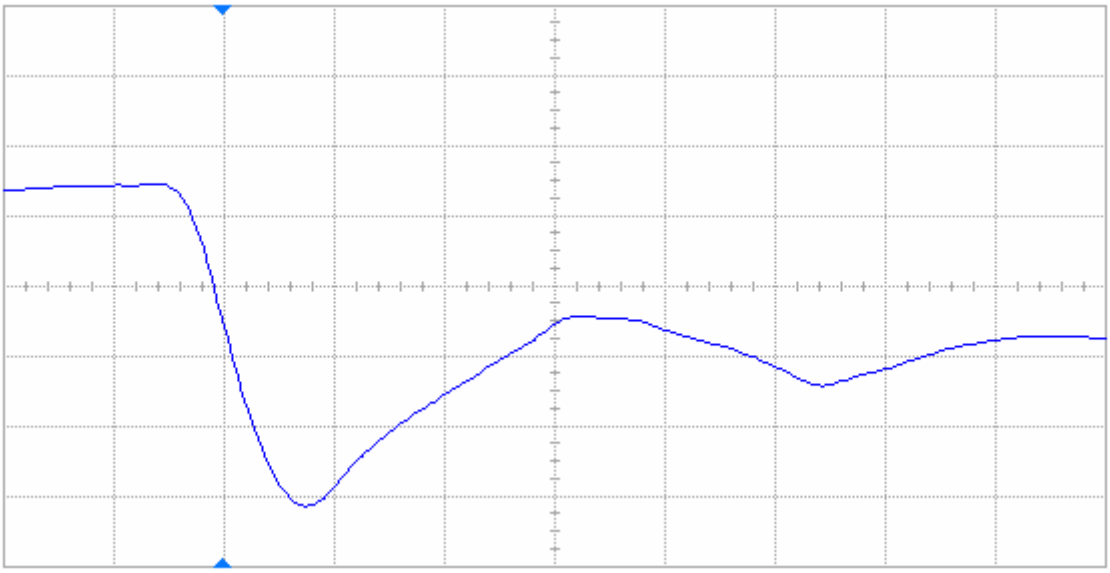


Figure 17(b) DUT 74871 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

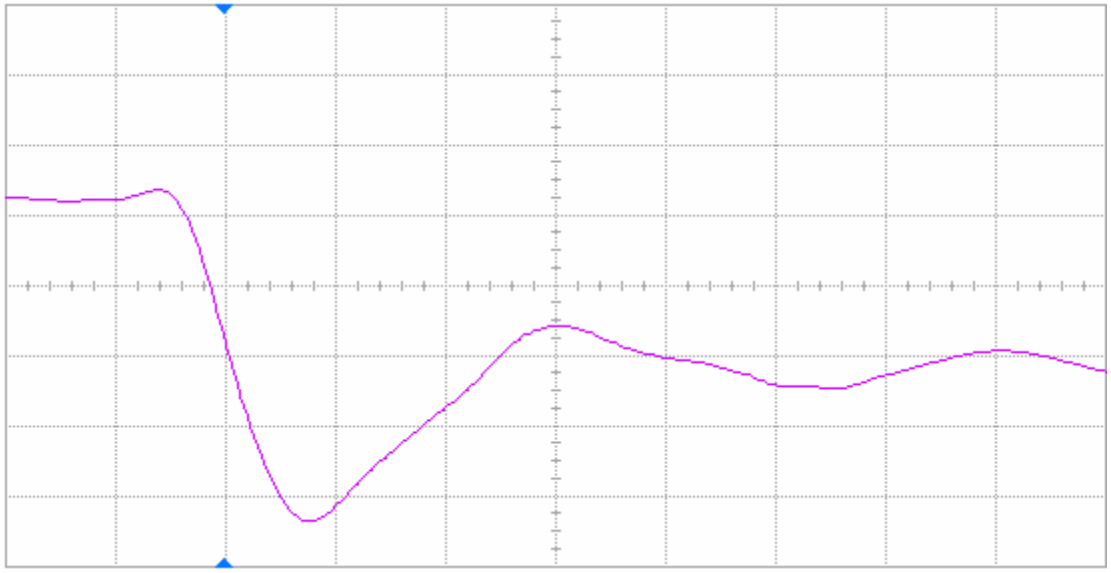


Figure 18(a) DUT 74912 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

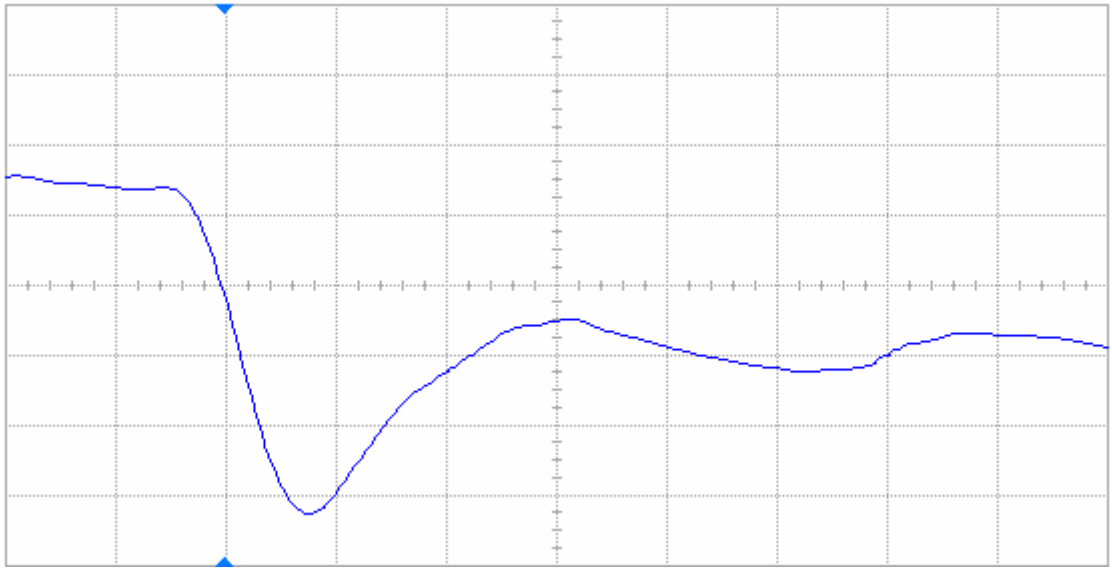


Figure 18(b) DUT 74912 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

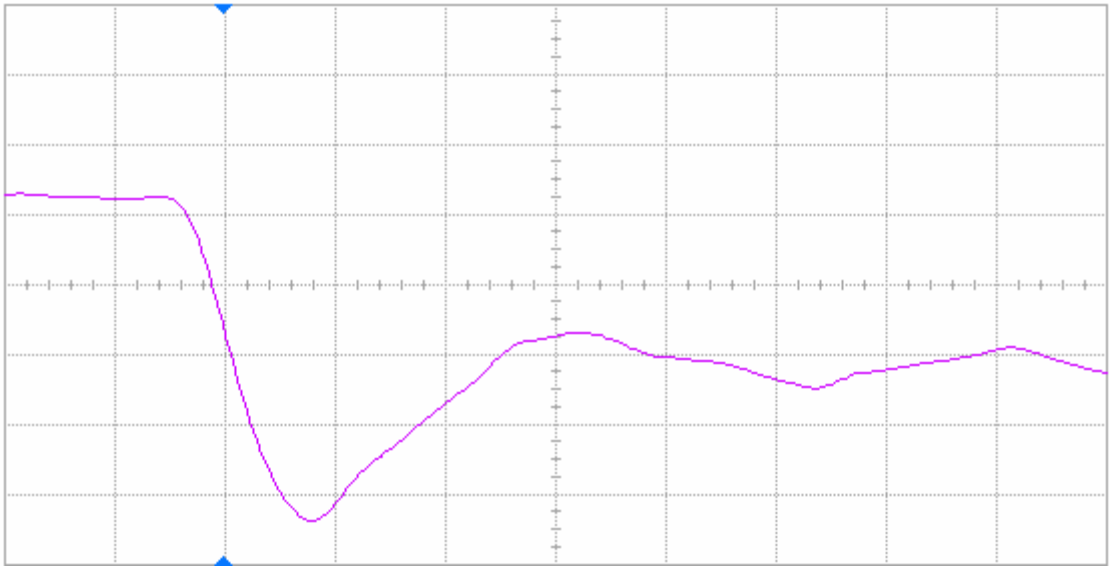


Figure 19(a) DUT 74953 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

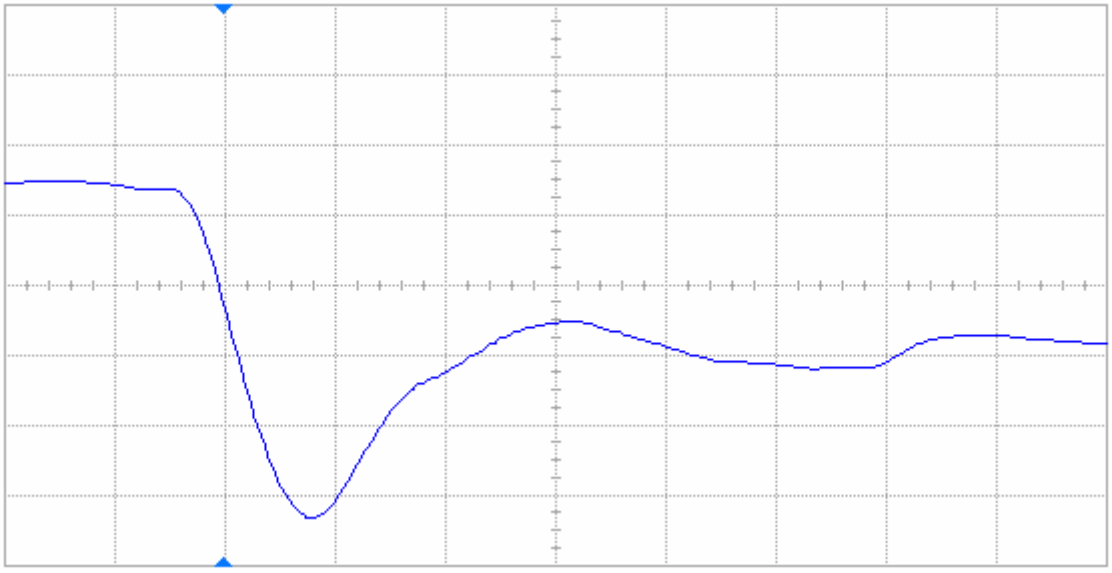
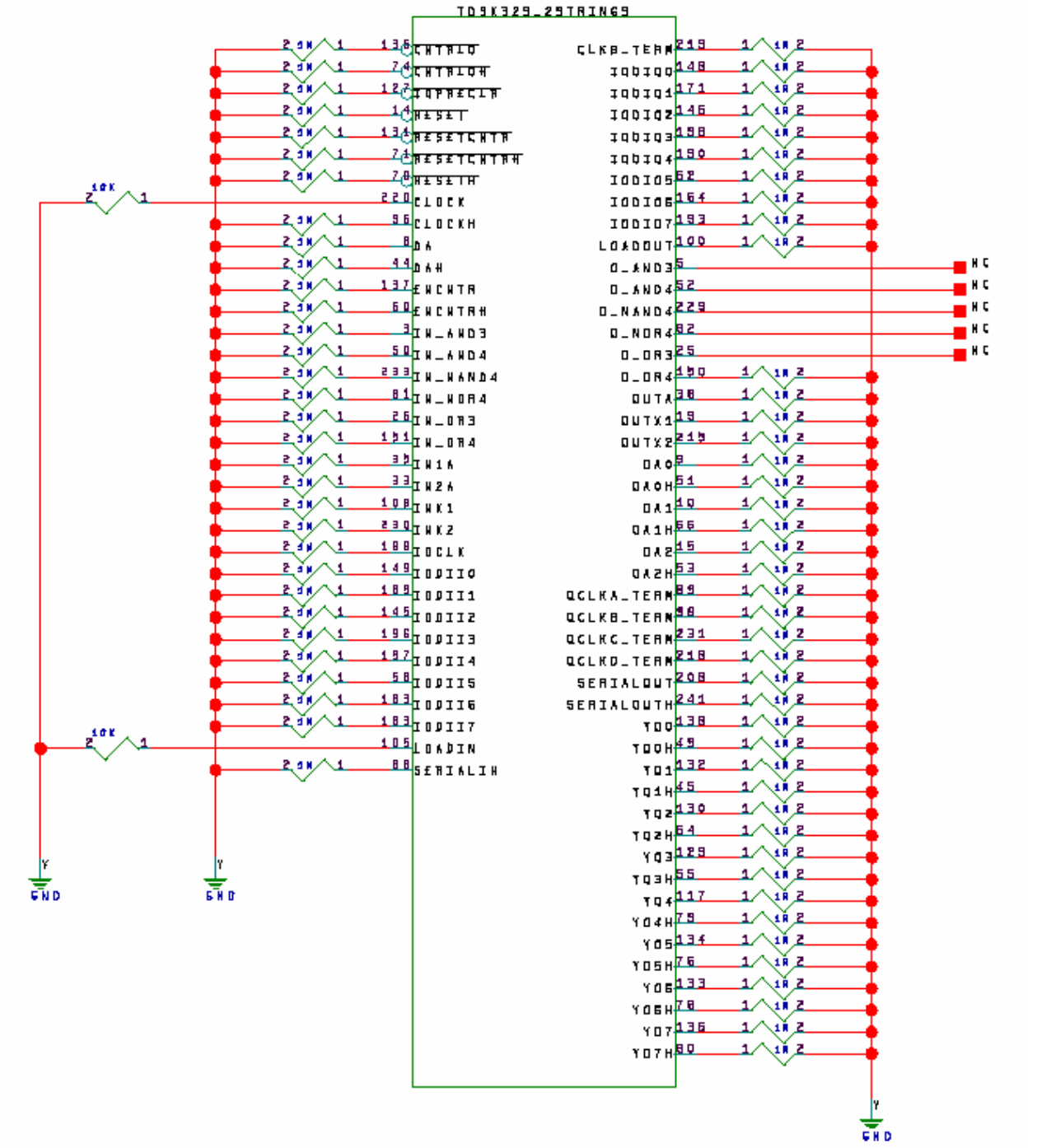
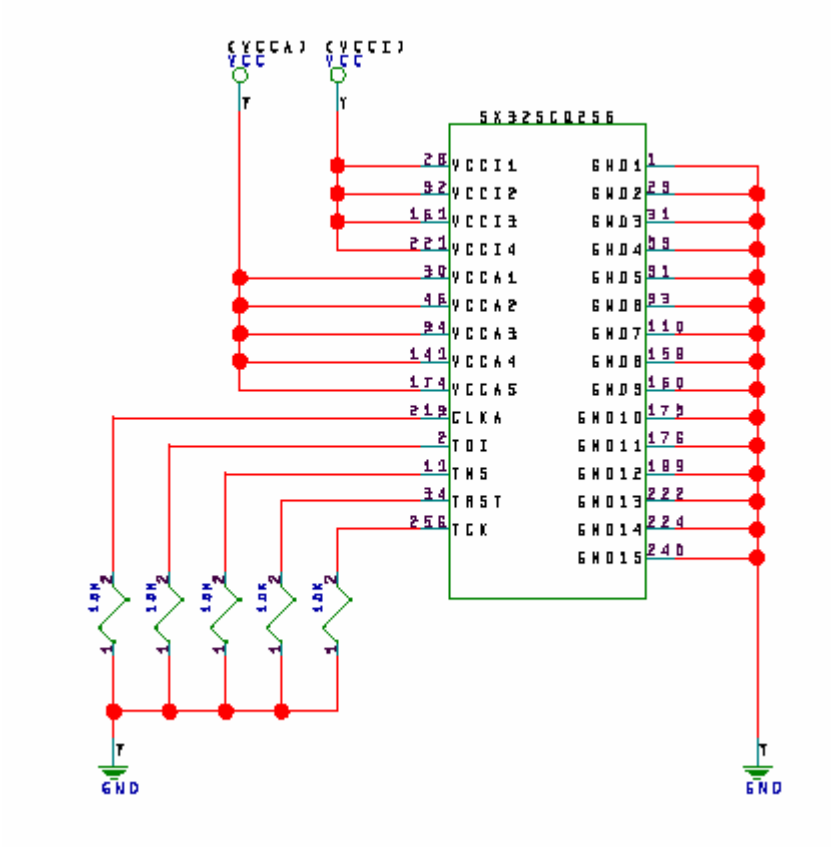


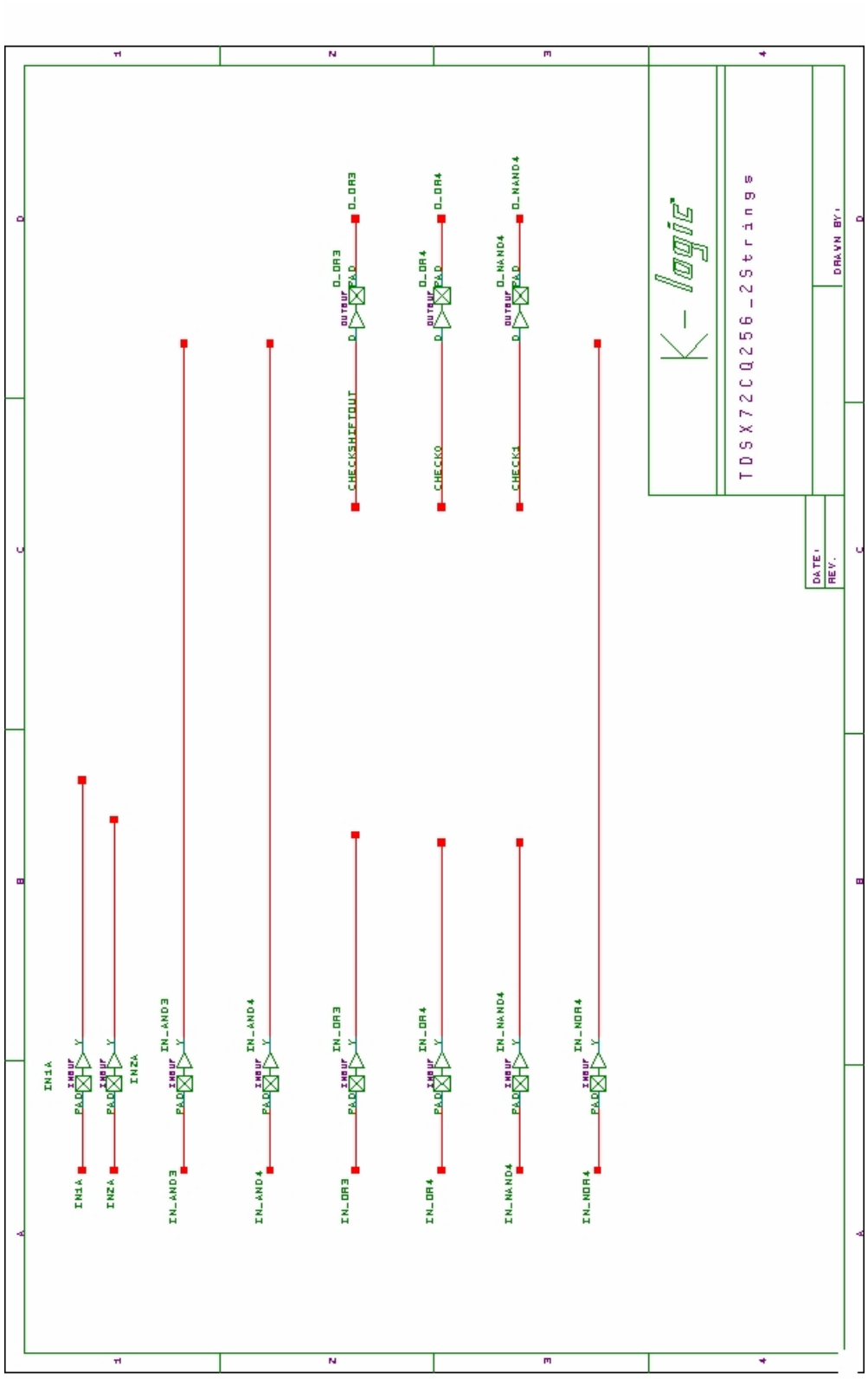
Figure 19(b) DUT 74953 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

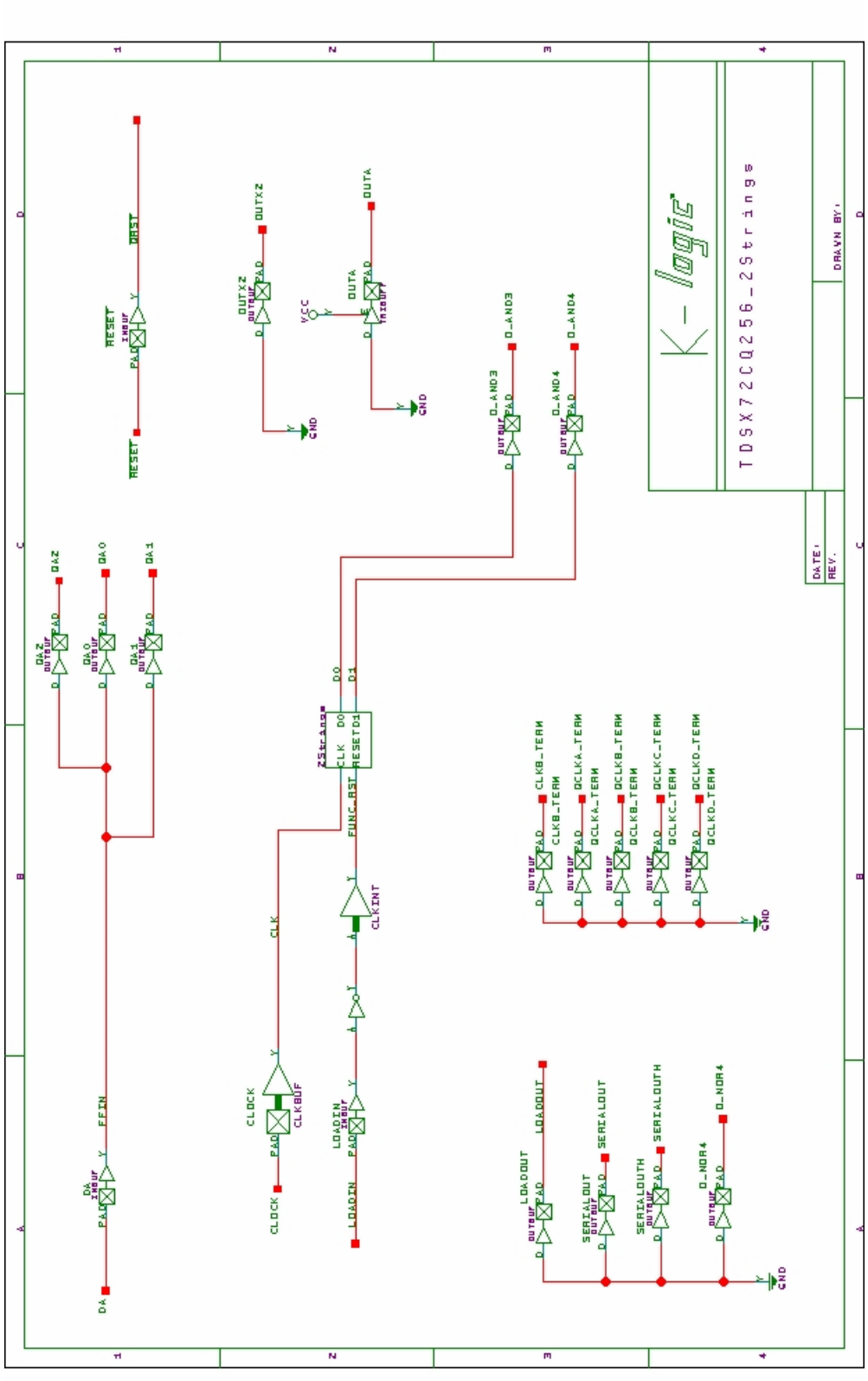
Appendix A DUT Bias

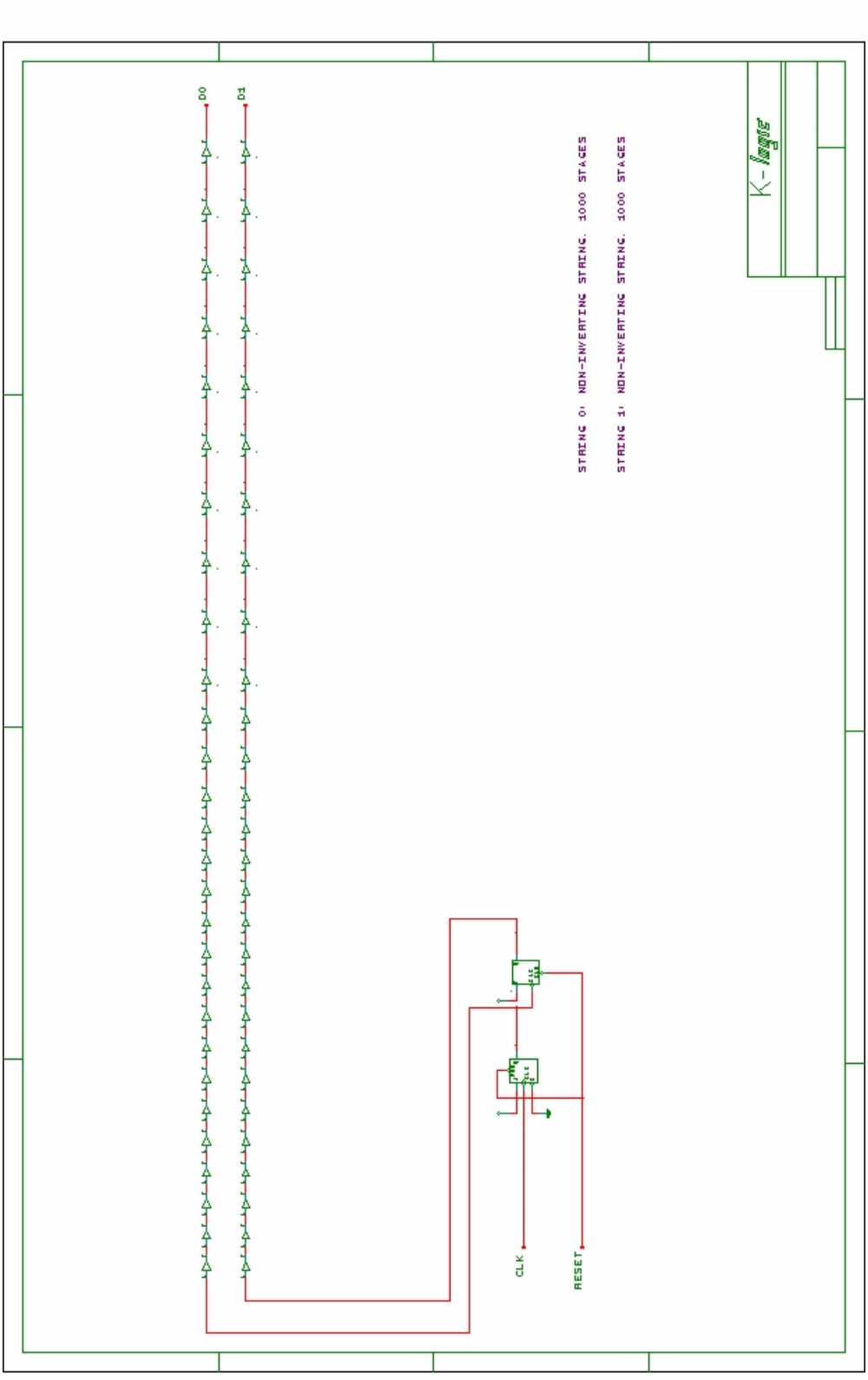



(VCCA)
(VCCI)
VCC
VCC
5X325CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
CLKA
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
10K
10K
10K
10K
10K
GND
GND

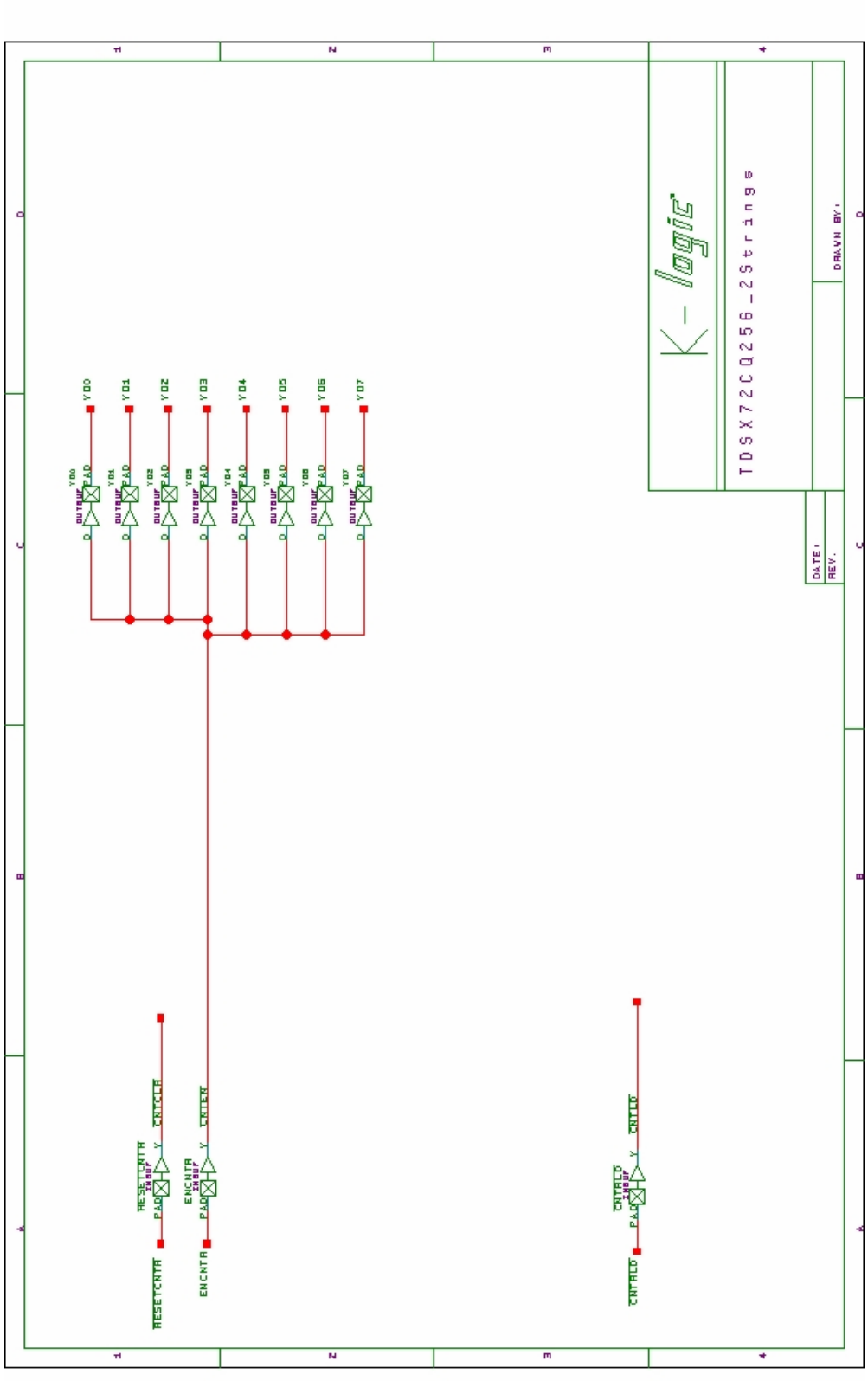
APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

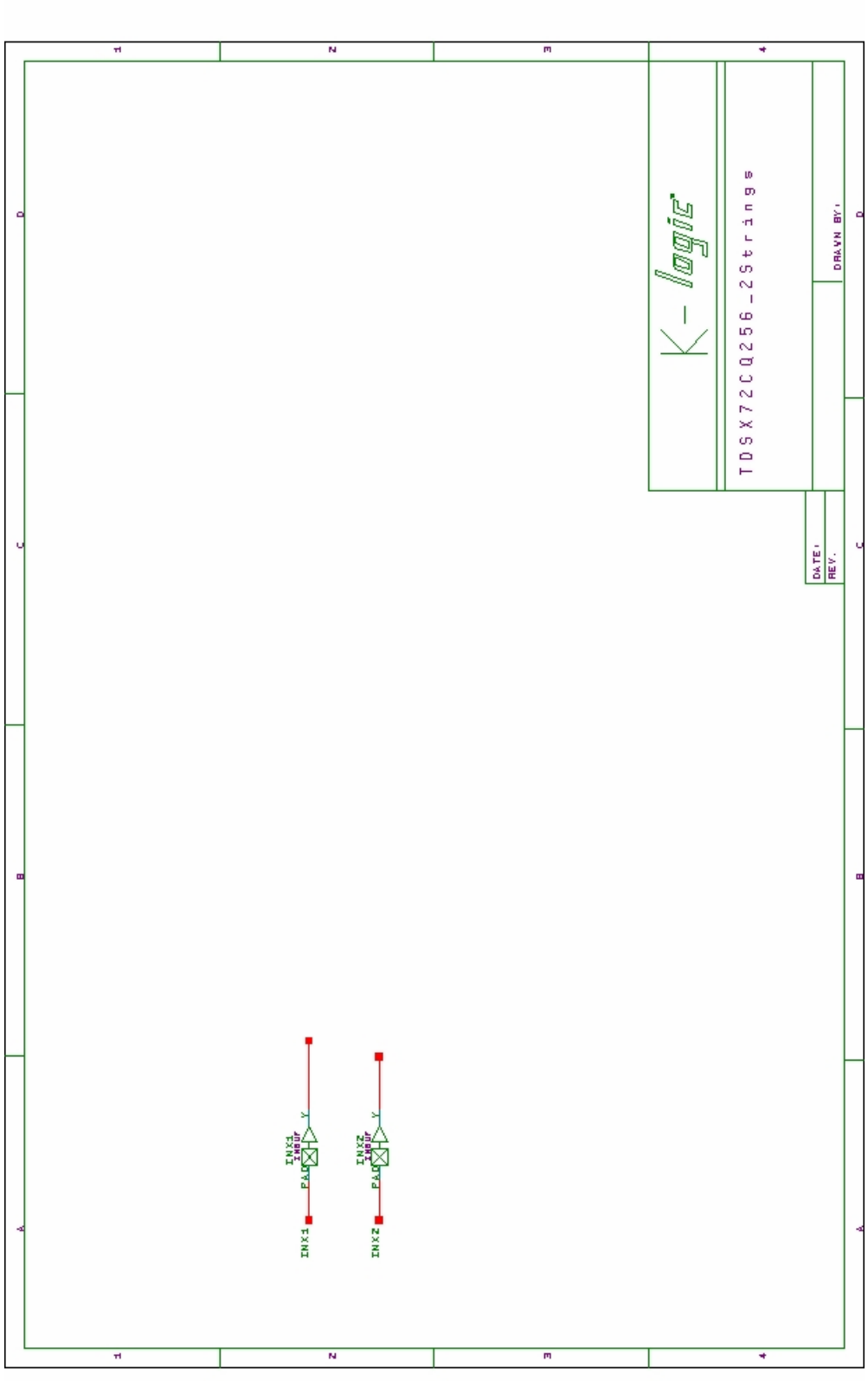


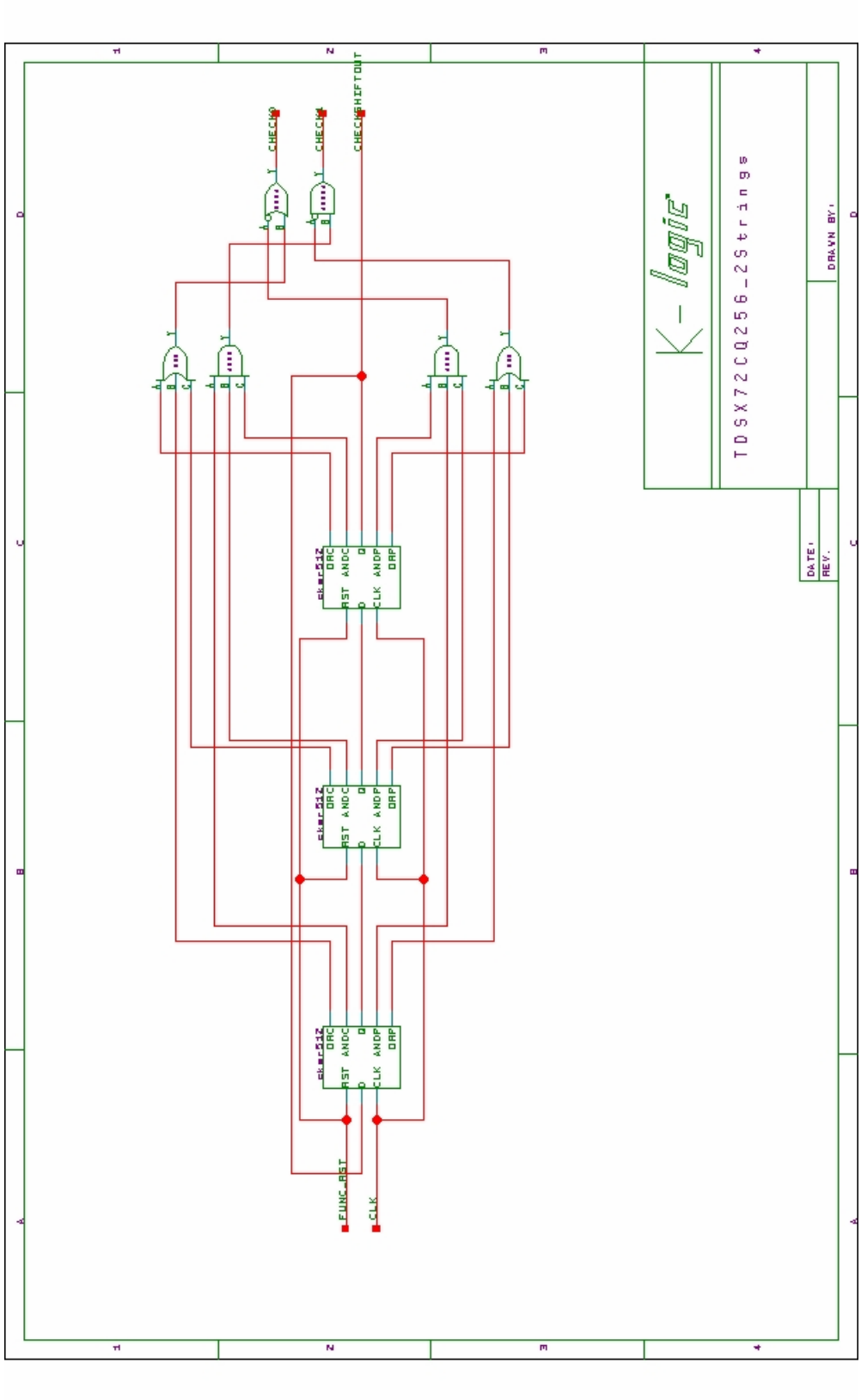

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV:
RESET
DRST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
CLOCK
CLKBUF
CLK
CLKINT
LOADIN
2Strings
CLK
D0
D1
RESET
FUNC_RST
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

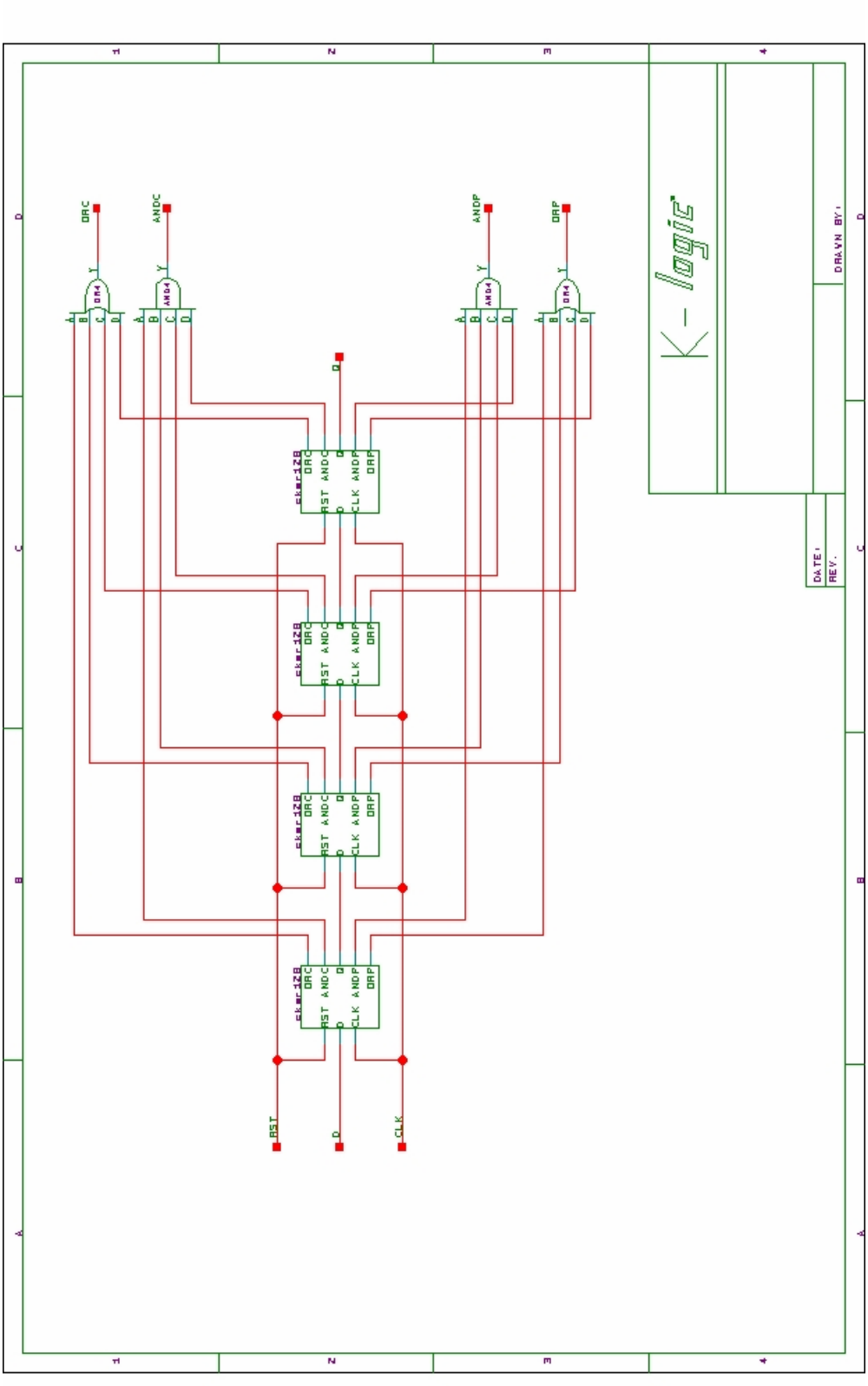

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-labs
CLK
RESET

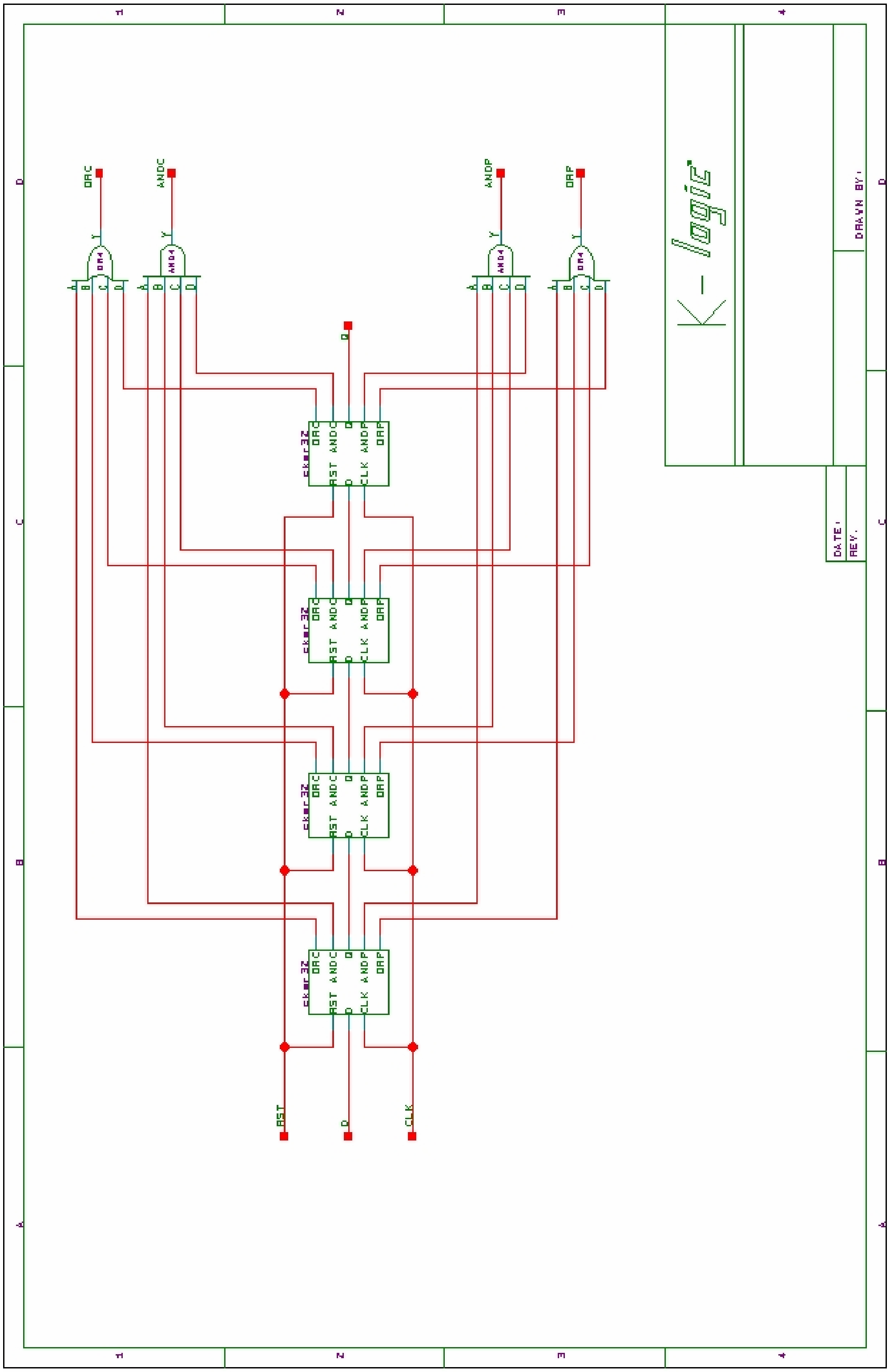

K-logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
YPRESERVE

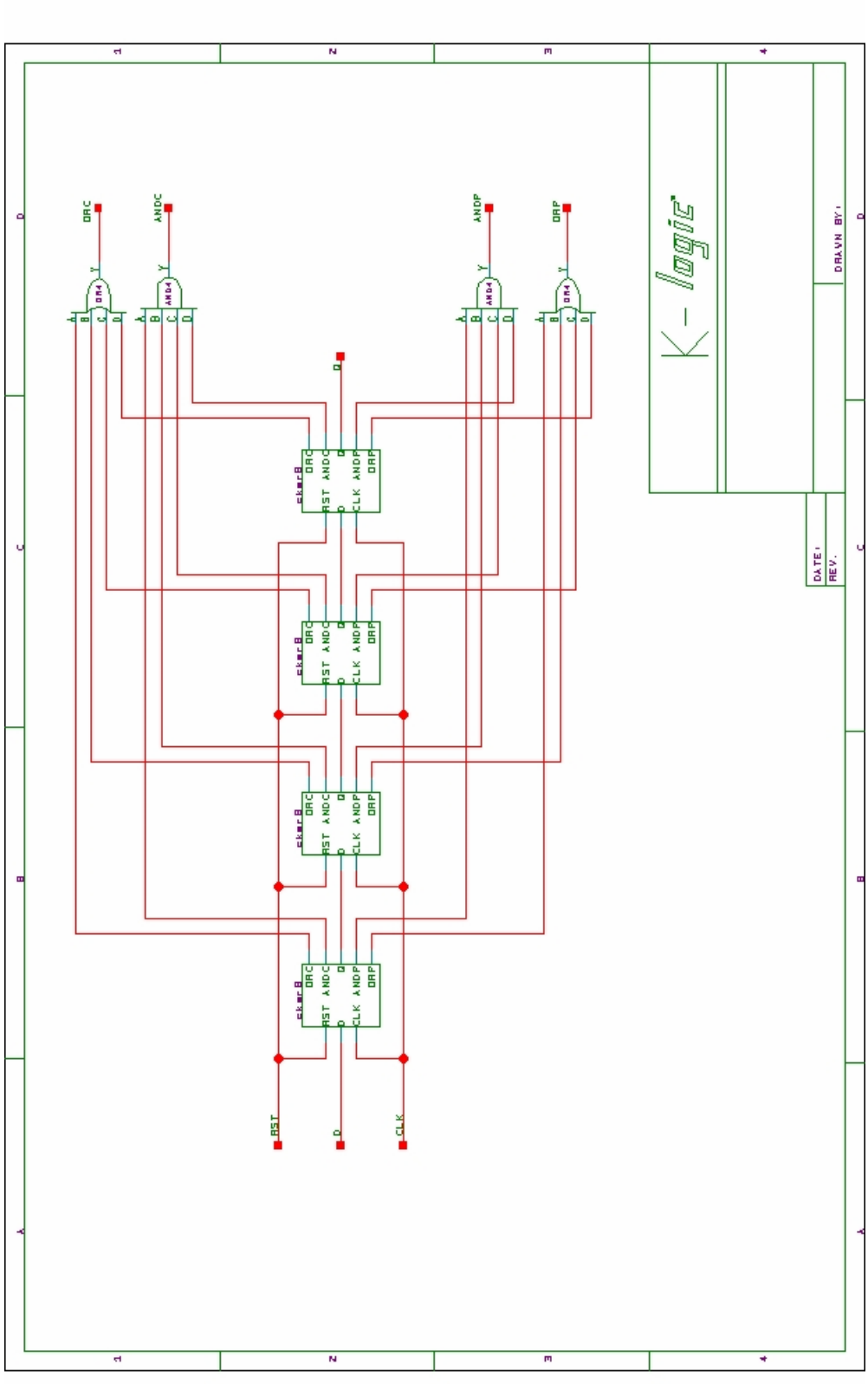

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTCLR
CNTEN
CNTLOD
INBUF

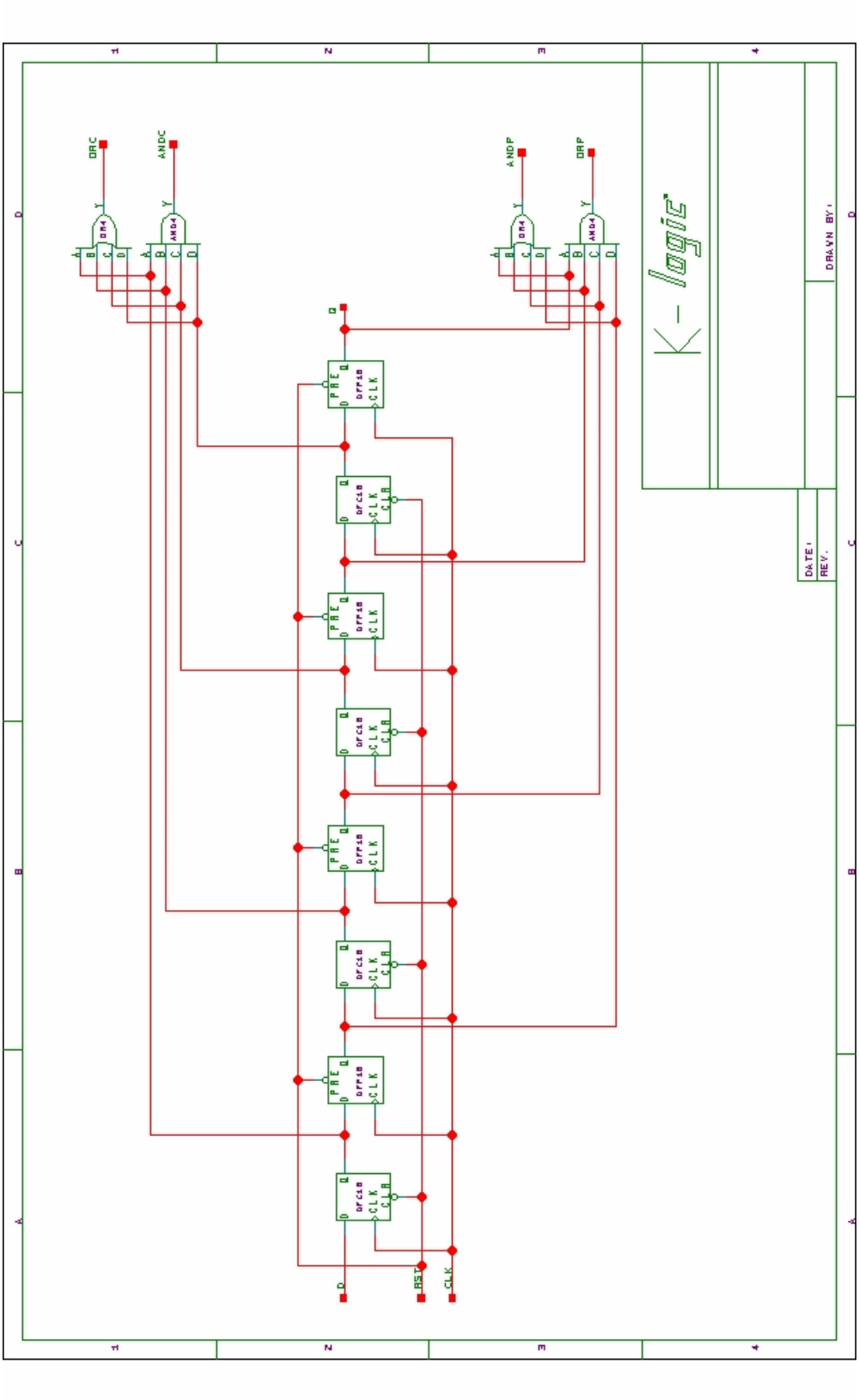

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

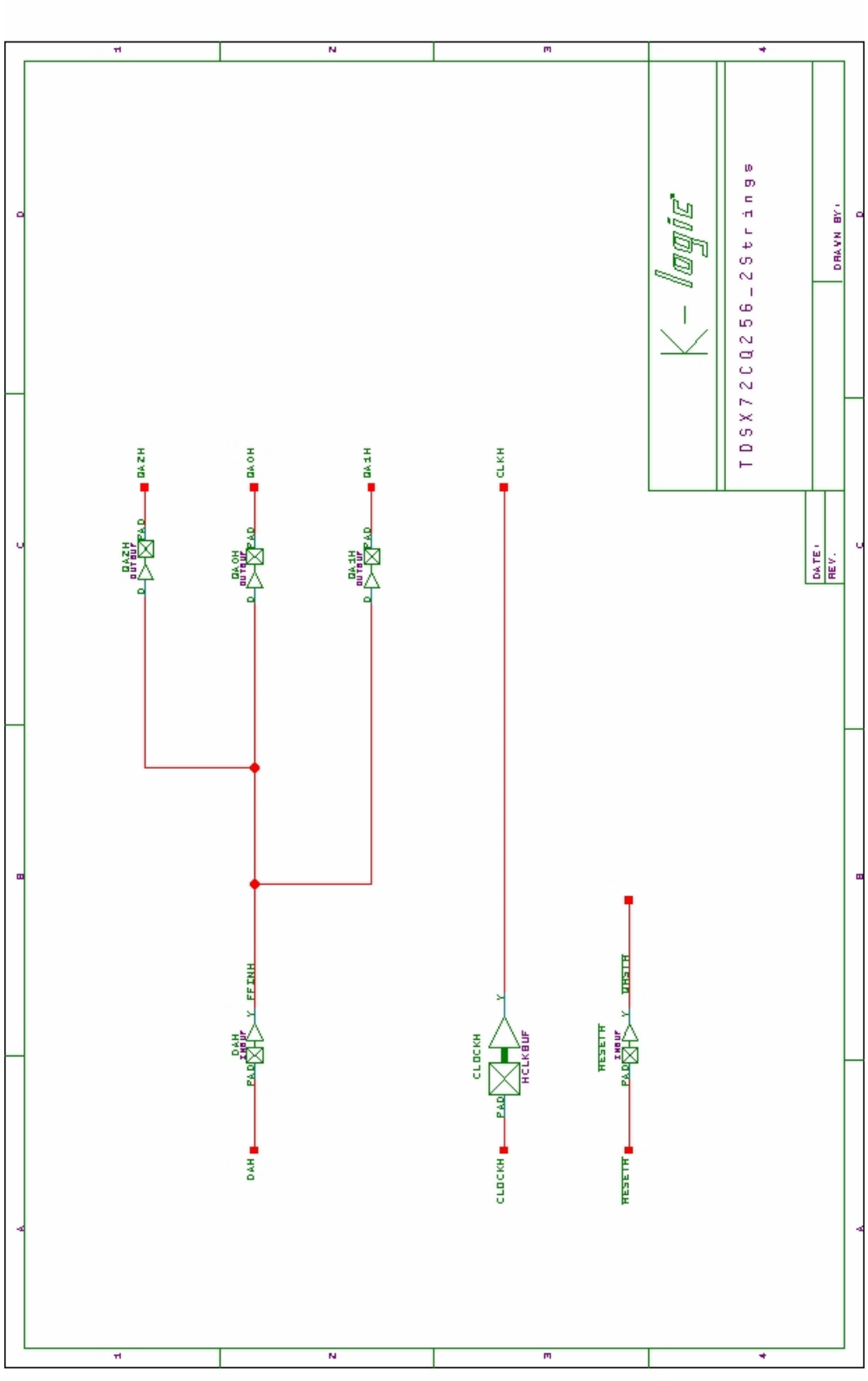

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECKSHIFTOUT
CHECK0
CHECK1
FUNC_RST
CLK

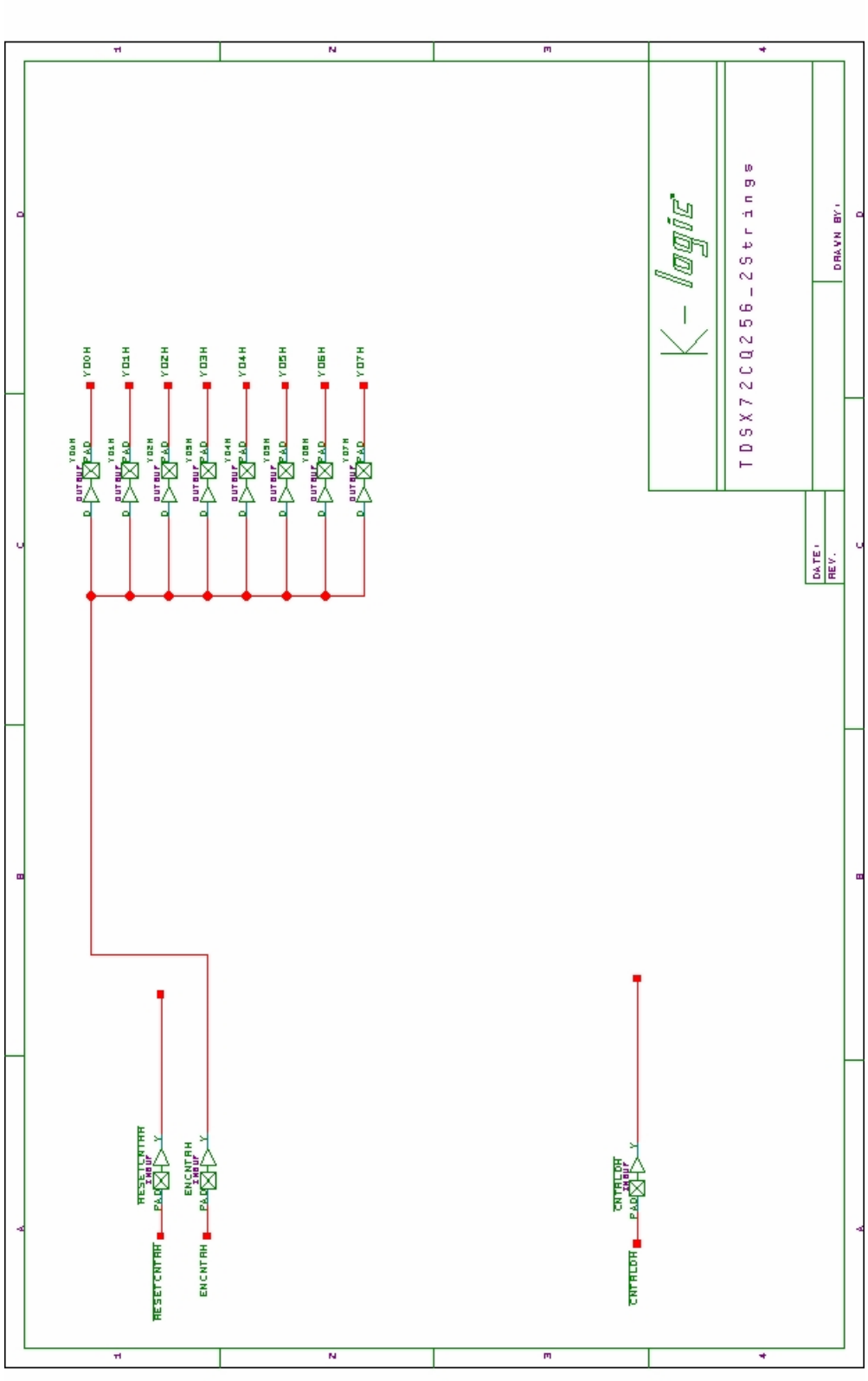

DRC
ANDC
ANDP
DRP
AND4
Y
A
B
C
D
Q
clkrst28
DRC
ANDC
ANDP
DRP
RST
CLK
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

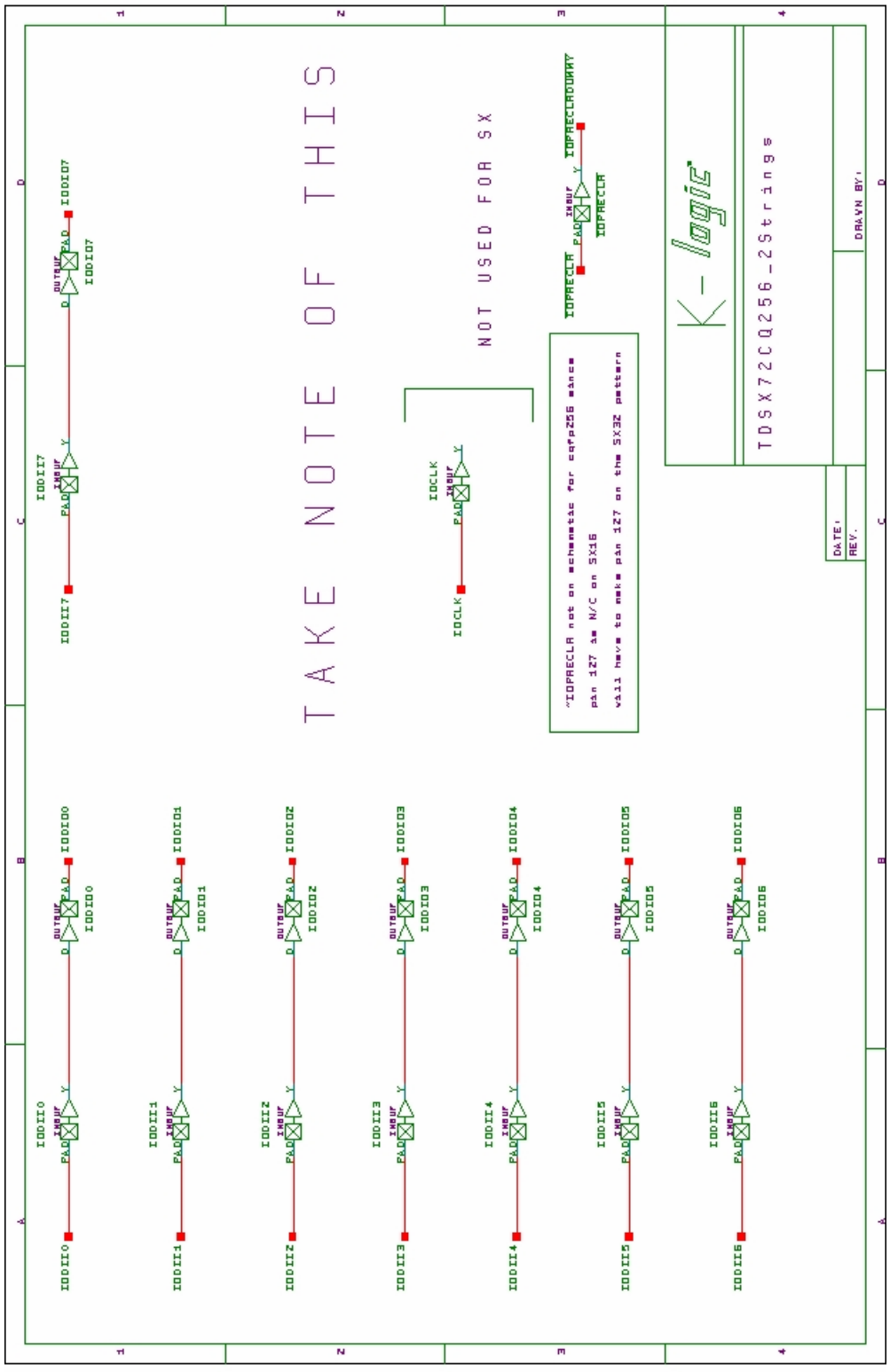

ORC
ANDC
ANDP
ORP
Q
ckmr32
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

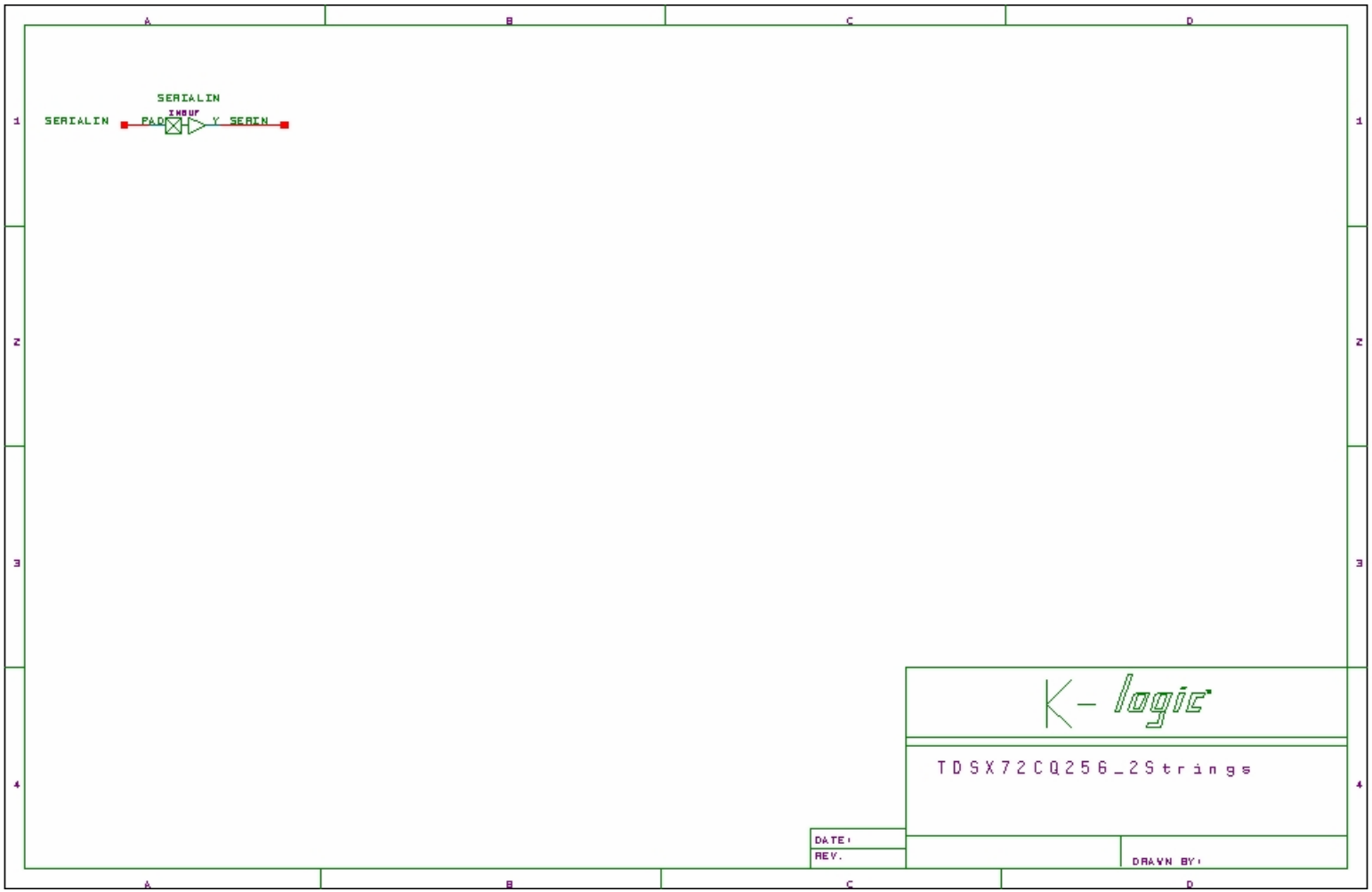

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDP
DRP
AND4
Y
A
B
C
D
Q
Ckmr8
DRC
ANDC
ANDP
DRP
RST
CLK
D
RST
D
CLK

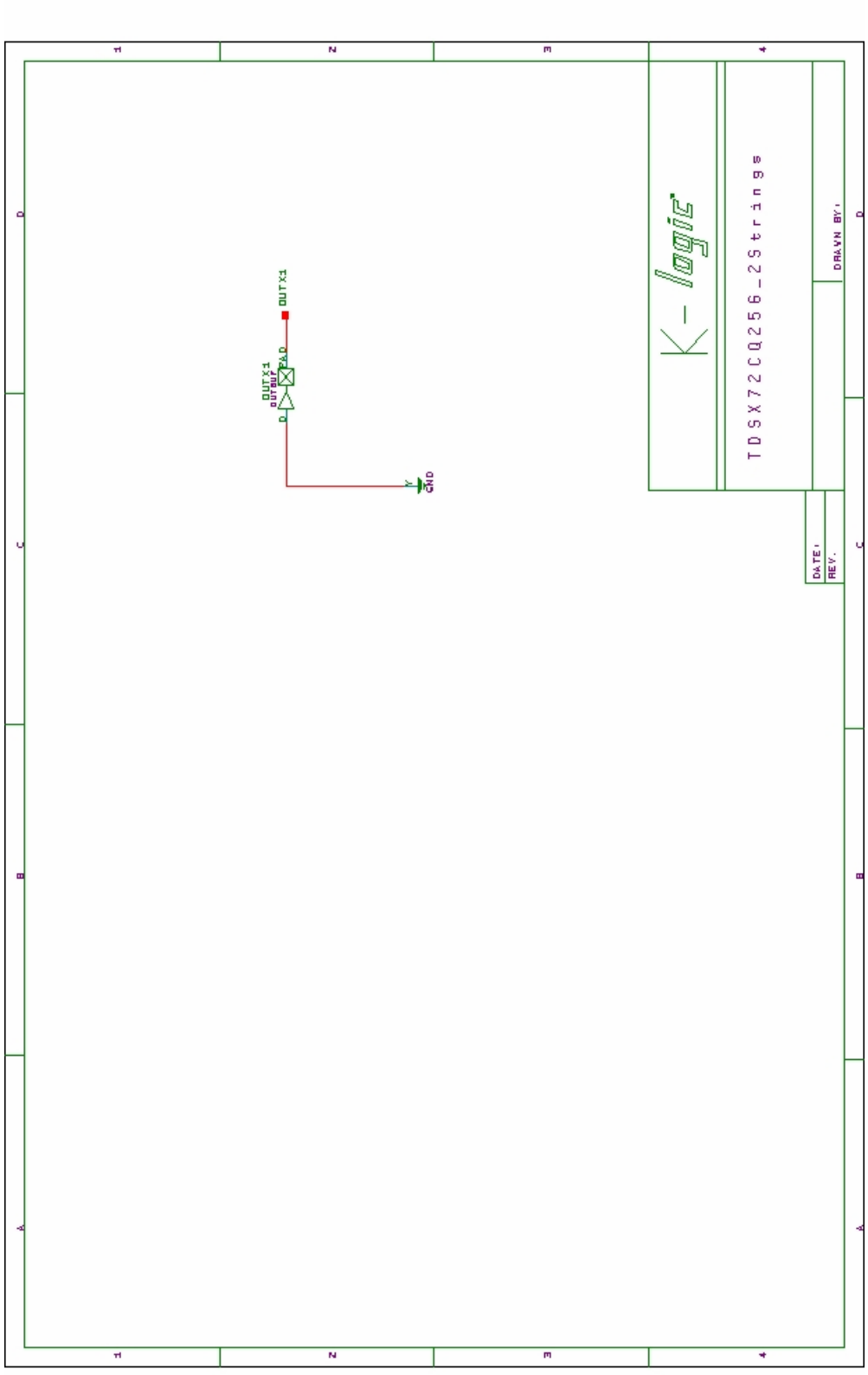

K- logic
DRAWN BY:
DATE:
REV.
ORC
ANDC
ANDF
ORF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH IMUX
Y FFINH
DAH
CLOCKH
Y
HCLKBUF
RESETH
RESETH IMUX
Y WRSTH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
RESETCNTAR
ENCNTAH
CNTALOH
IBUF


TAKE NOTE OF THIS
NOT USED FOR SX
IOPRECLR
IOPRECLR
IOPRECLRDUMMY
IOCLK
IOCLK
IOOII7
IOOII7
IOOID7
IOOID7
IOOII0
IOOII0
IOOID0
IOOID0
IOOII1
IOOII1
IOOID1
IOOID1
IOOII2
IOOII2
IOOID2
IOOID2
IOOII3
IOOII3
IOOID3
IOOID3
IOOII4
IOOII4
IOOID4
IOOID4
IOOII5
IOOII5
IOOID5
IOOID5
IOOII6
IOOII6
IOOID6
IOOID6
*IOPRECLR not on schematic for csfp256 mance
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
K-logic
TDSX72CQ256-2Strings
DATE:
REV:
DRAWN BY:


SERIALIN
SERIALIN
IBUF
PAD
Y
SERIN
A
B
C
D
1
2
3
4
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


OUTX1
OUTX1
PAD
OUTX1
OUTPUT
O
GND
K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV: