



TOTAL IONIZING DOSE TEST REPORT

No. 02T-RT54SX72S-T25KS005

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	> 113 krad(Si), full limit TBD
2. I _{DDSTDBY} (static I _{CC})	Reached 25 mA spec at ~51 krad(Si) worst case, 60 krad(Si) typical case, ~100 mA at 100 krad(Si)
3. Input Threshold (V _T)	Passed 100 krad(Si)
4. Output Drives (V _{OL} /V _{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 100 krad(Si)
6. Transition Time	Passed 100 krad(Si)
7. Power-up Transient	Passed 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT Information and Irradiation Conditions

Part Number	RT54SX72S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 μ m CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	T25KS005
Quantity Tested	4
Serial Number	LAN6501, LAN6502, LAN6503, LAN6504
Radiation Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	1 krad(Si)/hr ($\pm 10\%$)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V _{CC1} /V _{CCA})	5.0 V/2.5 V

B. Test Method

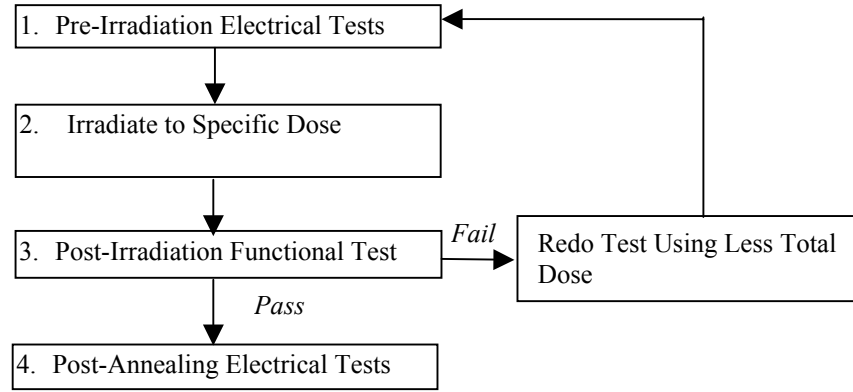


Fig 1 Parametric test flow chart

There are two types of radiation test regularly performed by Actel. For “functional test”, the DUT is irradiated to the total dose level at which the gross functional failure occurs. This total dose level is determined as the tolerance for functional failure (the first data row in the summary table). The task of testing AC/DC parameters is called “parametric test.” It follows the military standard test method 1019.5. Fig 1 shows the testing flow. In a previous product (RT54SX32S) manufactured by the same 0.25 μm CMOS process, the time dependent effect (TDE) was evaluated by comparing the results between a high dose rate (1 krad(Si)/min) and a low dose rate (1 krad(Si)/hr) exposure. No adverse TDE was observed. Consequently, the accelerated aging (rebound test) is omitted in this report.

C. Electrical Parameter Measurements

1) Type 1 Functional Test

All the parameters are measured in-flux. The parameters usually include I_{CC} , output voltage of combinatorial circuits and sequential circuits, and the propagation delay of an inverter string.

2) Type 2 Parametric Test

A high utilization design (in this report, TDSX72CQ256_2Strings) to address radiation effects is used. The circuit schematics are shown in appendix A.

Table 2 lists the electrical parameters measured in the parametric test. The functionality is measured pre and post-irradiation, and also in-flux monitored on the output pin (O_AND3 or O_AND4) of the two global combinatorial inverter-strings and on the output pin (O_OR3, O_OR4 and O_NAND4) of the global shift register. The I_{CC} is measured in-flux, statically on the power supply of the array (I_{CCA}) and I/O (I_{CCI}) respectively. The sampling rate is every 5 or 10 minutes. The input logic threshold (V_T) and output drives (V_{OH}/V_{OL}) are measured pre and post-irradiation on a combinatorial net, the input pin DA to the output pin QA0. The propagation delay is measured pre and post-irradiation and also in-flux on one of the global combinatorial inverter string with 1000 inverters, input pin LOADIN to output pin O_AND4. The transient time is measured pre and post-irradiation on the same design. The global combinatorial inverter strings are controlled by clocked D flip-flops during the propagation delay and transient measurements. Power up transient test measures the I_{CCA} when the V_{CCA} is ramping with V_{CCI} powered (5.0 V in this case).

During irradiation, unused inputs are grounded with a 10,000 ohm resistor.

Table 2. Logic Design for Parametric Test

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC}	DUT power supply
3. Input Threshold (V_T)	TTL compatible input buffer (pin DA to QA0)
4. Output Drives (V_{OH}/V_{OL})	TTL compatible output buffer (pin QA0)
5. Propagation Delays	String of 1000 inverters (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)
7. Power-up Transient	DUT power supply

III. TEST RESULTS

A. Type-1 Functional Test

Functional test to failure was not performed in this report.

B. Type-2 Parametric Test

1) Functionality

Fig 2, 3, 4 and 5 show the in-flux output of a combinatorial net for each DUT respectively. In each case, the degradation after irradiation is negligible. The pre and post-irradiation functional tests on both combinatorial and sequential nets also show no detectable radiation degradation of V_{OUT_HIGH} and V_{OT_LOW} on each DUT.

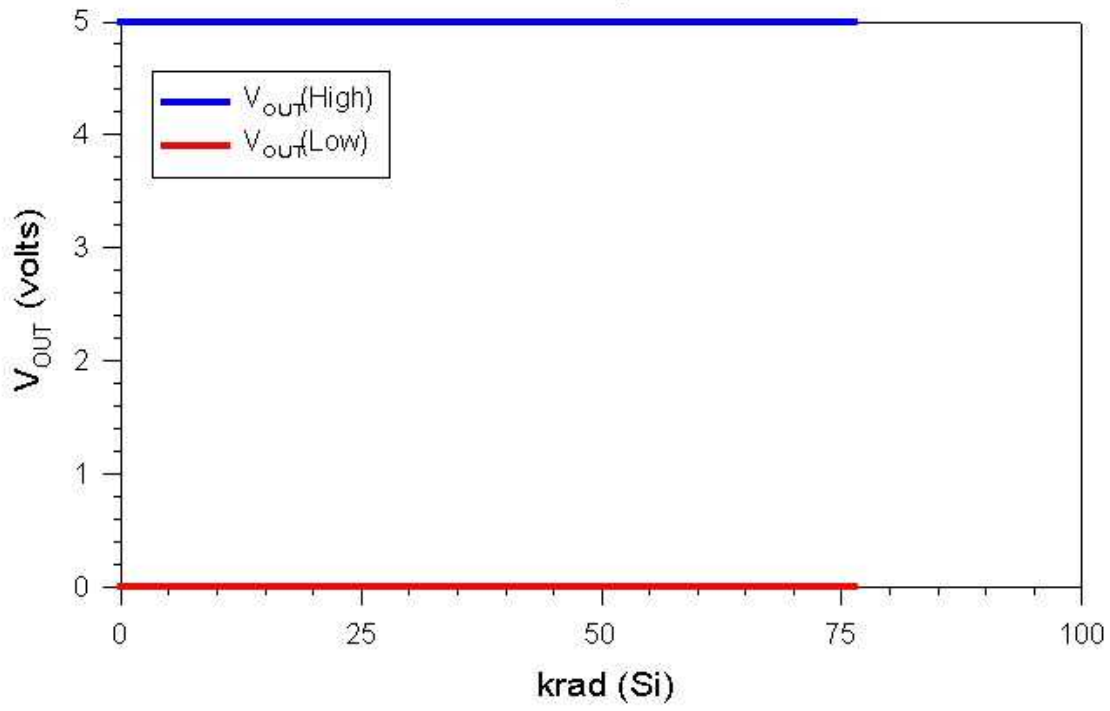


Fig 2 In-flux V_{OUT} of the functionality test circuit in LAN6501

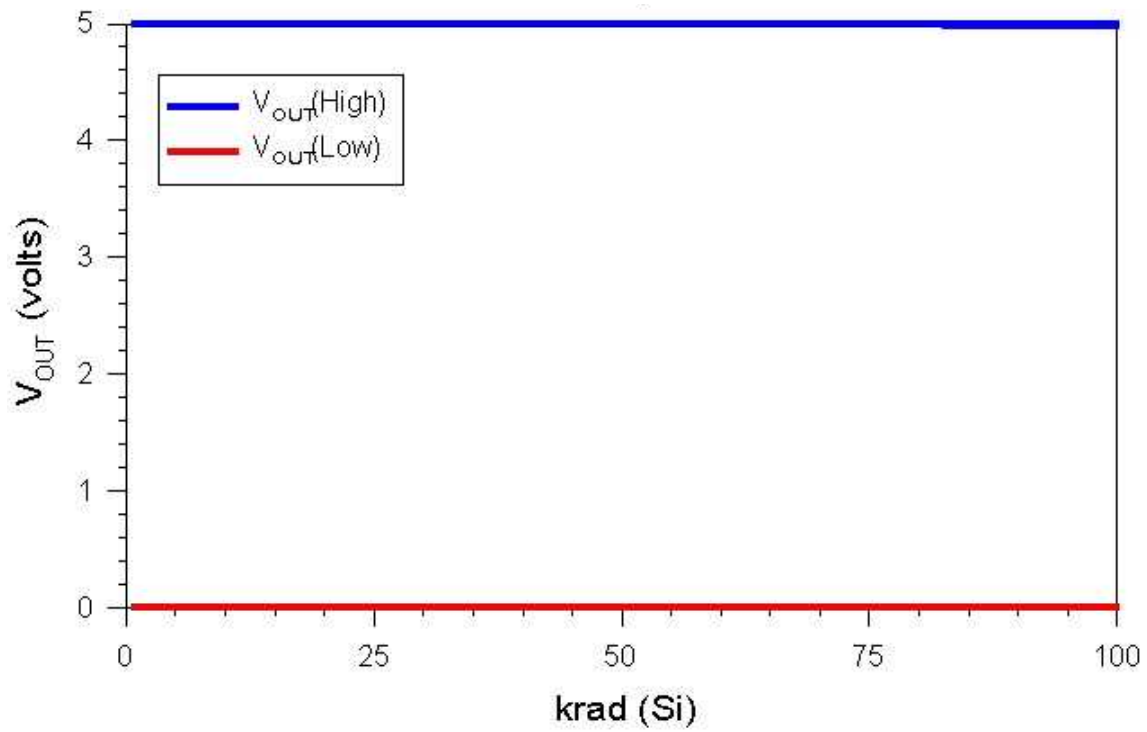


Fig 3 In-flux V_{OUT} of the functionality test circuit in LAN6502

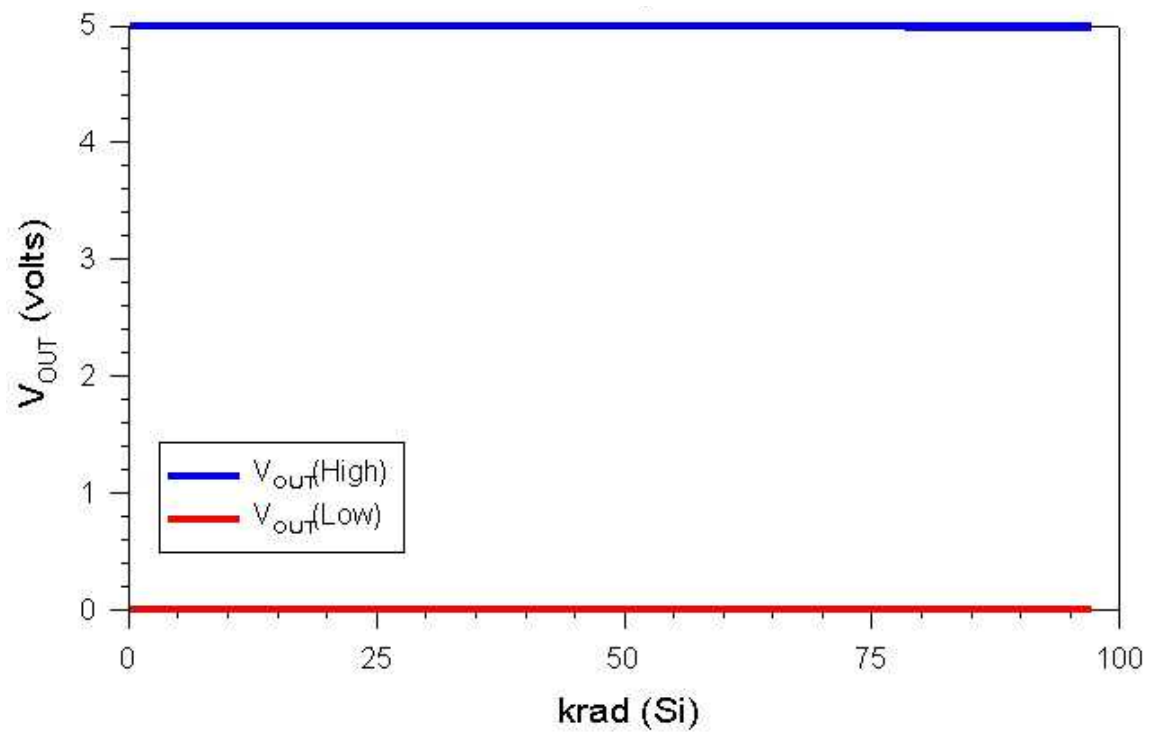


Fig 4 In-flux V_{OUT} of the functionality test circuit in LAN6503

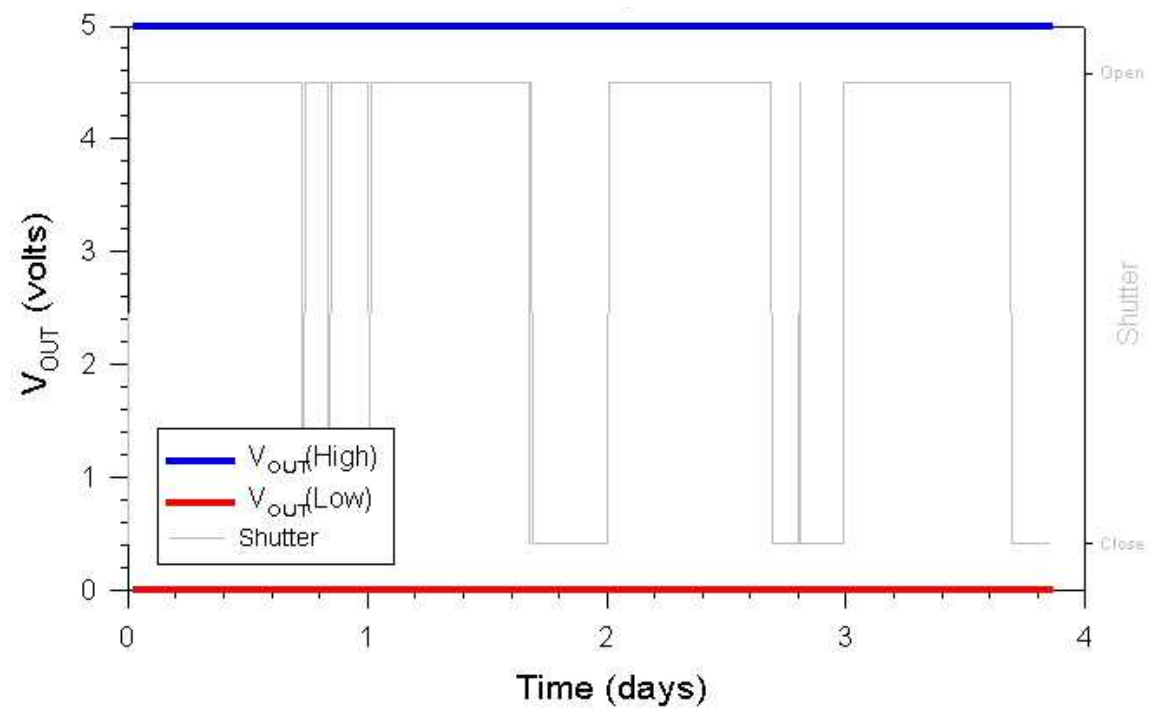


Fig 5 In-flux V_{OUT} of the functionality test circuit in LAN6504

2) *In-Flux I_{CC}*

Fig 6, 7, 8 and 9 show the in-flux I_{CCA} and I_{CCI} .

Table 3 lists the total dose level at which I_{CC} reaches the spec limit of 25 mA.

Table 3 Total Dose level at which $I_{CCA} = 25$ mA

DUT	Total Dose @ $I_{CCA} = 25$ mA
LAN6501	51 krad(Si)
LAN6502	62 krad(Si)
LAN6503	61 krad(Si)
LAN6504	60 krad(Si)

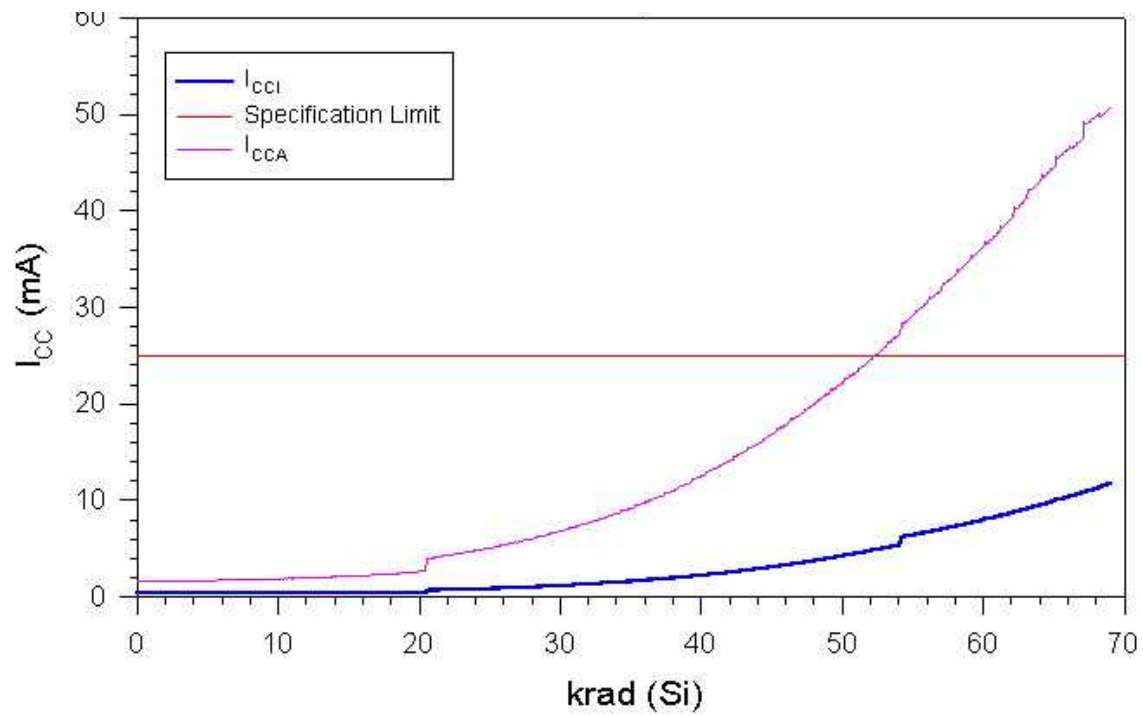


Fig 6 In-flux I_{CC} of LAN6501

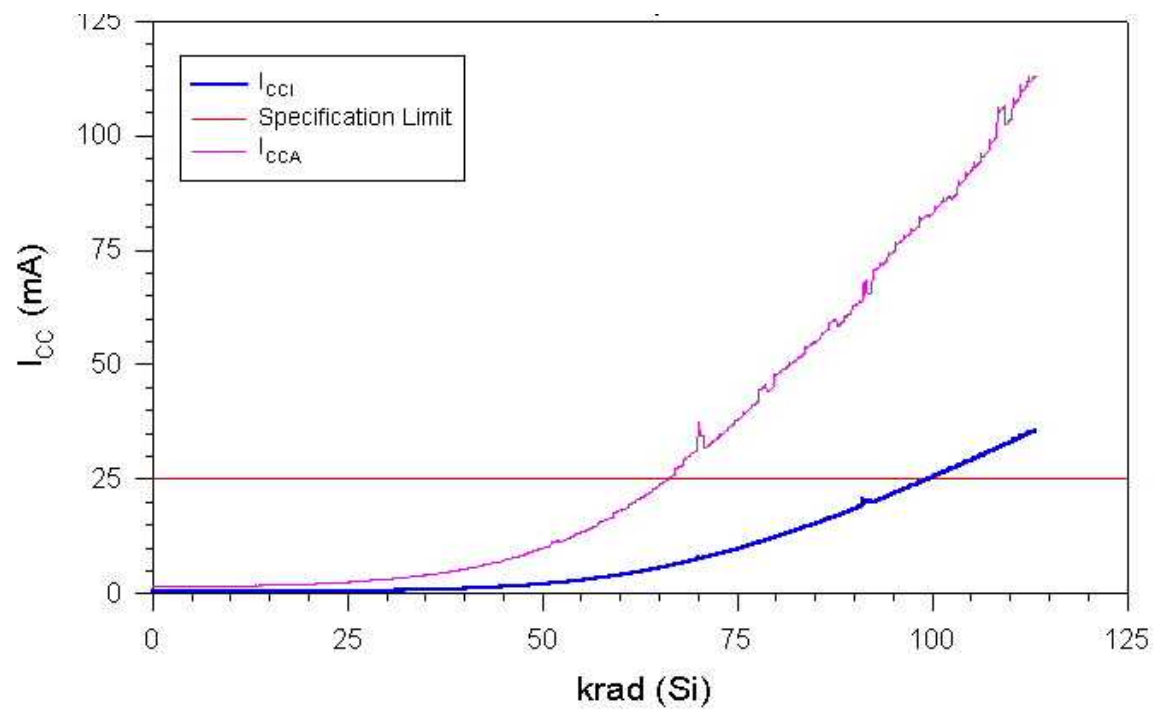


Fig 7 In-flux I_{CC} of LAN6502

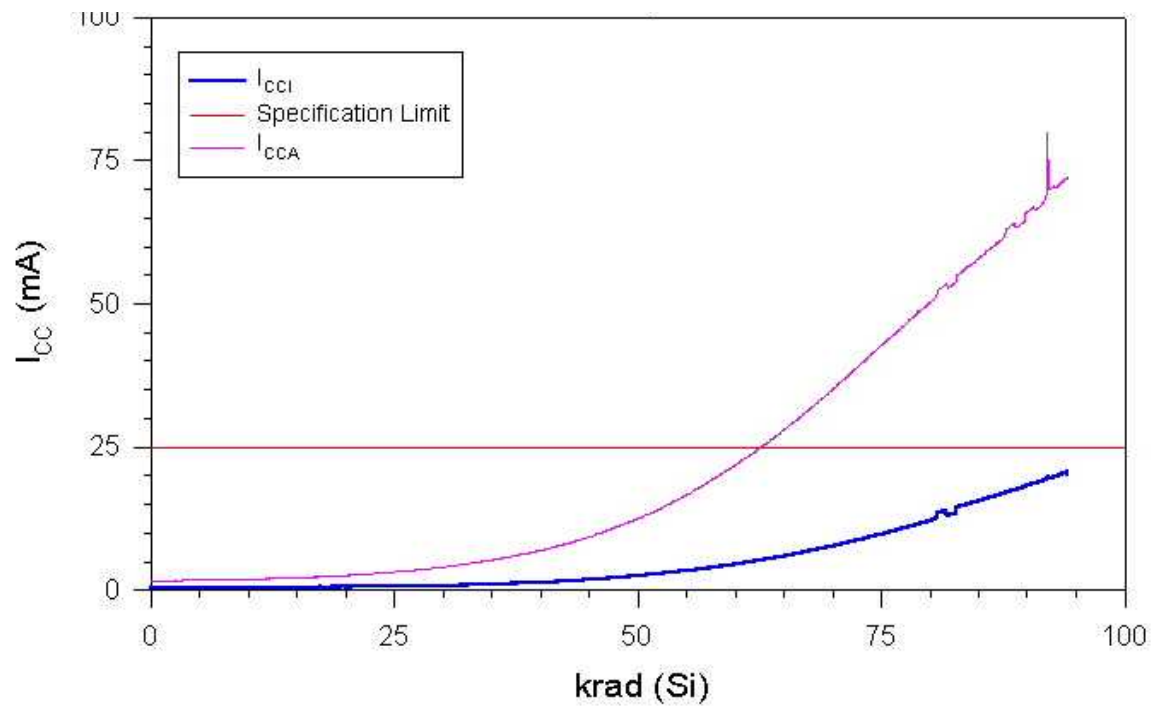


Fig 8 In-flux I_{CC} of LAN6503

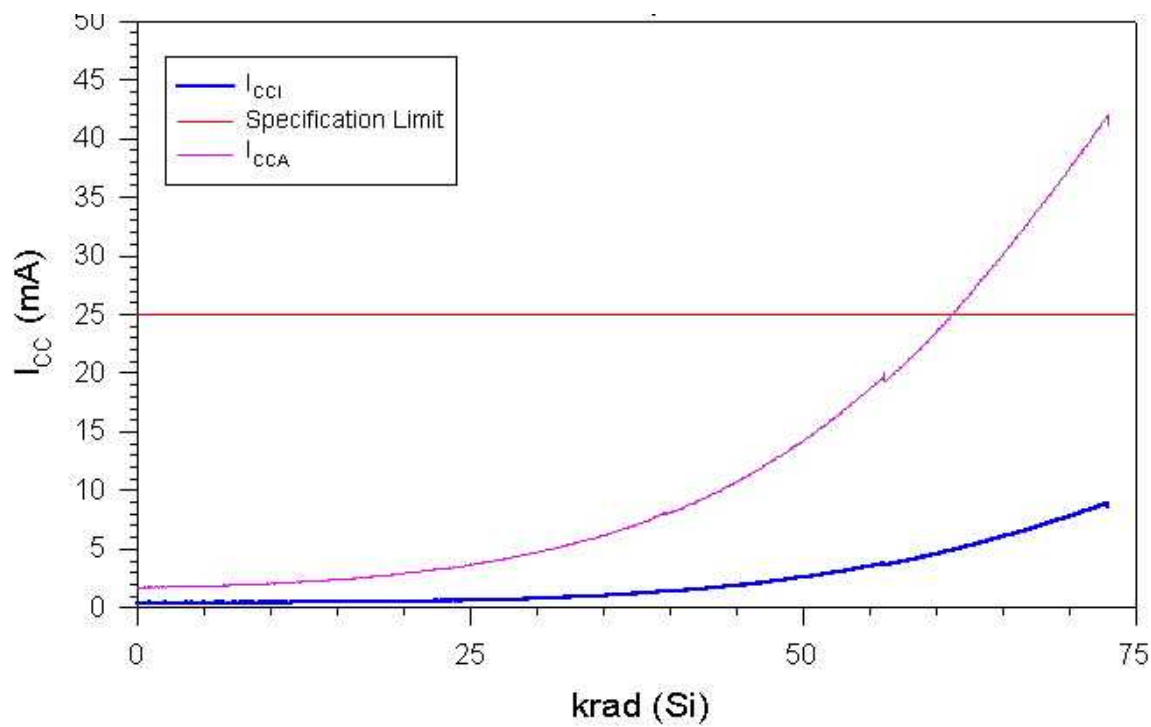


Fig 9 In-flux I_{CC} of LAN6504

3) *Input Logic Threshold*

Table 4 lists the pre and post-irradiation input logic threshold of each DUT. The radiation effect is negligible.

Table 4 Pre and Post-Irradiation Input Logic Threshold (V_{IL}/V_{IH})

	Pre-Irradiation	Post-Irradiation
LAN6501	1.4 V	1.4 V
LAN6502	1.4 V	1.4 V
LAN6503	1.4 V	1.4 V
LAN6504	1.4 V	1.4 V

4) *Output Characteristics*

Fig 10 and 11 show the pre and post-irradiation V_{OH} characteristics. In every case, the degradation after radiation is negligible. The pre and post-irradiation of V_{OL} of every DUT were also measured with negligible radiation effects.

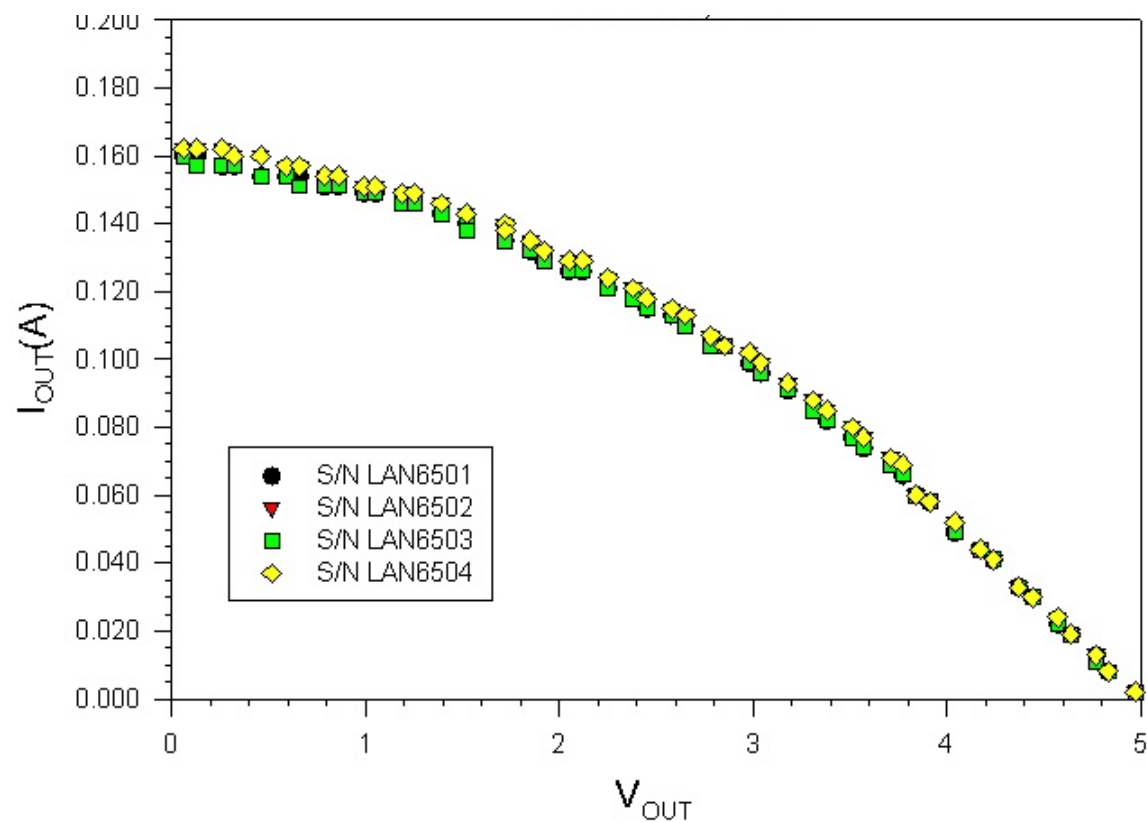


Fig 10 Pre-irradiation V_{OH} characteristic curves

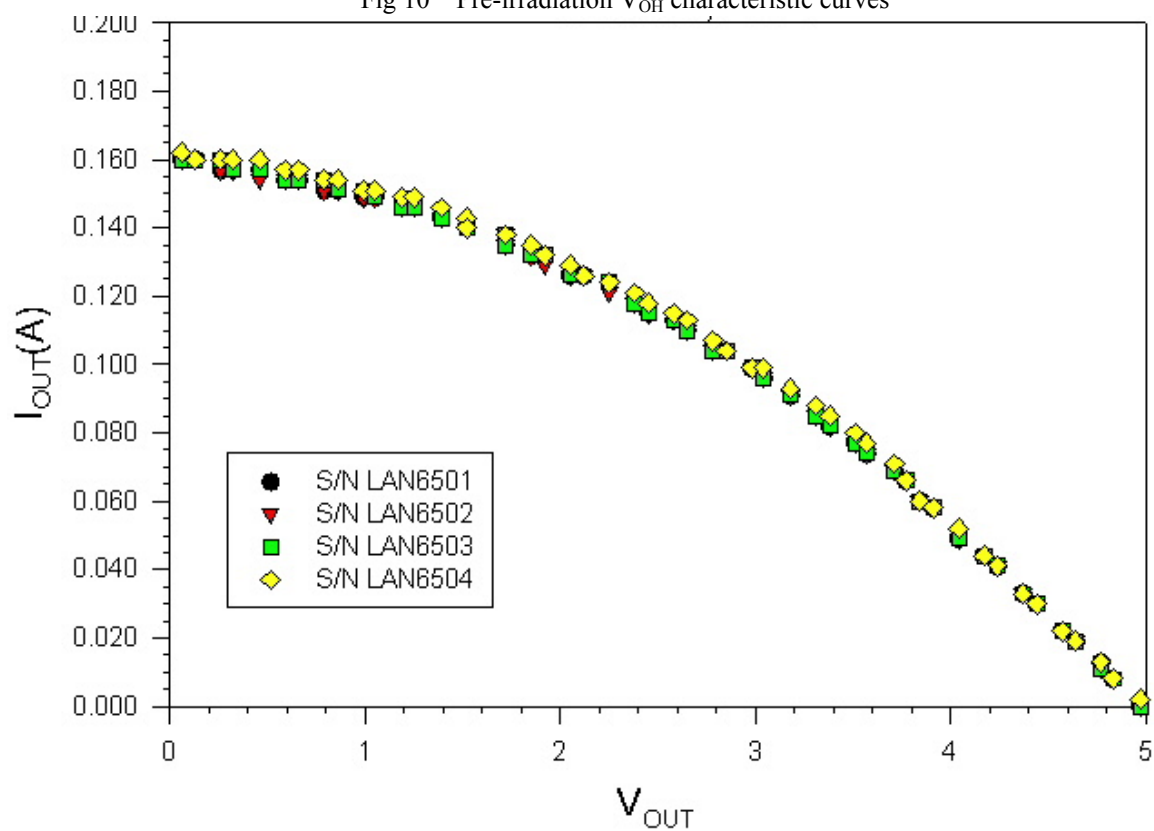


Fig 11 Post-irradiation V_{OH} characteristic curves

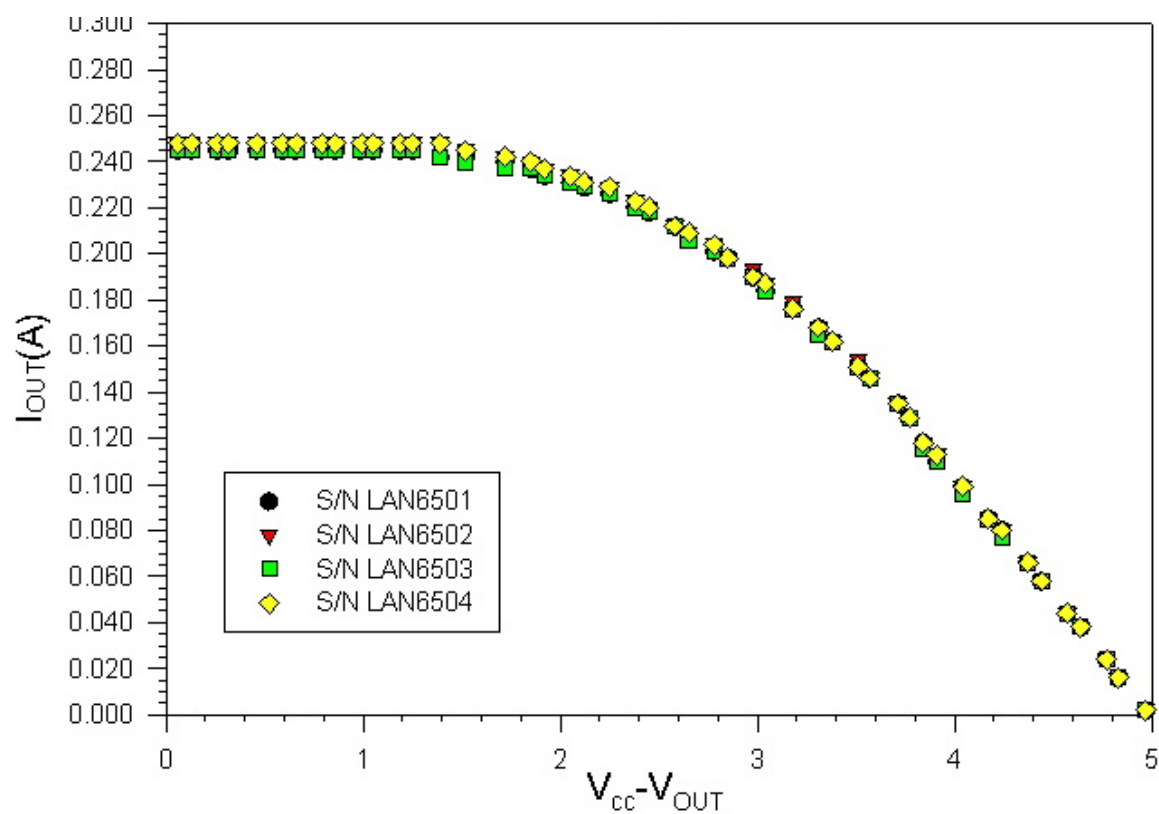


Fig 12 Pre-irradiation V_{OL} characteristic curves

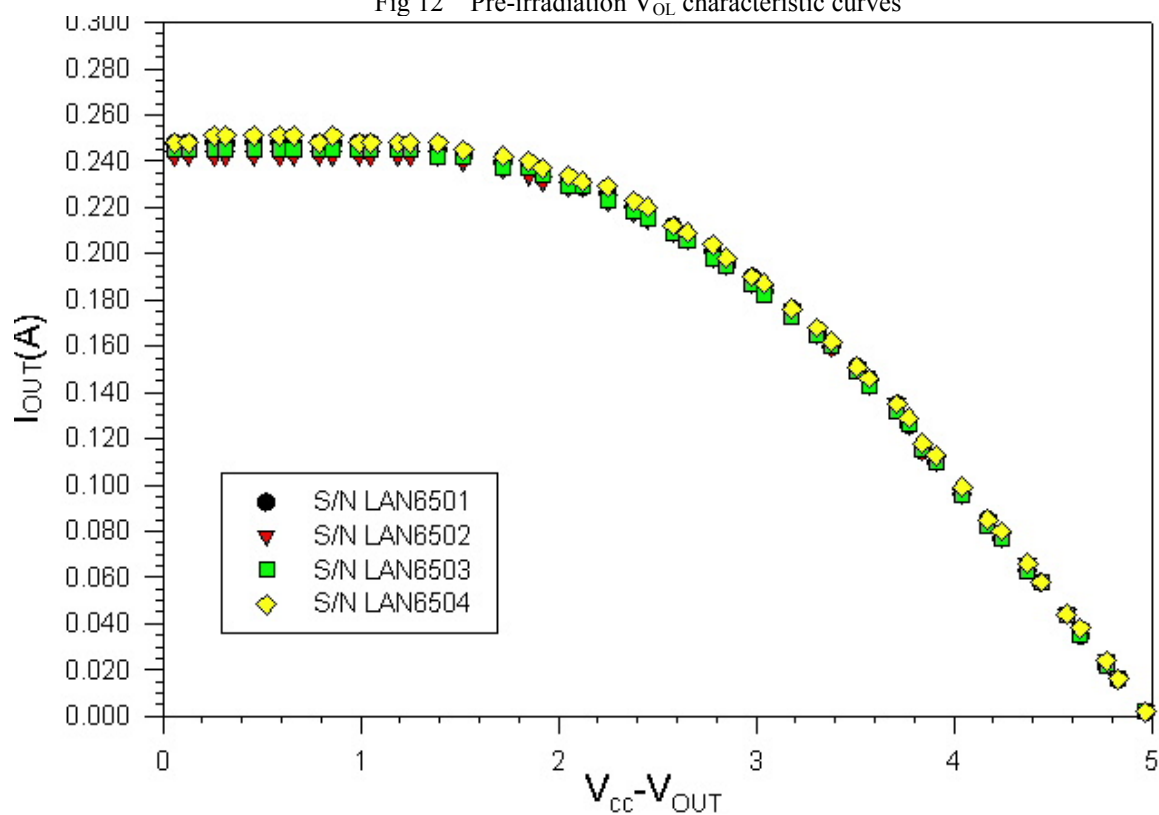


Fig 13 Post-irradiation V_{OL} characteristic curves

5) Propagation Delays

Table 5 lists the pre and post-irradiation propagation delays and radiation-induced degradations in percentages. Note that each DUT was irradiated to different total dose levels. However, the in-flux curves in Fig 14, 15, 16 and 17 show the continuous propagation delay changes with respect to total accumulative dose. Using 10% degradation criterion, the tolerance is approximately 100 krad(Si).

Table 5 Propagation delays (ns)

DUT	Rising Output			Falling Output		
	Pre-Irrad	Post-Irrad	Degradation	Pre-Irrad	Post-Irrad	Degradation
LAN6501	1316	1392	5.78% (69 krad)	1107	1167	5.42% (69 krad)
LAN6502	1301	1489	14.4% (113 krad)	1119	1260	12.6% (113 krad)
LAN6503	1290	1401	8.6% (95 krad)	1103	1210	9.70% (95 krad)
LAN6504	1310	1350	3.05% (73 krad)	1112	1150	3.42% (73 krad)

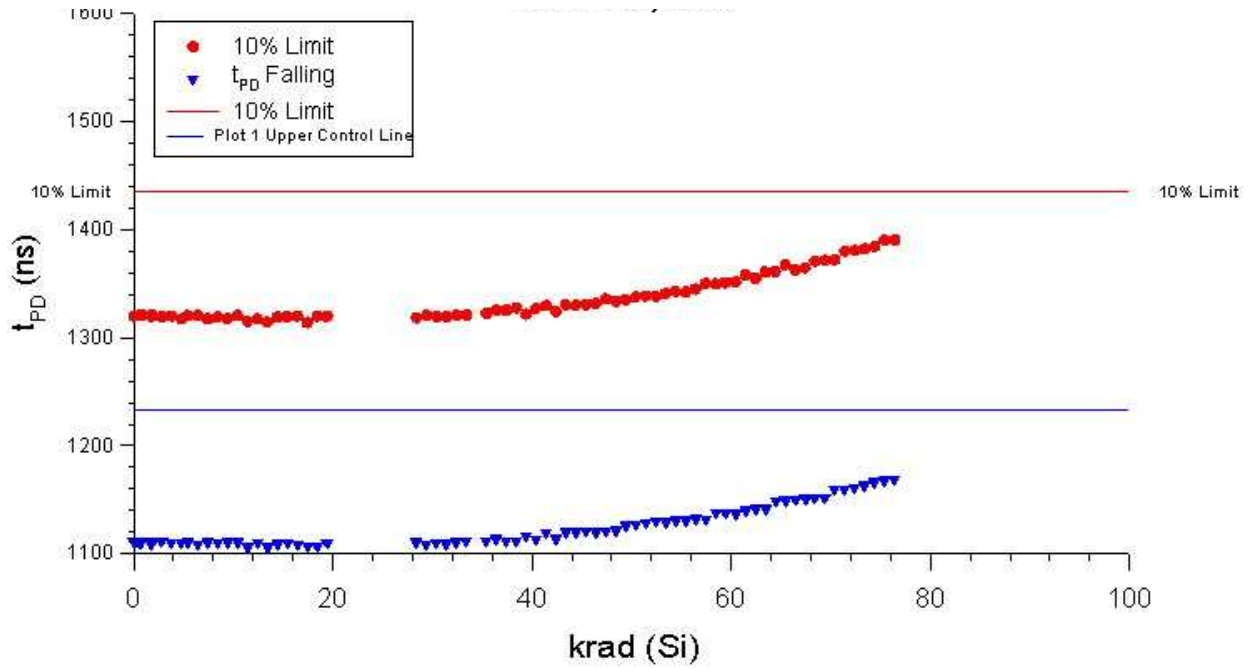


Fig 14 In-flux propagation delay of LAN6501

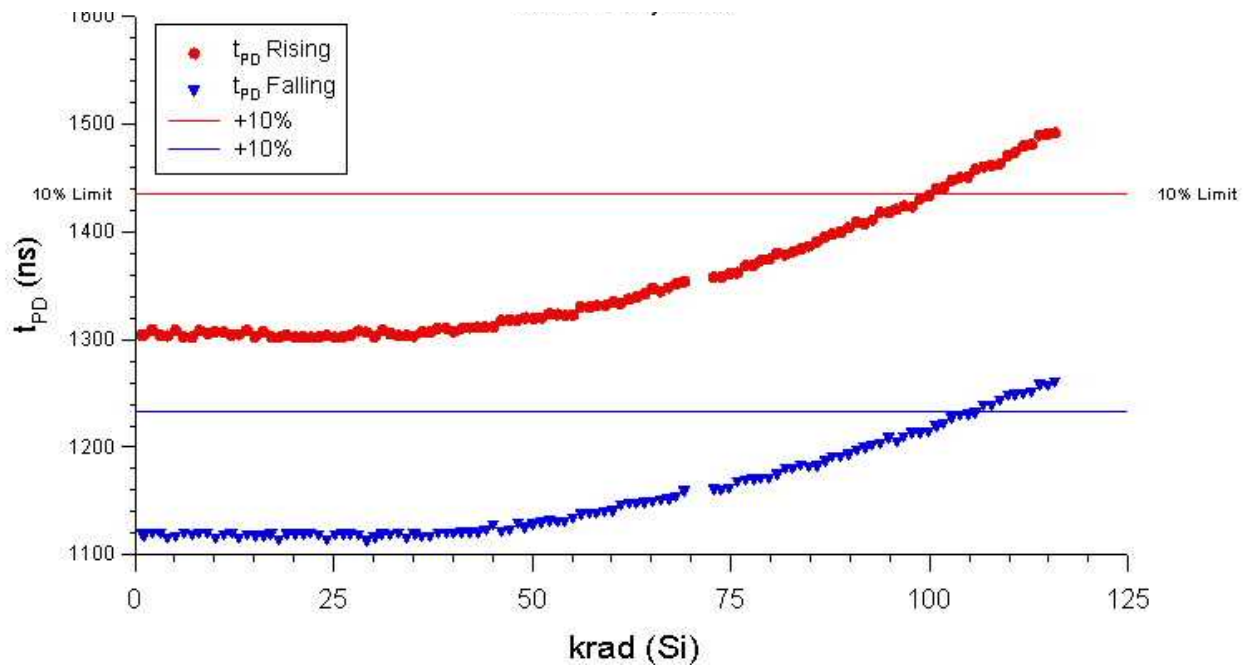


Fig 15 In-flux propagation delay of LAN6502

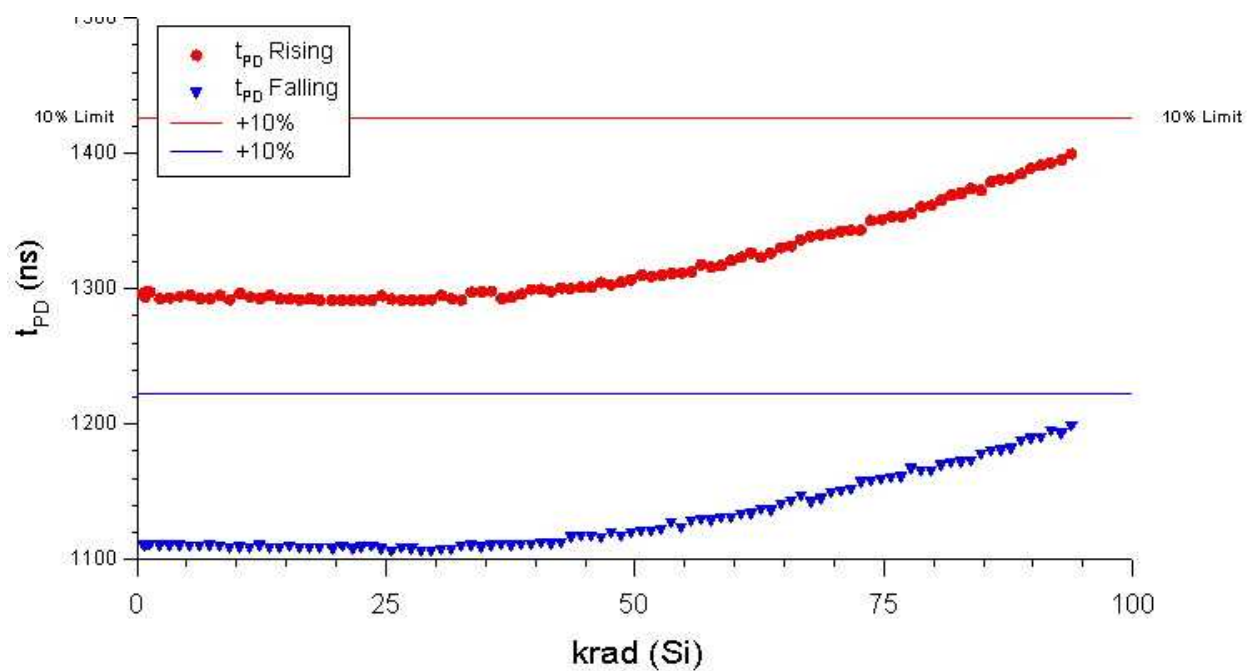


Fig 16 In-flux propagation delay of LAN6503

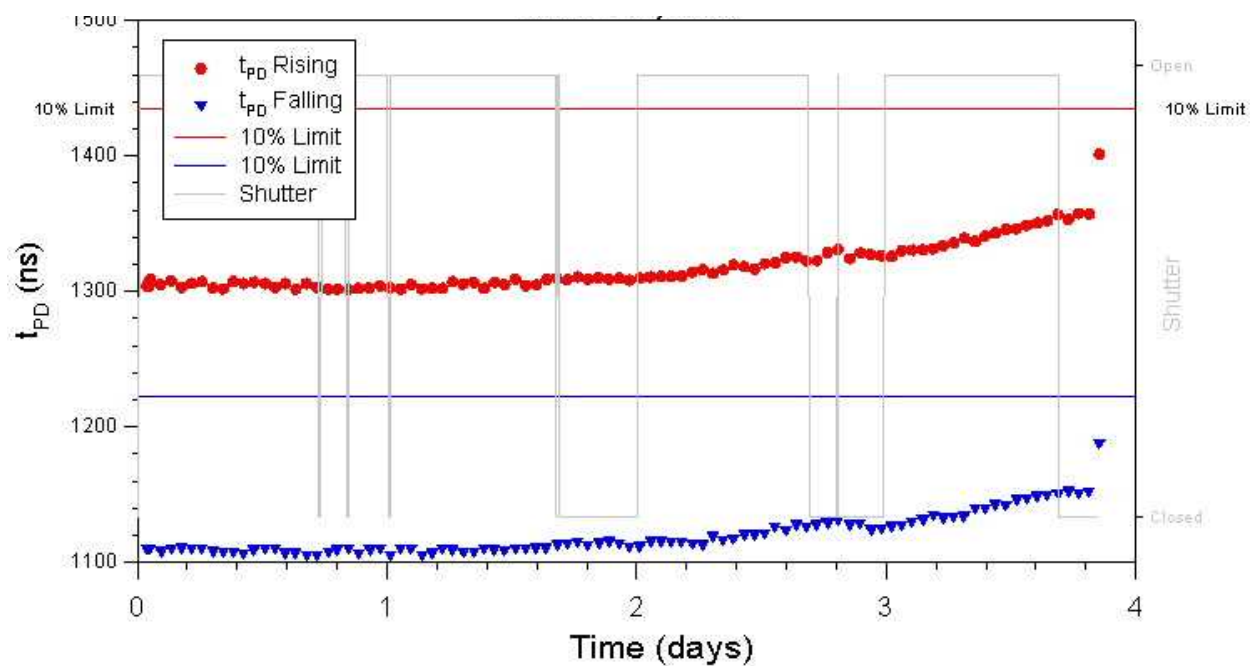


Fig 17 In-flux propagation delay of LAN6504

6) *Transition Time*

The pre and post-irradiation rising and falling time of every DUT were measured. Fig 18(a) and 18(b) show the typical pre and post-irradiation rising edge. There is no significant change in rising edge after irradiation for each DUT. Fig 19(a) and 19(b) show the typical pre and post-irradiation falling edge. Again, there is no detectable radiation effect on the falling edge for each DUT.

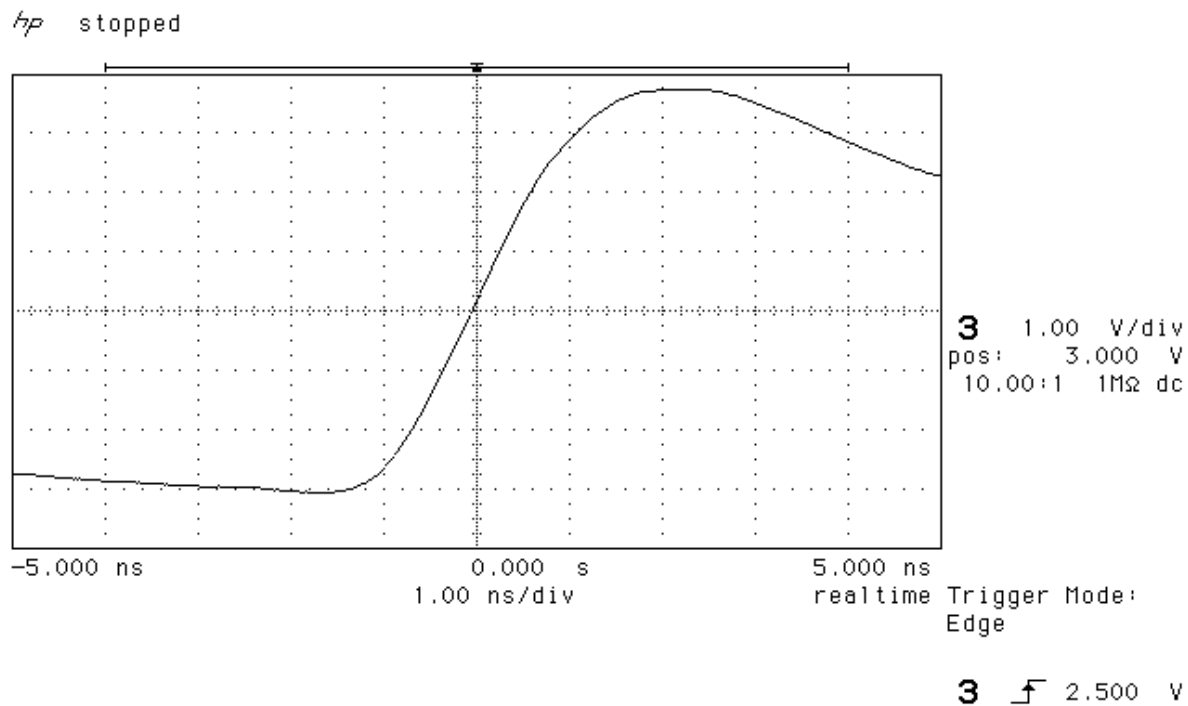


Fig 18(a) A typical pre-irradiation rising edge

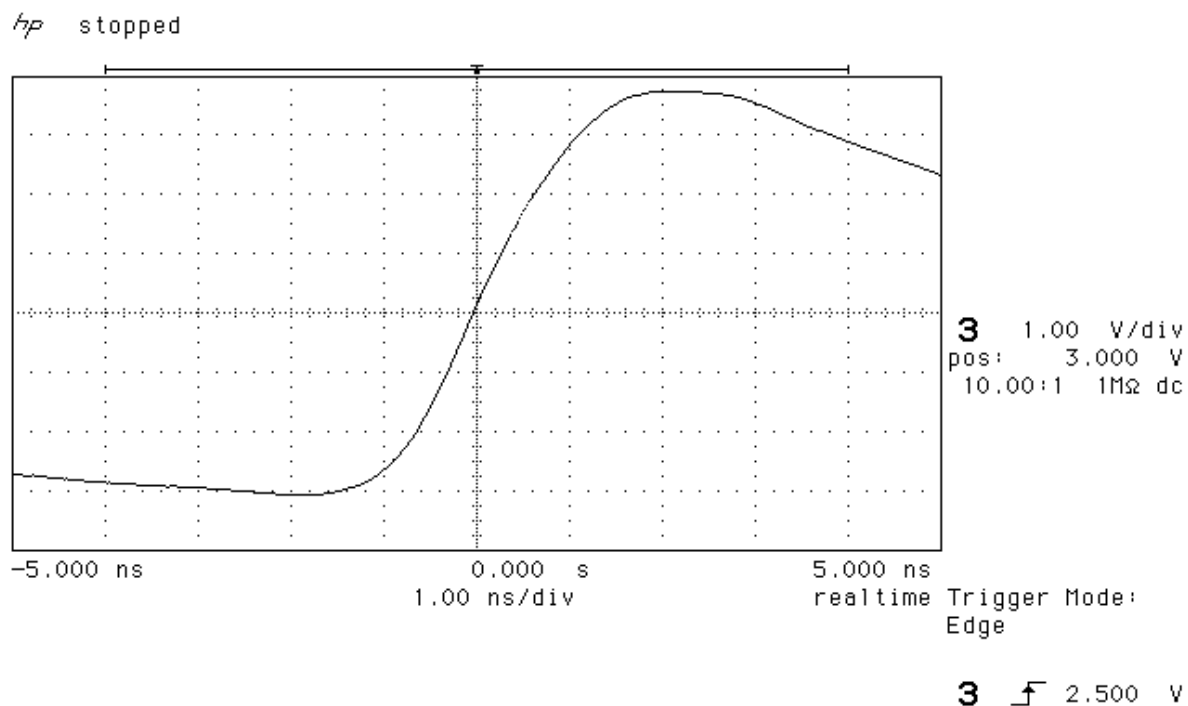


Fig 18(b) A typical post-irradiation rising edge

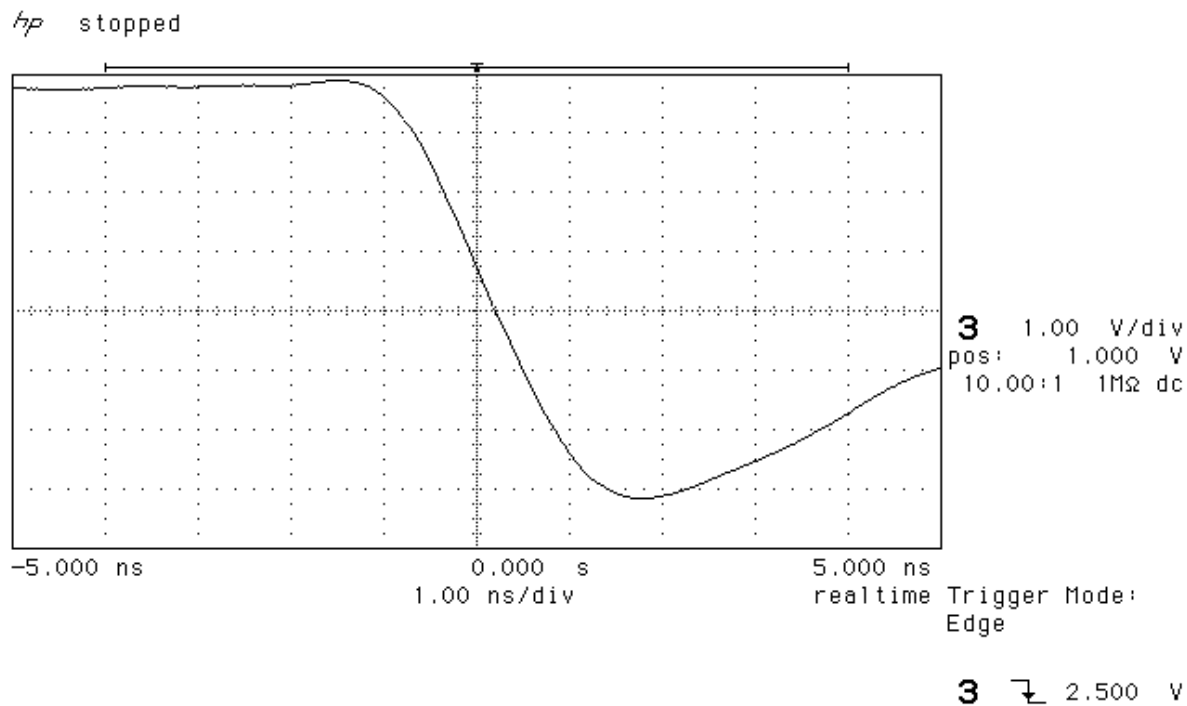


Fig 19(a) A typical pre-irradiation falling edge

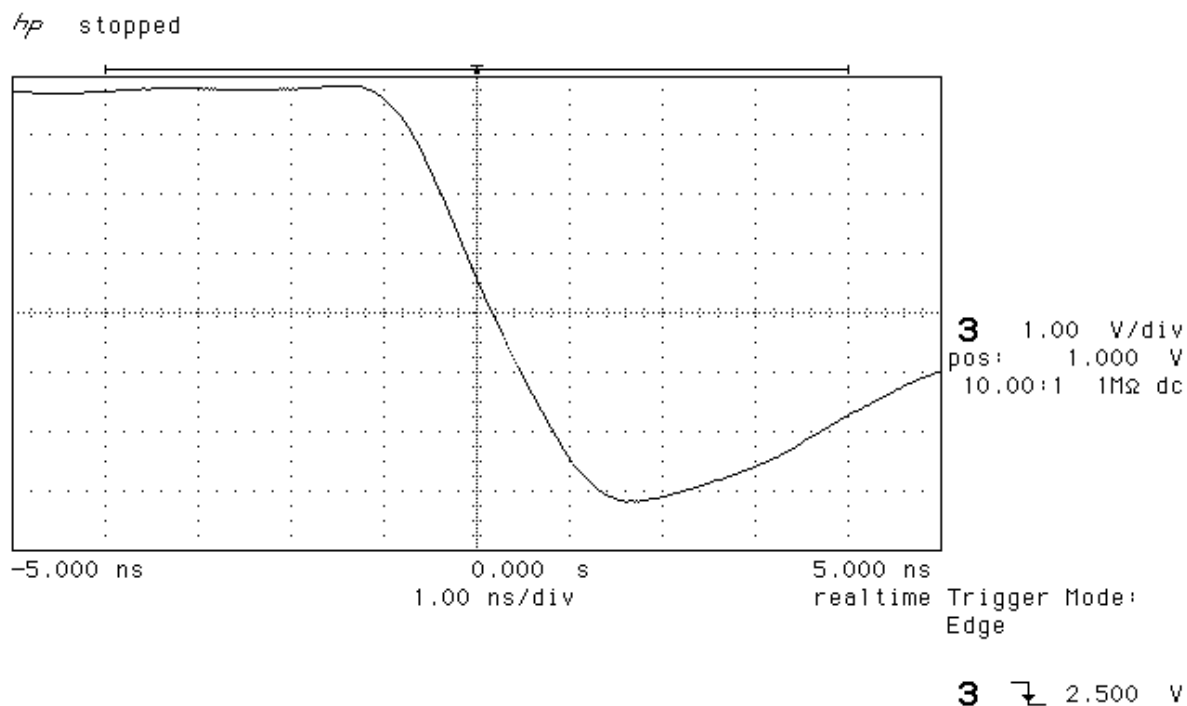


Fig 19(b) A typical post-irradiation falling edge

7) *Power-Up Transient*

Fig 20(a) and 20(b) show the typical pre and post-irradiation power-up transient for I_{CCA} at $V_{CCI} = 0$ V. There is no detectable radiation effect on this characteristic in every DUT.

Fig 21(a) and 21(b) show the typical pre and post-irradiation power-up transient for I_{CCA} at $V_{CCI} = 5.0$ V. There is no detectable radiation effect on this characteristic in every DUT.

Fig 22(a) and 22(b) show the typical pre and post-irradiation power-up transient for I_{CCI} at $V_{CCA} = 0$ V. There is no detectable radiation effect on this characteristic in every DUT.

Fig 23(a) and 23(b) show the typical pre and post-irradiation power-up transient for I_{CCI} at $V_{CCA} = 2.5$ V. There is no detectable radiation effect on this characteristic in every DUT.

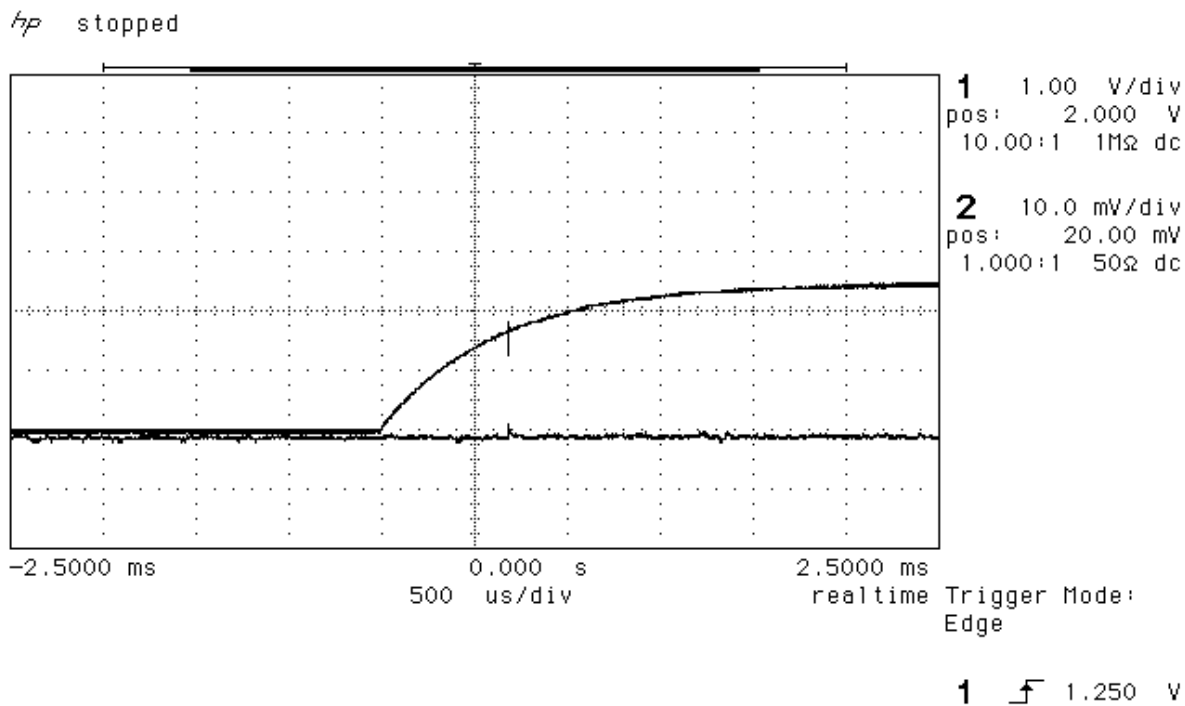


Fig 20(a) A typical pre-irradiation power up I_{CCA} transient at $V_{CCI} = 0$ V

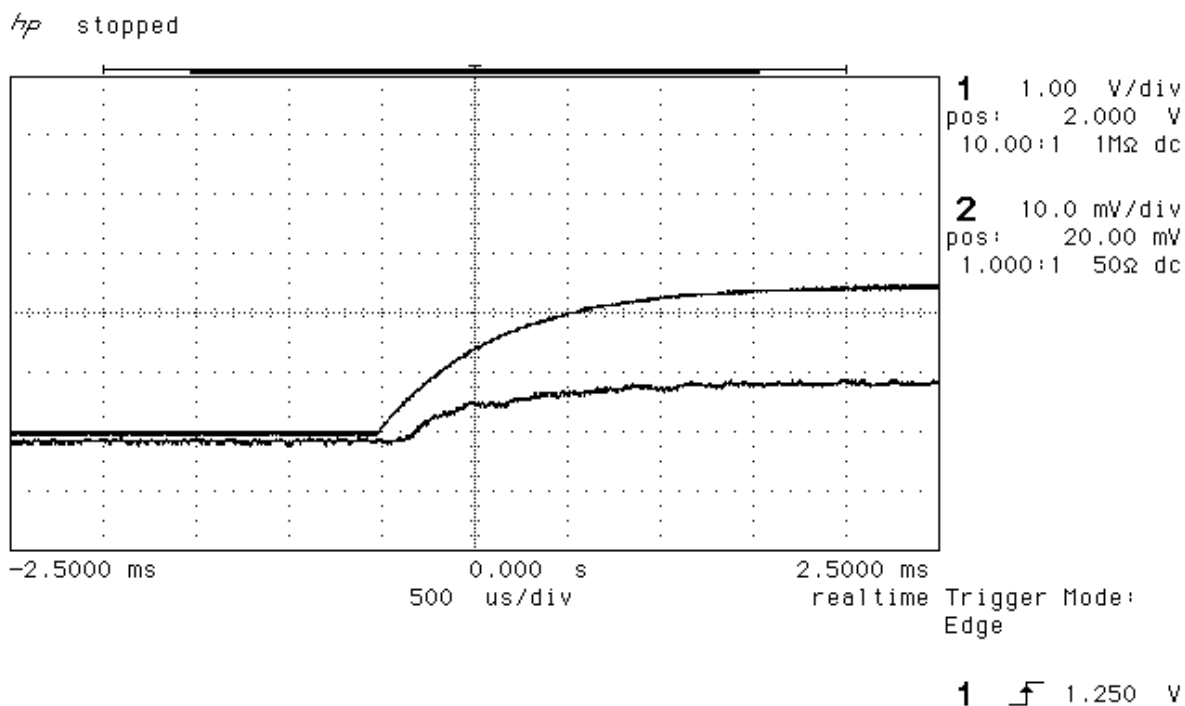


Fig 20(b) A typical post-irradiation power up I_{CCA} transient at $V_{CCI} = 0$ V

hp stopped

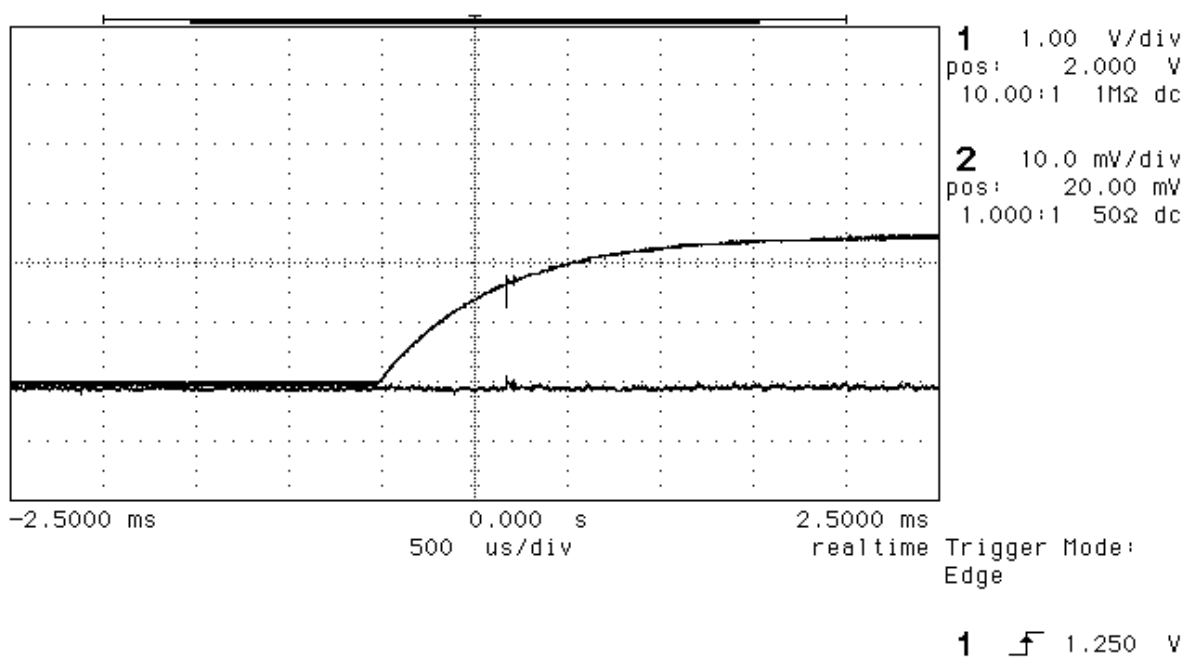


Fig 21(a) A typical pre-irradiation power up I_{CCA} transient at $V_{CCI} = 5.0$ V

hp stopped

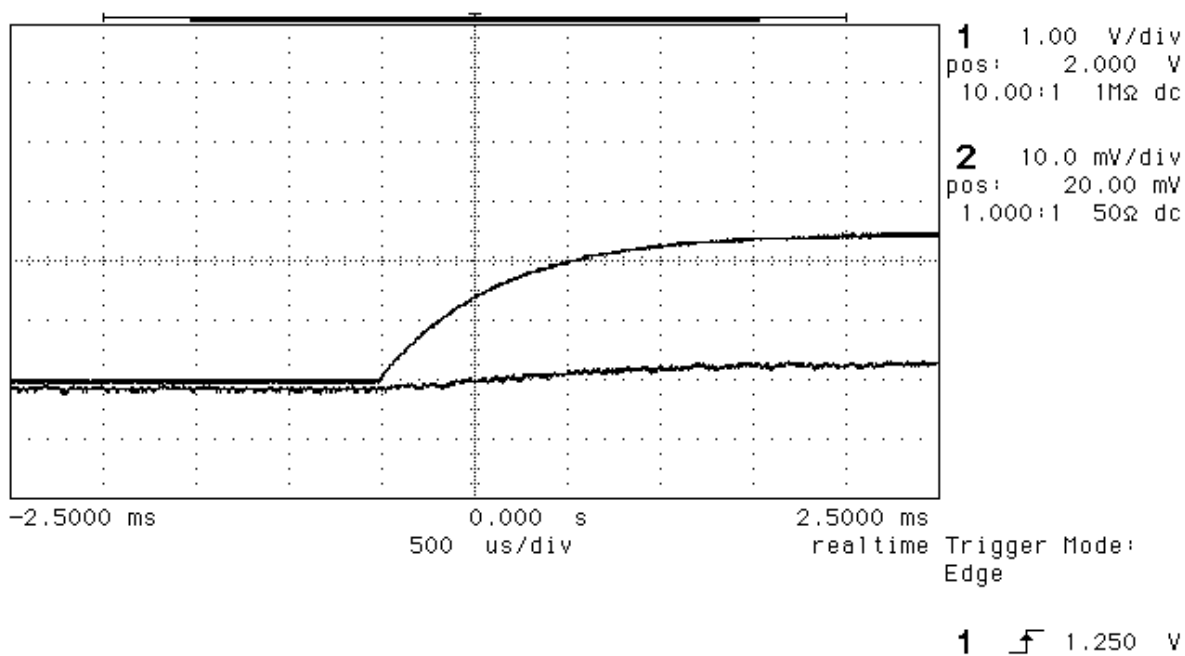


Fig 21(b) A typical post-irradiation power up I_{CCA} transient at $V_{CCI} = 5.0$ V

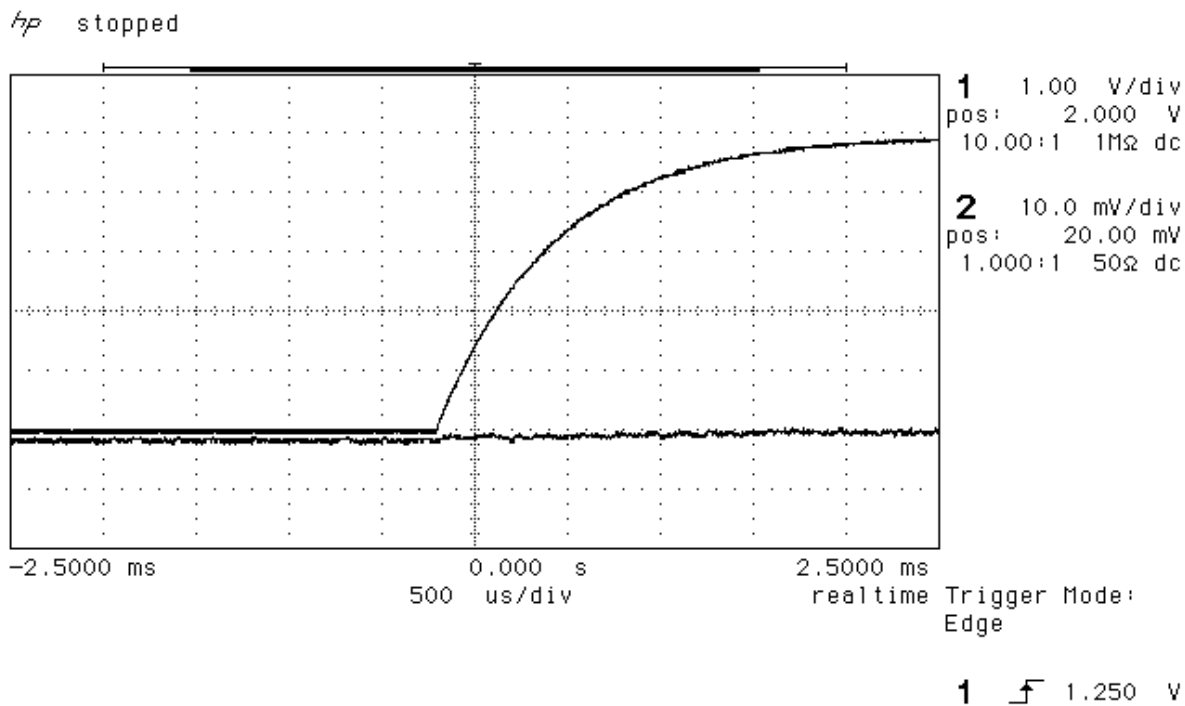


Fig 22(a) A typical pre-irradiation power up I_{CCI} transient at $V_{CCA}=0$ V

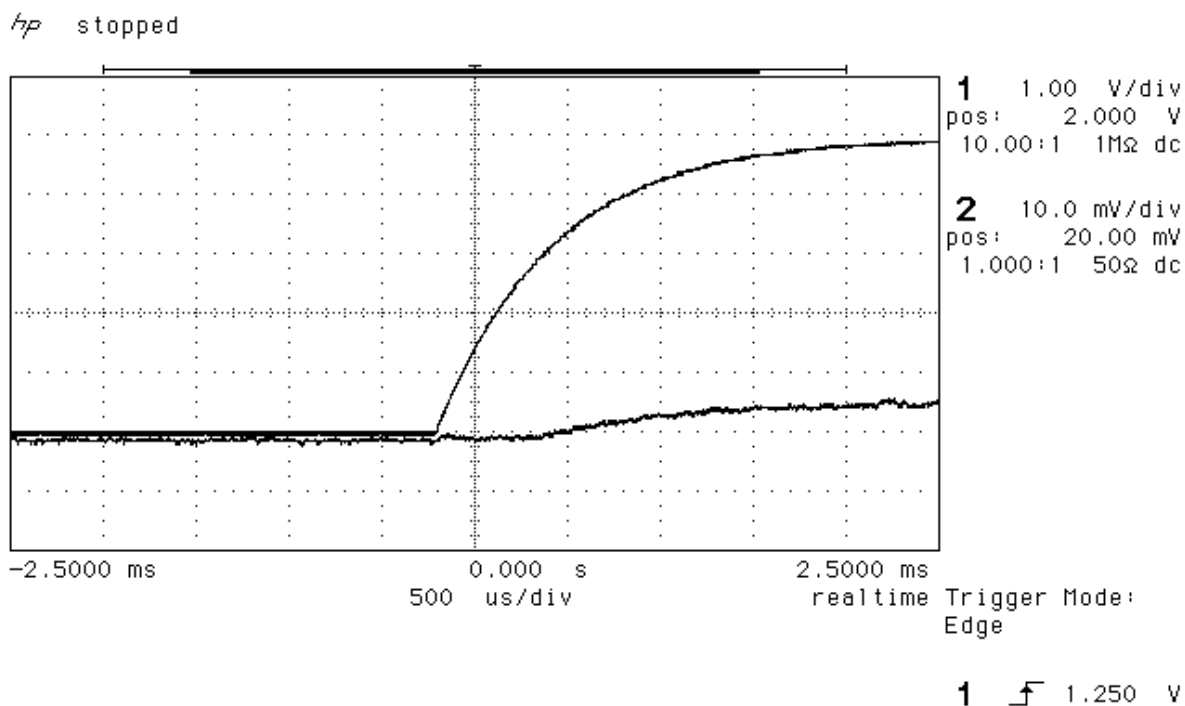


Fig 22(b) A typical post-irradiation power up I_{CCI} transient at $V_{CCA}=0$ V

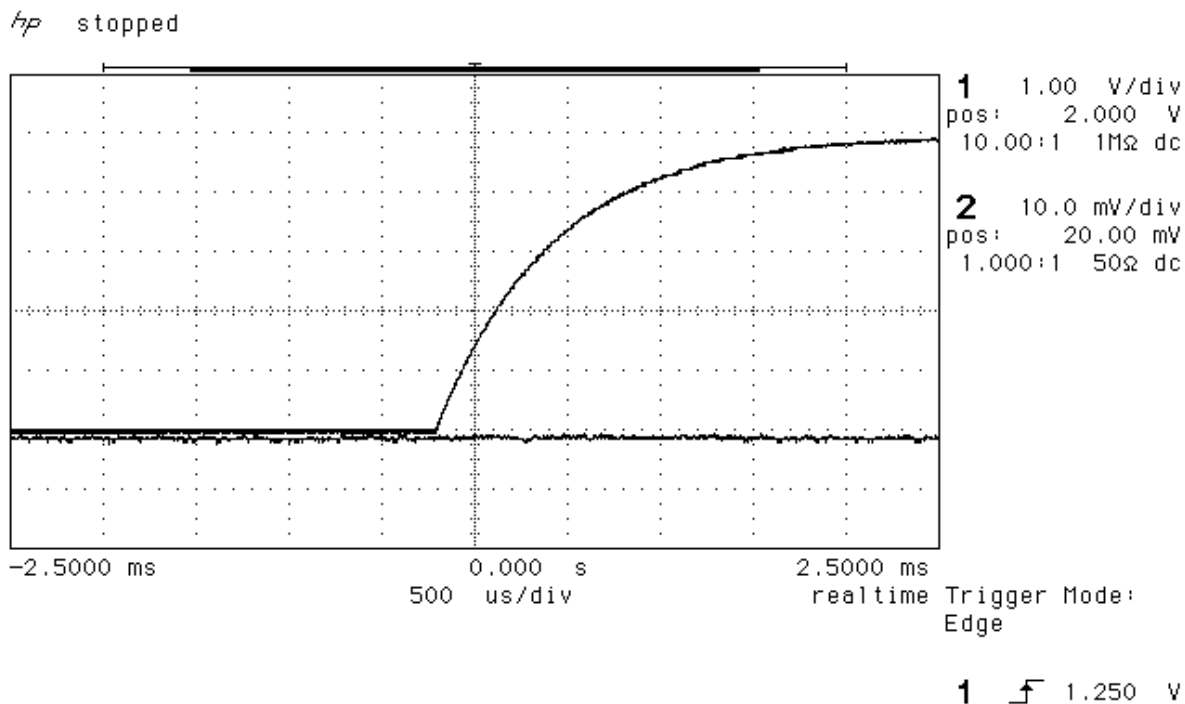


Fig 23(a) A typical pre-irradiation power up I_{CCI} transient at $V_{CCA}=2.5$ V

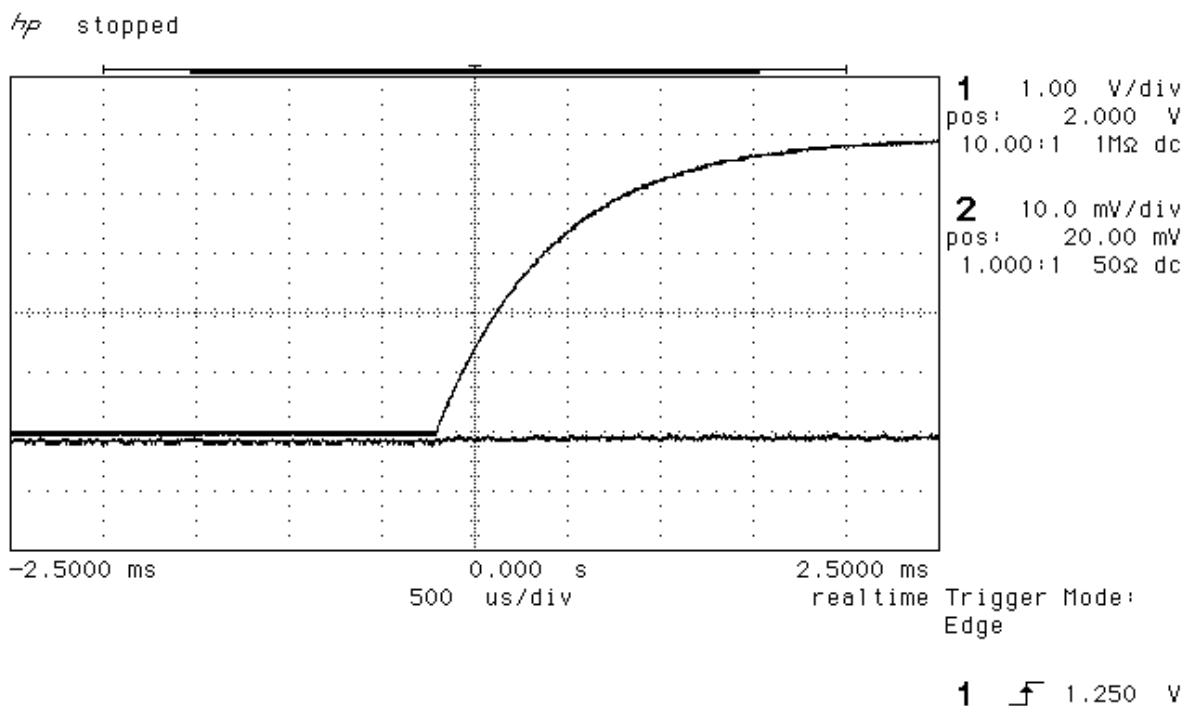
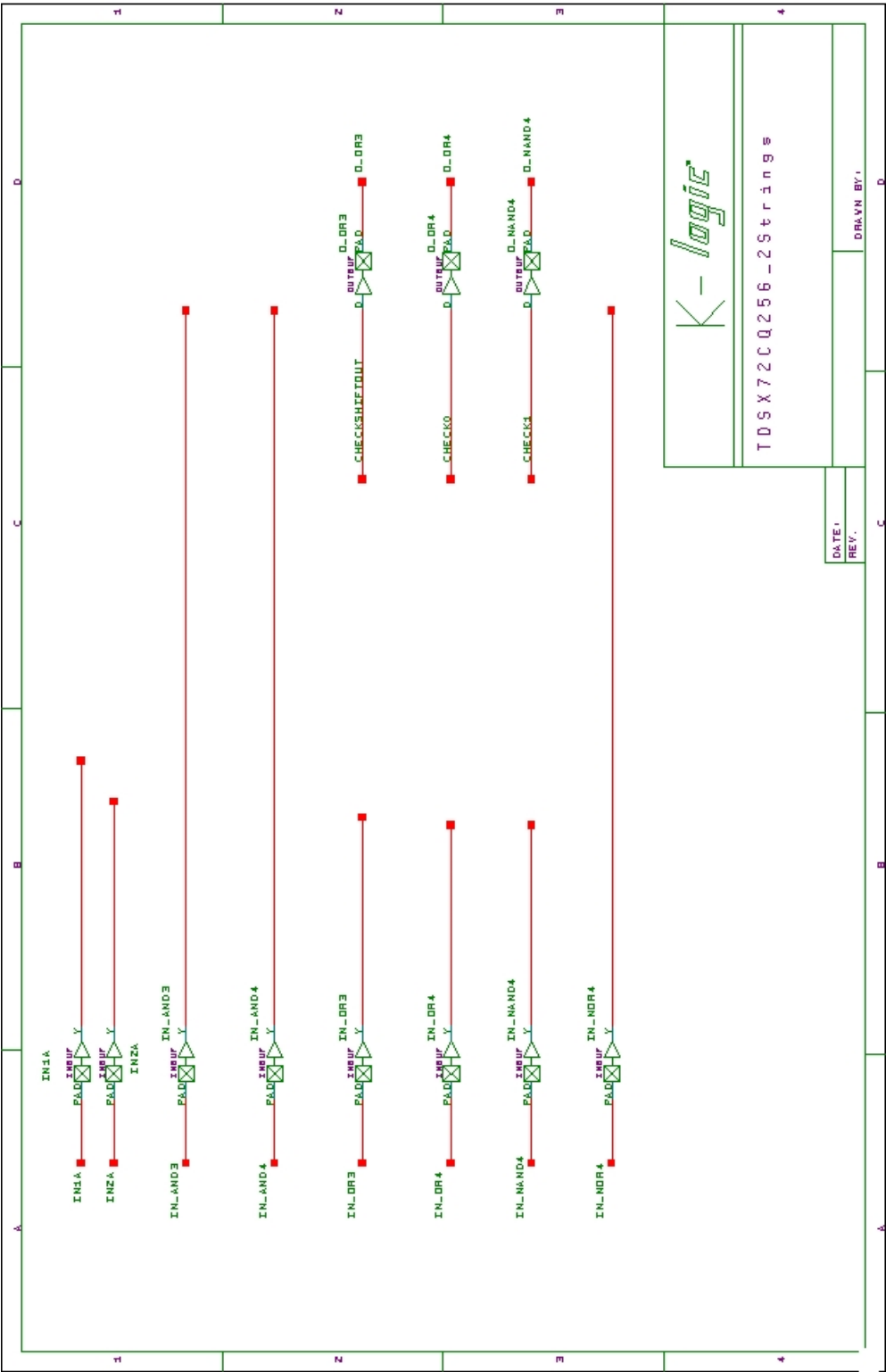
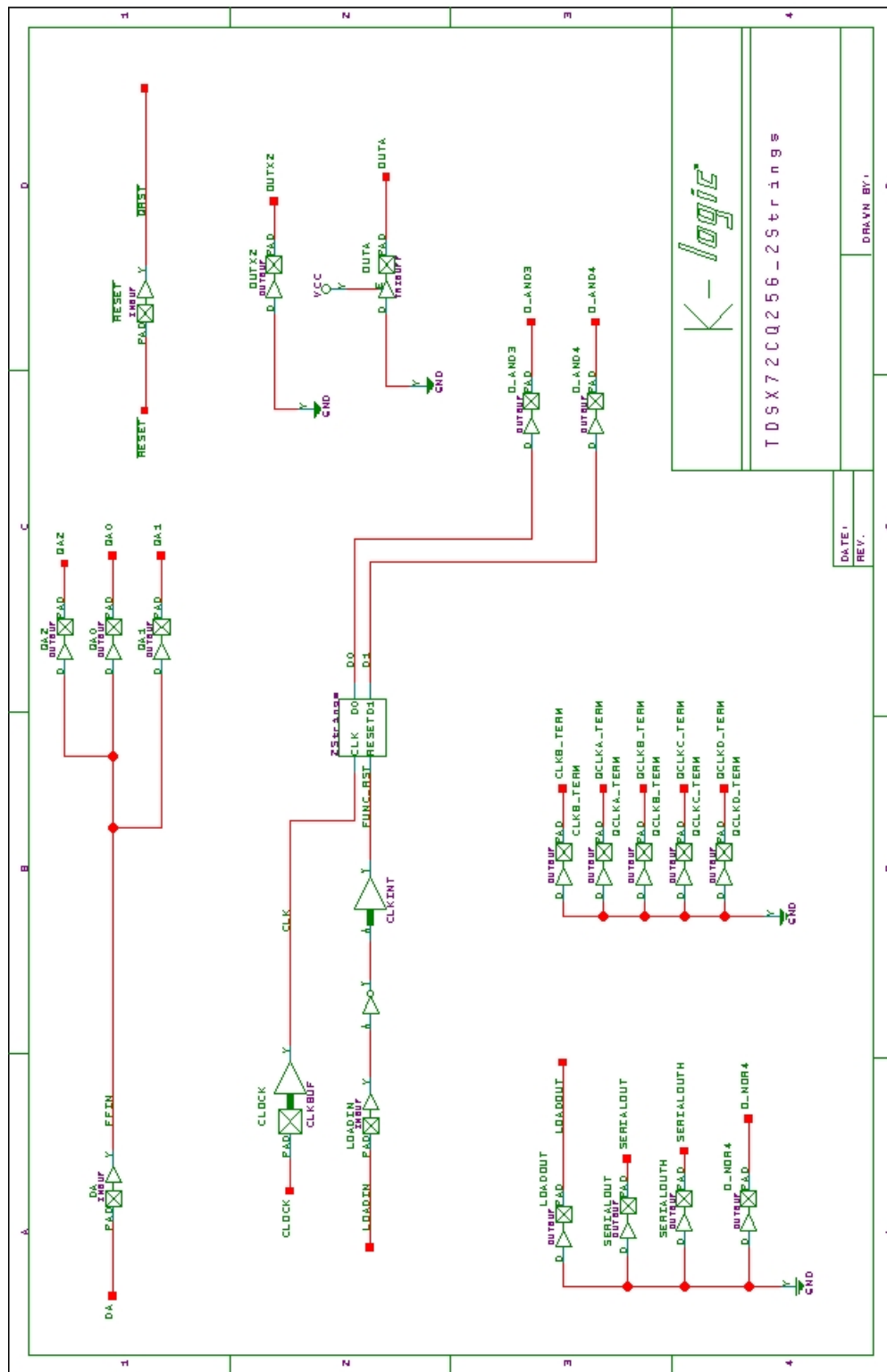


Fig 23(b) A typical post-irradiation power up I_{CCI} transient at $V_{CCA}=2.5$ V

APPENDIX A DUT DESIGN SCHEMATICS

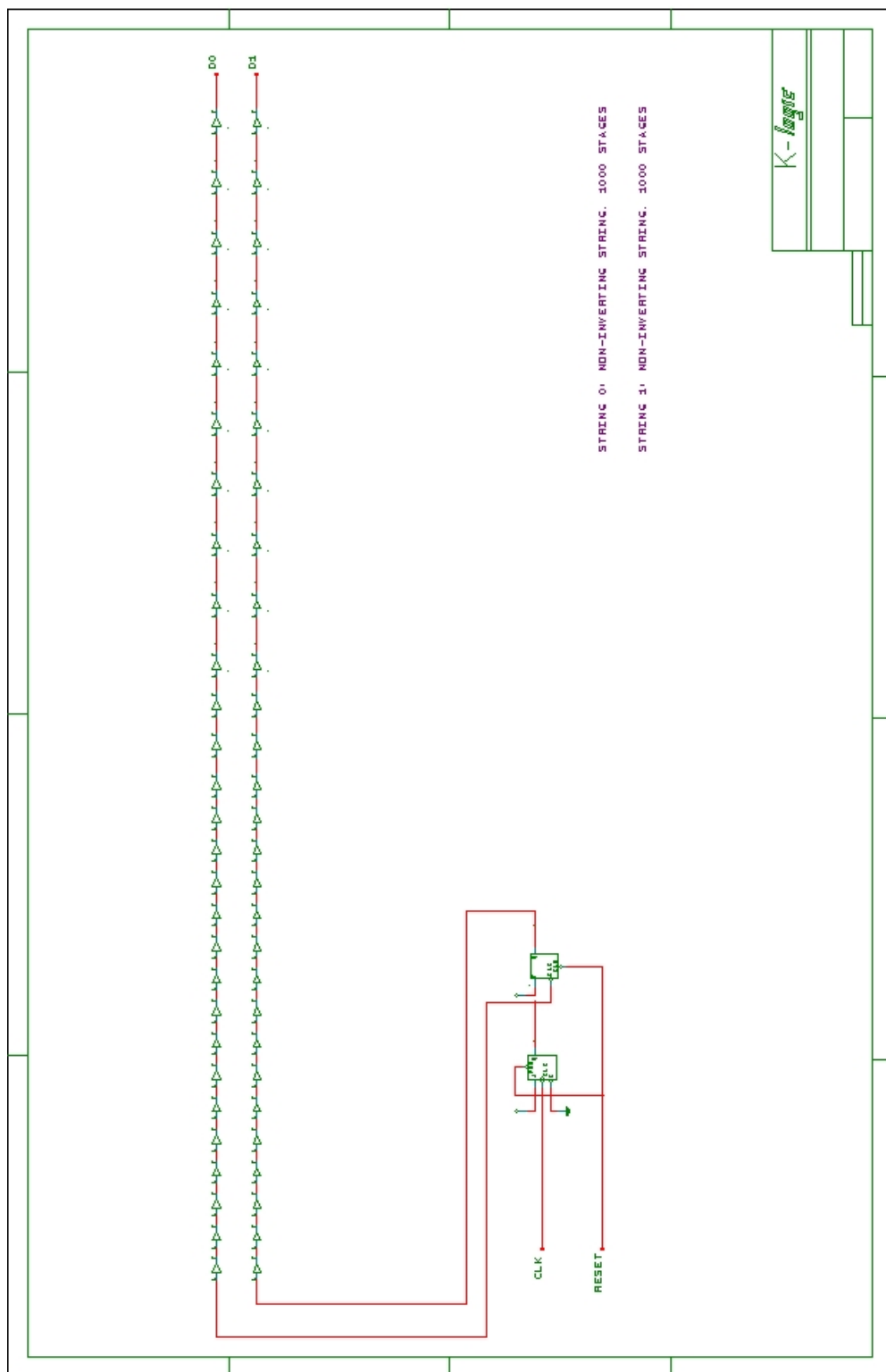


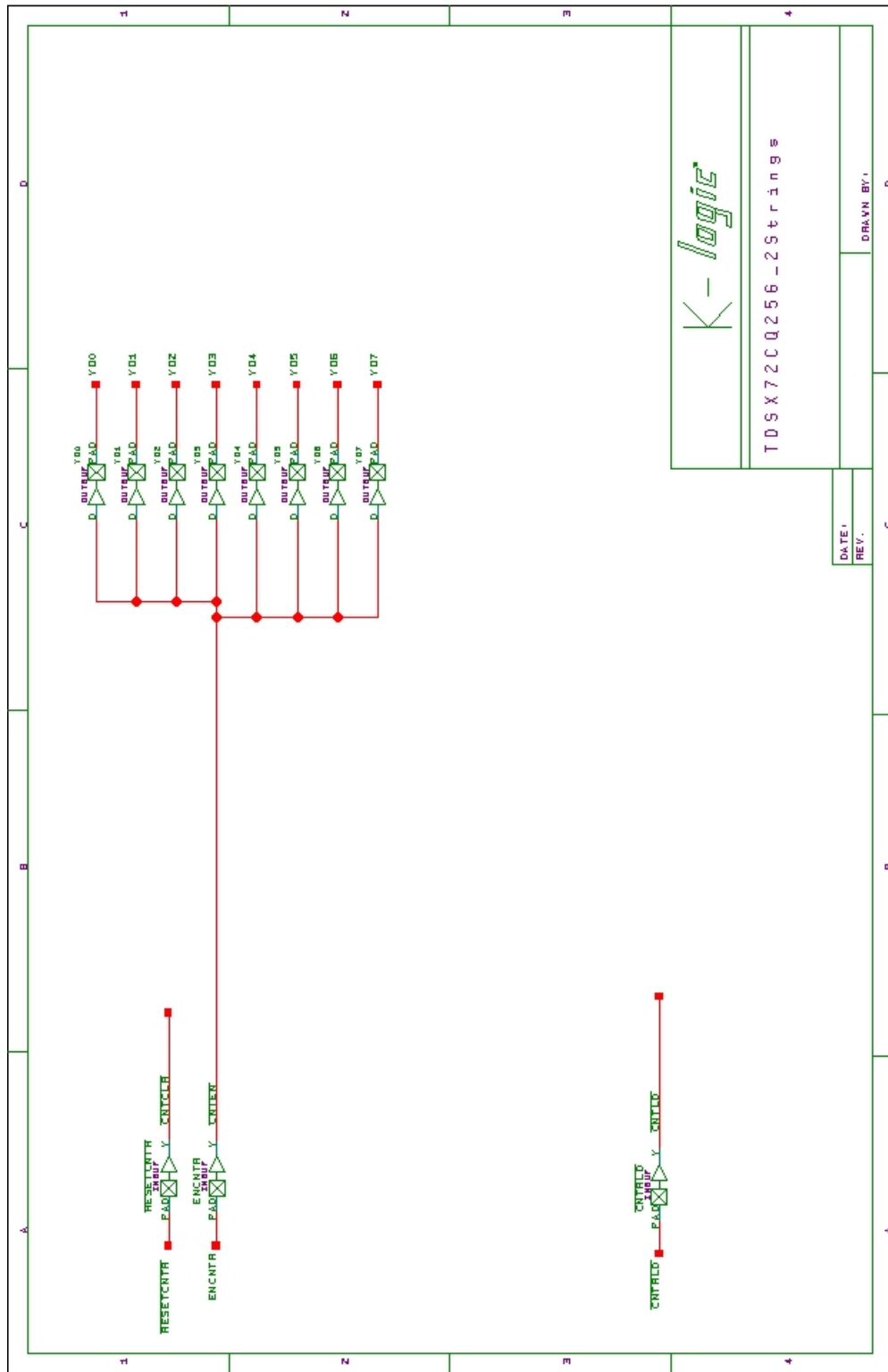


TDSX72CQ256-2 Strings

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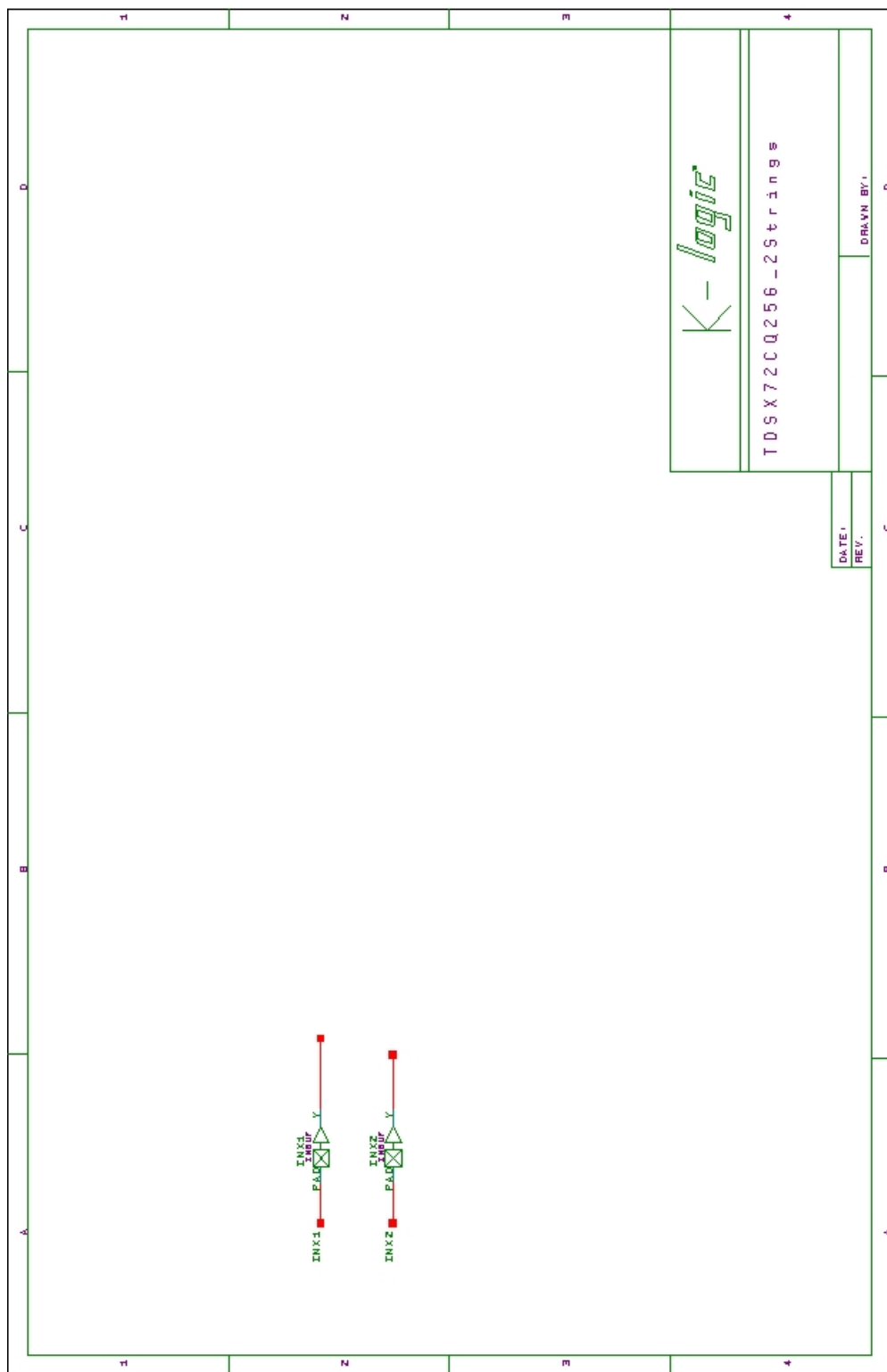


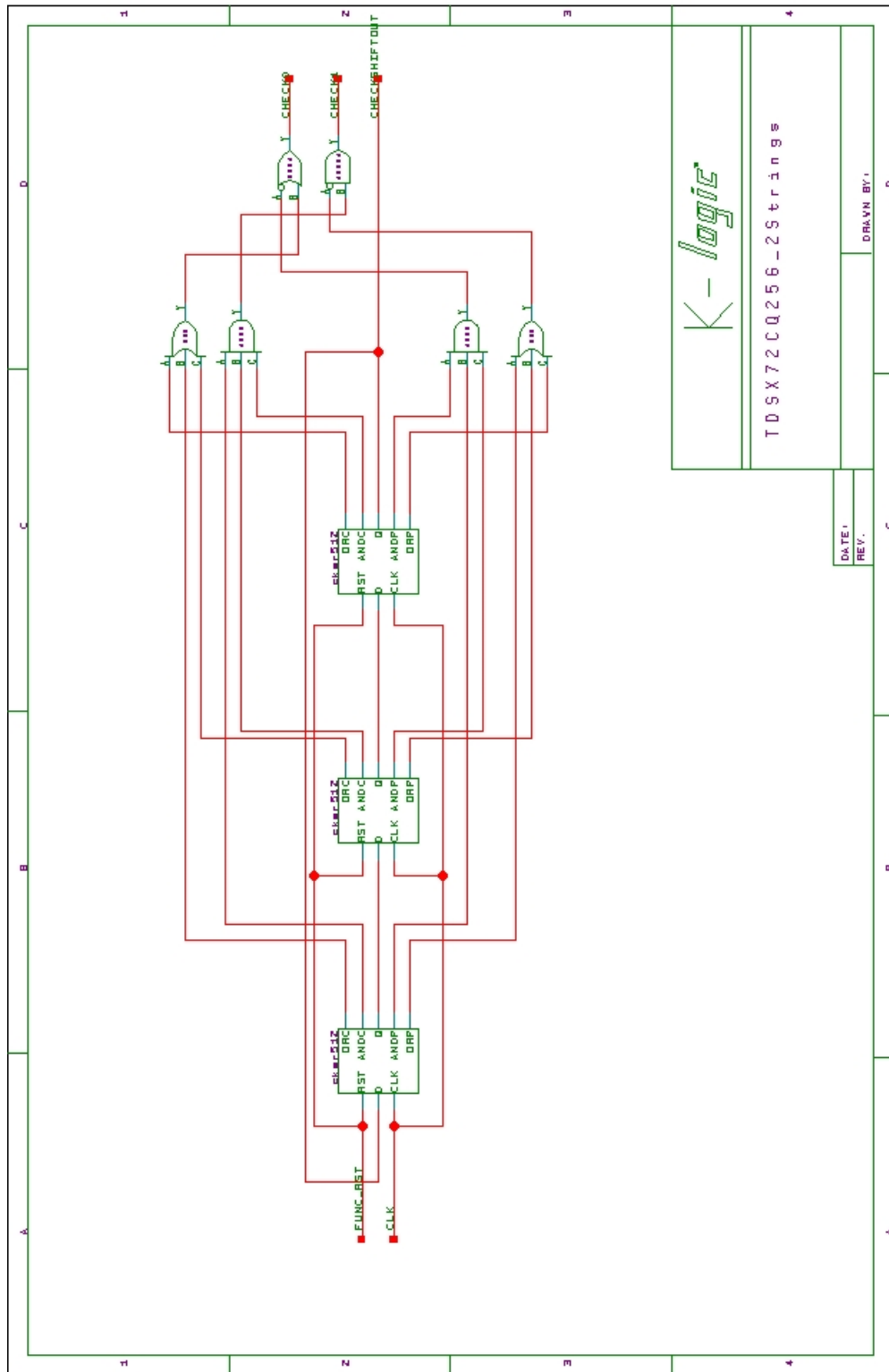
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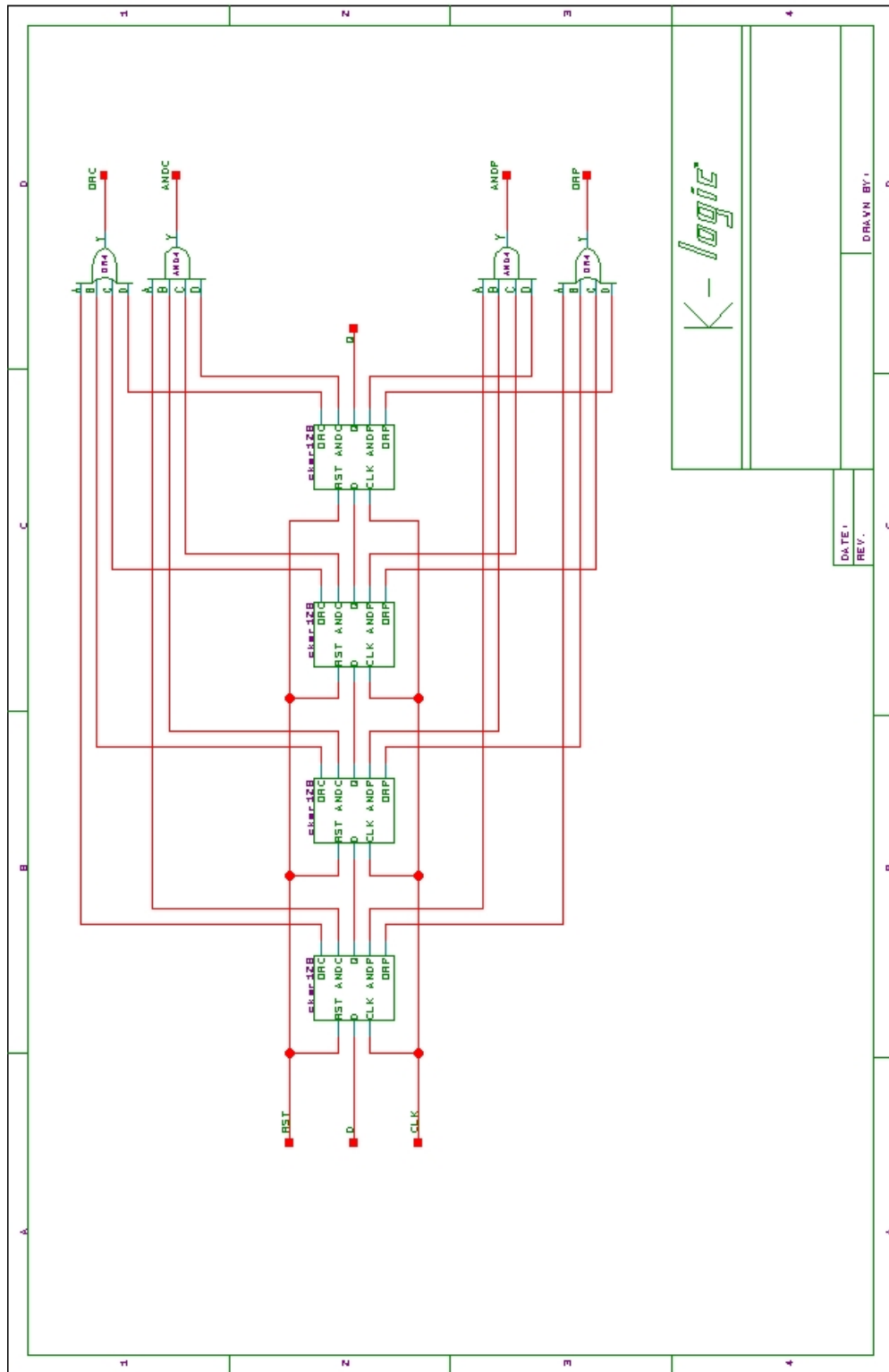


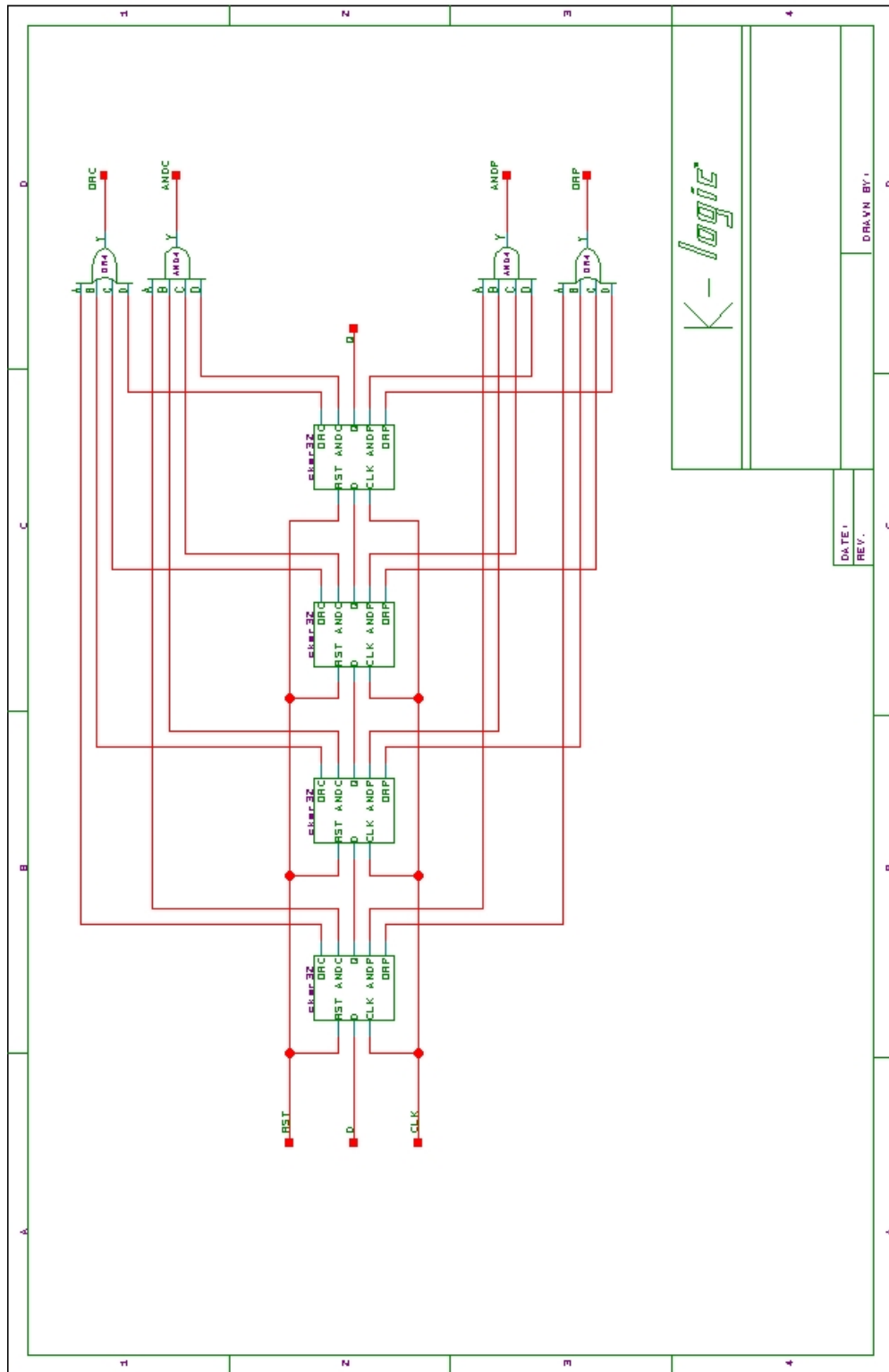
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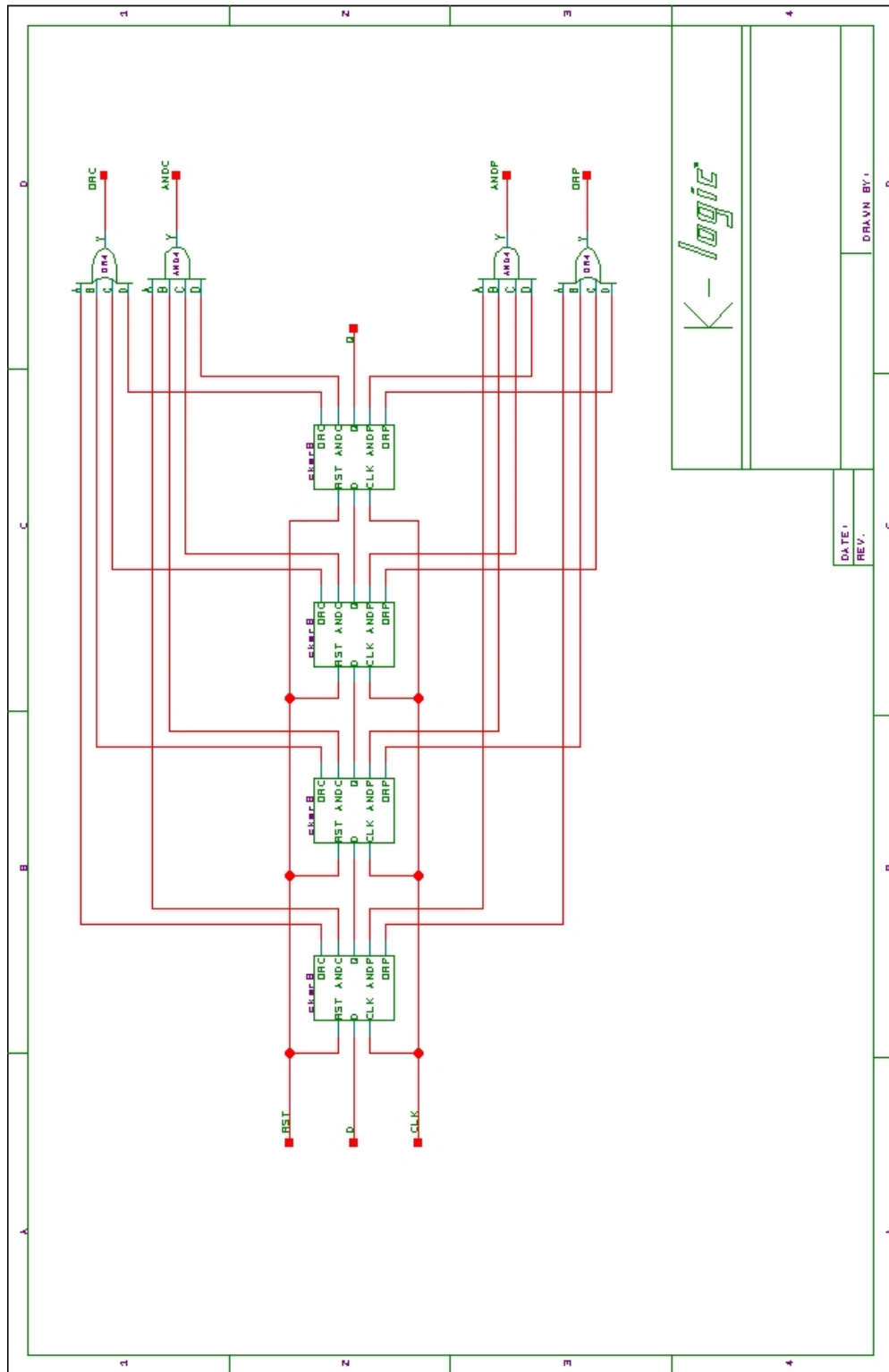
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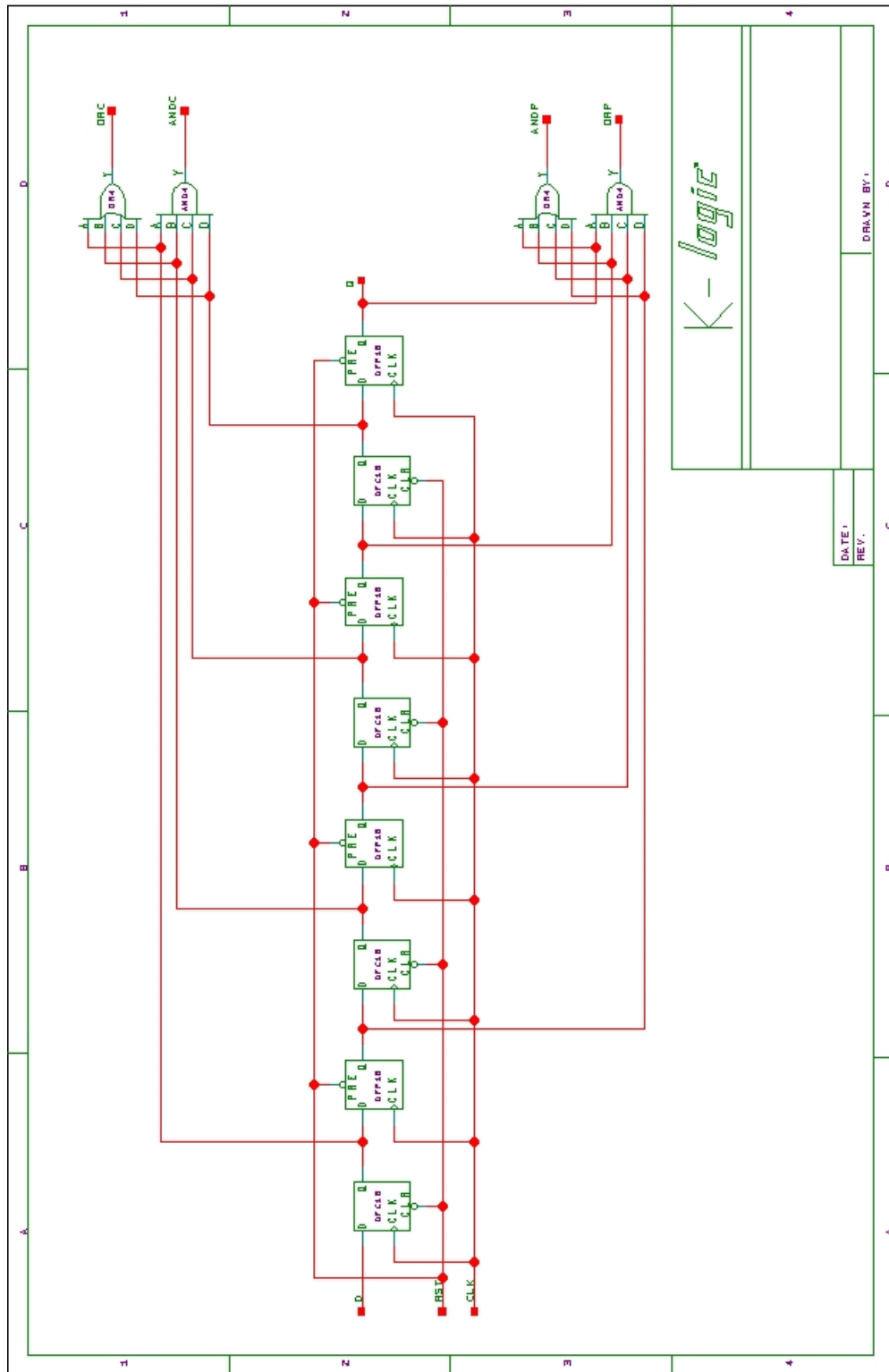
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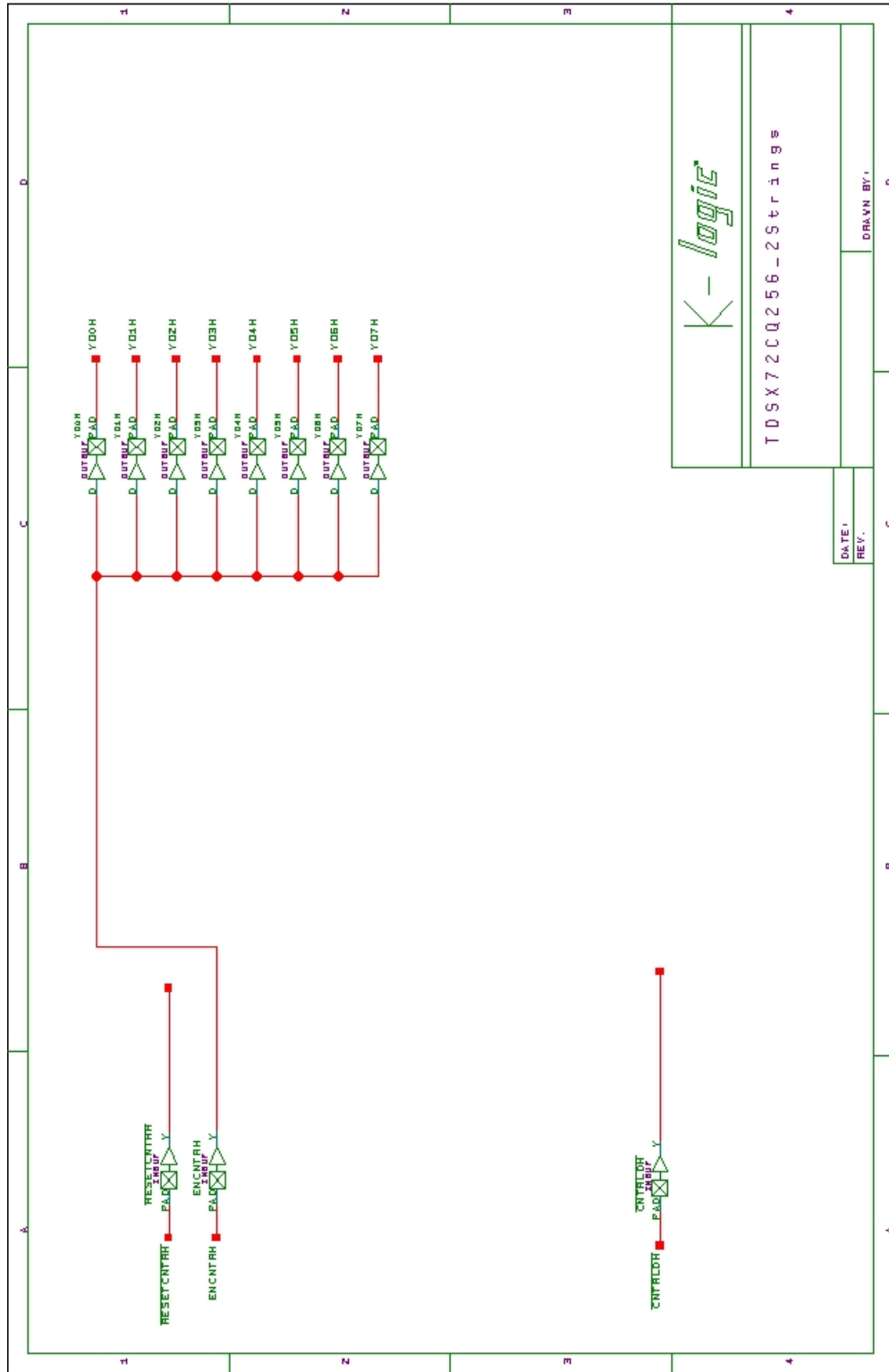
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K-logic

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