TOTAL IONIZING DOSE TEST REPORT

No. 01T-RT1280A-U1H611
March 19, 2001

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I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	63krad(Si) static case
2. $I_{DDSTDBY}$	Passed 7.6krad(Si)
3. V_{IL}/V_{IH}	Passed 7.6krad(Si)
4. V_{OL}/V_{OH}	Passed 7.6krad(Si)
5. Propagation Delays	Passed 7.6krad(Si)
6. Rising/Falling Edge Transient	Passed 7.6krad(Si)
7. Power-up Transient Current	Passed 7.6krad(Si)

Note: This test was performed in NASA/Goddard radiation facility following their radiation guidelines.

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT1280A
Package	CQFP172
Foundry	MEC
Technology	1.0µm CMOS
Die Lot Number	U1H611
Quantity Tested	6
Serial Numbers	LAN4701, LAN4702, LAN4703, LAN4704, LAN4705, LAN4706

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	6-9krad(Si)/hr (+/-10%)
Data Mode	Static
Temperature	Room
Bias	5.0V

C. Test Method

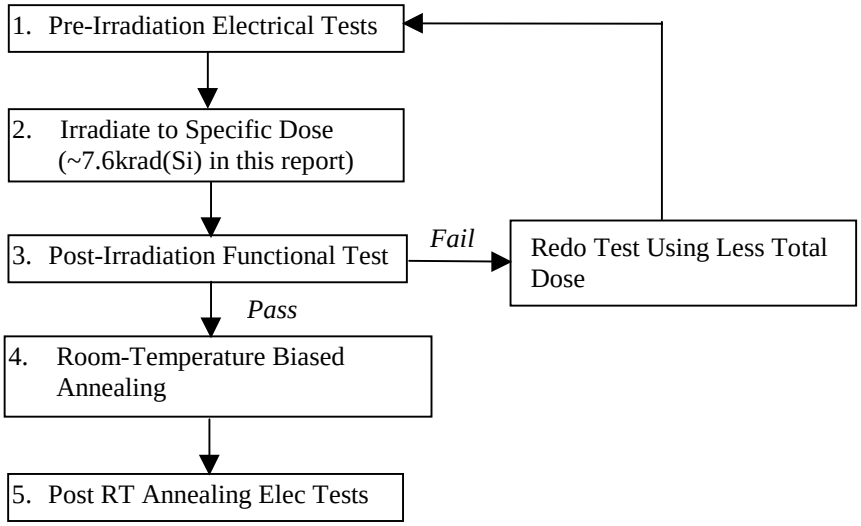

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019.5. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, this bench setup has much less noise but only sample few pins (due to logistics, not inability). However, usually $I_{DDstandby}$ determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation, which is impractical for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured accurately on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. Test Results

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced static I_{CC} versus total dose for DUT LAN4701 and LAN4702. During irradiation, the DUT was at static. In-situ functional failure was detected by clocking out the data and comparing them with the truth table. The earliest failure occurred at ~63krad(Si) (LAN4701). As reported earlier (see Report No. 00T-RT54SX16-T6HP12D), the sudden surge of I_{CC} at functional failure only occurs in static case.

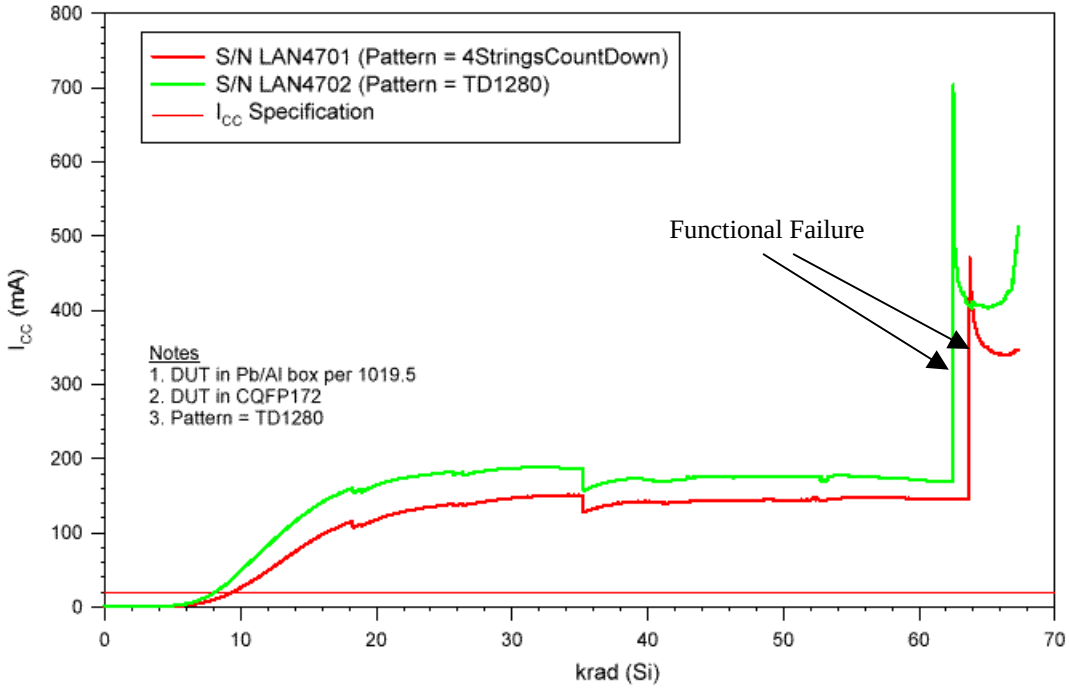

Figure 2. Radiation-induced I_{CC} (Delta I_{CC}) versus total dose for two DUT (LAN4701 and LAN4702).

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post room temperature annealing test (step 5). The room temperature annealing was performed. The DUT used for this test are LAN4703, LAN4704, LAN4705 and LAN4706.

1) Functional Test

Table 4 lists results of the functional test results.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Annealing
LAN4703	passed	passed
LAN4704	passed	passed
LAN4705	passed	passed
LAN4706	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

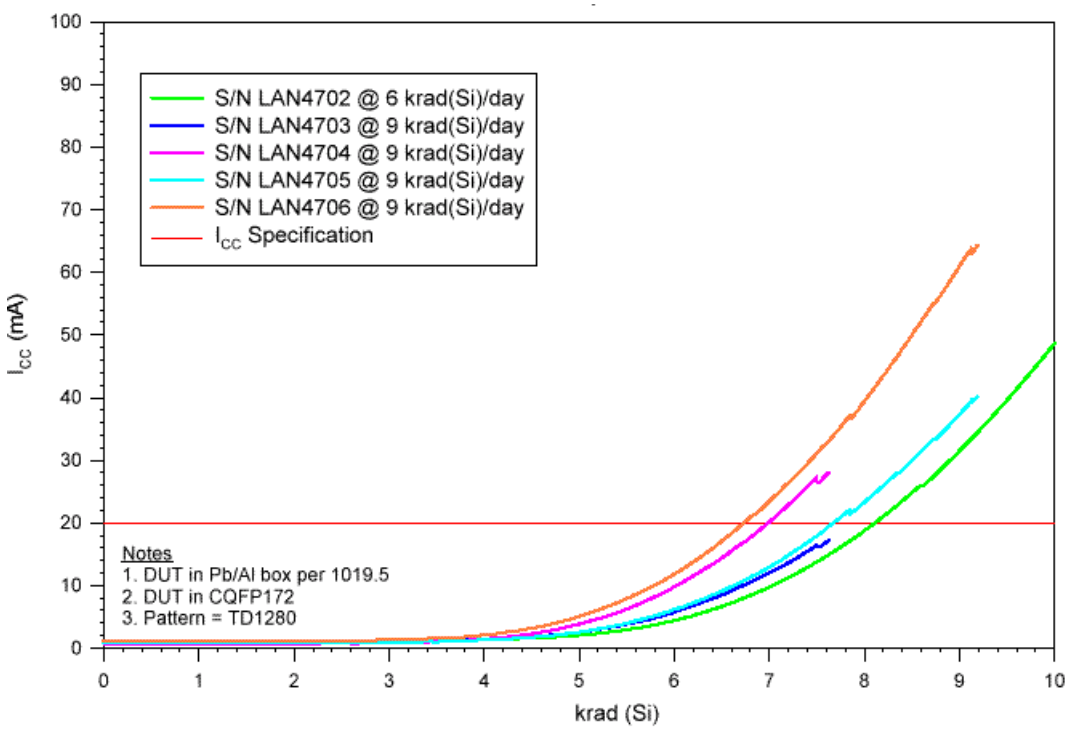

Figure 3. Radiation-induced Delta $I_{DDstandby}$ (I_{CC}) versus total dose for LAN4703, LAN4704, LAN4705 and LAN4706, in-situ monitoring.

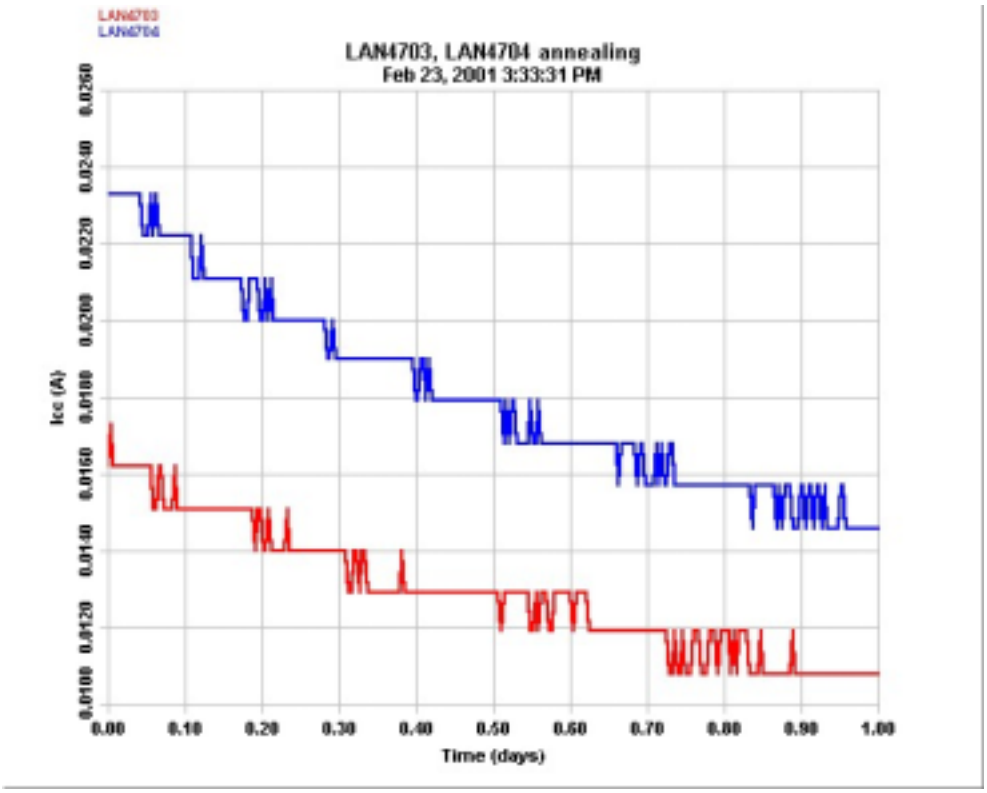

Figure 4. Post-irradiation room temperature biased annealing effects on I_{DDSTDY} of LAN4703 and LAN4704.

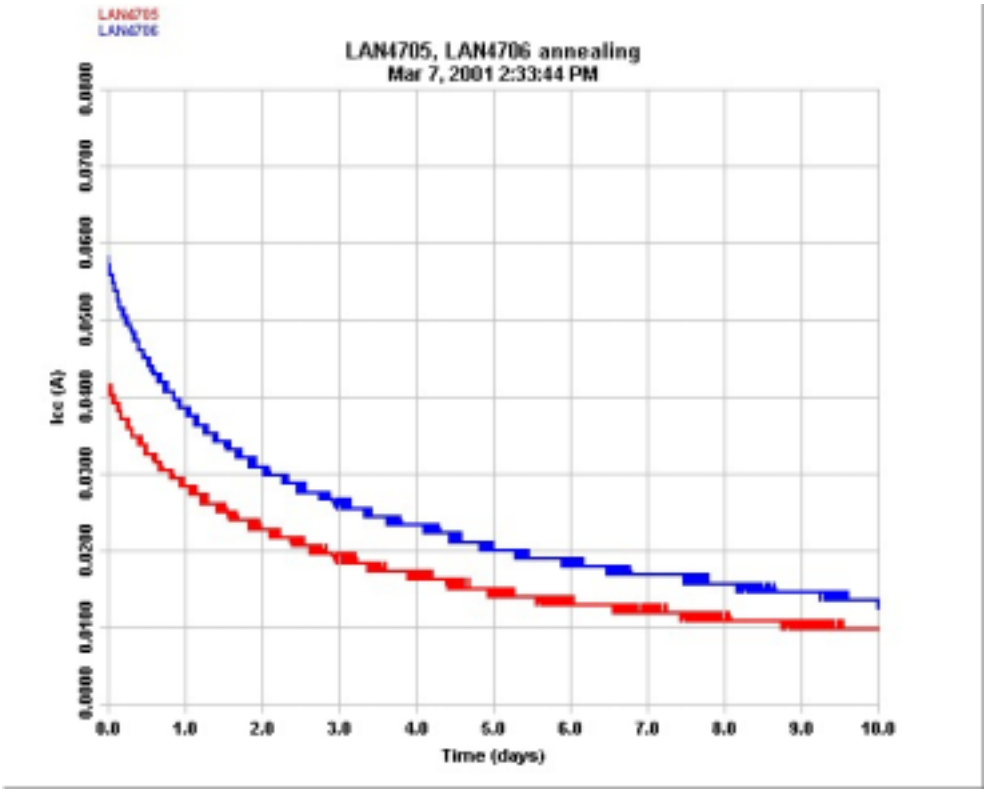

Figure 5. Post-irradiation room temperature biased annealing effects on I_{DDSTDY} of LAN4705 and LAN4706.

LAN4703 and LAN4704 were irradiated to 7.6krad(Si), and LAN4705 and LAN4706 were irradiated to 9krad(Si). As shown in Figure 3, only LAN4703 passed the I_{DDSTDY} specification right after irradiation. So room temperature biased annealing were performed to recover this spec. Figure 4 shows that 1-day annealing is enough for LAN4703 and LAN4704. Figure 5 shows that after 10-days annealing, LAN4705 and LAN4706 passed spec.

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing. The post-annealed DUT are within the spec and the change of this parameter for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Annealing
LAN4703	1.33	1.30
LAN4704	1.34	1.31
LAN4705	1.35	1.30
LAN4706	1.37	1.31

4) Output Characteristic

Figure 6a and 6b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUT. All irradiated DUT are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 6mA, V_{OL} cannot exceed 0.4V.

Figure 7a and 7b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUT. All DUT pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 4mA, V_{OH} cannot be lower than 3.7V.

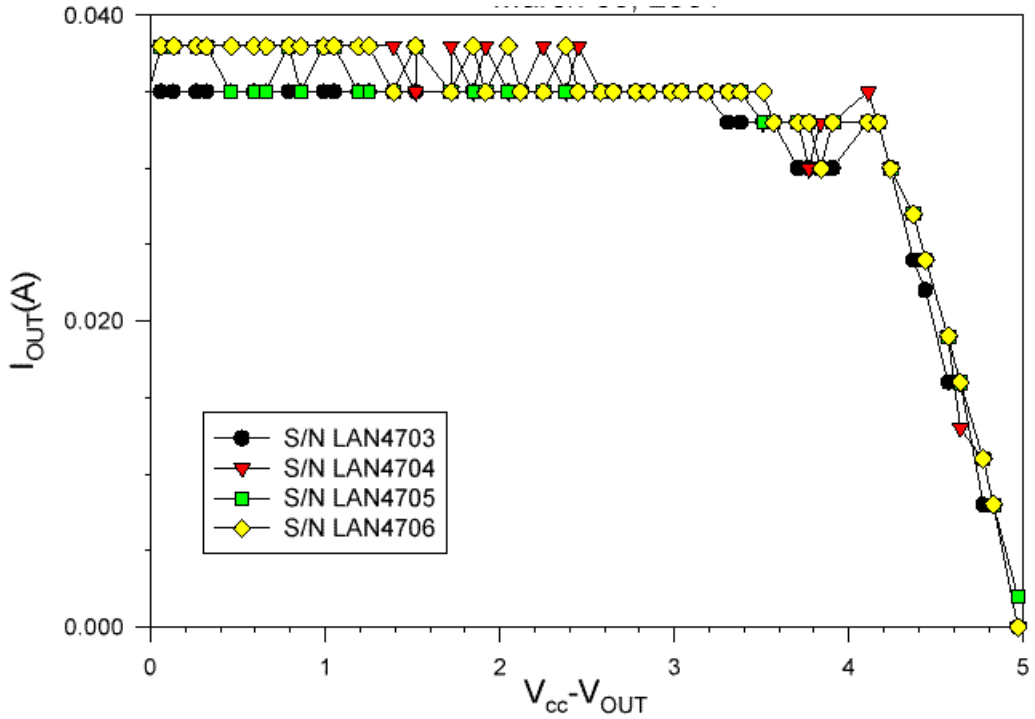

Figure 6a. Pre-irradiation V_{OL} characteristic curves.

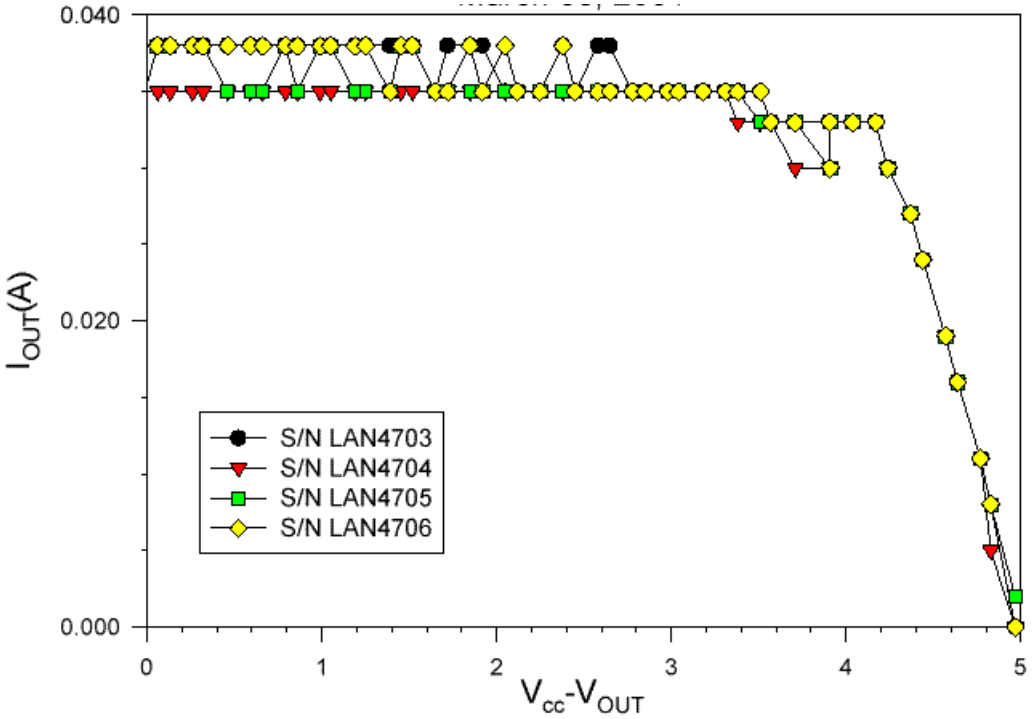

Figure 6b. Post-annealing V_{OL} characteristic curves.

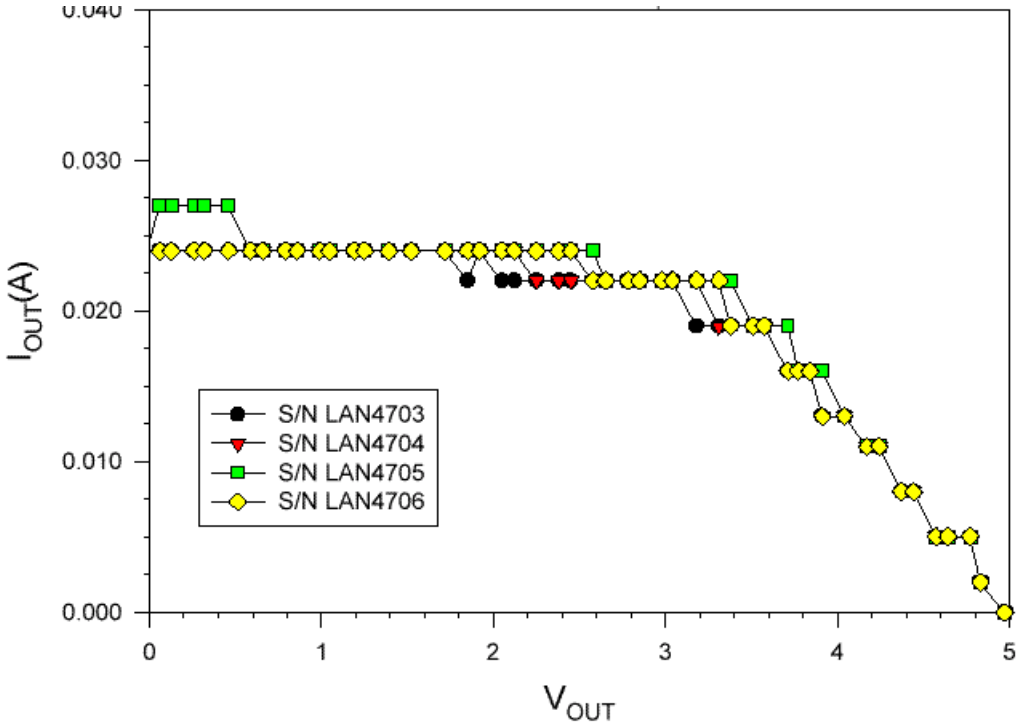

Figure 7a. Pre-irradiation V_{OH} characteristic curves.

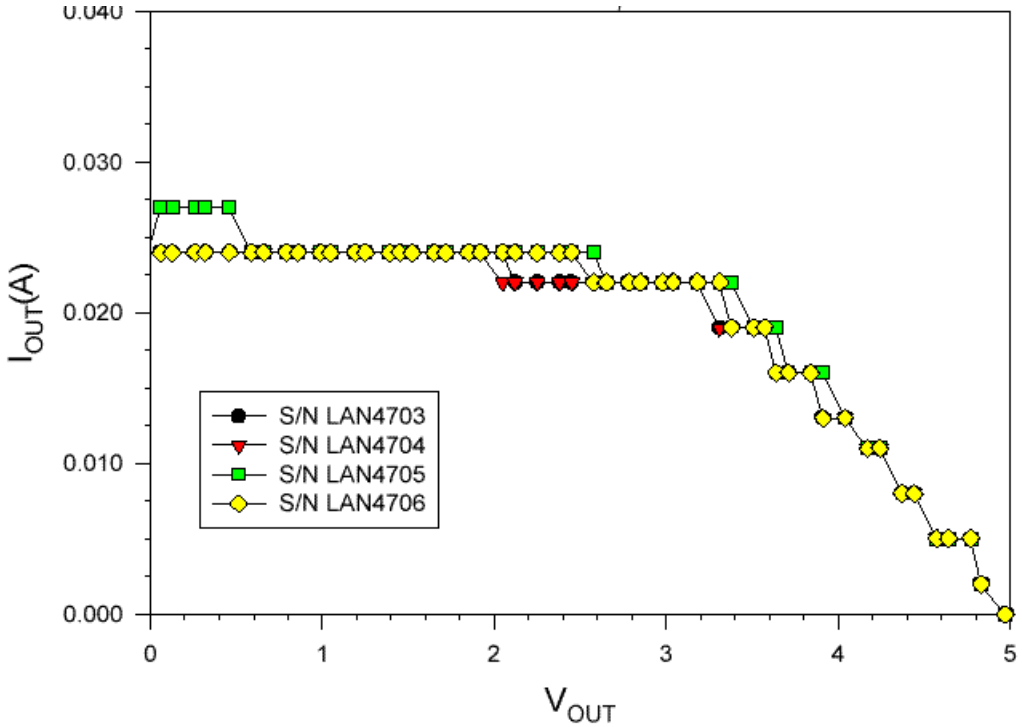

Figure 7b. Post-annealing V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on a combinatorial path. Both the rising edge and falling edge were measured. Table 6 lists the results. The delta due to radiation effect is within the noise. Some post-annealing delays are less than their pre-irradiation counterparts.

Table 6. Propagation Delays of Combinatorial Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4703	1232	1228	1224	1207
LAN4704	1214	1211	1206	1190
LAN4705	1220	1216	1214	1197
LAN4706	1220	1224	1212	1199

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 8-11 show the rising edge transient. Figures 12-15 show the falling edge transient. The radiation effect is basically negligible.

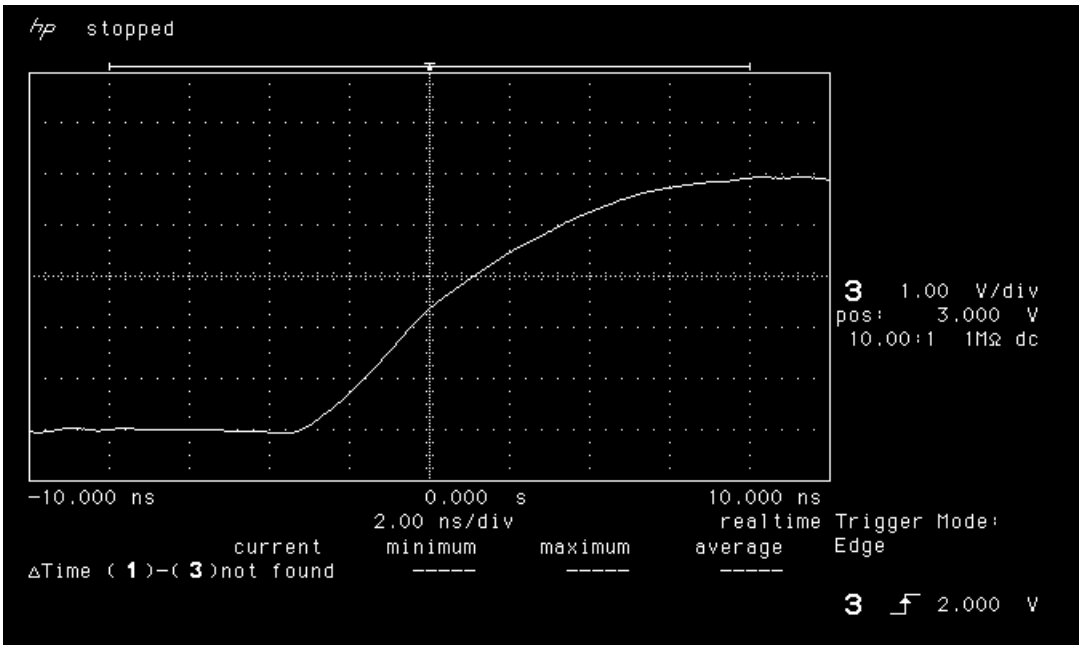

Figure 8a. Rising edge of LAN4703 pre-irradiation.

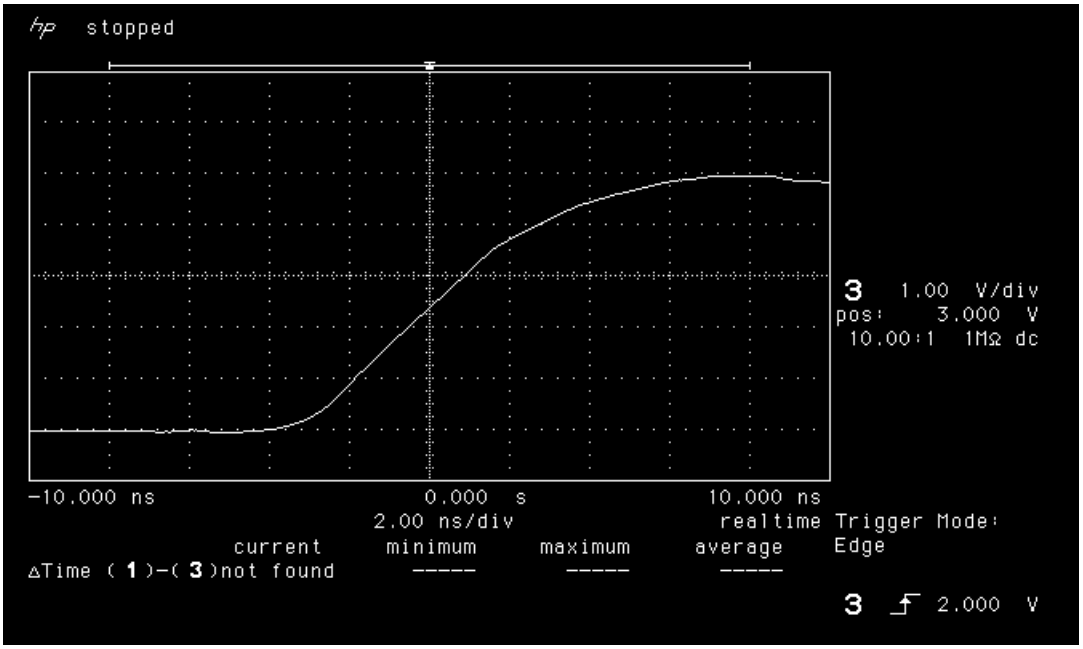

Figure 8b. Rising edge of LAN4703 post-annealing.

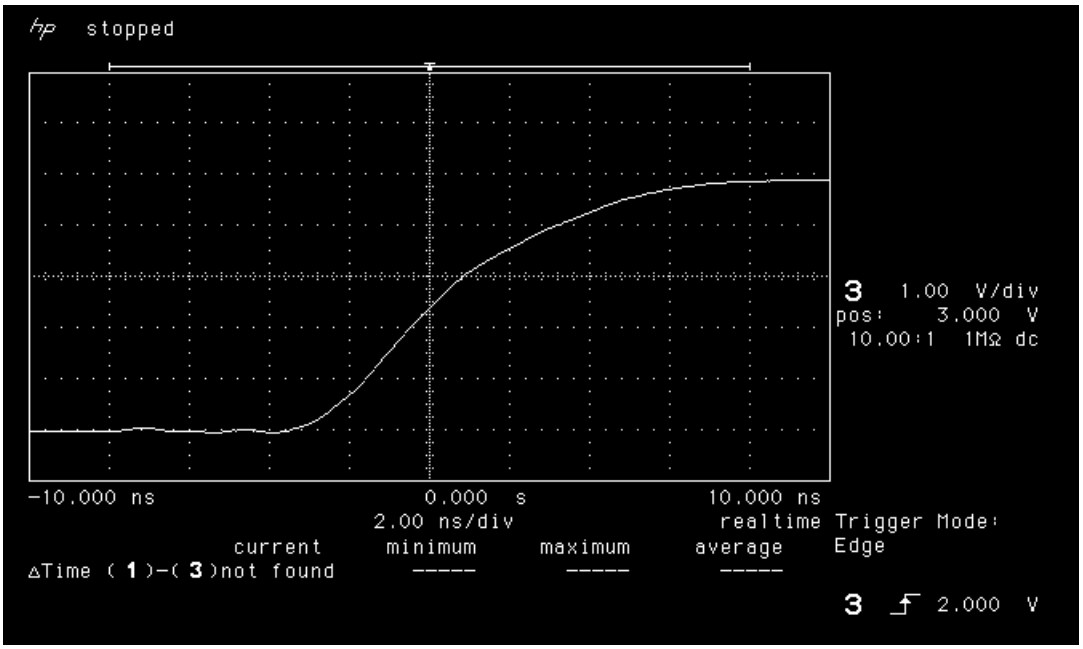

Figure 9a. Rising edge of LAN4704 pre-irradiation.

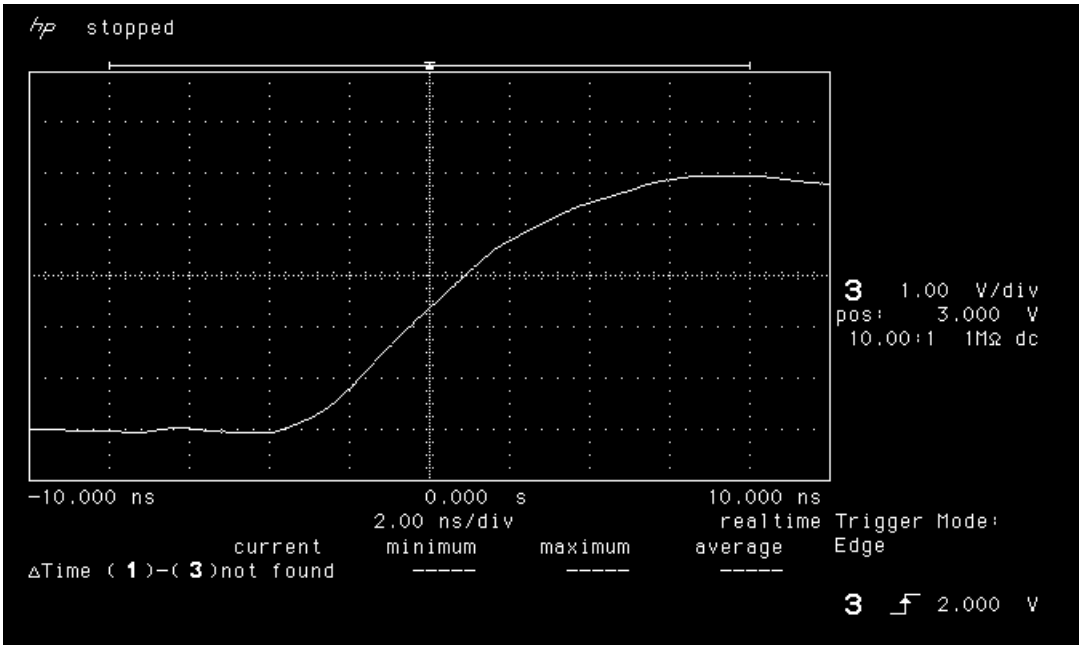

Figure 9b. Rising edge of LAN4704 post-annealing.

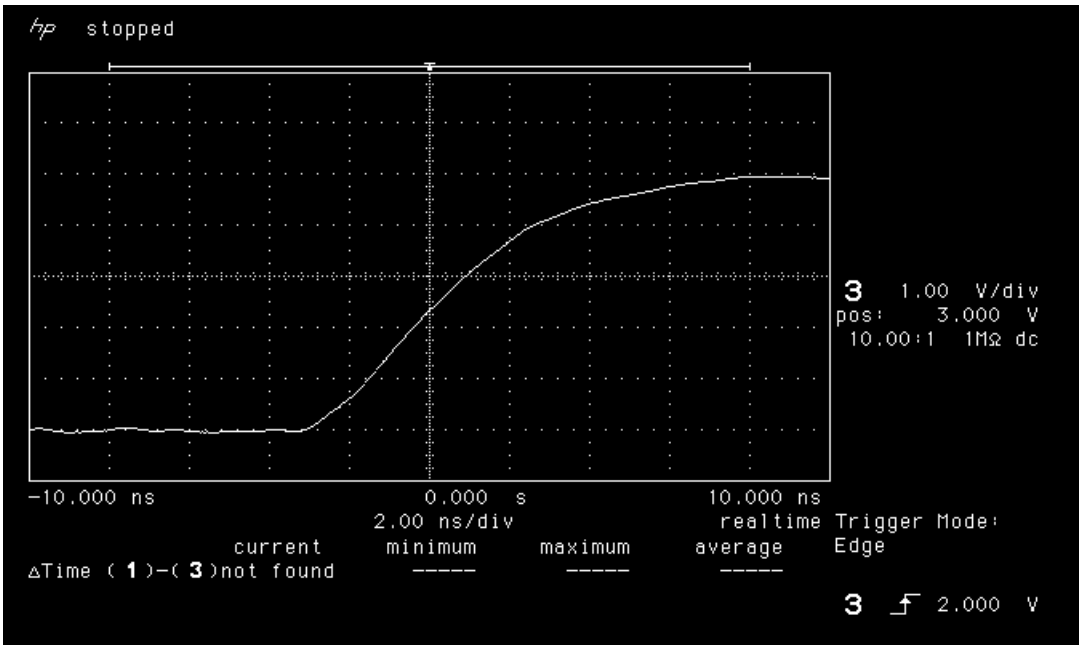

Figure 10a. Rising edge of LAN4705 pre-irradiation.

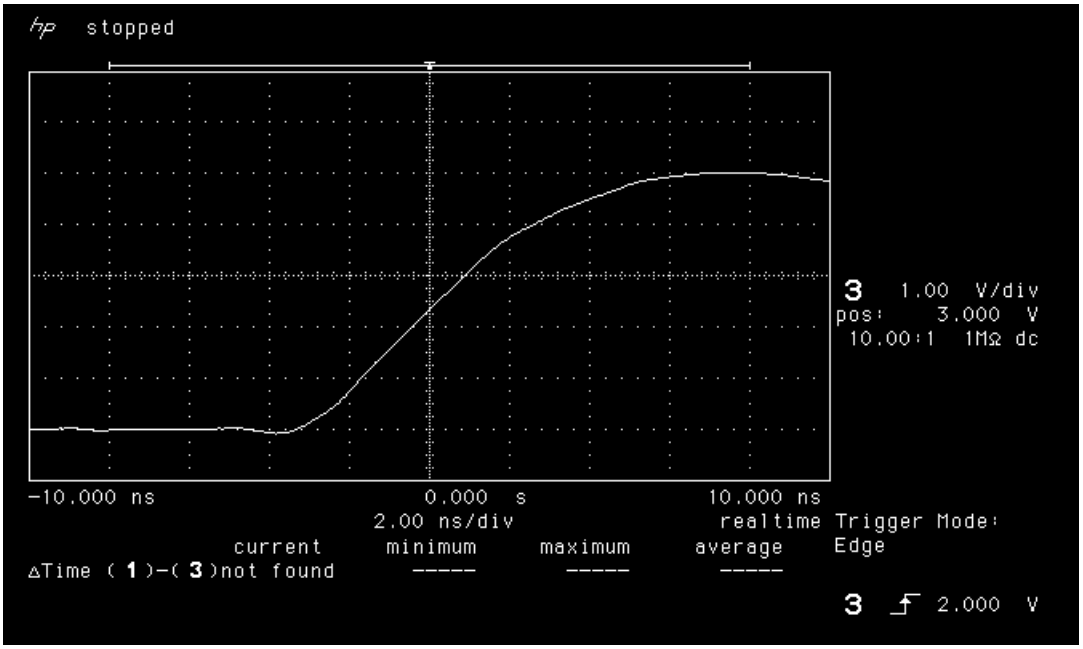

Figure 10b. Rising edge of LAN4705 post-annealing.

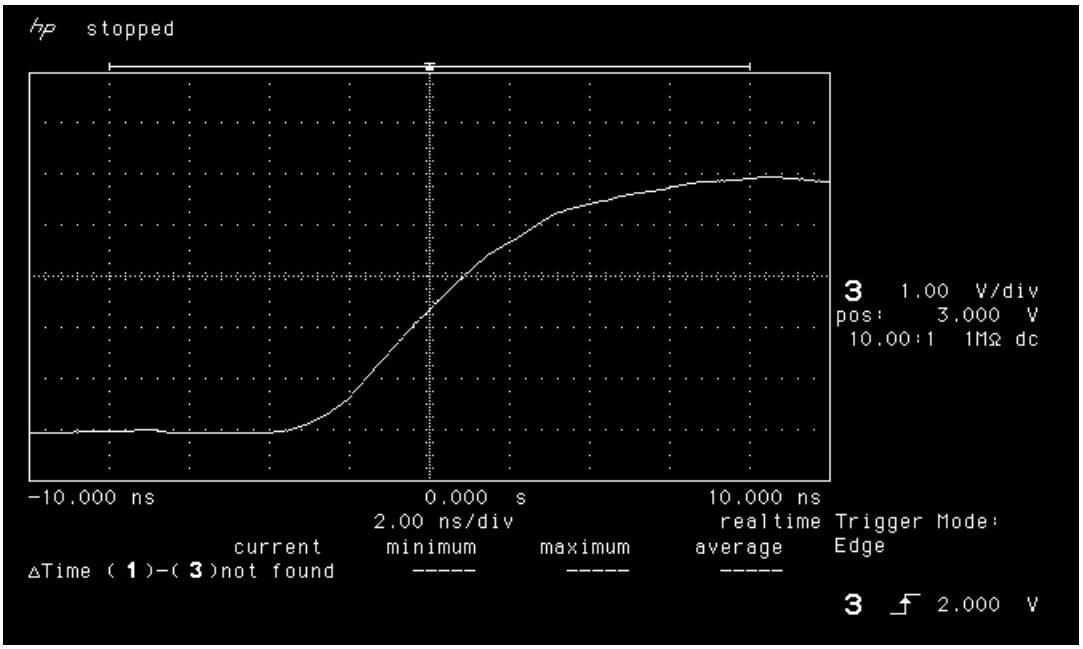

Figure 11a. Rising edge of LAN4706 pre-irradiation.

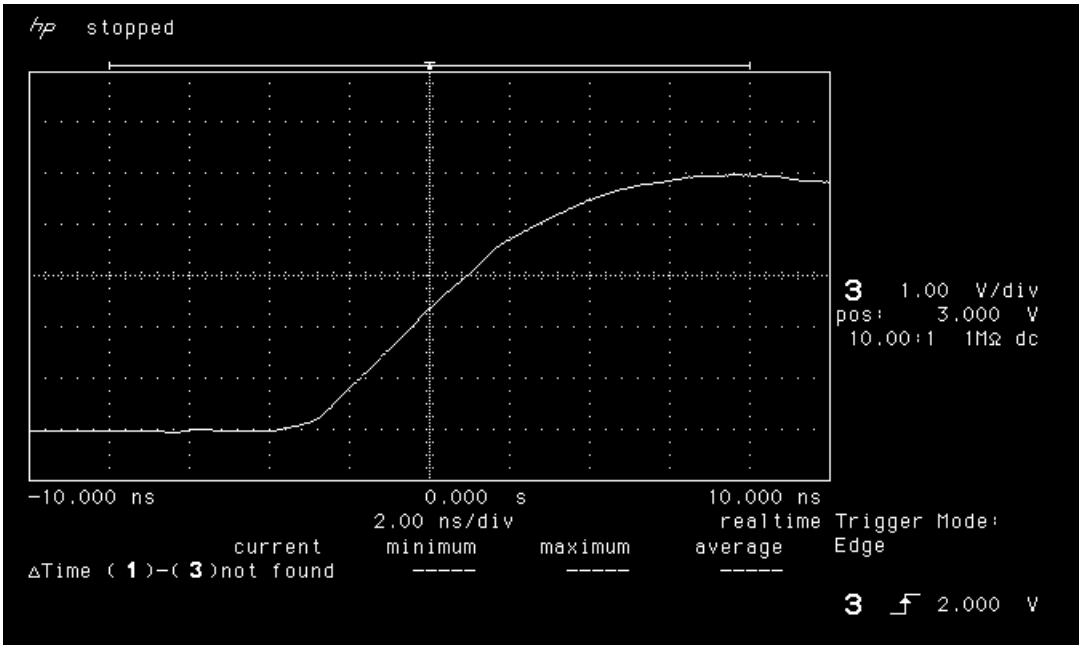

Figure 11b. Rising edge of LAN4706 post-annealing

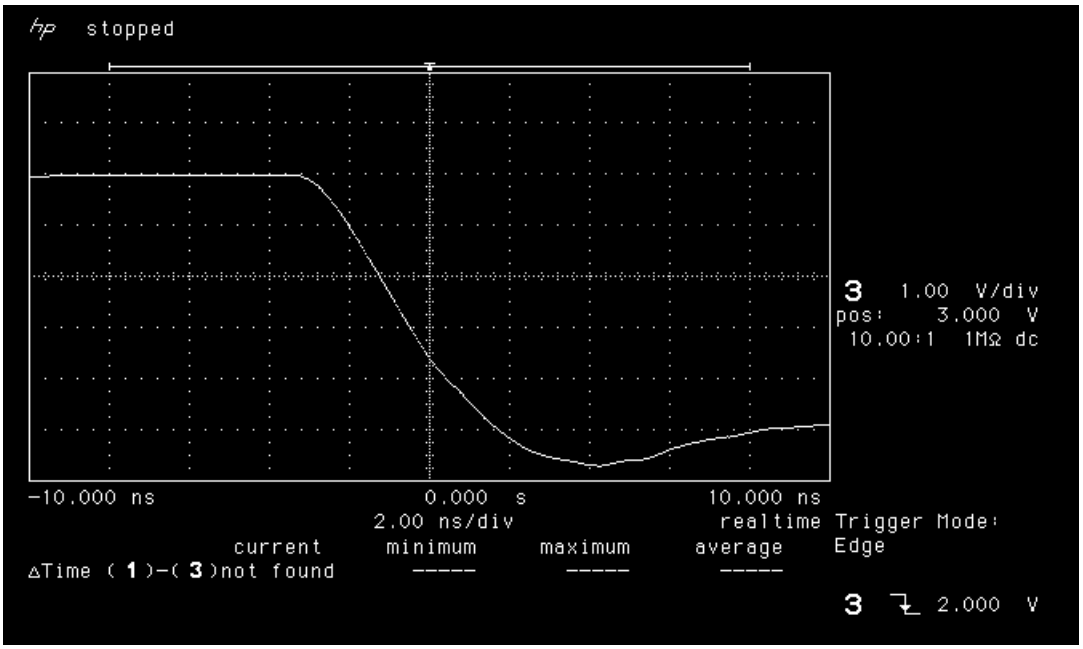

Figure 12a. Falling edge of LAN4703 pre-irradiation

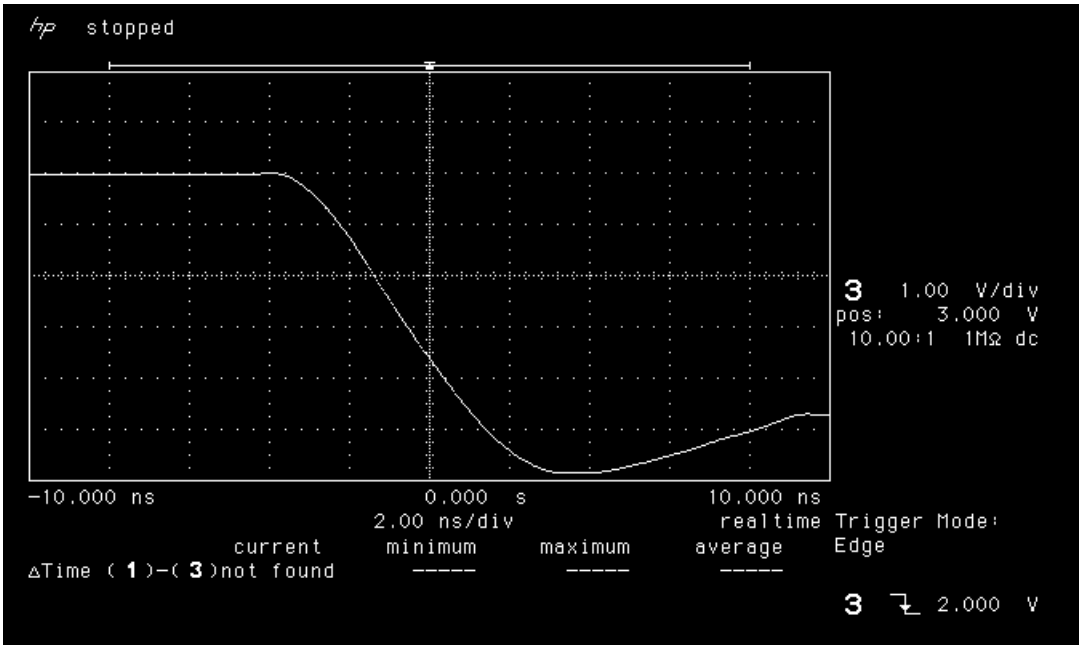

Figure 12b. Falling edge of LAN4703 post-annealing.

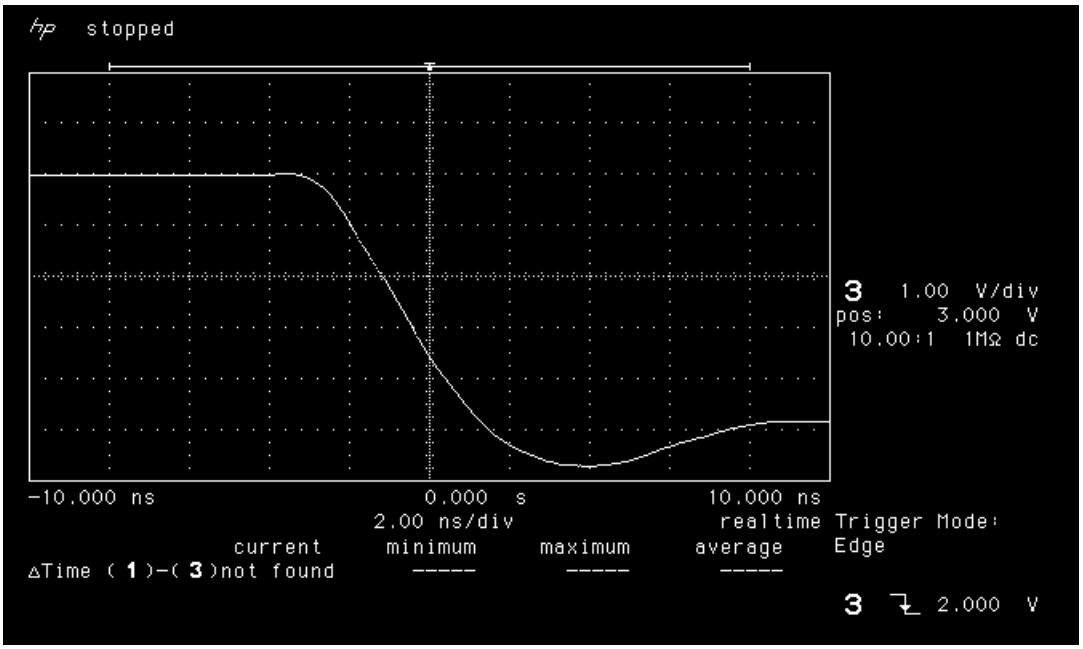

Figure 13a. Falling edge of LAN4704 pre-irradiation.

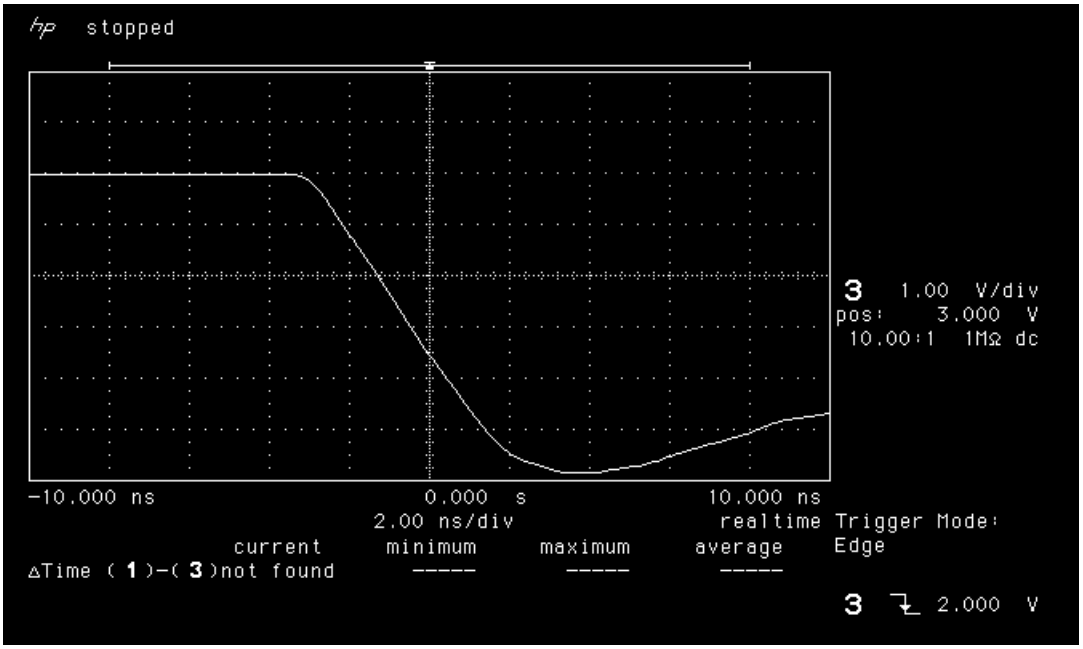

Figure 13b. Falling edge of LAN4704 post-annealing.

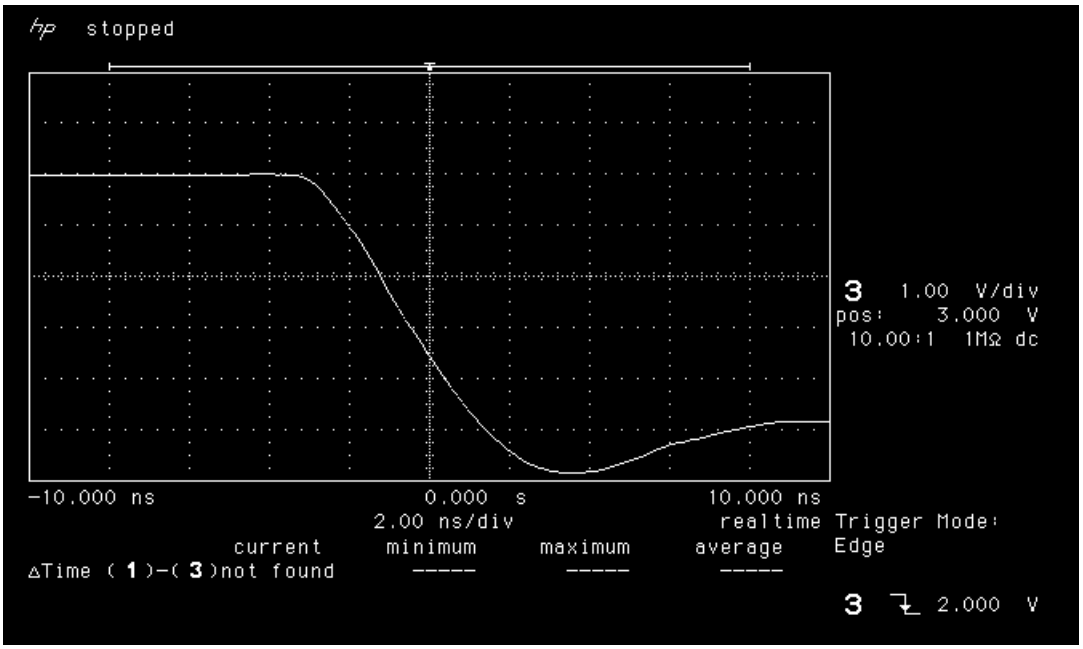

Figure 14a. Falling edge of LAN4705 pre-irradiation.

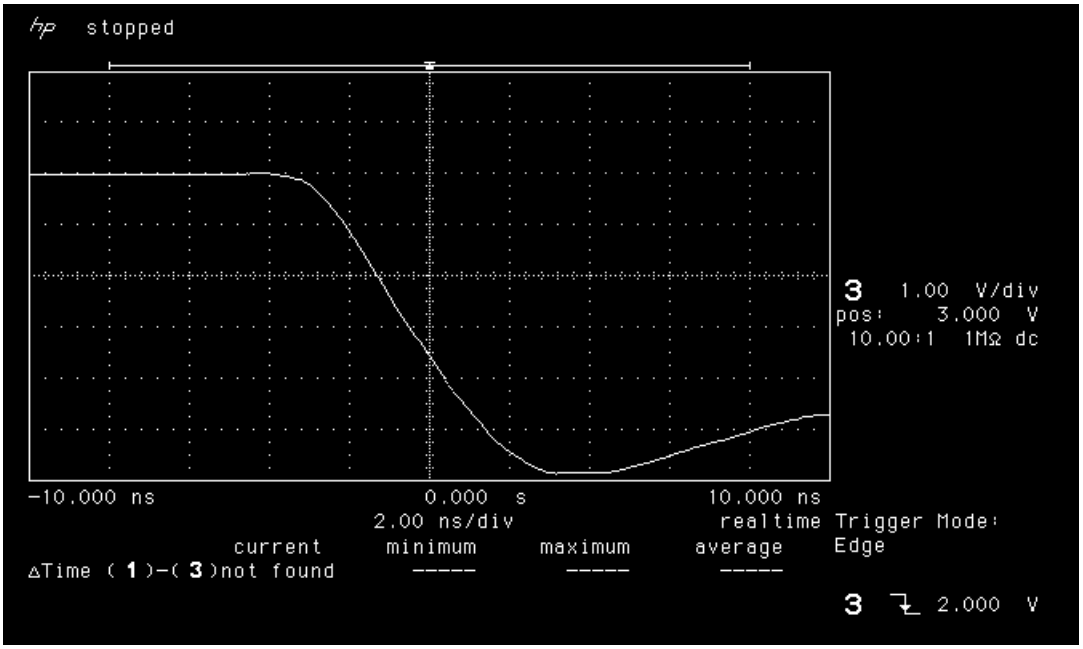

Figure 14b. Falling edge of LAN4705 post-annealing.

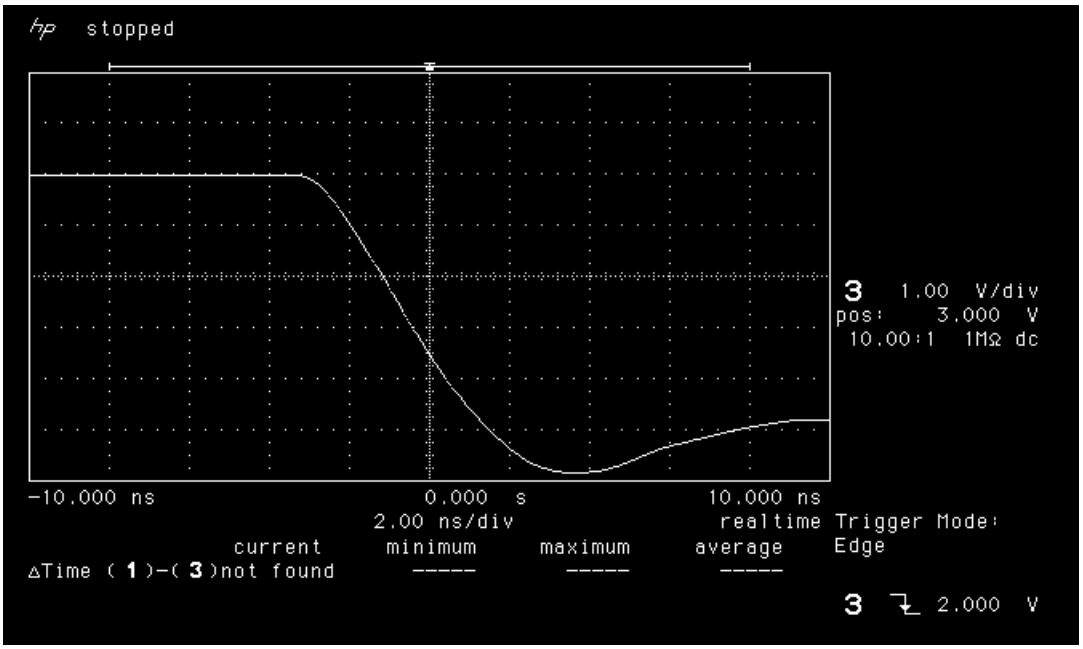

Figure 15a. Falling edge of LAN4706 pre-irradiation

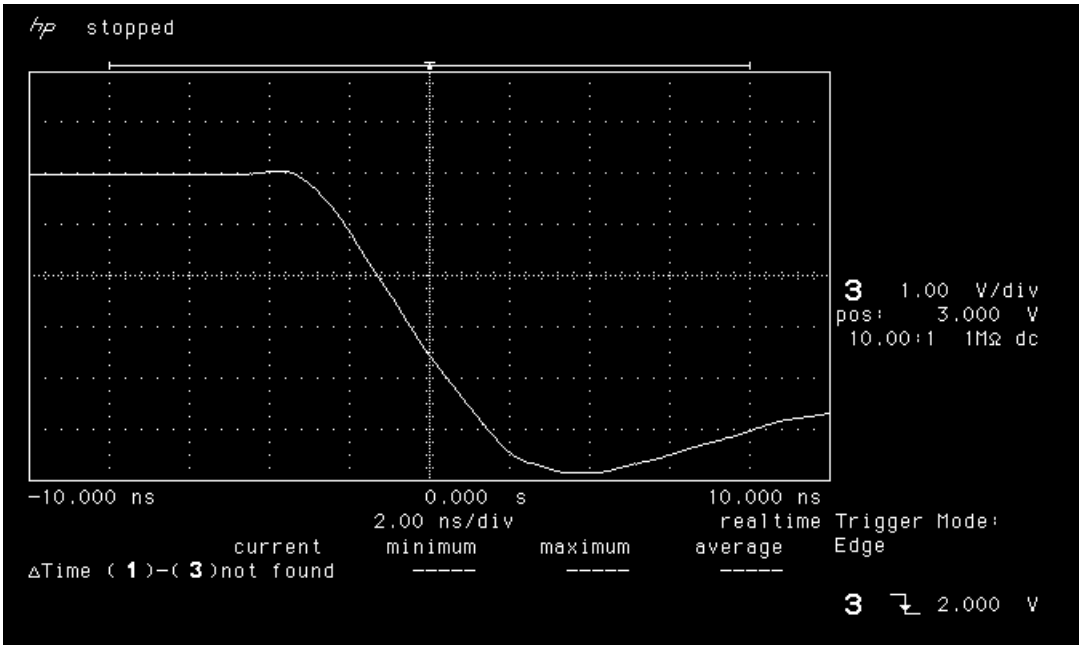

Figure 15b. Falling edge of LAN4706 post-annealing

7) Power-Up Transient

In each measurement, the rise time of the power supply voltage (V_{CC}) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 16-19 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 5.0V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. Post 7.6krad(Si) irradiation/annealing DUT have a radiation-induced transient current during power up (see Figure 16b). However, this transient is due to the relatively high dose rate used in this report. In space, the much lower dose rate will render this a non-issue. The details about power up transient has been previously published at RADECS ("Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278.)

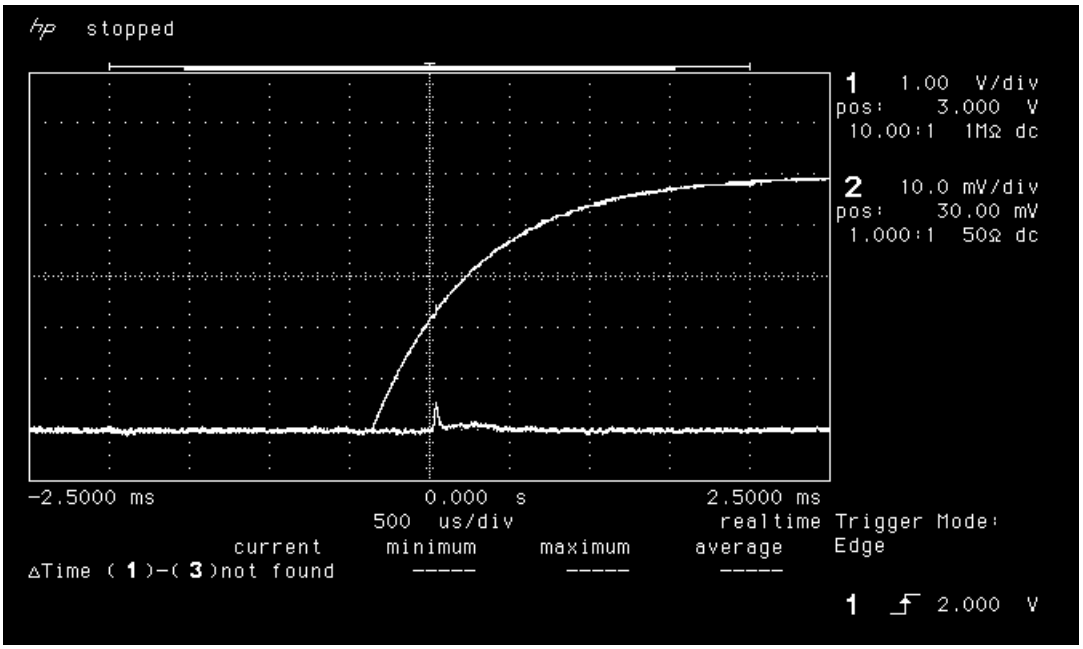

Figure 16a. Power-up transient of LAN4703 pre-irradiation.

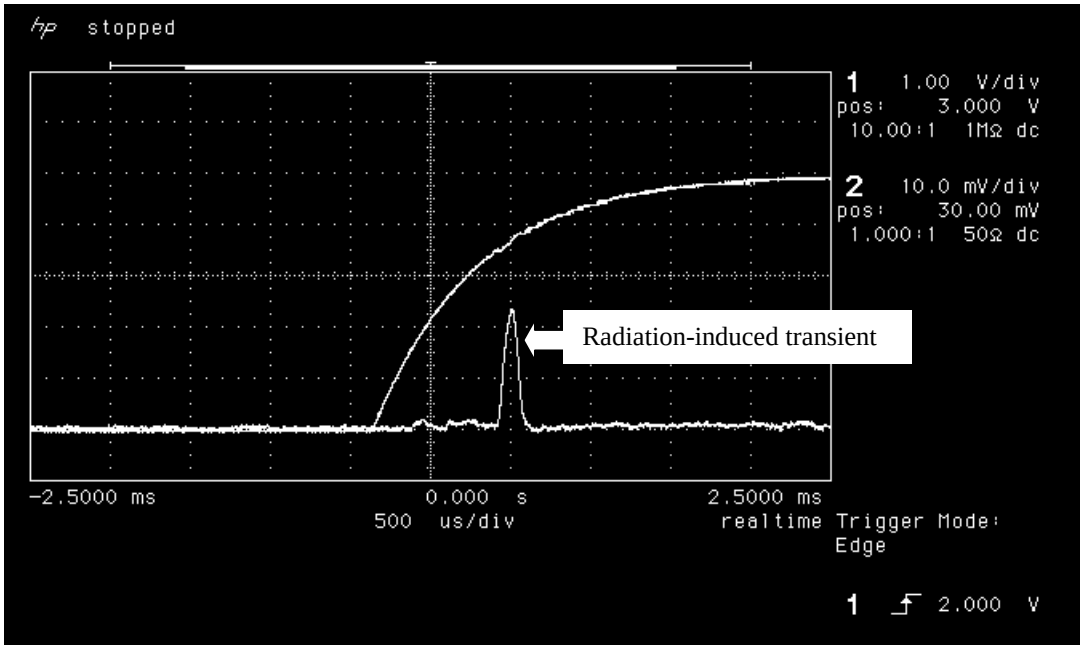

Figure 16b. Power-up transient of LAN4703 post-annealing.

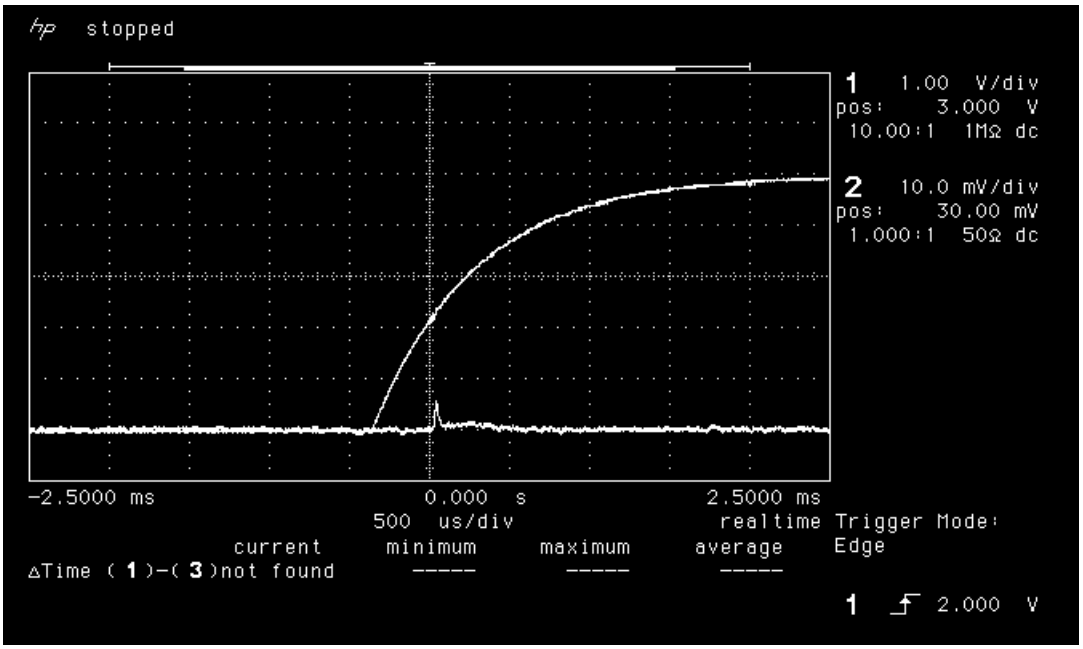

Figure 17a. Power-up transient of LAN4704 pre-irradiation.

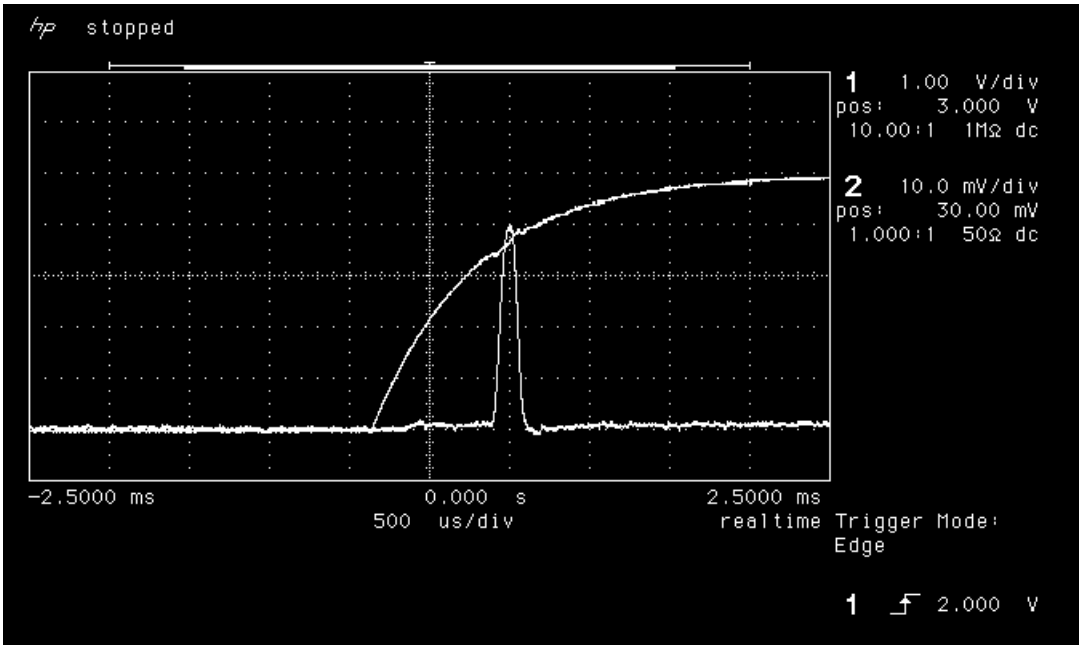

Figure 17b. Power-up transient of LAN4704 post-annealing.

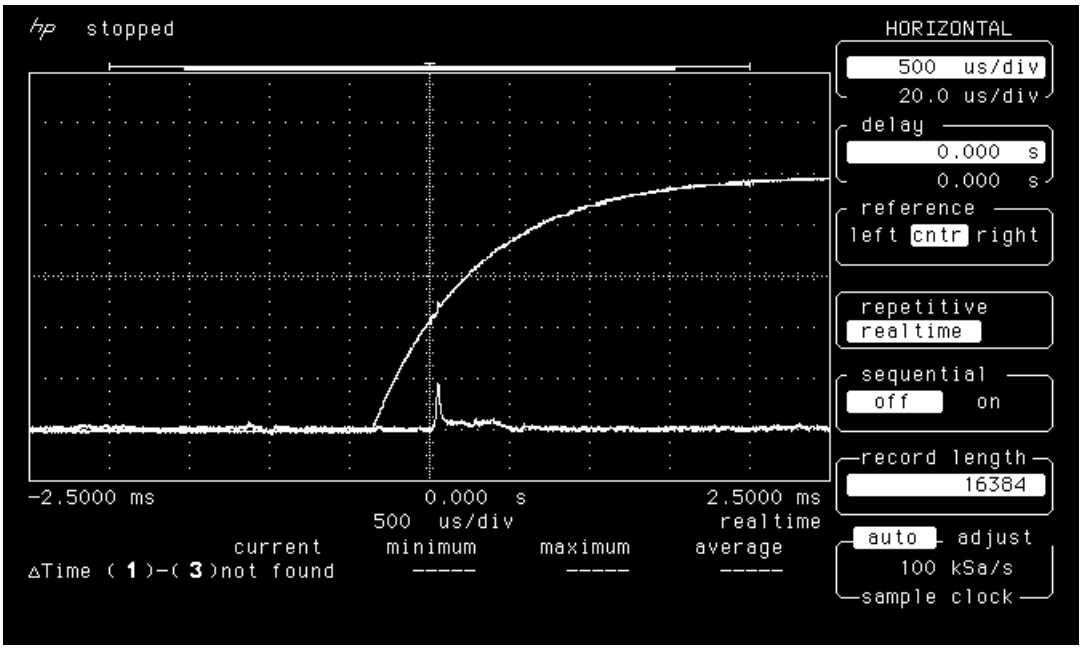

Figure 18a. Power-up transient of LAN4705 pre-irradiation.

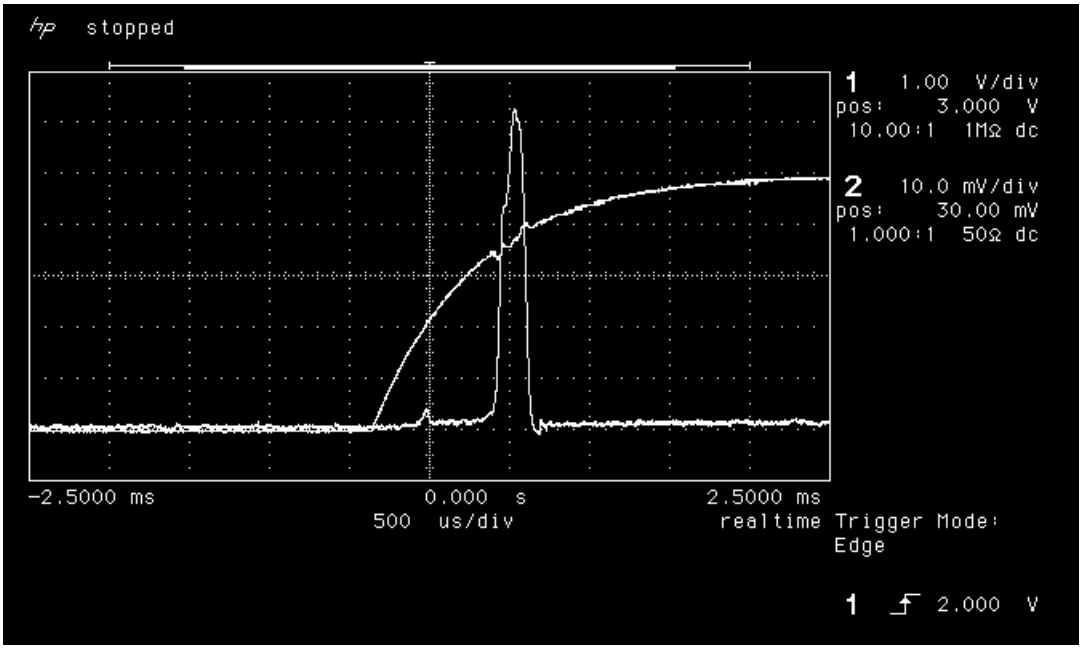

Figure 18b. Power-up transient of LAN4705 post-annealing.

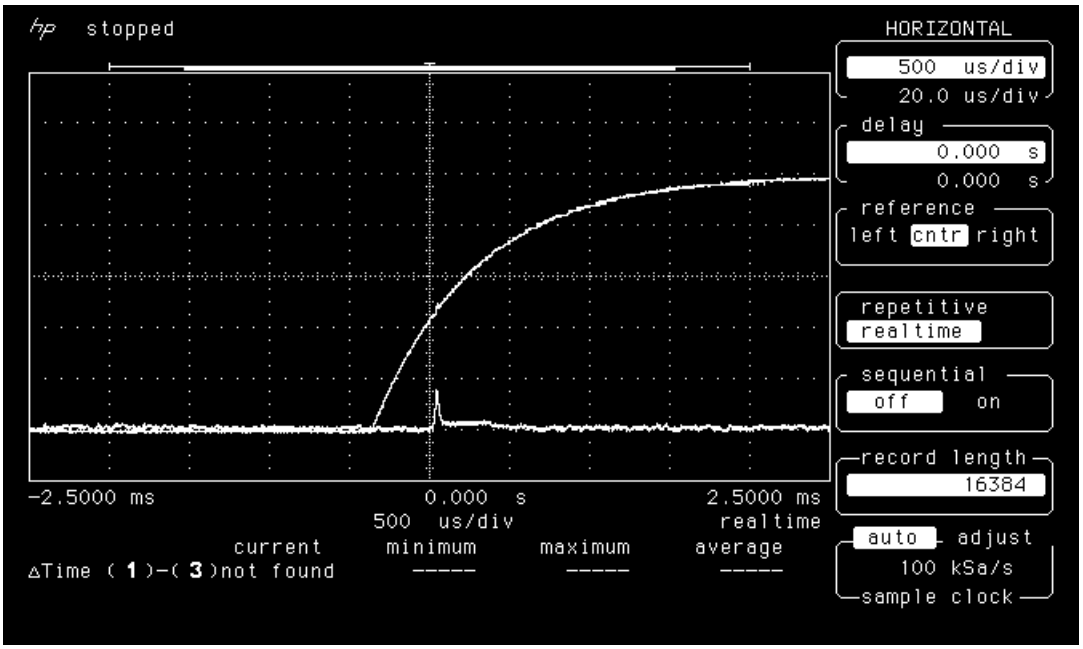

Figure 19a. Power-up transient of LAN4706 pre-irradiation

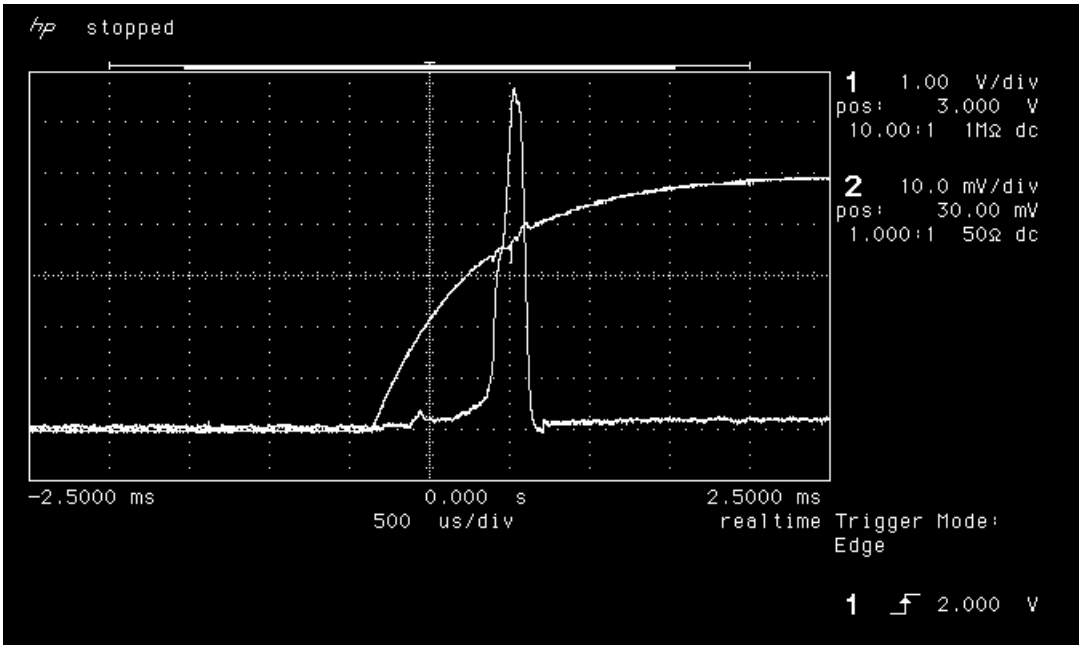

Figure 19b. Power-up transient of LAN4706 post-annealing