# TOTAL IONIZING DOSE TEST REPORT

*No. 01T-RT1280A-U1H609*

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## I. SUMMARY TABLE

| Parameters | Tolerance |
|---|---|
| 1. Gross Functional | 32krad(Si) static biased |
| 2. $I_{CC}$ | Passed 10krad(Si) (based on extrapolation of annealing) |
| 3. $V_{IL}/V_{IH}$ | Passed 10krad(Si) |
| 4. $V_{OL}/V_{OH}$ | Passed 10krad(Si) |
| 5. Propagation Delays | Passed 10krad(Si) |
| 6. Rising/Falling Edge Transient | Passed 10krad(Si) |
| 7. Power-up Transient Current | Passed 10krad(Si) (based on extrapolation of annealing) |

Note: This test was performed in NASA/Goddard radiation facility following their radiation guidelines.

## II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

### A. *Device Under Test (DUT)*

Table 1 lists the DUT information.

Table 1. DUT Information

| Part Number | RT1280A |
|---|---|
| Package | CQFP172 |
| Foundry | MEC |
| Technology | 1.0µm CMOS |
| Die Lot Number | U1H609 |
| Quantity Tested | 6 |
| Serial Numbers | LAN5201, LAN5202, LAN5203, LAN5204, LAN5205, LAN5206 |

### B. *Irradiation*

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

| Facility | NASA/Goddard |
|---|---|
| Radiation Source | Co-60 |
| Dose Rate | 6krad(Si)/hr (+/-10%) |
| Data Mode | Static |
| Temperature | Room |
| Bias | 5.0V |

## *C. Test Method*

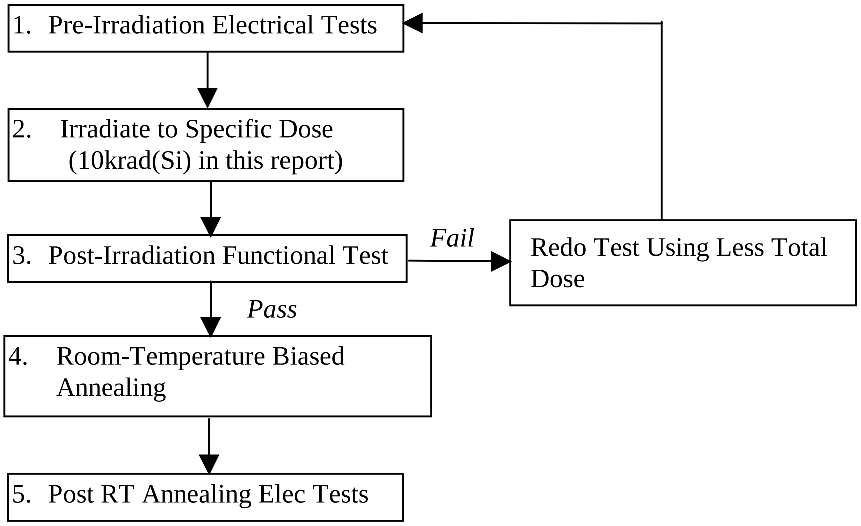


Figure 1. Parametric test flow chart.

We use two methods to evaluate the TID performance. Method one performs irradiation and in-situ gross functional test. The output (in high state) of one sub-design in the DUT is monitored during irradiation. When this output state changed significantly, usually to the other state, we define the functional failure occurred and call the measured total dose as the tolerance for functional failure.

Method two performs irradiation and parametric test. This method is basically following TM1019. Biased room-temperature-annealing is sometimes used to simulate the low-dose-rate space environment. This new annealing methodology is included in TM1019.5, the newest version of TM1019. Figure 1 shows the process flow. Rebound annealing at 100°C for 168hrs is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no adverse rebound effects.

## *D. Electrical Parameter Measurements*

The electrical parameters are measured on the bench. Compared to an automatic tester, the bench setup has much less noise but only sample some pins (due to logistics). However, sampling pins is sufficient because $I_{CC}$ (usually measured in standby mode), a device level parameter, is the first parameter that goes out of the spec limit and determines the radiation tolerance of the device. Applying the $I_{CC}$ spec to determine the tolerance is very conservative because the accelerated dose rate in radiation test causes it to be higher than that in the real space environment. For logistic reason, even applying room temperature annealing, the space dose rate can never be reached. In fact, $I_{CC}$ spec should be relaxed at user's discretion. The total dose induced $I_{CC}$ leakage in this device primarily comes from the effects of the edge and field leakage in NMOS. It is not due to degradation of important properties, such as gate oxide integrity, which will affect the long-term reliability of the device. Table 3 lists the corresponding logic design for each test parameter

Table 3. Logic Design for each Measured Parameter

| Parameter/Characteristics | Logic Design |
|---|---|
| 1. Functionality | All key architectural functions |
| 2. $I_{DDSTDBY}$ | DUT power supply |
| 3. $V_{IL}/V_{IH}$ | TTL compatible input buffer |
| 4. $V_{OL}/V_{OH}$ | TTL compatible output buffer |
| 5. Propagation Delays | String of inverters |
| 6. Rising/Falling Edge | D flip-flop output |
| 7. Power-up Transient Current | DUT power supply |

## III. TEST RESULTS

### *A. Method One: Irradiate to Gross Functional Failure*

DUT LAN5201 and LAN5202 were irradiated to find the total dose tolerance for functional failure. As shown in Figure 2, LAN5201 failed functionally at ~32krad(Si), LAN5202 failed functionally at ~33krad(Si). Use the worst data point, we conclude that the functional failure tolerance in this measurement as 32krad(Si).

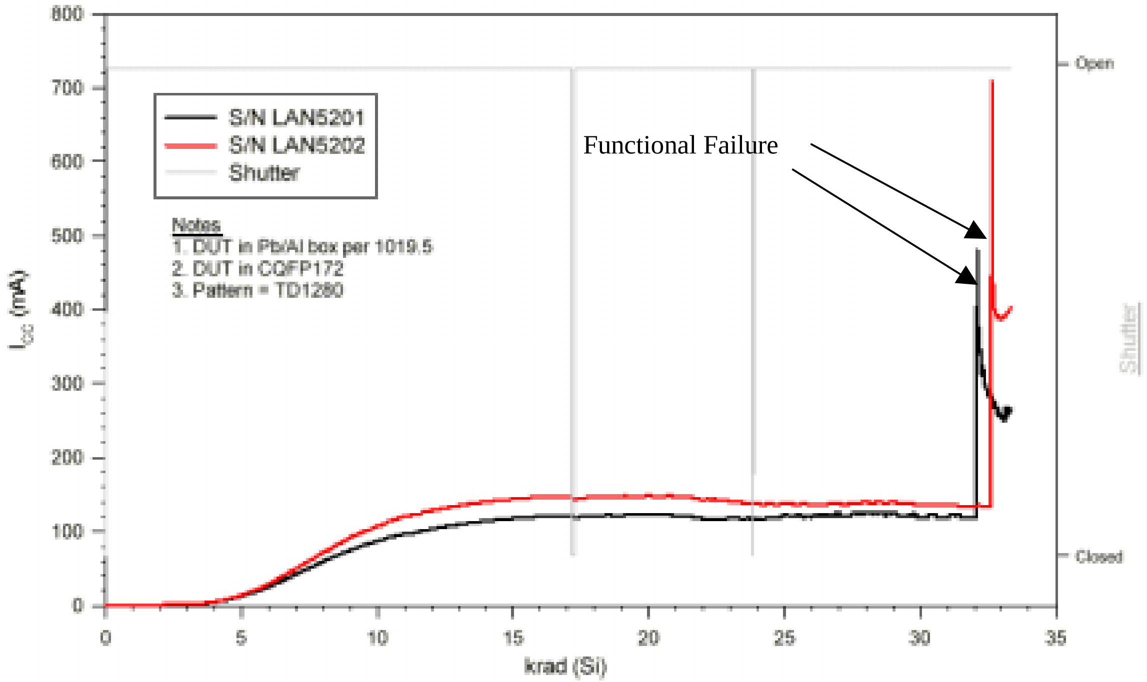


Figure 2. Radiation-induced $I_{CC}$ versus total dose for two DUT (LAN5201 and LAN5202).

### *B. Method Two: Irradiation and Parametric Test*

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post-irradiation-and-annealing (step 5). The DUT used for this test are LAN5203, LAN5204, LAN5205 and LAN5206.

#### *1) Functional Test*

Table 4 lists the gross-functional test results.

Table 4. Functional Test Results

| | Pre-Irradiation | Post-Irrad-and-Anneal |
|---|---|---|
| LAN5203 | passed | passed |
| LAN5204 | passed | passed |
| LAN5205 | passed | passed |
| LAN5206 | passed | passed |

### 2) $I_{CC}$

$I_{CC}$, the power supply current, of each DUT was monitored during irradiation. Since the input states are static, it is the stand by leakage. Figure 3 shows the in-situ $I_{CC}$ of LAN5201, LAN5202, LAN5203 and LAN5204 irradiated at dose rate of 6krads/day to final total dose ~10krad(Si). All four DUT were biased annealed at room temperature because their final $I_{CC}$ was out of the 25mA spec. Their in-situ $I_{CC}$ curves during annealing are shown in Figure 4 (a) and (b), and Figure 5. Although $I_{CC}$ still above the 25mA spec at the end of annealing, in very case the reduction of radiation induced current is significant. These annealing curves show typical characteristic so that performing extrapolations should be safe. The extrapolations of these curves indicate that all the $I_{CC}$ will be annealed within the spec in few weeks. The effective dose rate, according to TM1019.5, will be well above that of the space environment.

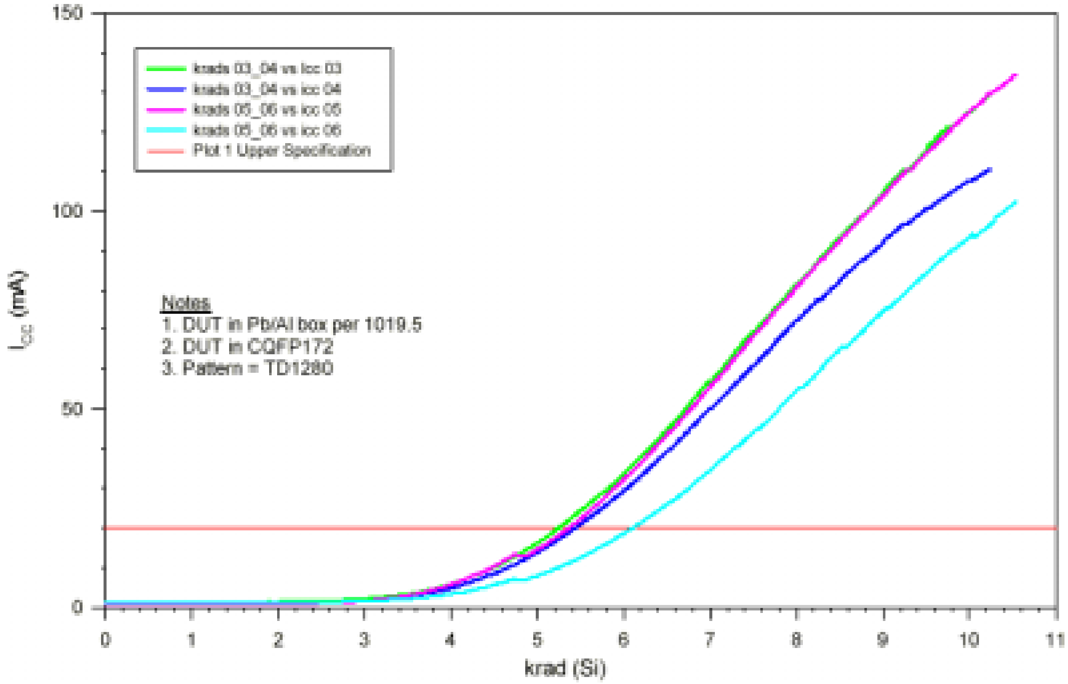
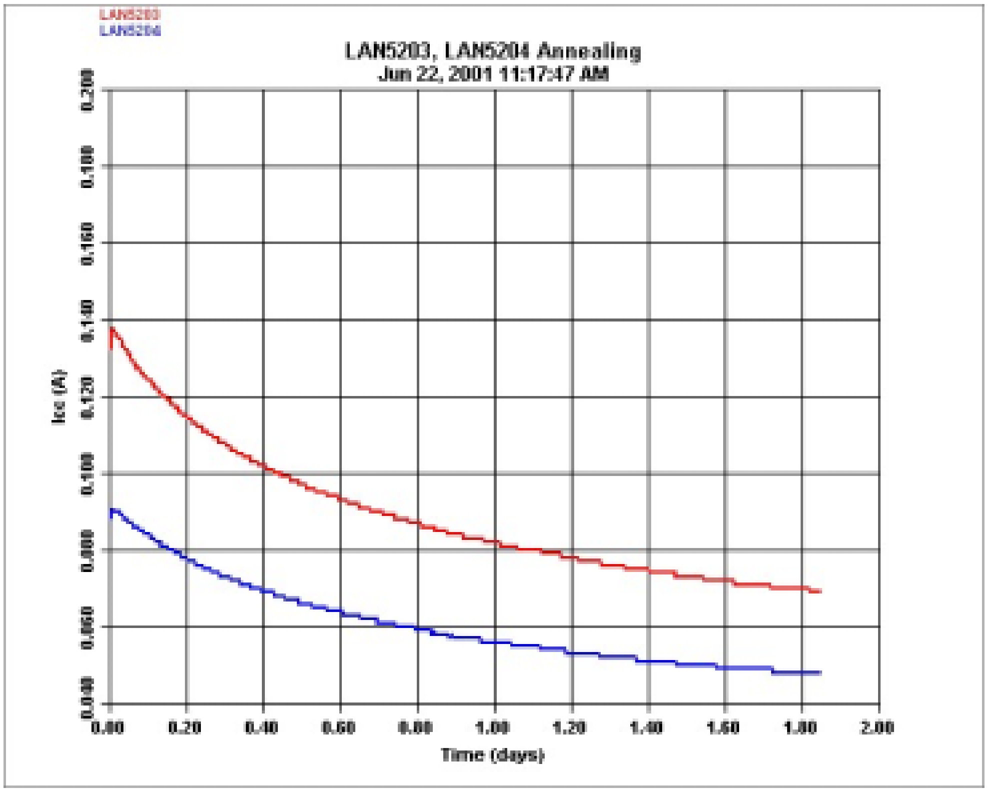
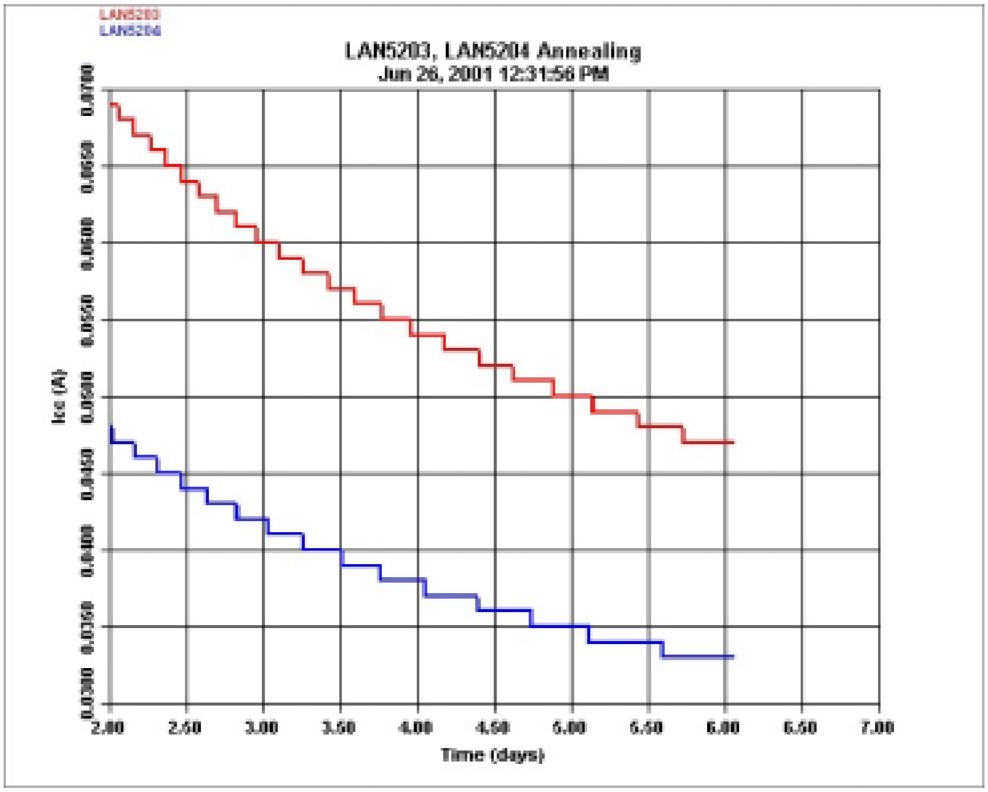


Figure 3. Radiation-induced $I_{CC}$ versus total dose for LAN5203, LAN5204, LAN5205 and LAN5206.



(a)



(b)

Figure 4(a) and (b). Post-irradiation room temperature biased annealing effects on $I_{CC}$ of LAN5203 and LAN5204.

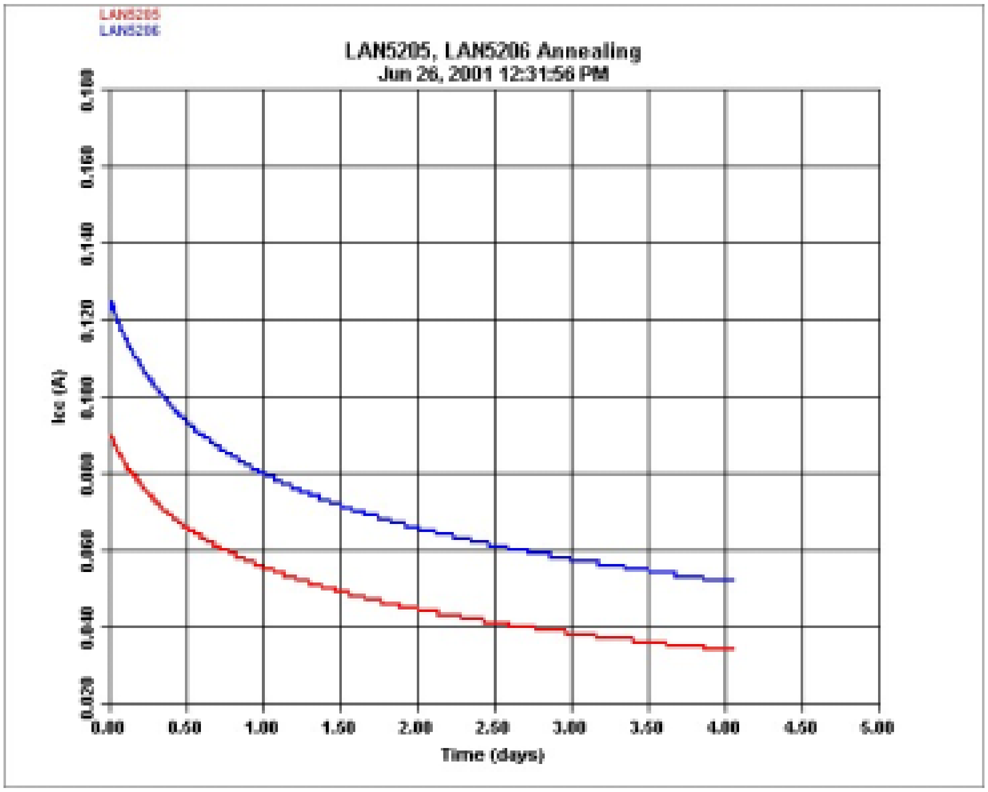


Figure 5. Post-irradiation room temperature biased annealing effects on $I_{CC}$ of LAN5205 and LAN5206.

*3) Input Logic Threshold*

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-irradiation-and-annealing. Judging by these data, the 10krad(Si)-radiation effect is negligible on this parameter.

Table 5. Input Logic Threshold ($V_{IL}/V_{IH}$) Results (V)

| | Pre-Irradiation | Post-Irrad-and-Anneal |
|---|---|---|
| LAN5203 | 1.36 | 1.32 |
| LAN5204 | 1.37 | 1.33 |
| LAN5205 | 1.34 | 1.34 |
| LAN5206 | 1.36 | 1.34 |

*4) Output Characteristic*

Figure 6a and 6b show the $V_{OL}$ characteristic curves for the pre-irradiated and post-irradiation-and-annealed DUT. All DUT are within the spec, and no significant radiation effect can be detected. The spec is, at $I_{OL}$ = 6mA, $V_{OL}$ cannot exceed 0.4V.

Figure 7a and 7b show the $V_{OH}$ characteristic curves for the pre-irradiated and post-irradiation-and-annealed DUT. All DUT pass the spec, and the radiation effect is negligible. The spec is, at $I_{OH}$ = 4mA, $V_{OH}$ cannot be lower than 3.7V.

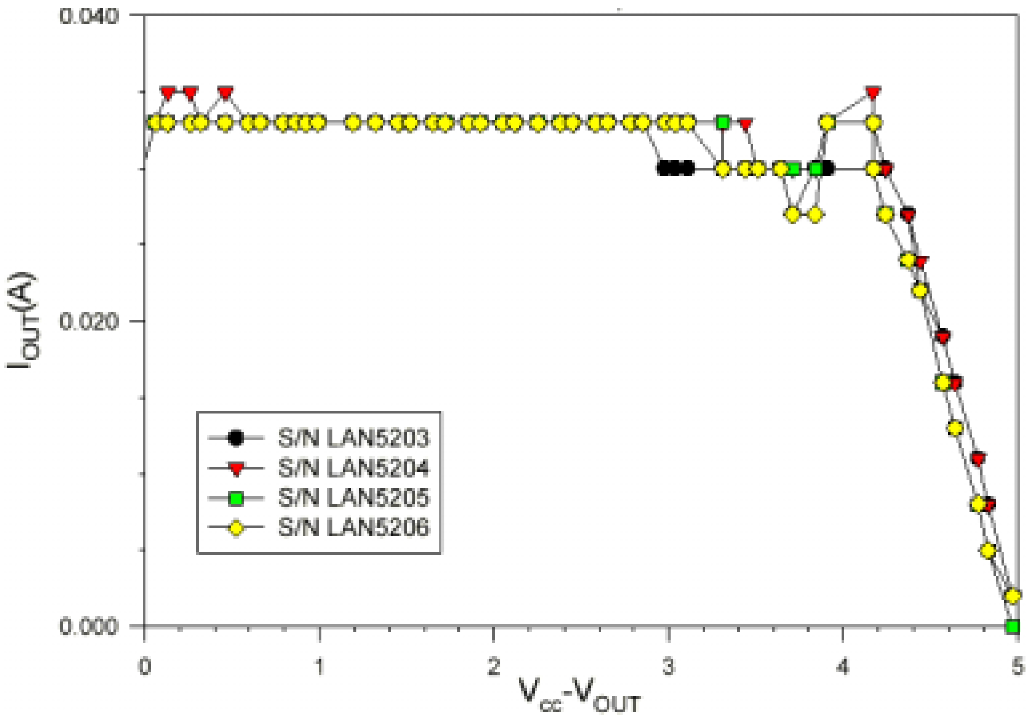


Figure 6a. Pre-irradiation $V_{OL}$ characteristic curves.

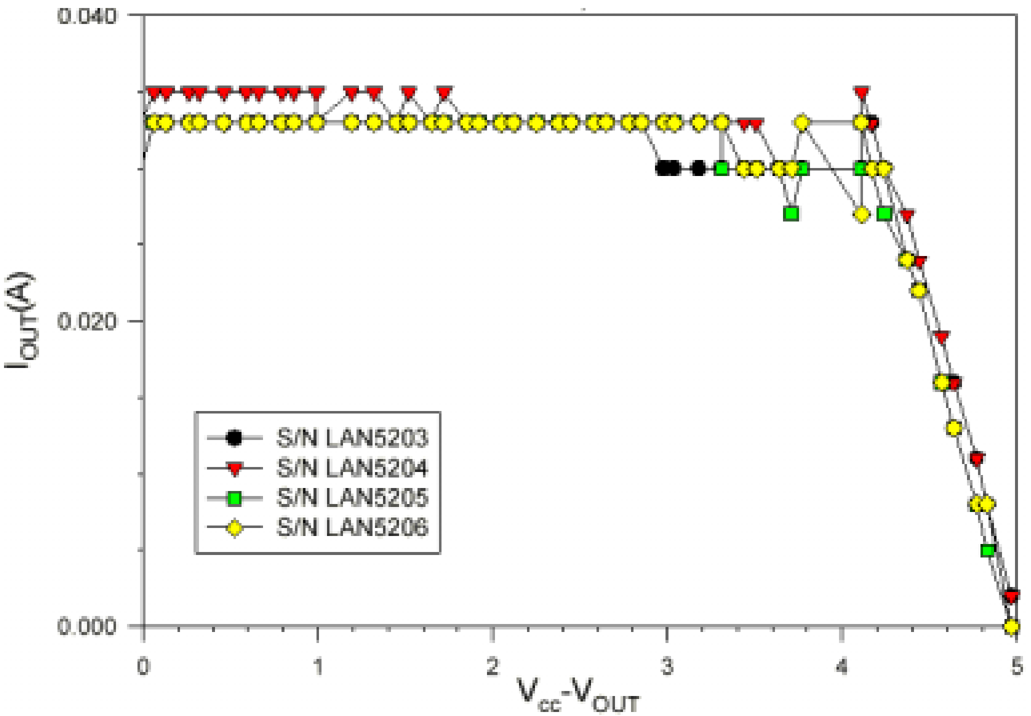


Figure 6b. Post-irradiation-and-annealing $V_{OL}$ characteristic curves.

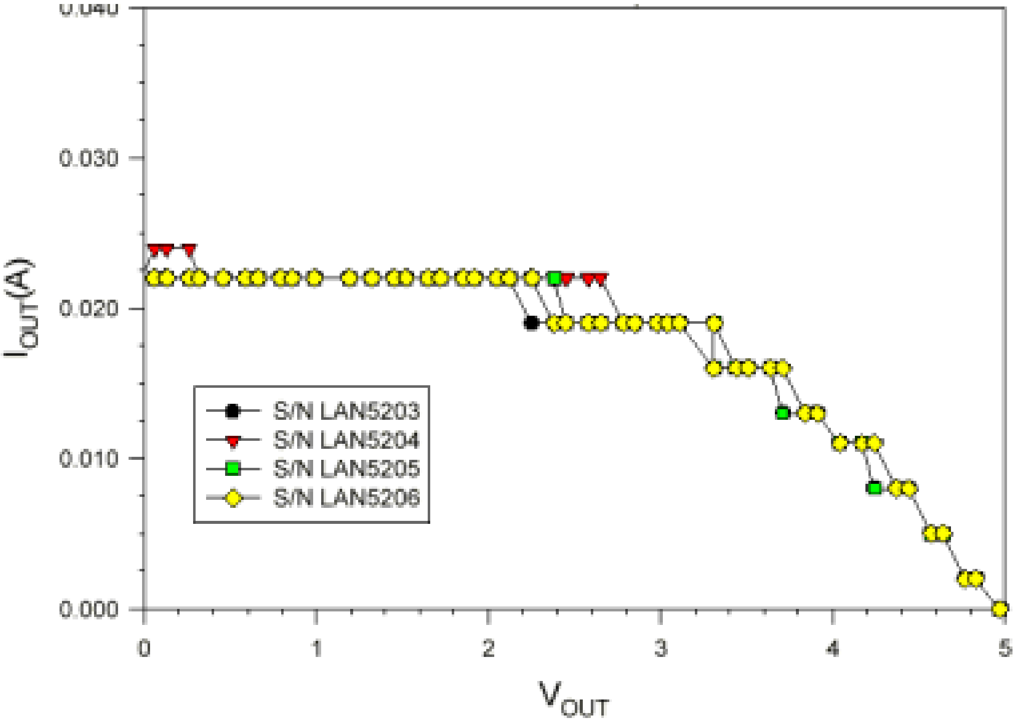


Figure 7a. Pre-irradiation $V_{OH}$ characteristic curves.

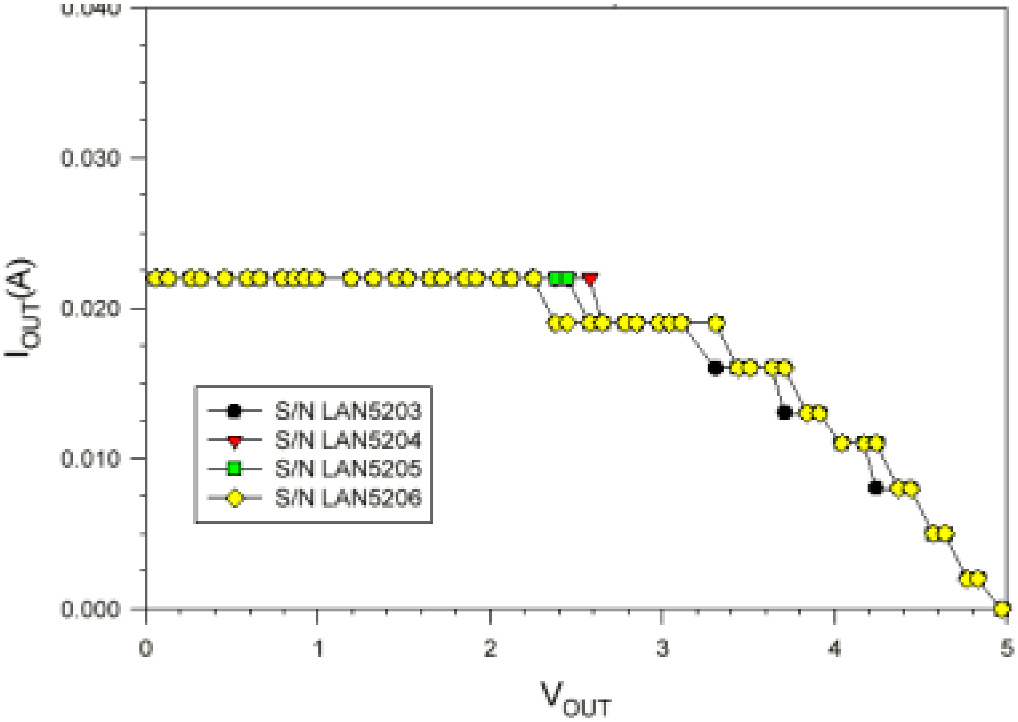


Figure 7b. Post-irradiation-and-annealing $V_{OH}$ characteristic curves.

### 5) *Propagation Delays*

The propagation delays were measured on a combinatorial path. Both the rising edge and falling edge were measured. Table 6 lists the results. The delta due to radiation effect is well within 10%.

Table 6. Propagation Delays of Combinatorial Path (ns)

| | Rising Output | | Falling Output | |
|---|---|---|---|---|
| | Pre-Irrad | Post-Irrad-and-Annl | Pre-Irrad | Post-Irrad-and-Annl |
| LAN5203 | 1295 | 1304 | 1287 | 1282 |
| LAN5204 | 1324 | 1329 | 1316 | 1299 |
| LAN5205 | 1309 | 1305 | 1297 | 1281 |
| LAN5206 | 1366 | 1362 | 1358 | 1329 |

### 6) *Rising/Falling Edge Transient*

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-irradiation-and-annealing. Figures 8-11 show the rising edge transient. Figures 12-15 show the falling edge transient. The radiation effect is negligible in every case.

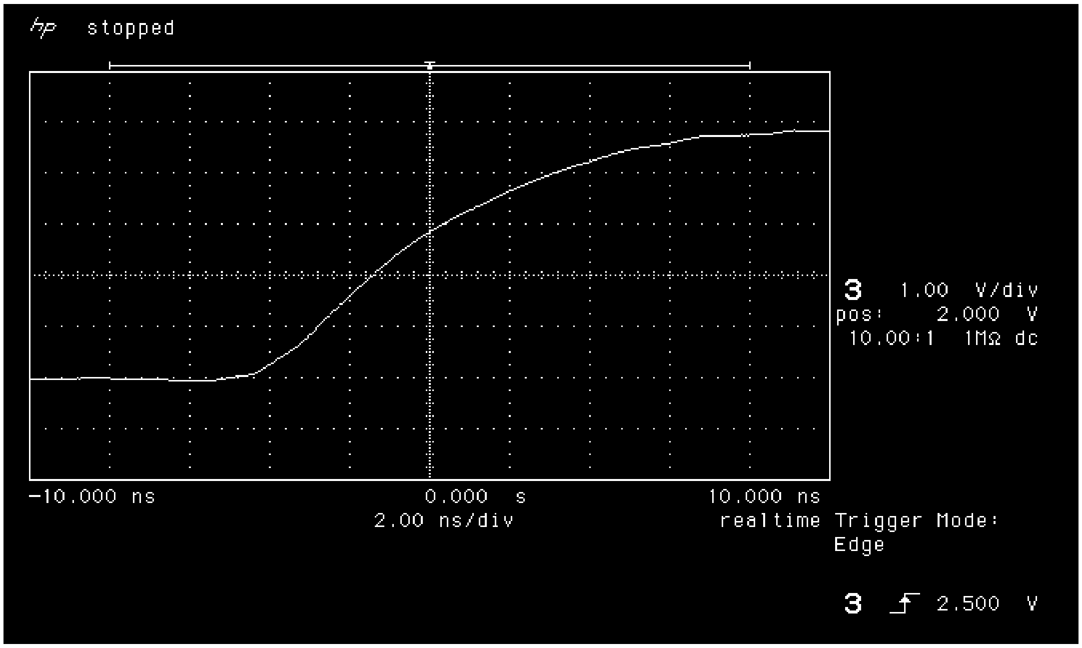


Figure 8a. Rising edge of LAN5203 pre-irradiation.

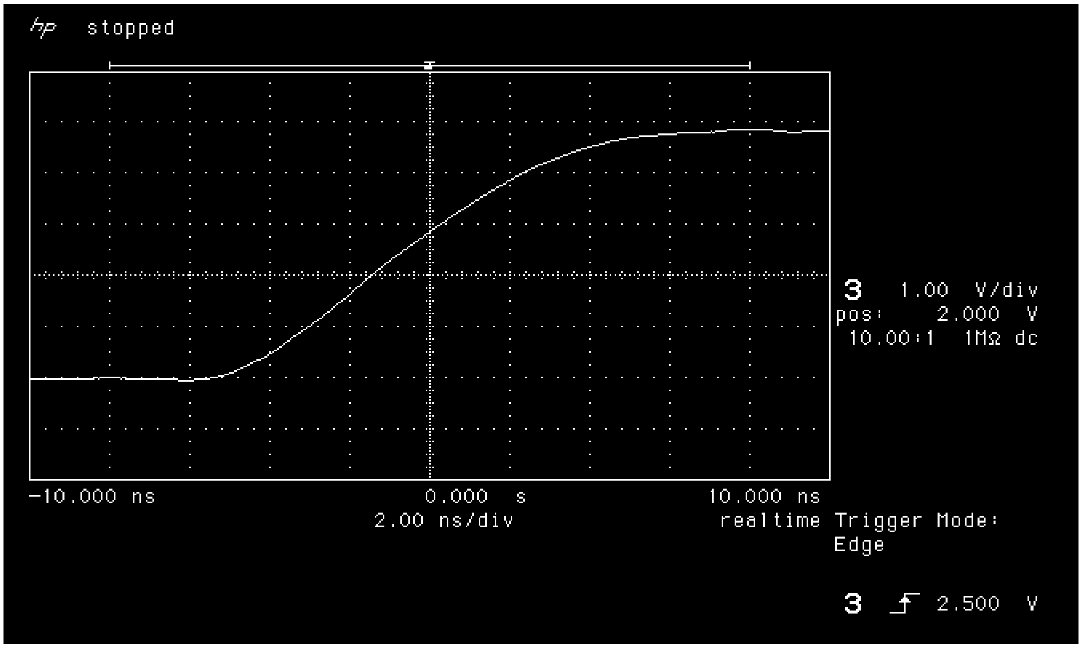
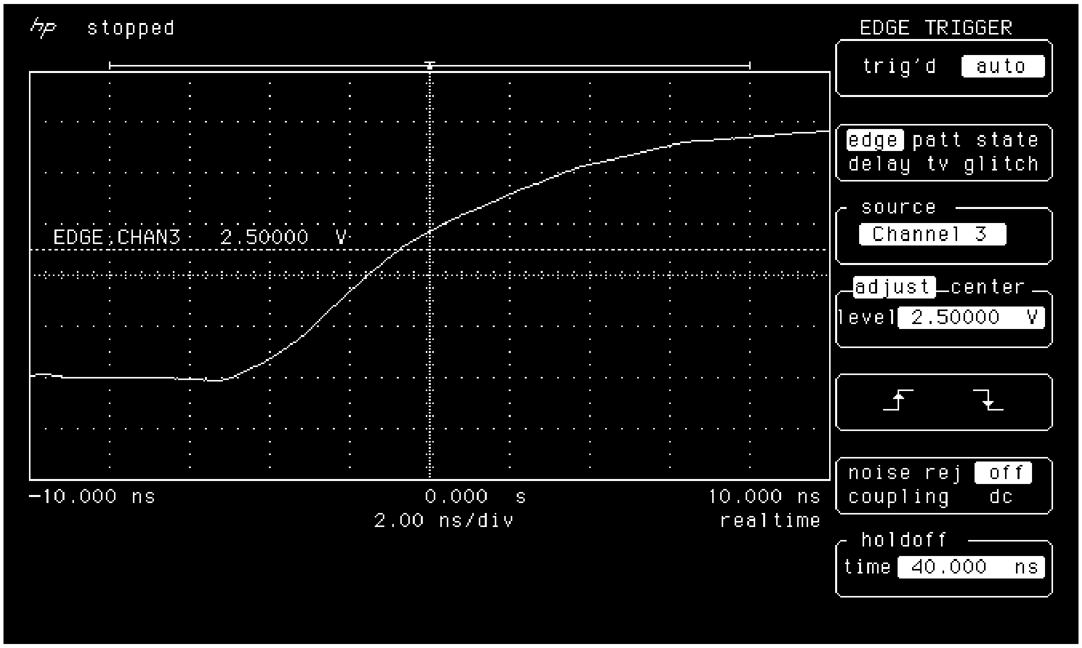
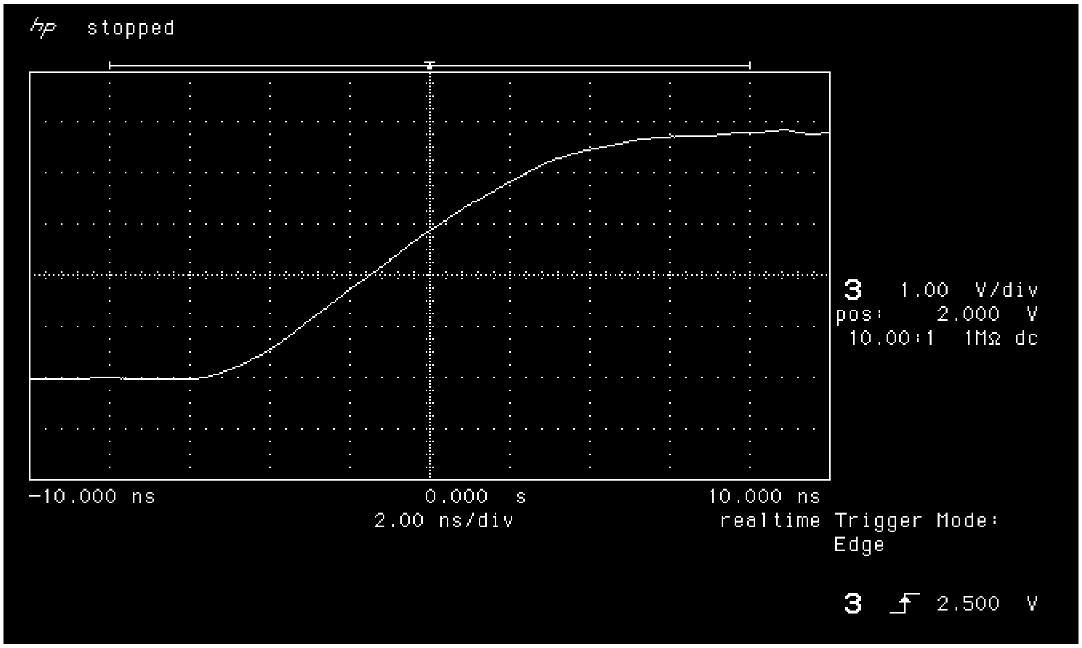


Figure 8b. Rising edge of LAN5203 post-irradiation-and-annealing.



EDGE,CHAN3 2.50000 V
trig'd auto
source Channel 3
adjust center
level 2.50000 V
noise rej off
coupling dc
holdoff
time 40.000 ns

Figure 9a. Rising edge of LAN5204 pre-irradiation.



3 1.00 V/div
pos: 2.000 V
10.00:1 1MΩ dc
Trigger Mode:
Edge
3 2.500 V

Figure 9b. Rising edge of LAN5204 post-irradiation-and-annealing.

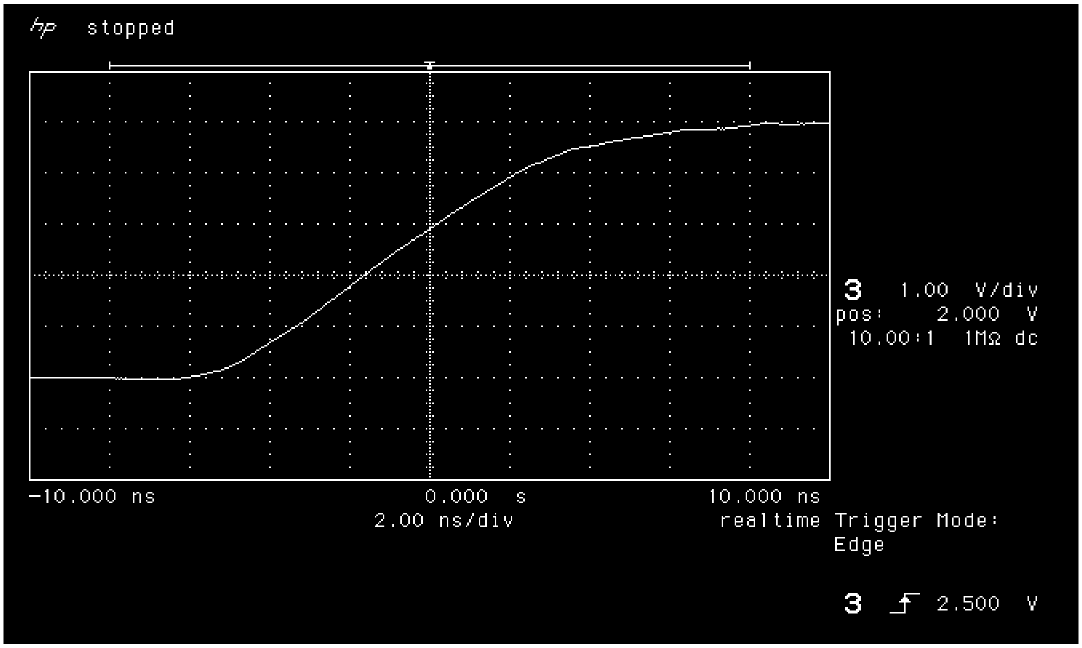


Figure 10a. Rising edge of LAN5205 pre-irradiation.

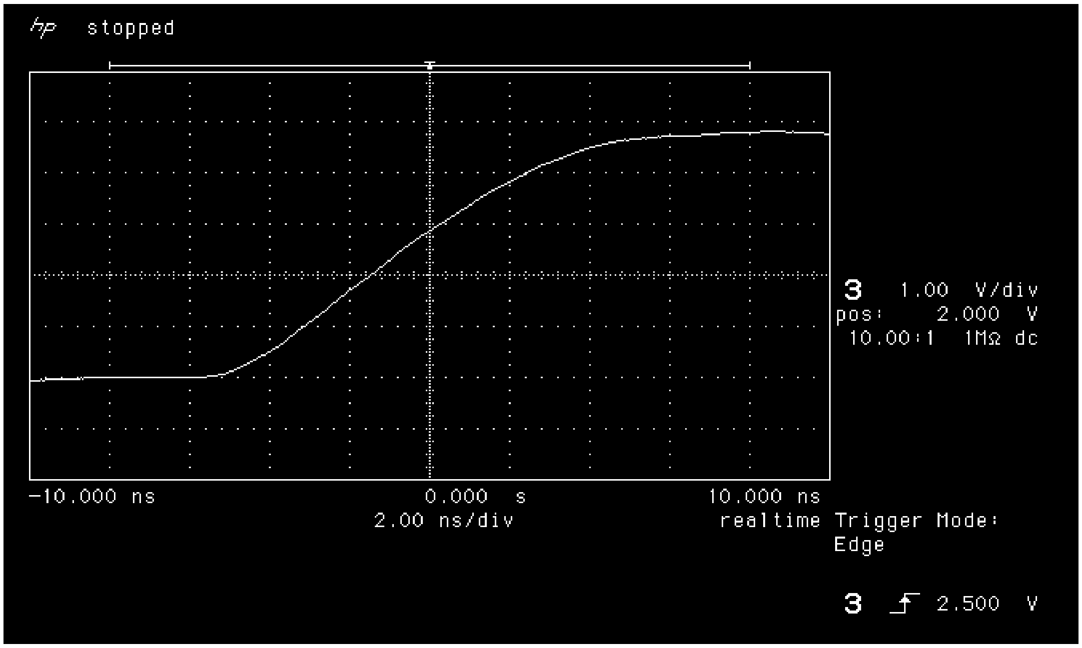


Figure 10b. Rising edge of LAN5205 post-irradiation-and-annealing.

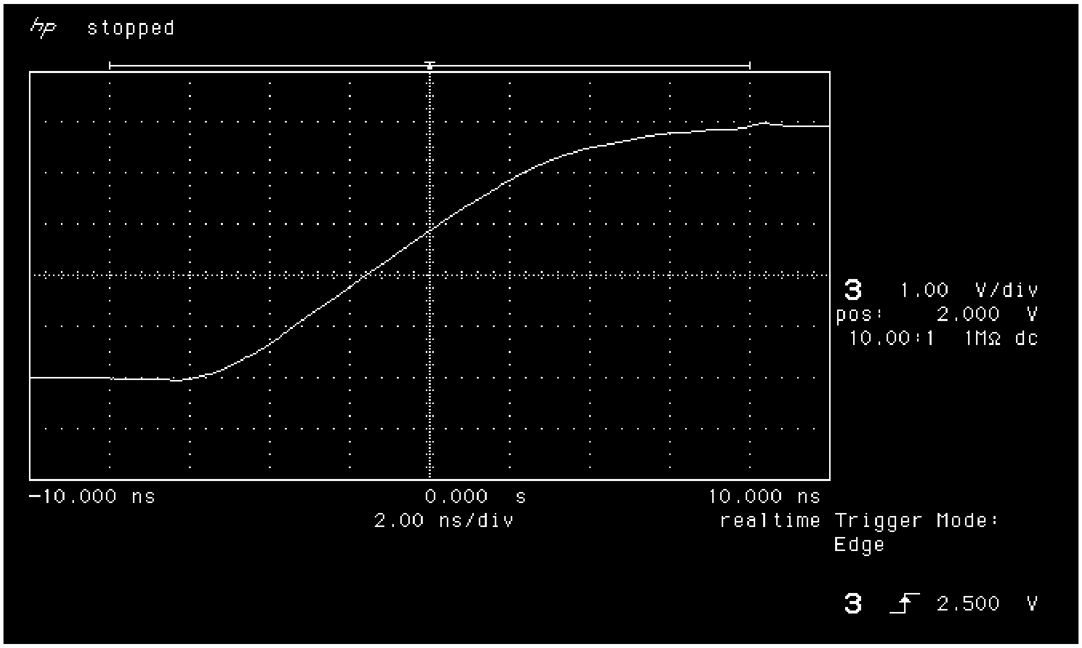


Figure 11a. Rising edge of LAN5206 pre-irradiation.

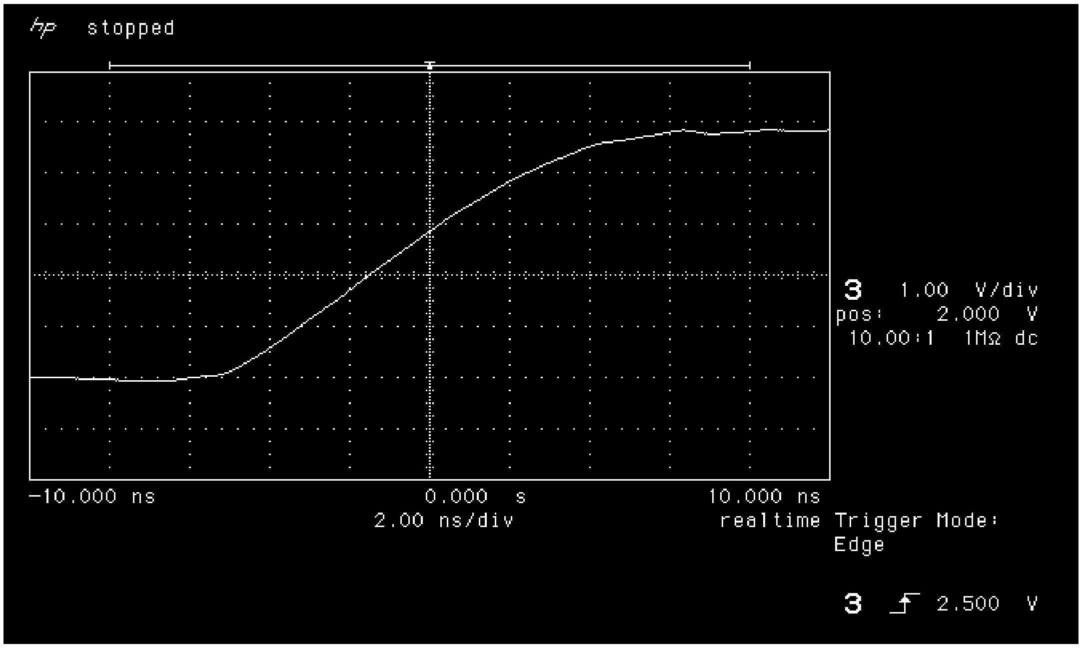


Figure 11b. Rising edge of LAN5206 post-irradiation-and-annealing

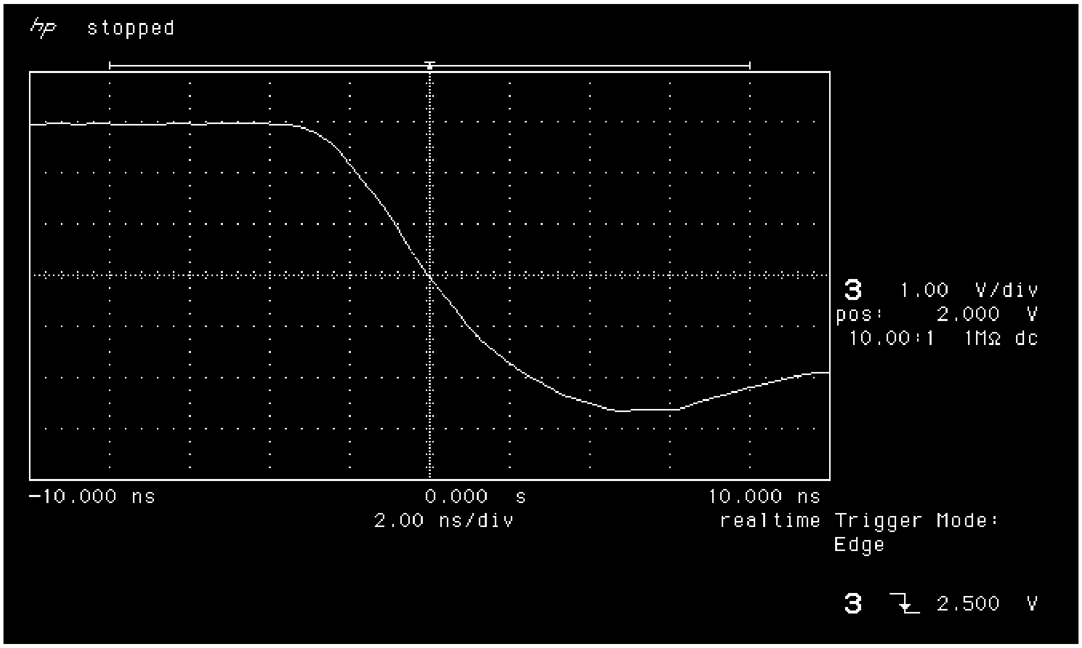


Figure 12a. Falling edge of LAN5203 pre-irradiation

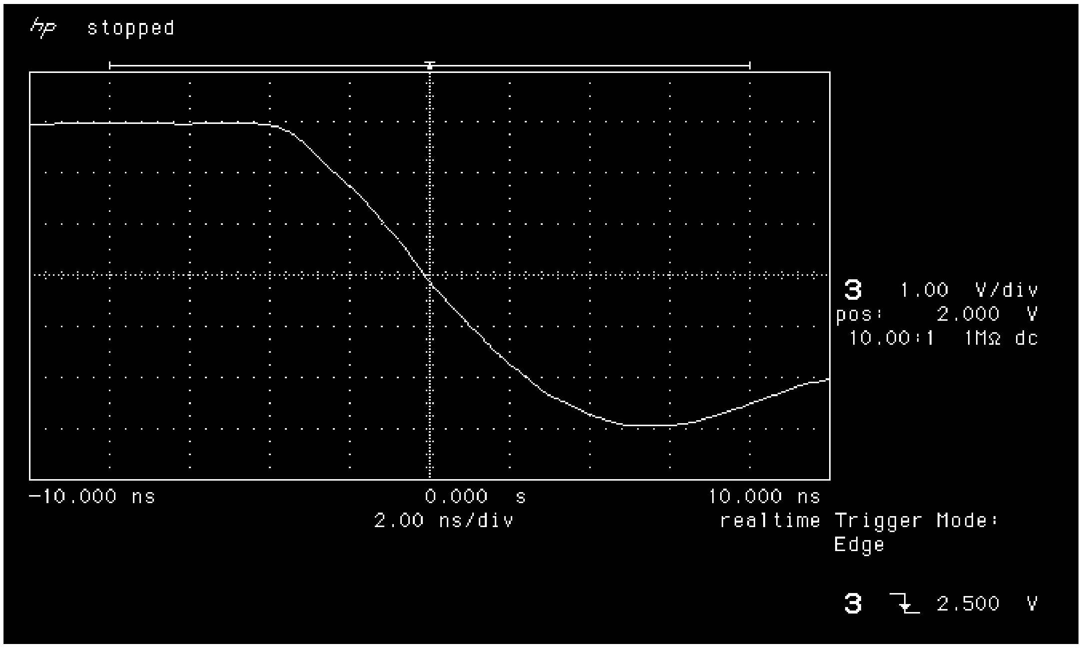


Figure 12b. Falling edge of LAN5203 post-irradiation-and-annealing.

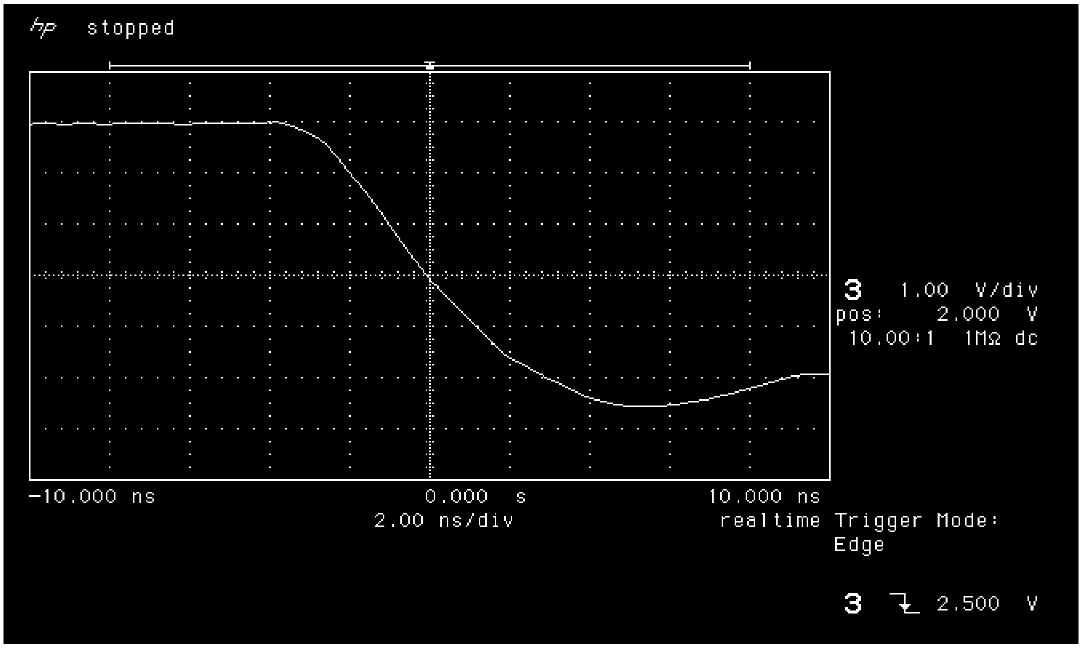


Figure 13a. Falling edge of LAN5204 pre-irradiation.

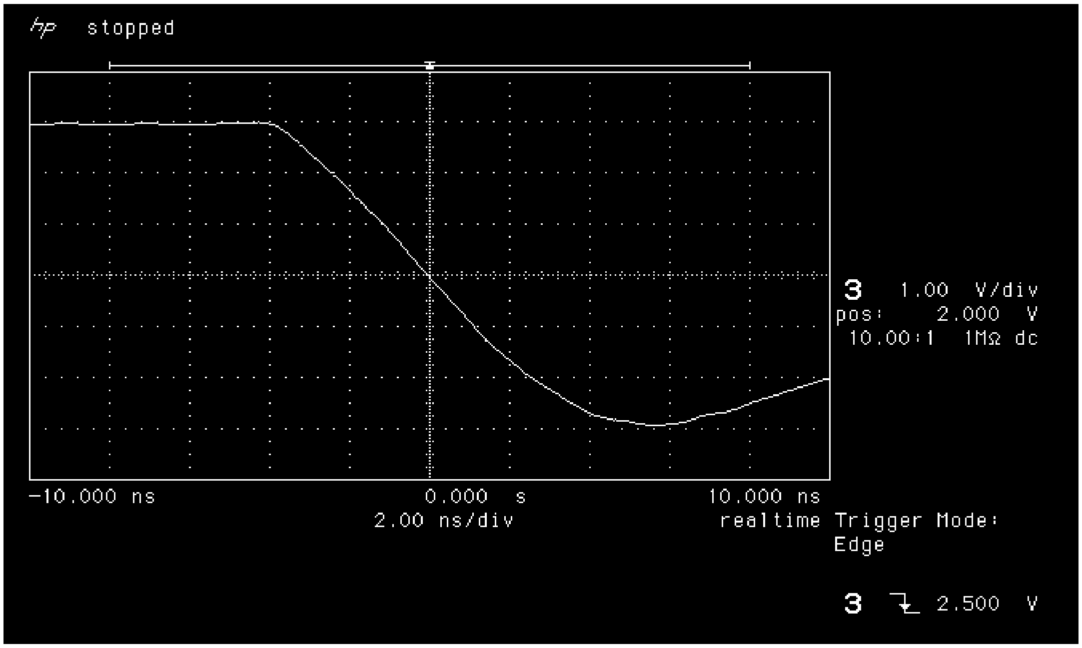


Figure 13b. Falling edge of LAN5204 post-irradiation-and-annealing.

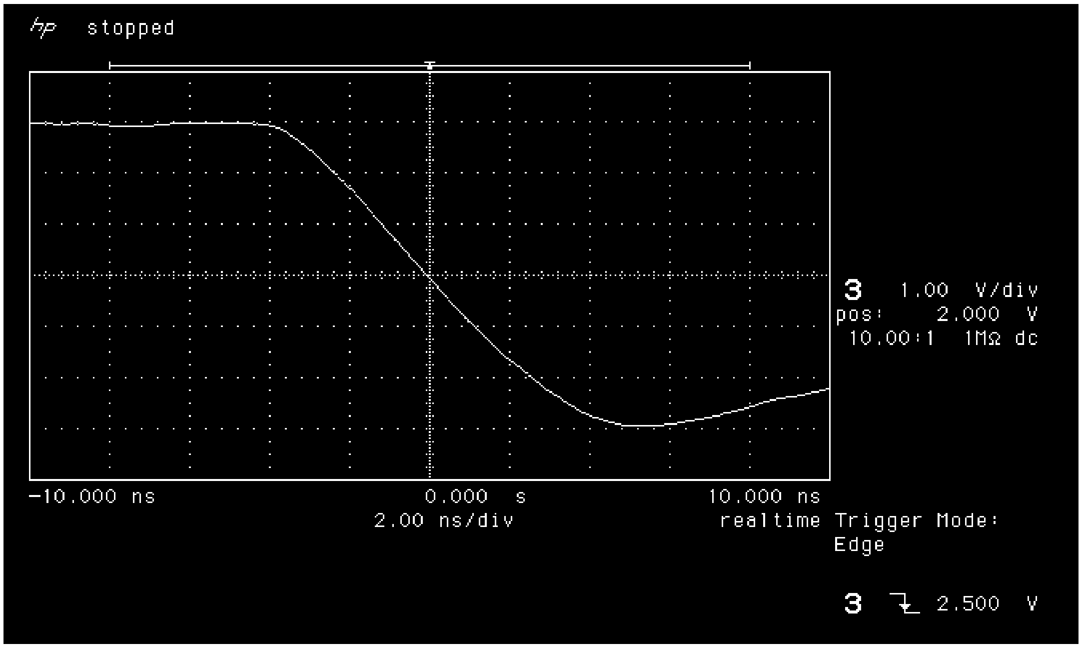


Figure 14a. Falling edge of LAN5205 pre-irradiation.

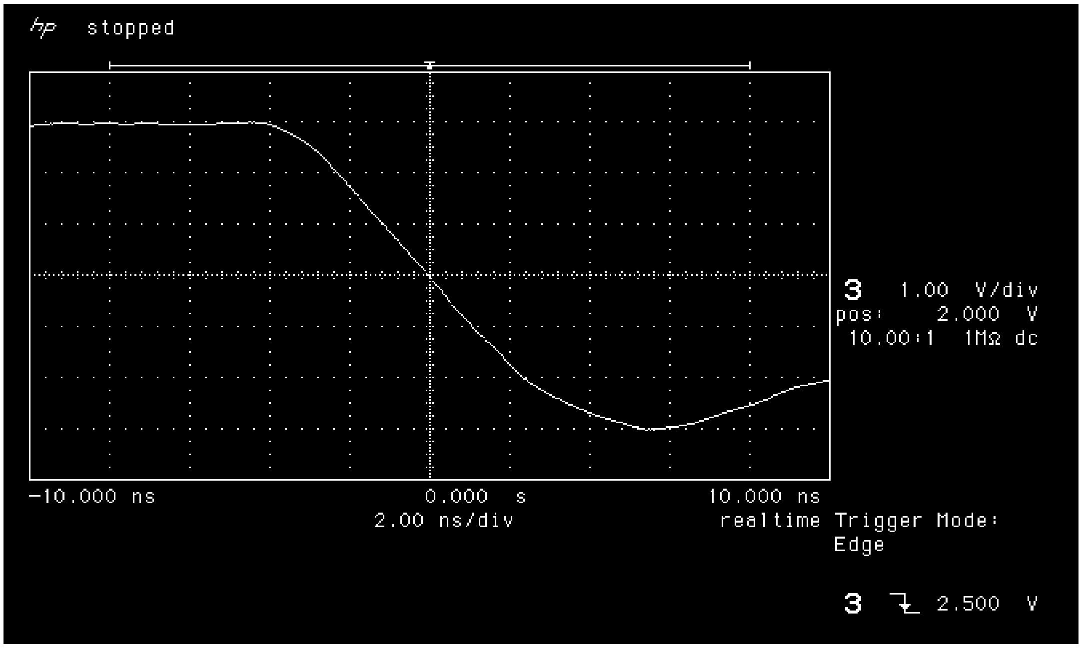


Figure 14b. Falling edge of LAN5205 post-irradiation-and-annealing.

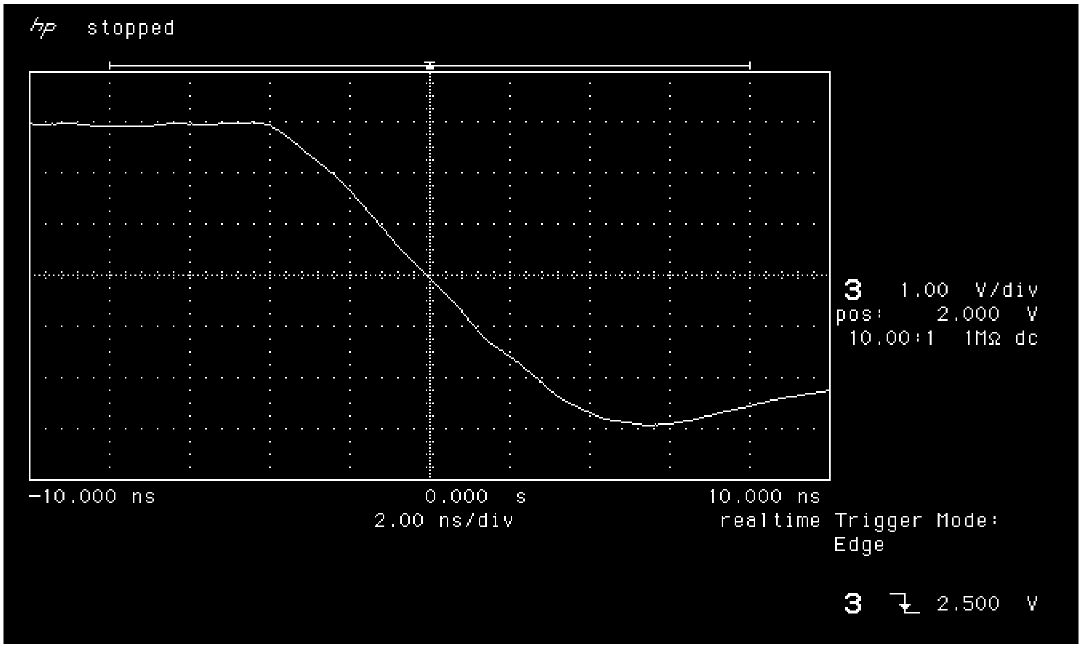


Figure 15a. Falling edge of LAN5206 pre-irradiation

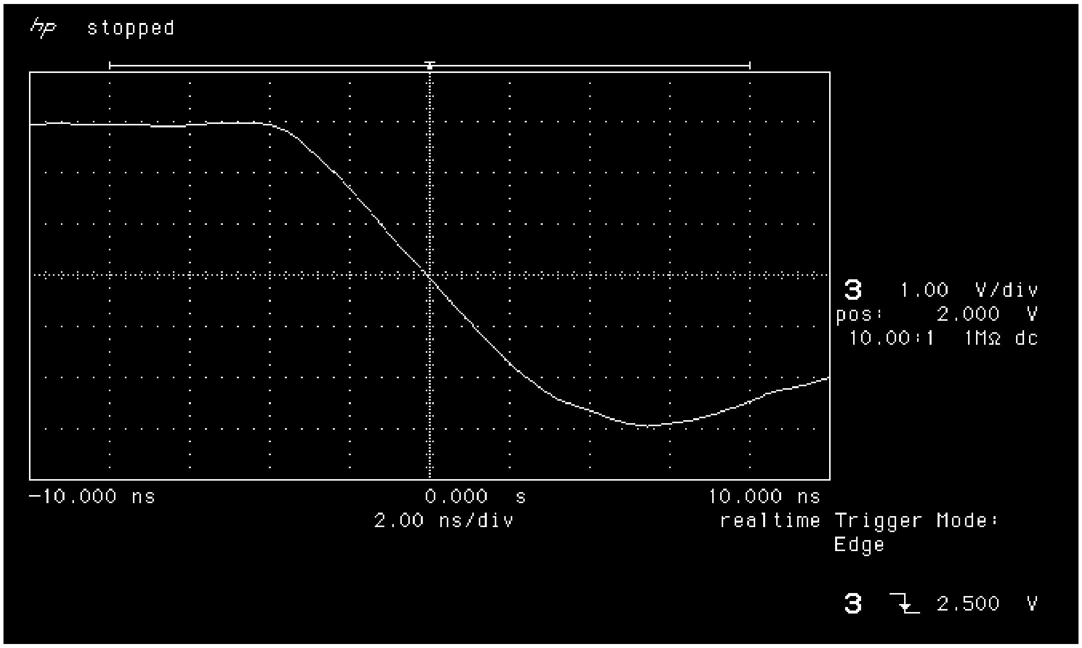


Figure 15b. Falling edge of LAN5206 post-irradiation-and-annealing

### *7) Power-Up Transient*

In each measurement, the rise time of the power supply voltage ($V_{CC}$) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 16-19 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing $V_{CC}$ ramping from GND to 5.0V, and another curve showing $I_{CC}$. The scale is 1V per division for $V_{CC}$ and 100mA per division for $I_{CC}$. Post 10krad(Si) irradiation/annealing DUT have a radiation-induced transient current during power up (see an example in Figure 16b). However, this transient is due to the relatively high dose rate used in this report. Annealing at room temperature will finally reduce this transient to negligible. In space, the much lower dose rate will render this a non-issue. Users interested in this issue can consult the paper published by Actel previously at RADECS, titled "Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278.

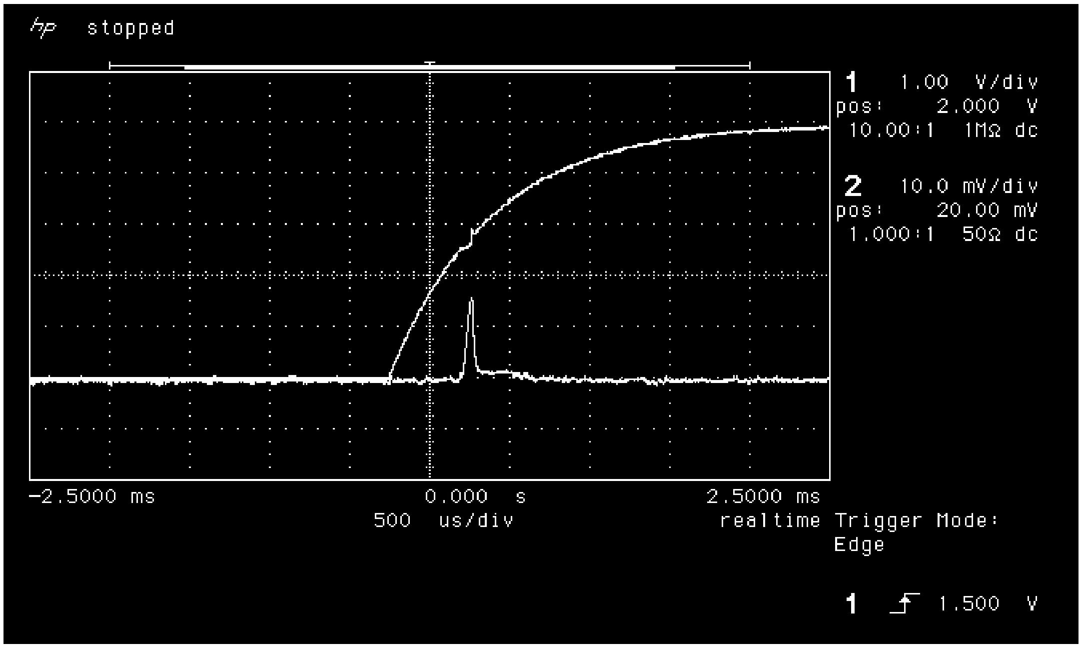


Figure 16a.  Power-up transient of LAN5203 pre-irradiation.

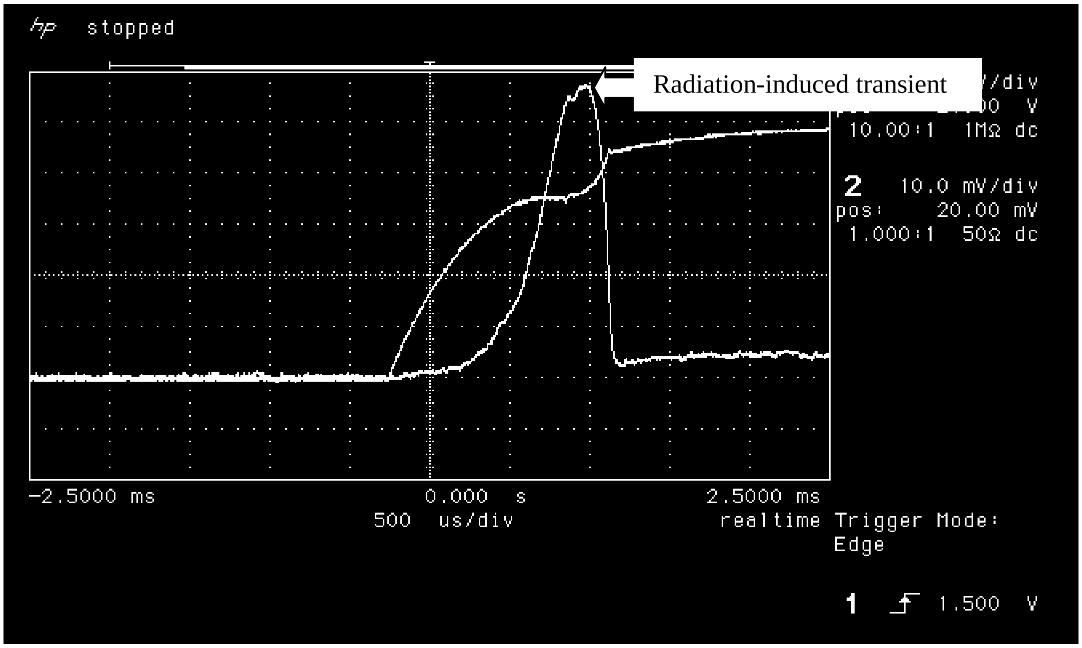


Figure 16b.  Power-up transient of LAN5203 post-irradiation-and-annealing.

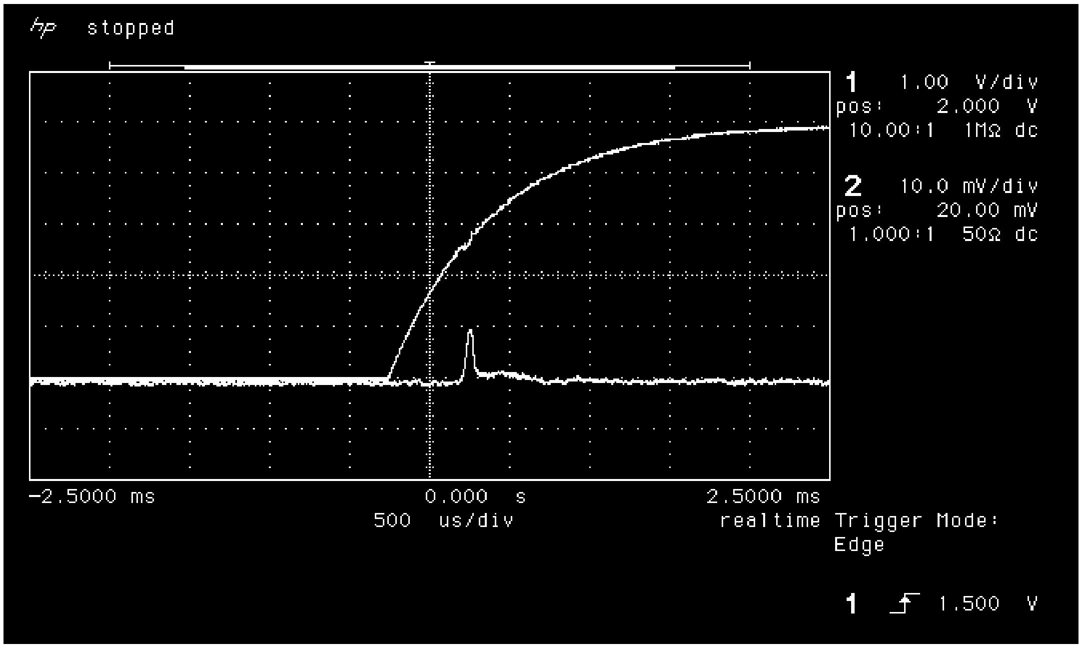


Figure 17a. Power-up transient of LAN5204 pre-irradiation.

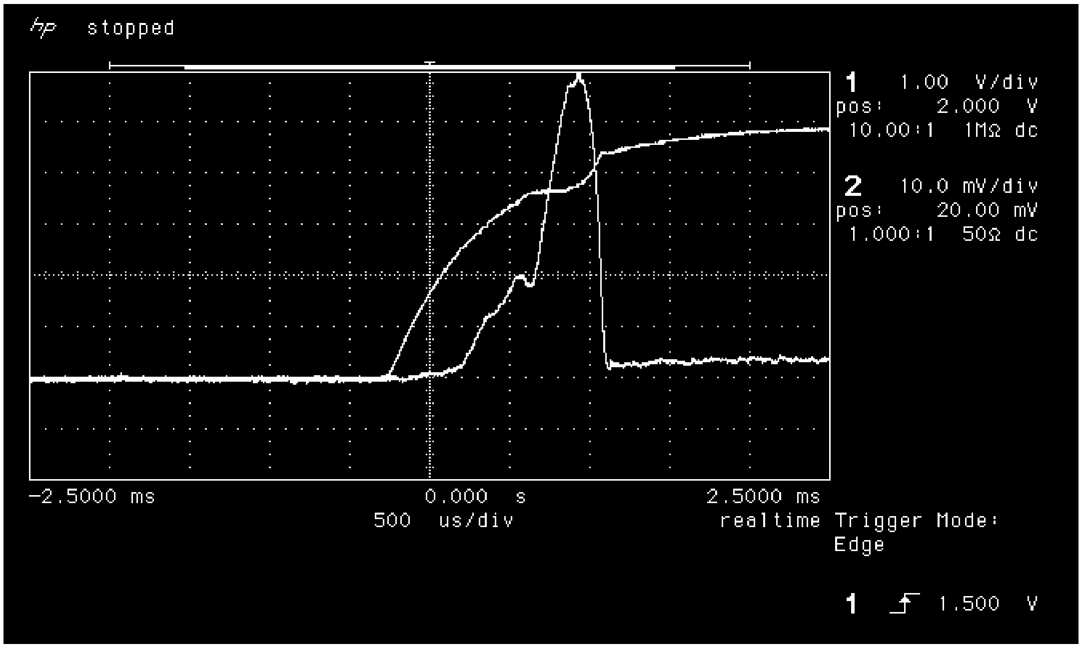


Figure 17b. Power-up transient of LAN5204 post-irradiation-and-annealing.

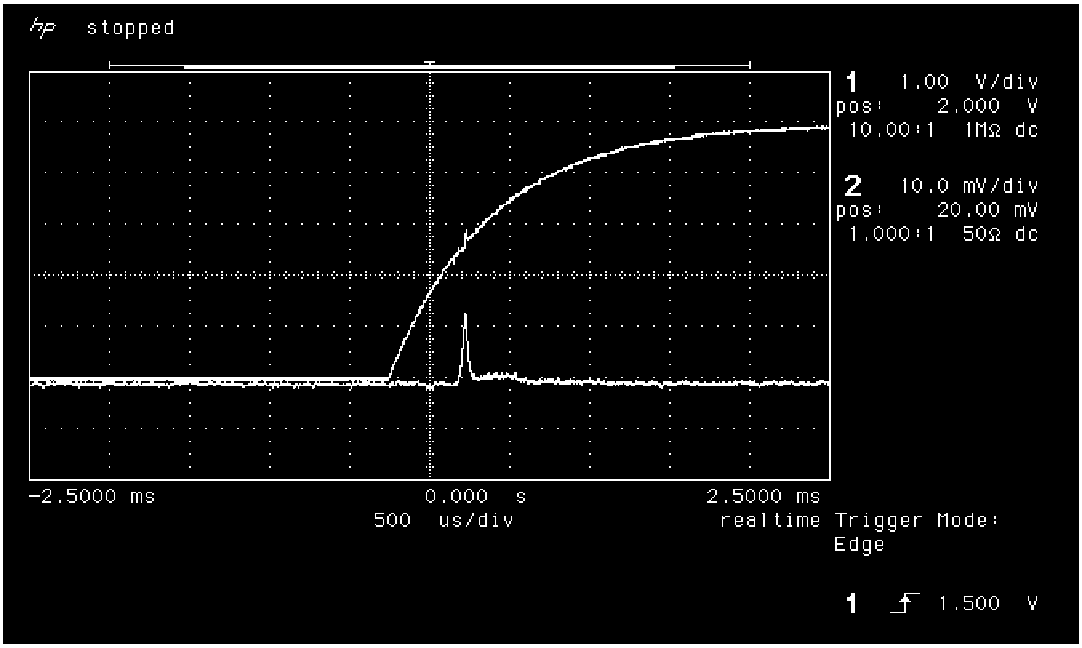


Figure 18a. Power-up transient of LAN5205 pre-irradiation.

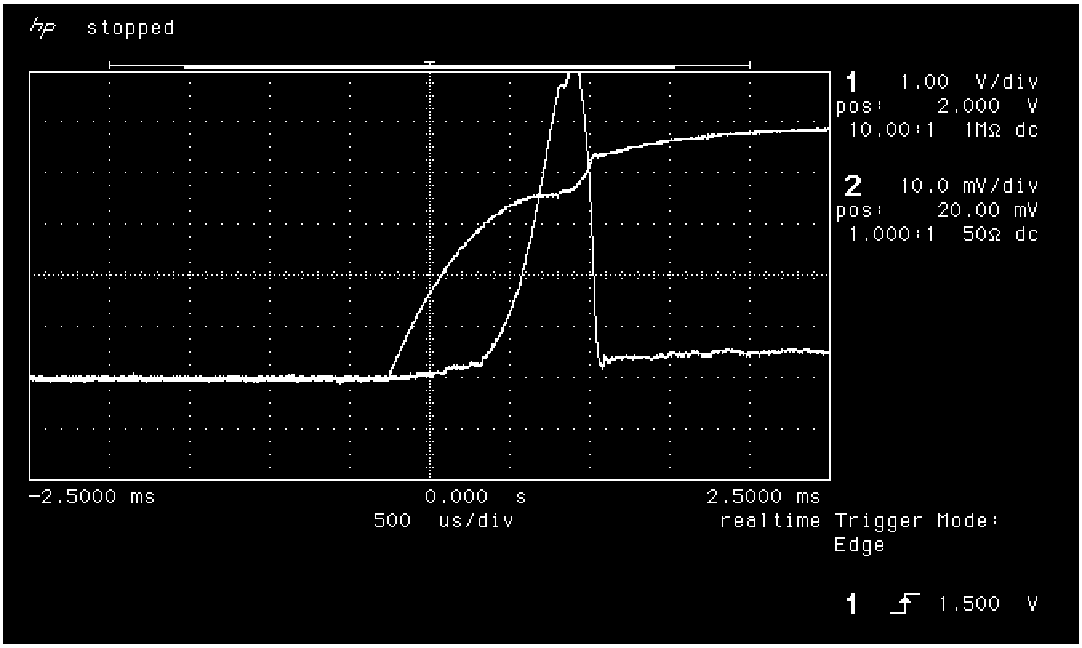


Figure 18b. Power-up transient of LAN5205 post-irradiation-and-annealing.

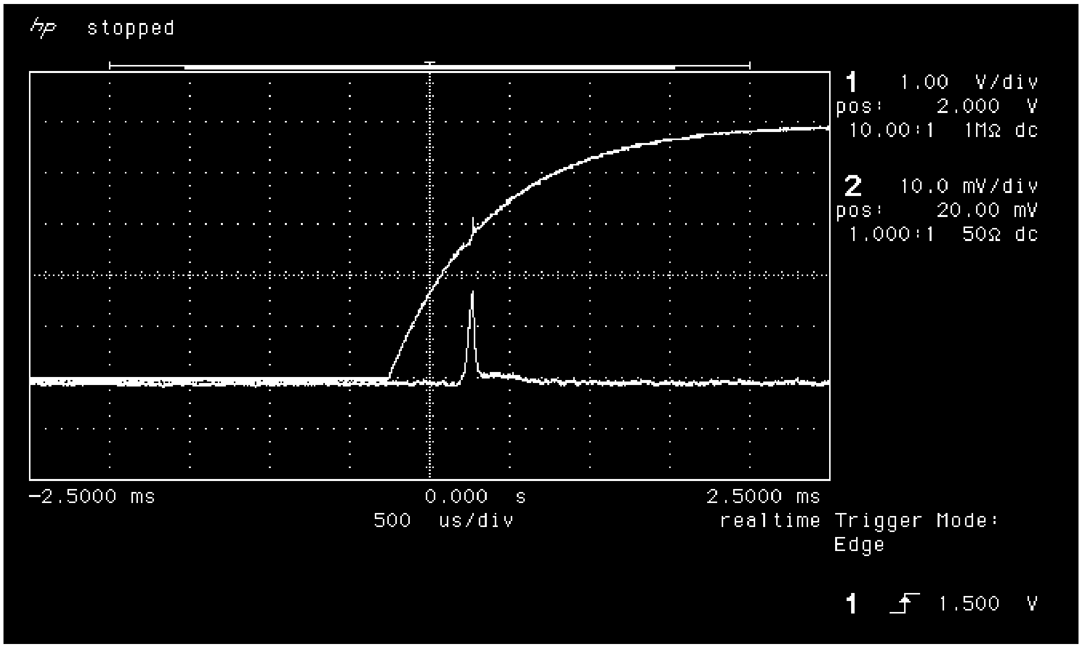


Figure 19a. Power-up transient of LAN5206 pre-irradiation

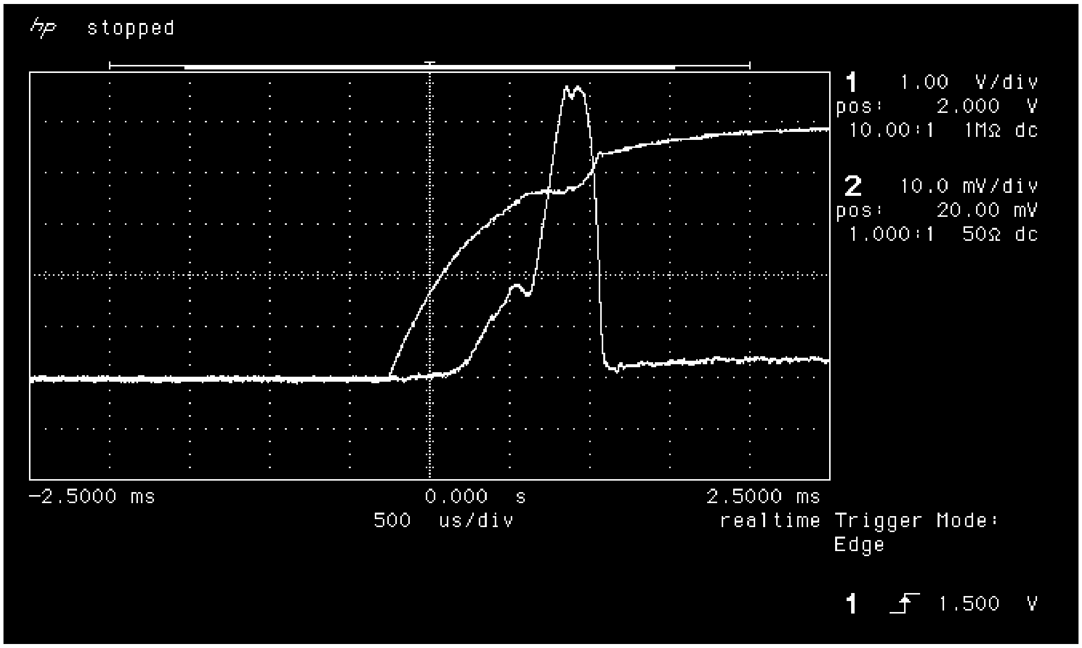


Figure 19b. Power-up transient of LAN5206 post-irradiation-and-annealing