TOTAL IONIZING DOSE TEST REPORT

No. 01T-RT54SX32-T6JP05

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I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	102krad(Si) static case
2. $I_{DDSTDBY}$	Passed 80krad(Si)
3. V_{IL}/V_{IH}	Passed 80krad(Si)
4. V_{OL}/V_{OH}	Passed 80krad(Si)
5. Propagation Delays	Passed 80krad(Si)
6. Rising/Falling Edge Transient	Passed 80krad(Si)
7. Power-up Transient Current	Passed 80krad(Si)

Note: This test was performed in NASA/Goddard radiation facility following their radiation guidelines.

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. *Device Under Test (DUT)*

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT54SX32
Package	CQFP256
Foundry	MEC
Technology	0.6µm CMOS
Die Lot Number	T6JP05
Quantity Tested	6
Serial Numbers	LAN4401, LAN4402, LAN4403, LAN4404, LAN4405, LAN4406

B. *Irradiation*

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	1krad(Si)/hr (+/-10%)
Data Mode	Static
Temperature	Room
Bias	3.3V/5.0V

C. Test Method

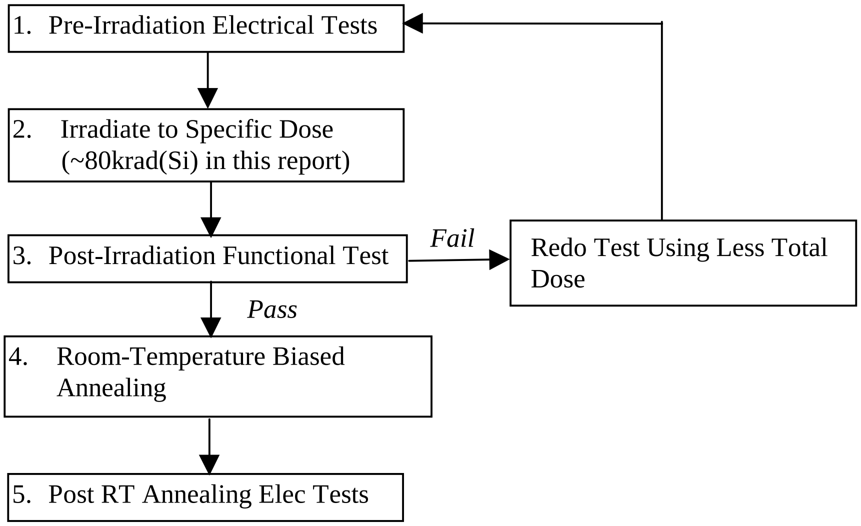


Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has much less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This is almost logistically impossible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured accurately on the bench. Table 3 lists the corresponding logic design for each test parameter.

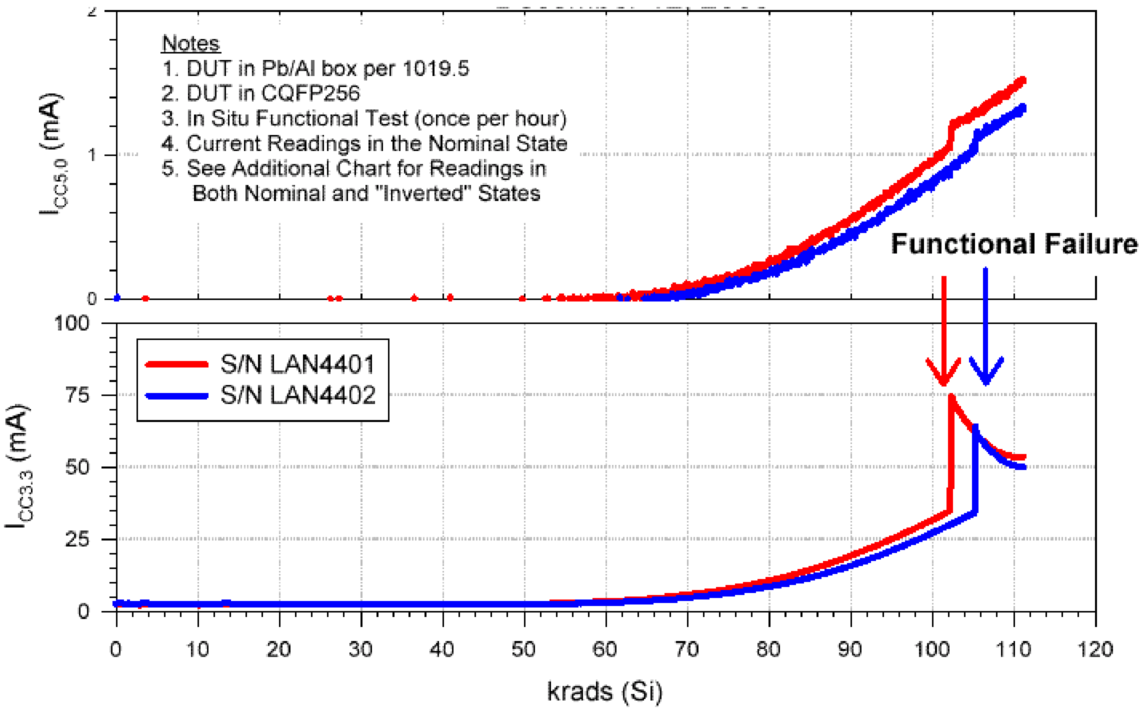
Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. TEST RESULTS

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced I_{CC} versus total dose for DUT LAN4401 and LAN4402. During irradiation, the logic states in the DUT was static. Failure in static case was detected by clocking out the data and comparing them with the truth table. The earliest failure occurred at ~102krad(Si) (LAN4401). As reported earlier (see Report No. 00T-RT54SX16-T6HP12D), the sudden surge of I_{CC} at functional failure only occurs in static case. If the DUT was running dynamically during irradiation, its I_{CC} curve would be smooth over functional failure.



Notes
1. DUT in Pb/Al box per 1019.5
2. DUT in CQFP256
3. In Situ Functional Test (once per hour)
4. Current Readings in the Nominal State
5. See Additional Chart for Readings in Both Nominal and "Inverted" States

Figure 2. Radiation-induced I_{CC} (Delta I_{CC}) versus total dose for two DUTs (LAN4401 and LAN4402).

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post room temperature annealing test (step 5). The room temperature annealing was performed for approximately 10 days to reduce the static leakage current and power-up transient current. The DUTs used for this test are LAN4403, LAN4404, LAN4405 and LAN4406.

1) Functional Test

Table 4 lists results of the functional test results.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Annealing
LAN4403	passed	passed
LAN4404	passed	passed
LAN4405	passed	passed
LAN4406	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

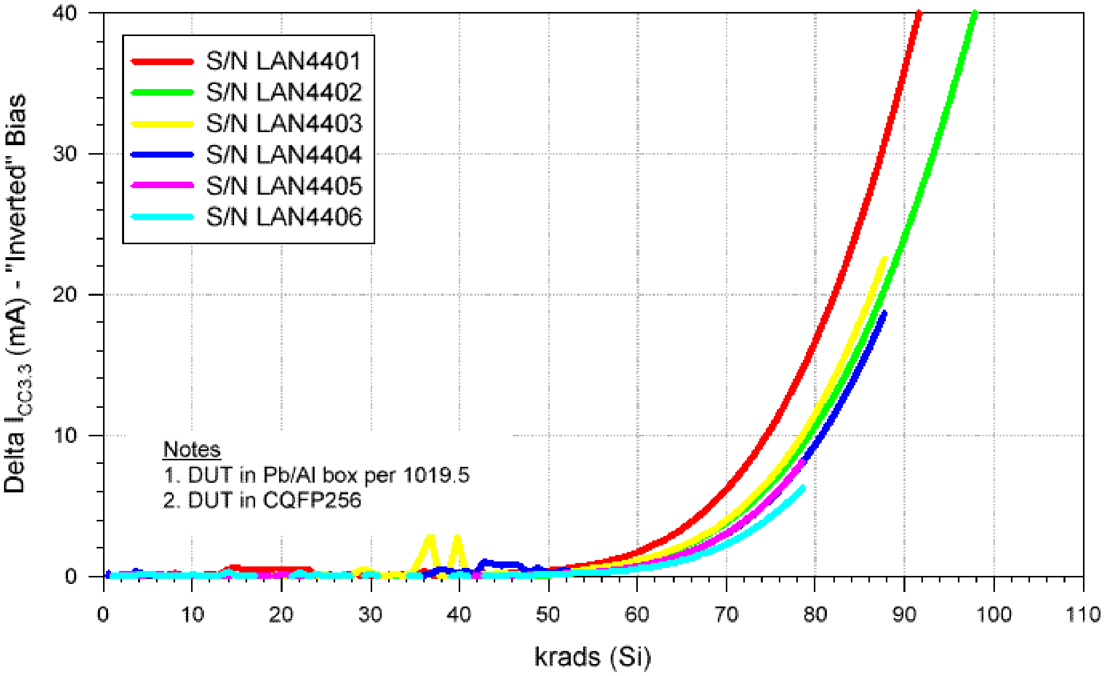


Figure 3. Radiation-induced Delta $I_{DDstandby}$ (I_{CC}) versus total dose for four DUTs (LAN4403, LAN4404, LAN4405 and LAN4406).

As shown in Figure 3, LAN4403, LAN4404, LAN4405 and LAN4406 were irradiated to more than 80krad(Si). The I_{CC} is two times the value on this curve if the static state of the device during irradiation was reversed (see Report No. 00T-RT54SX16-T6HP12D for details). Since the doubled I_{CC} of DUT LAN4405 or LAN4406 at 80krad(Si) is passed 25mA spec, room temperature annealing was performed to reduce it. Post-annealed I_{CC} of every DUT is within spec.

3) *Input Logic Threshold*

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing. The post-annealed DUTs are within the spec and the change of this parameter for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Annealing
LAN4403	1.51	1.49
LAN4404	1.52	1.49
LAN4405	1.50	1.49
LAN4406	1.50	1.49

4) Output Characteristic

Figure 4a and 4b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUTs. All irradiated DUTs are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 5a and 5b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUTs. All DUTs pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.

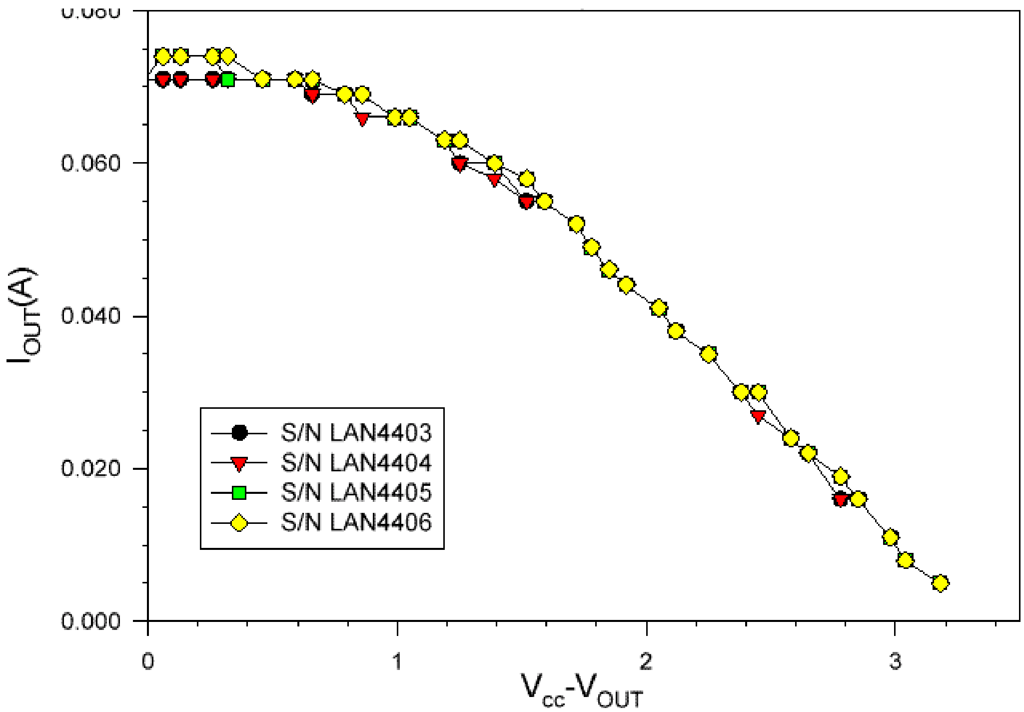


Figure 4a. Pre-irradiation V_{OL} characteristic curves.

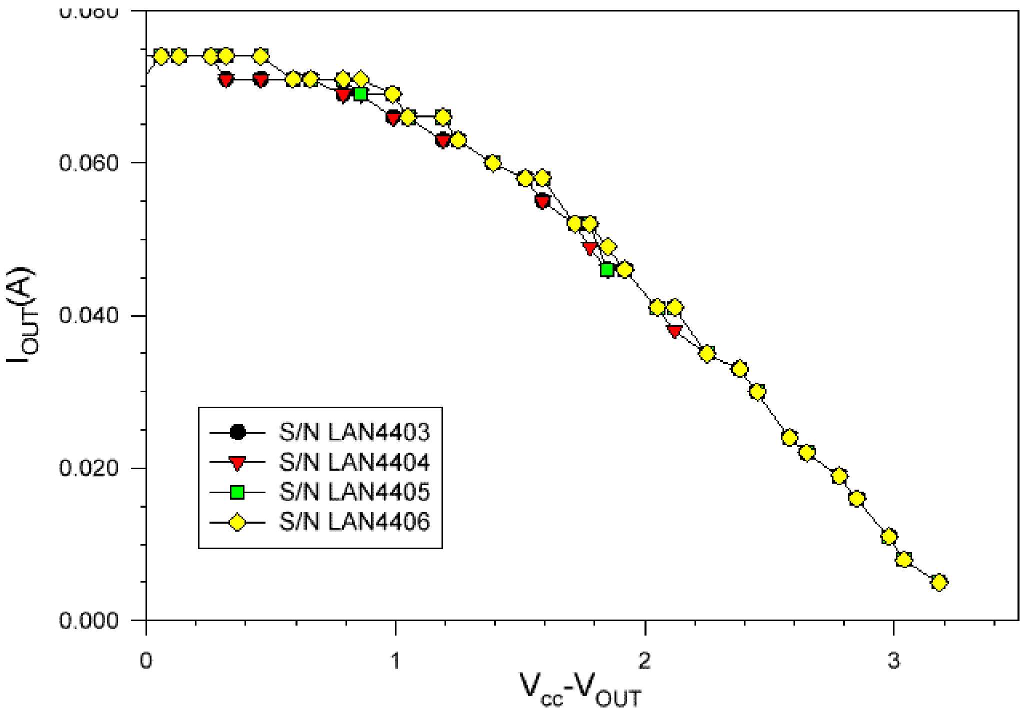


Figure 4b. Post-annealing V_{OL} characteristic curves.

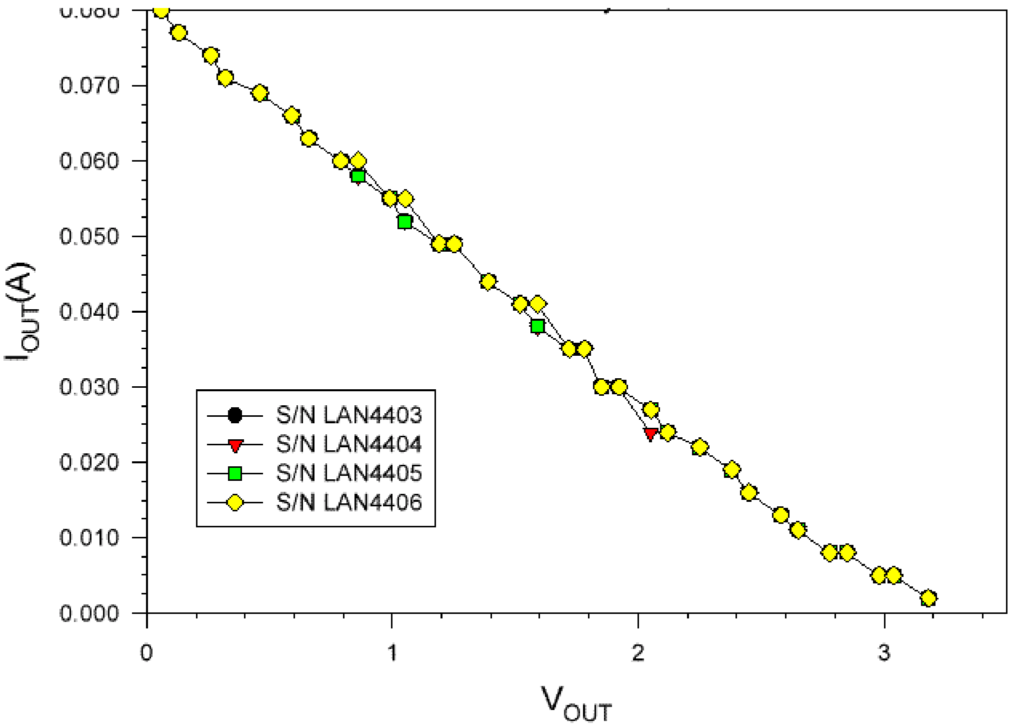


Figure 5a. Pre-irradiation V_{OH} characteristic curves.

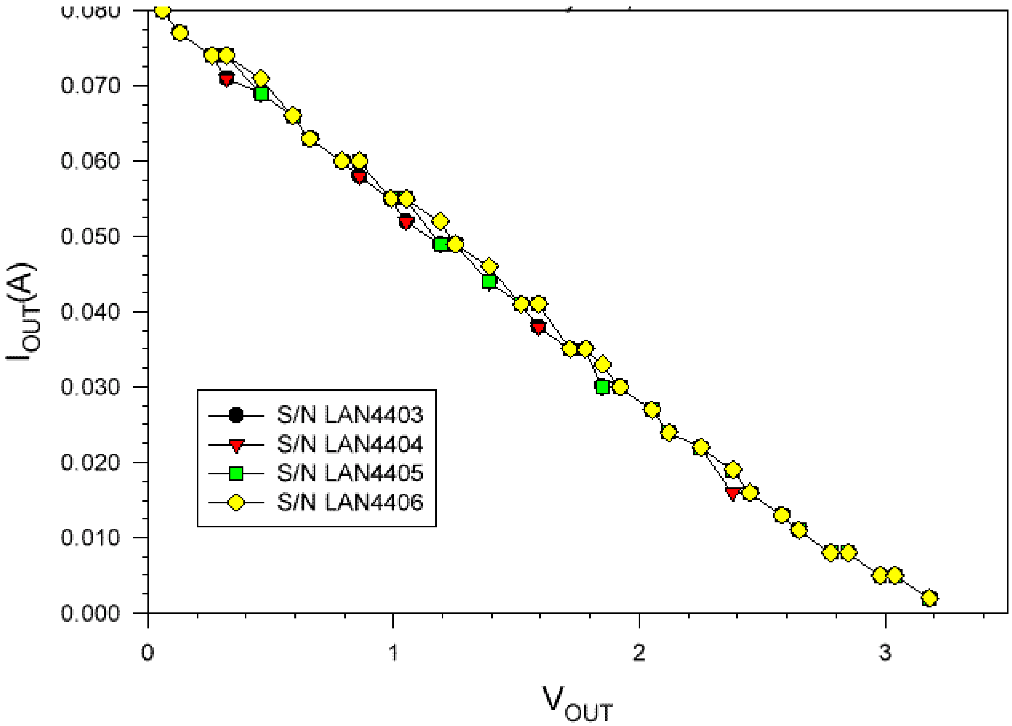


Figure 5b. Post-annealing V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4403	1439	1430	1439	1414
LAN4404	1442	1439	1443	1420
LAN4405	1398	1392	1397	1378
LAN4406	1377	1372	1376	1356

Table 7. Serial-In Delays (ns)

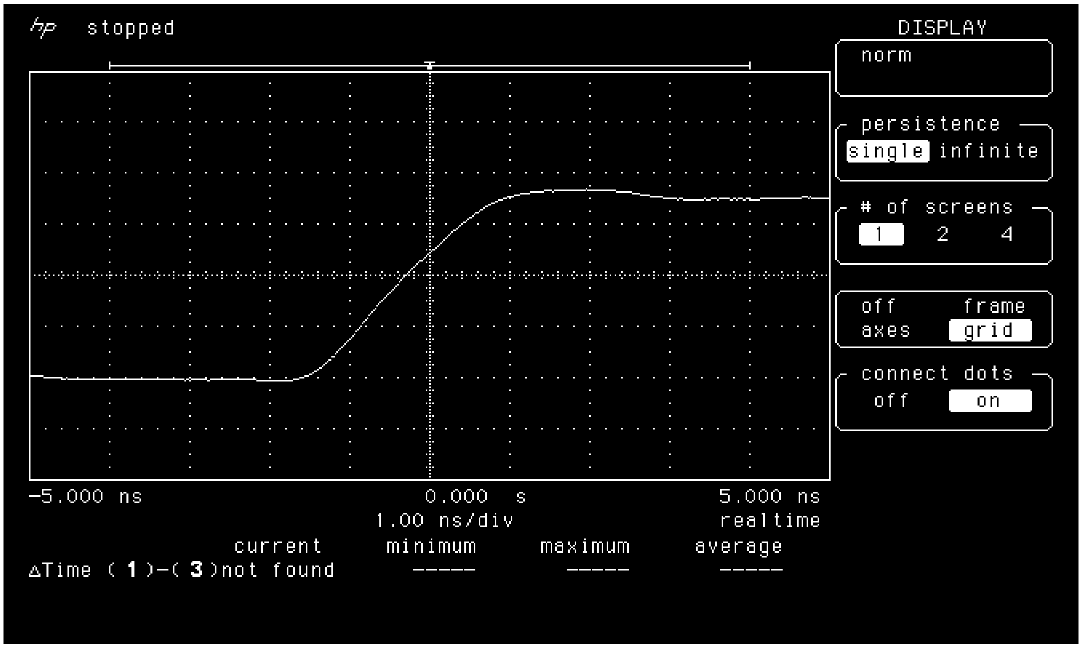
	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4403	58.1	56.7	59.4	57.2
LAN4404	57.1	57.0	57.9	57.7
LAN4405	56.0	55.6	56.9	56.4
LAN4406	55.5	55.3	56.4	56.2

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4403	56.9	58.0	57.6	58.9
LAN4404	58.5	58.3	56.9	59.1
LAN4405	57.3	56.9	58.9	58.3
LAN4406	56.7	56.5	58.3	57.8

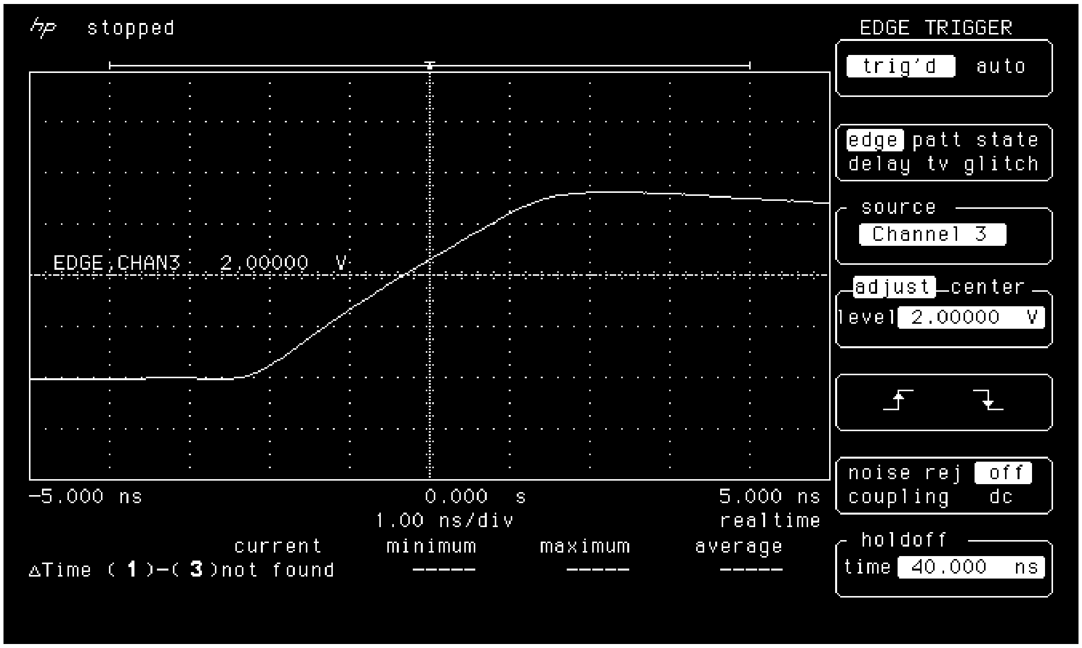
6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The radiation effect is basically negligible.



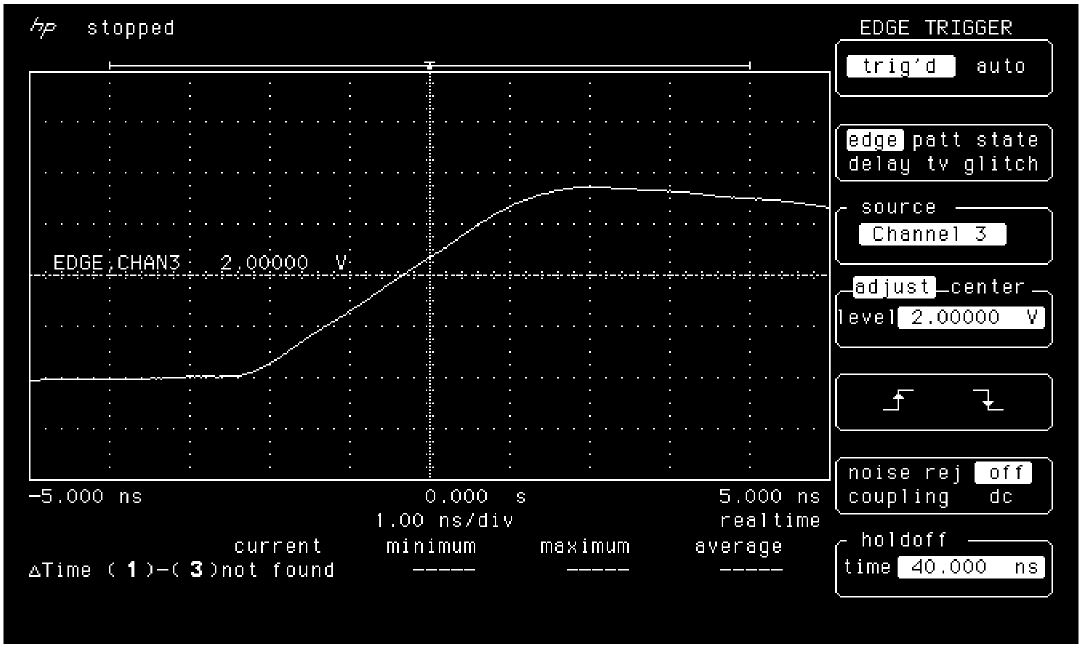
current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 6a. Rising edge of LAN4403 pre-irradiation.



current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 6b. Rising edge of LAN4403 post-annealing.



EDGE,CHAN3 : 2.00000 V

source Channel 3

level 2.00000 V

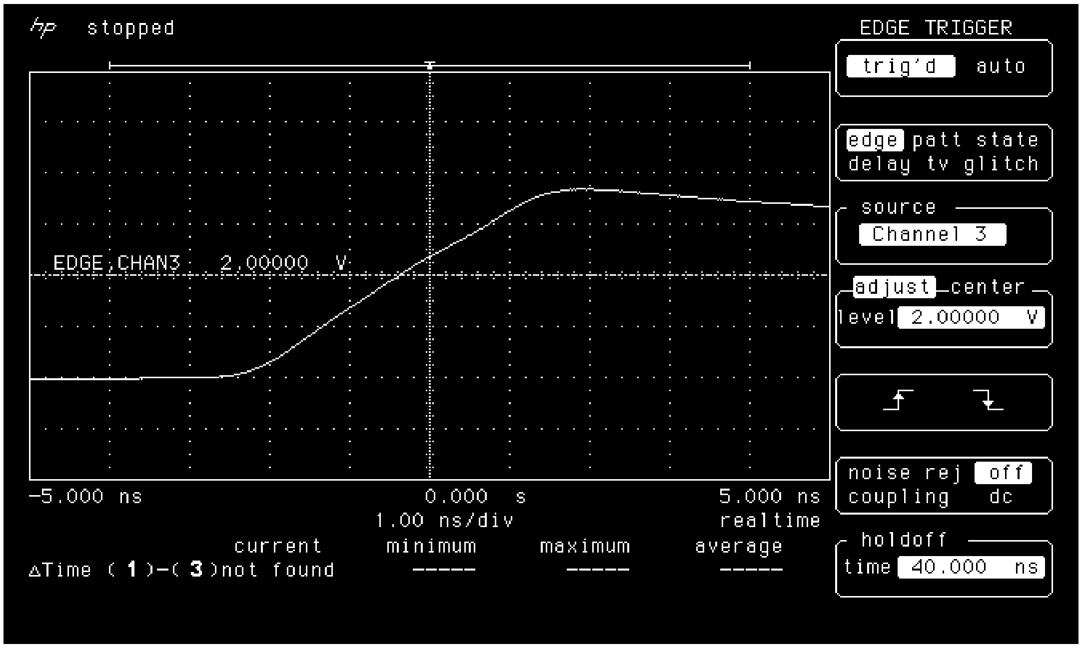
coupling dc

holdoff time 40.000 ns

1.00 ns/div realtime

	current	minimum	maximum	average
ΔTime (1)-(3)	not found	-----	-----	-----

Figure 7a. Rising edge of LAN4404 pre-irradiation.



EDGE,CHAN3 : 2.00000 V

source Channel 3

level 2.00000 V

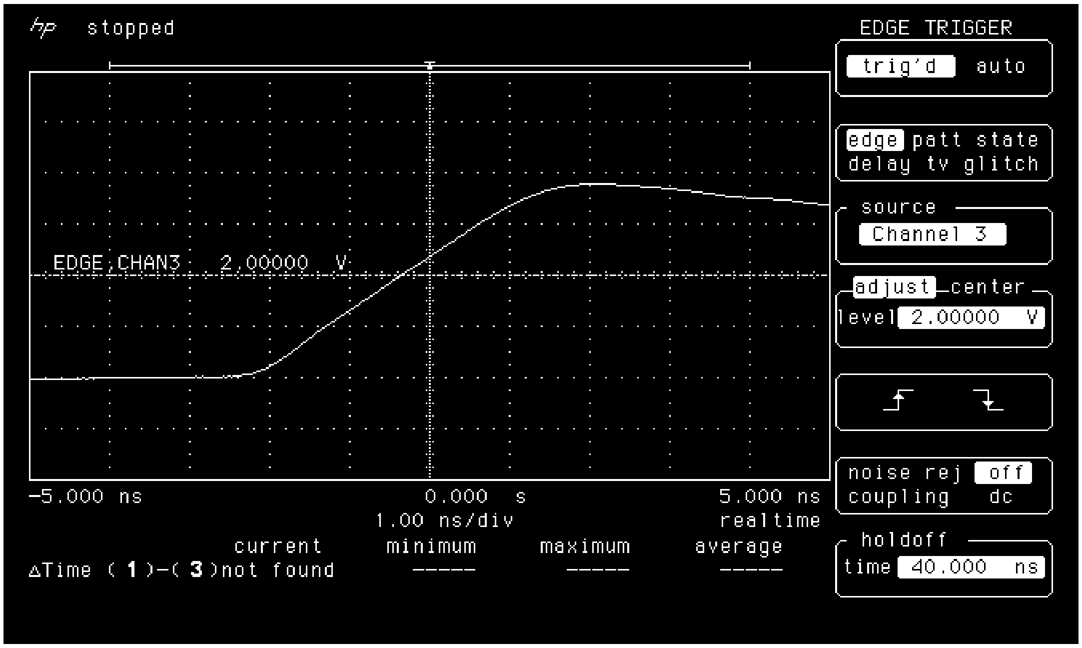
coupling dc

holdoff time 40.000 ns

1.00 ns/div realtime

	current	minimum	maximum	average
ΔTime (1)-(3)	not found	-----	-----	-----

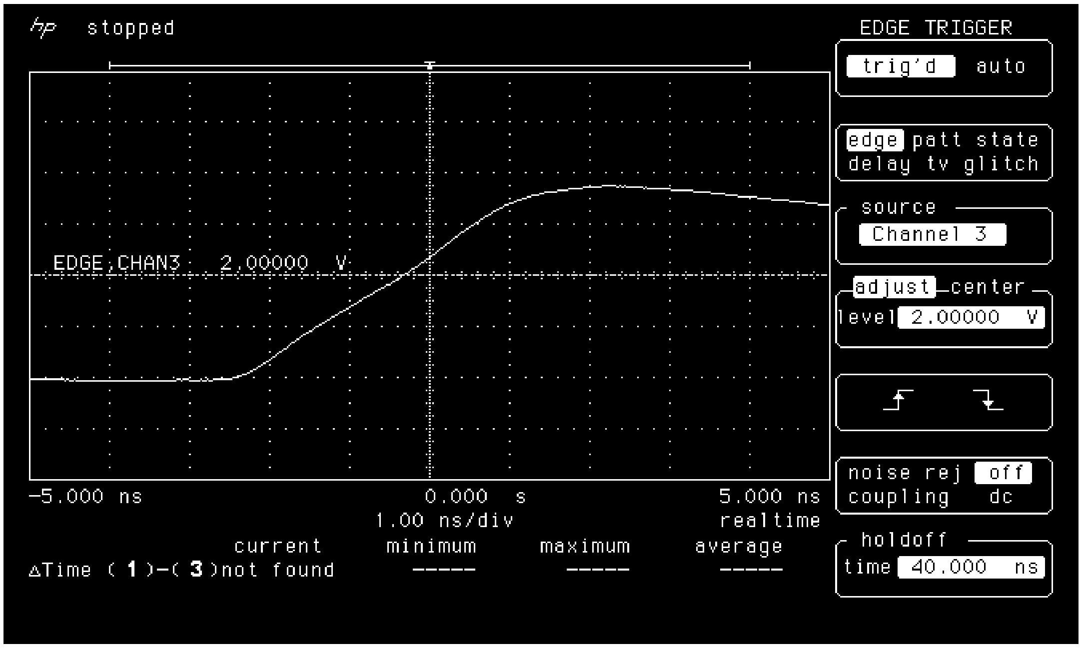
Figure 7b. Rising edge of LAN4404 post-annealing.



```
stopped                                                    EDGE TRIGGER
                                                           trig'd   auto
                                                           edge patt state
                                                           delay tv glitch
                                                           source
  EDGE,CHAN3 :  2.00000  V                                 Channel 3
                                                           adjust center
                                                           level 2.00000  V

                                                           noise rej  off
-5.000 ns                  0.000  s          5.000 ns     coupling    dc
                        1.00 ns/div          realtime
                 current   minimum   maximum   average     holdoff
ΔTime ( 1 )-( 3 )not found  -----     -----     -----      time 40.000  ns
```

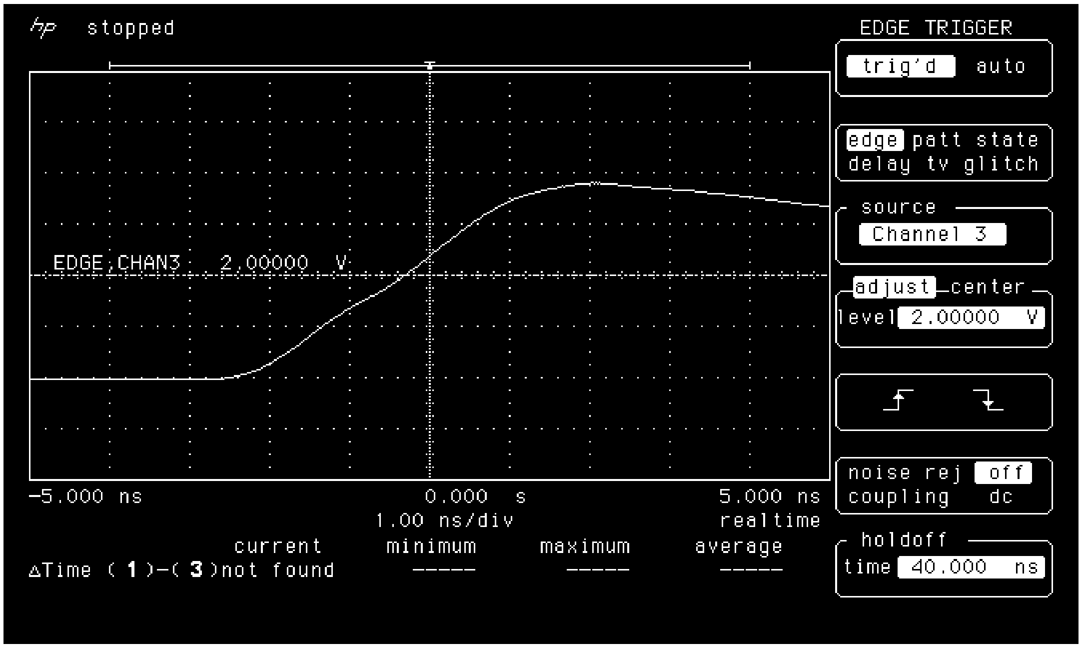
Figure 8a. Rising edge of LAN4405 pre-irradiation.



```
stopped                                                    EDGE TRIGGER
                                                           trig'd   auto
                                                           edge patt state
                                                           delay tv glitch
                                                           source
  EDGE,CHAN3 :  2.00000  V                                 Channel 3
                                                           adjust center
                                                           level 2.00000  V

                                                           noise rej  off
-5.000 ns                  0.000  s          5.000 ns     coupling    dc
                        1.00 ns/div          realtime
                 current   minimum   maximum   average     holdoff
ΔTime ( 1 )-( 3 )not found  -----     -----     -----      time 40.000  ns
```

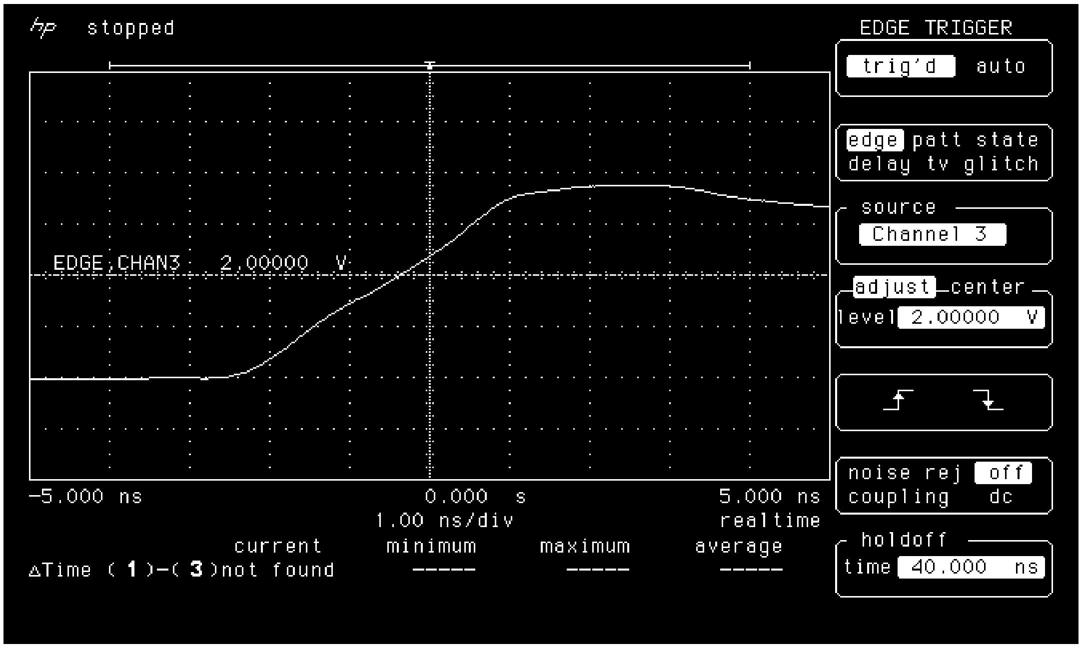
Figure 8b. Rising edge of LAN4405 post-annealing.



EDGE;CHAN3 : 2.00000 V
source Channel 3
level 2.00000 V
noise rej off
coupling dc
holdoff time 40.000 ns

```
                         current   minimum   maximum   average
ΔTime ( 1 )-( 3 )not found   -----     -----     -----
```

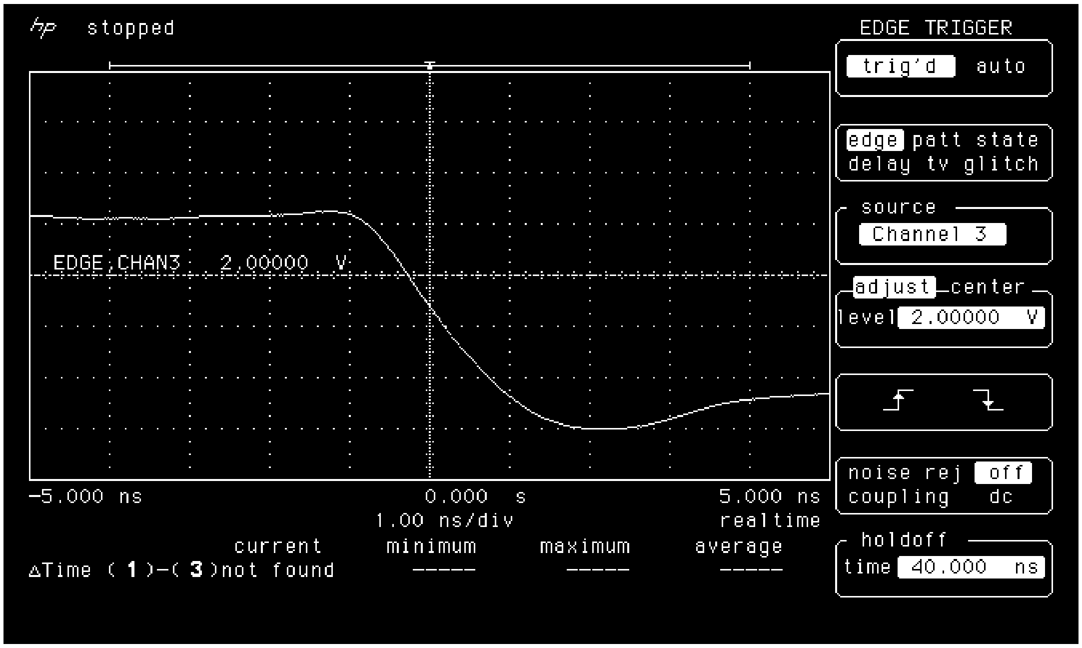
Figure 9a. Rising edge of LAN4406 pre-irradiation.



EDGE;CHAN3 : 2.00000 V
source Channel 3
level 2.00000 V
noise rej off
coupling dc
holdoff time 40.000 ns

```
                         current   minimum   maximum   average
ΔTime ( 1 )-( 3 )not found   -----     -----     -----
```

Figure 9b. Rising edge of LAN4406 post-annealing



EDGE;CHAN3 : 2.00000 V

Channel 3

level 2.00000 V

noise rej off

coupling dc

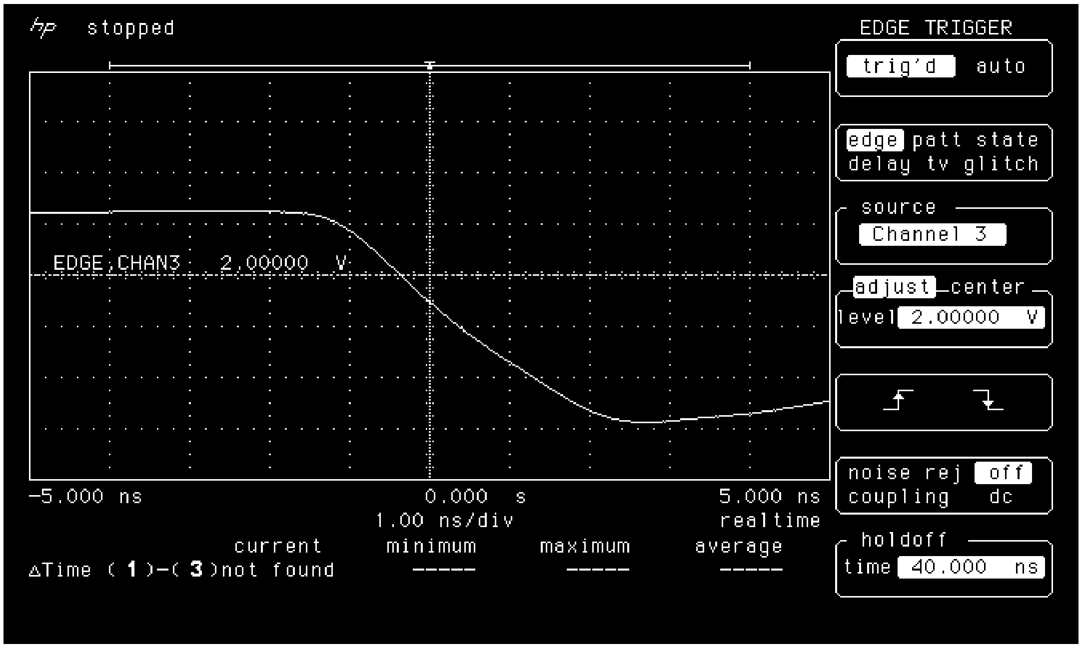
holdoff time 40.000 ns

-5.000 ns 0.000 s 5.000 ns

1.00 ns/div realtime

```
                   current     minimum    maximum    average
ΔTime ( 1 )-( 3 )not found     -----      -----      -----
```

Figure 10a. Falling edge of LAN4403 pre-irradiation



EDGE;CHAN3 : 2.00000 V

Channel 3

level 2.00000 V

noise rej off

coupling dc

holdoff time 40.000 ns

-5.000 ns 0.000 s 5.000 ns

1.00 ns/div realtime

```
                   current     minimum    maximum    average
ΔTime ( 1 )-( 3 )not found     -----      -----      -----
```

Figure 10b. Falling edge of LAN4403 post-annealing.

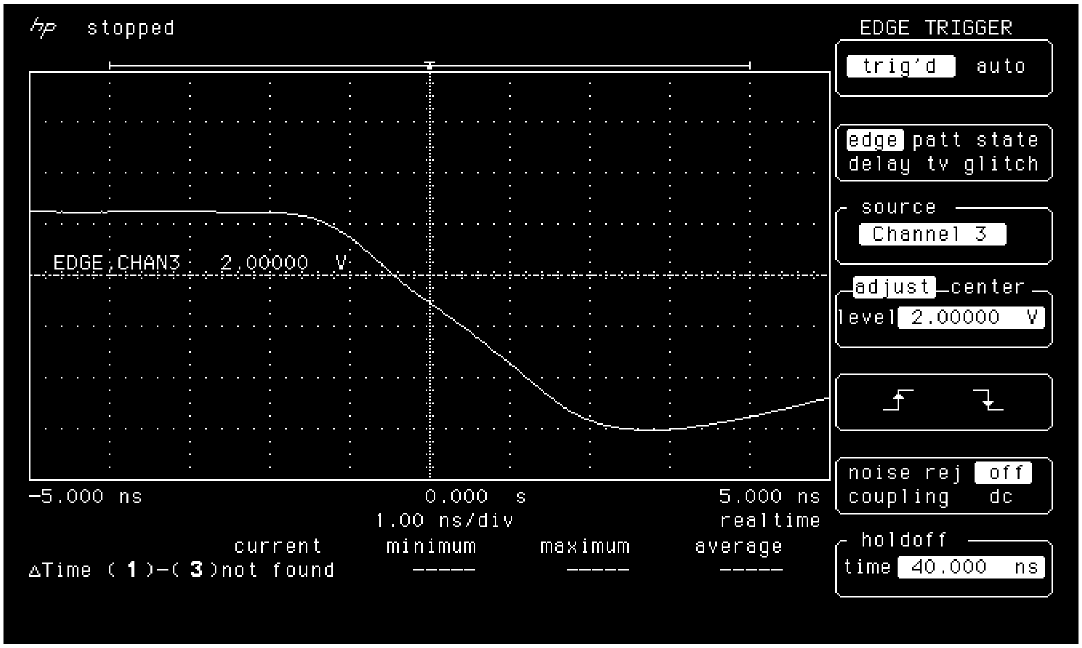


Figure 11a. Falling edge of LAN4404 pre-irradiation.

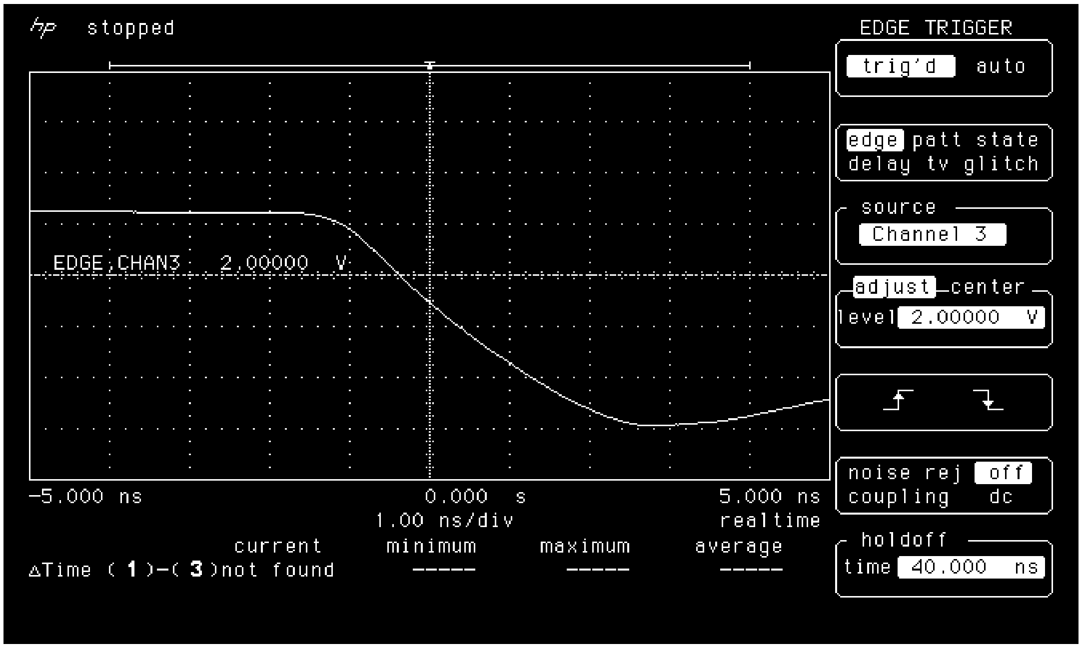
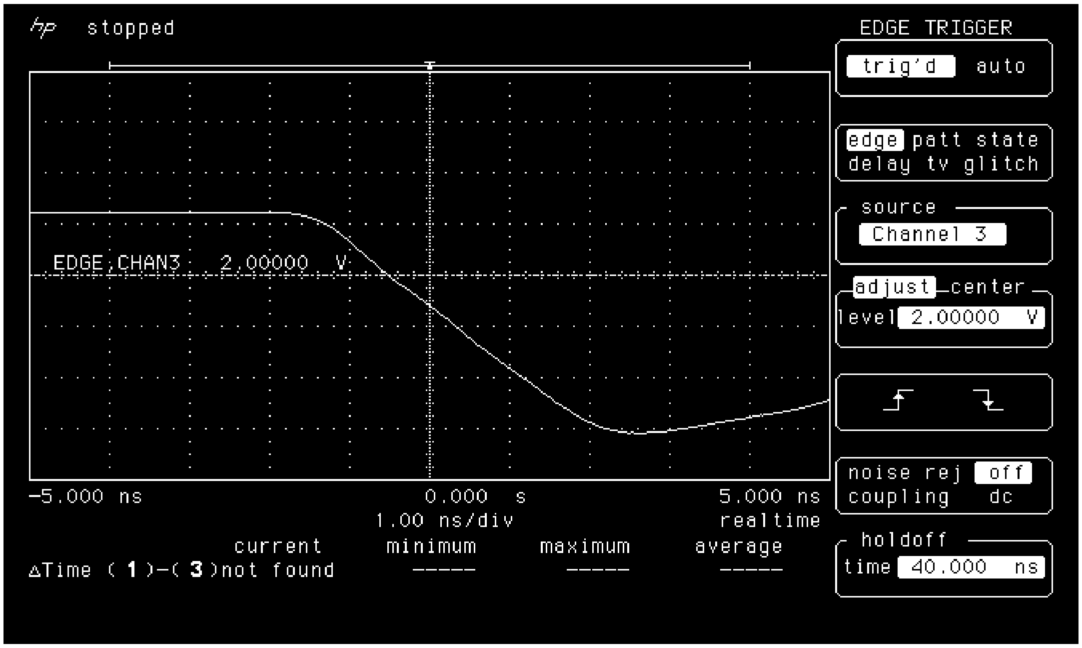
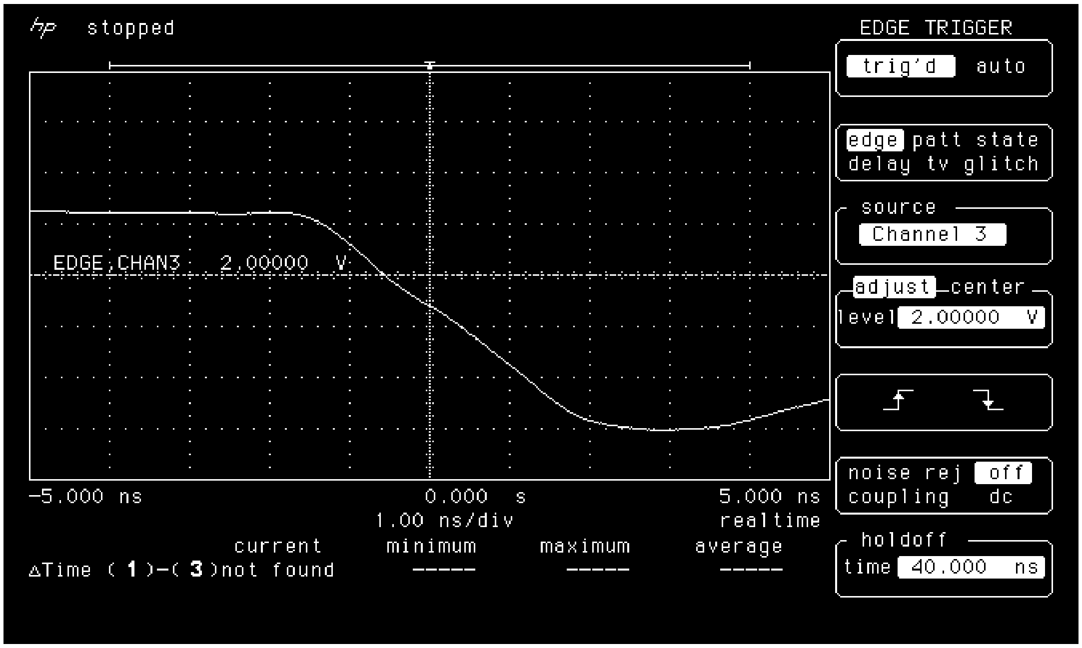


Figure 11b. Falling edge of LAN4404 post-annealing.



```
stopped                                              EDGE TRIGGER
                                                     trig'd  auto
                                                     edge patt state
                                                     delay tv glitch
                                                     source
                                                      Channel 3
 EDGE,CHAN3 :  2.00000  V                            adjust center
                                                     level 2.00000 V
                                                     noise rej  off
                                                     coupling   dc
                 current   minimum   maximum   average   holdoff
ΔTime ( 1 )-( 3 )not found   -----     -----     -----   time  40.000  ns
```

Figure 12a. Falling edge of LAN4405 pre-irradiation.



```
stopped                                              EDGE TRIGGER
                                                     trig'd  auto
                                                     edge patt state
                                                     delay tv glitch
                                                     source
                                                      Channel 3
 EDGE,CHAN3 :  2.00000  V                            adjust center
                                                     level 2.00000 V
                                                     noise rej  off
                                                     coupling   dc
                 current   minimum   maximum   average   holdoff
ΔTime ( 1 )-( 3 )not found   -----     -----     -----   time  40.000  ns
```

Figure 12b. Falling edge of LAN4405 post-annealing.

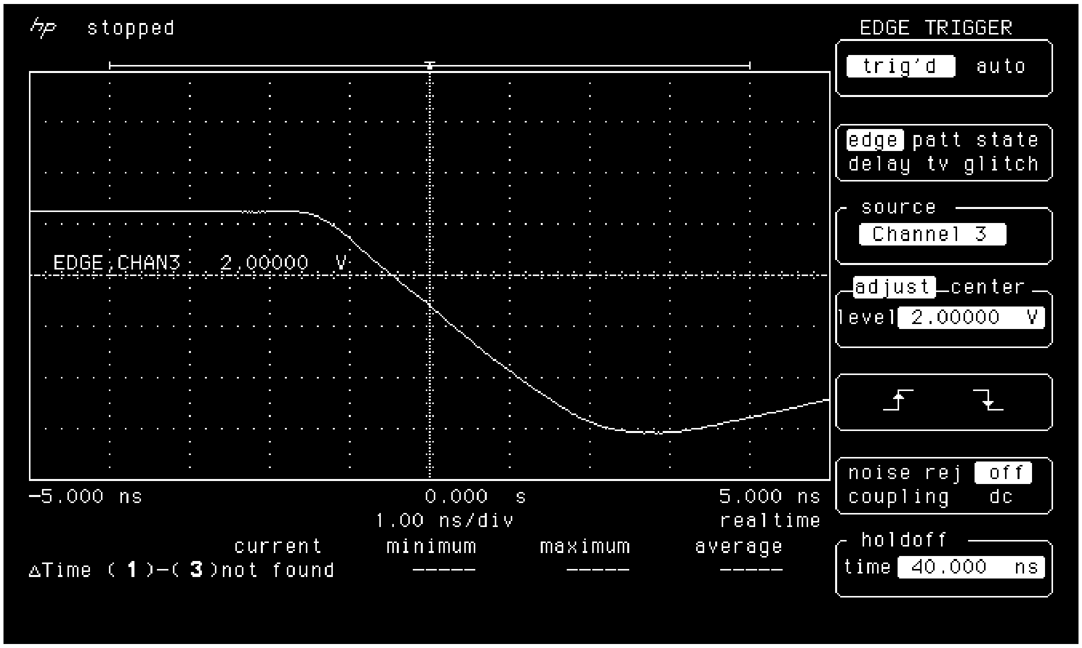


Figure 13a. Falling edge of LAN4406 pre-irradiation

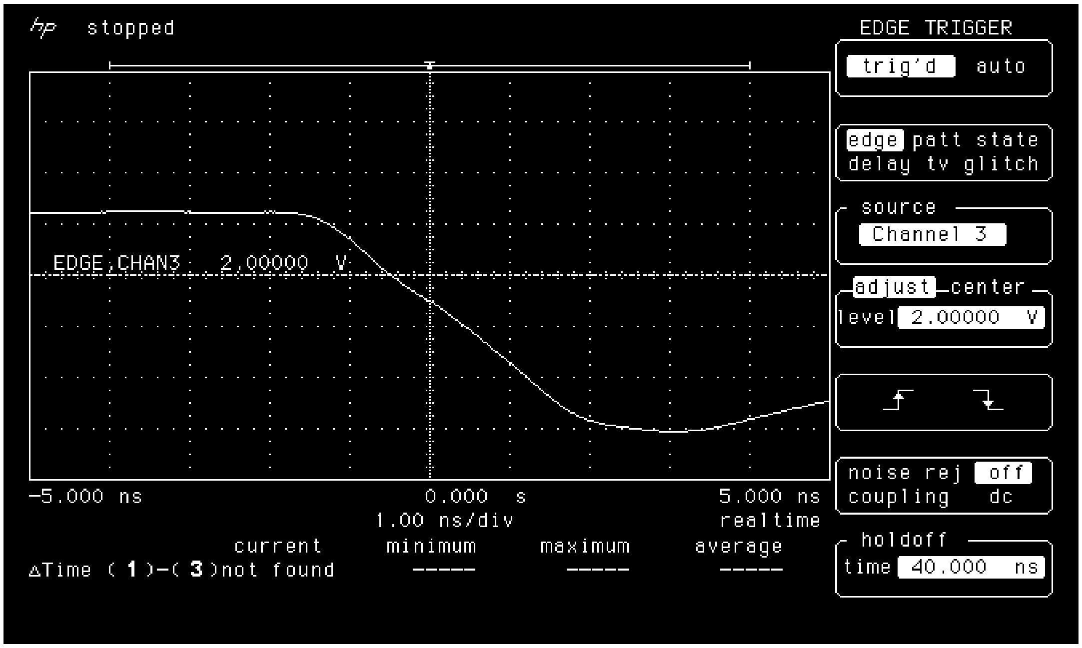
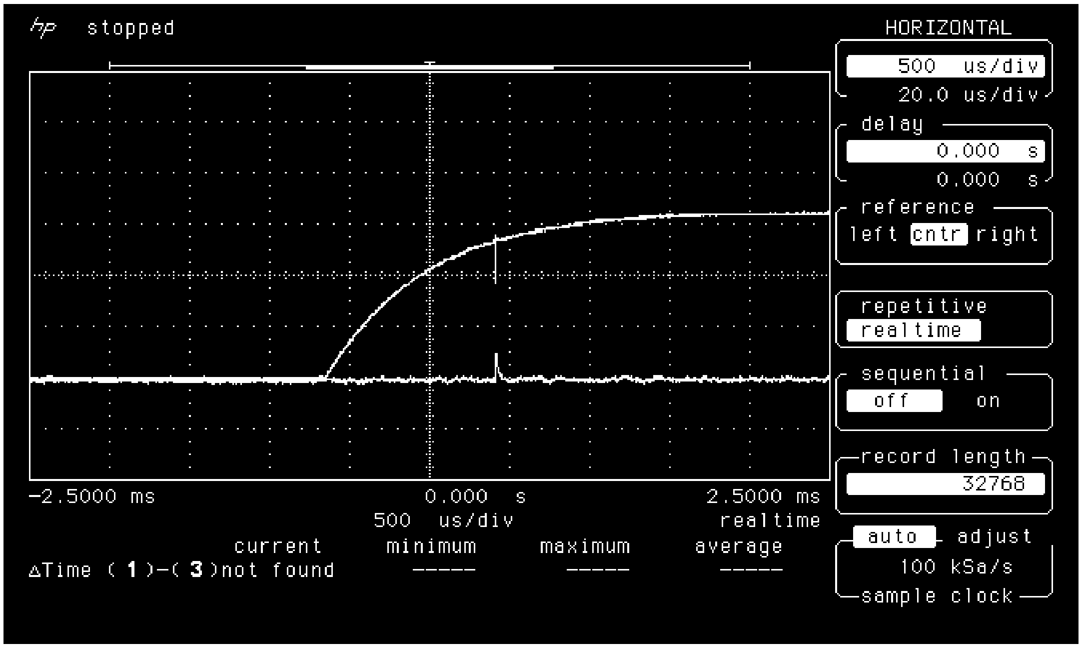


Figure 13b. Falling edge of LAN4406 post-annealing

7) Power-Up Transient

In each measurement, the rise time of the power supply voltage (V_{CC}) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 13-17 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 3.3V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. Post 80krad(Si) irradiation/annealing DUTs have a radiation induced transient current during power up (see, for example, Figure 13b). However, this transient is very minute. In most case, it can be annealed out completely if annealing time is long enough. Power-up transient current issue has been previously published in RADECS ("Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278.)

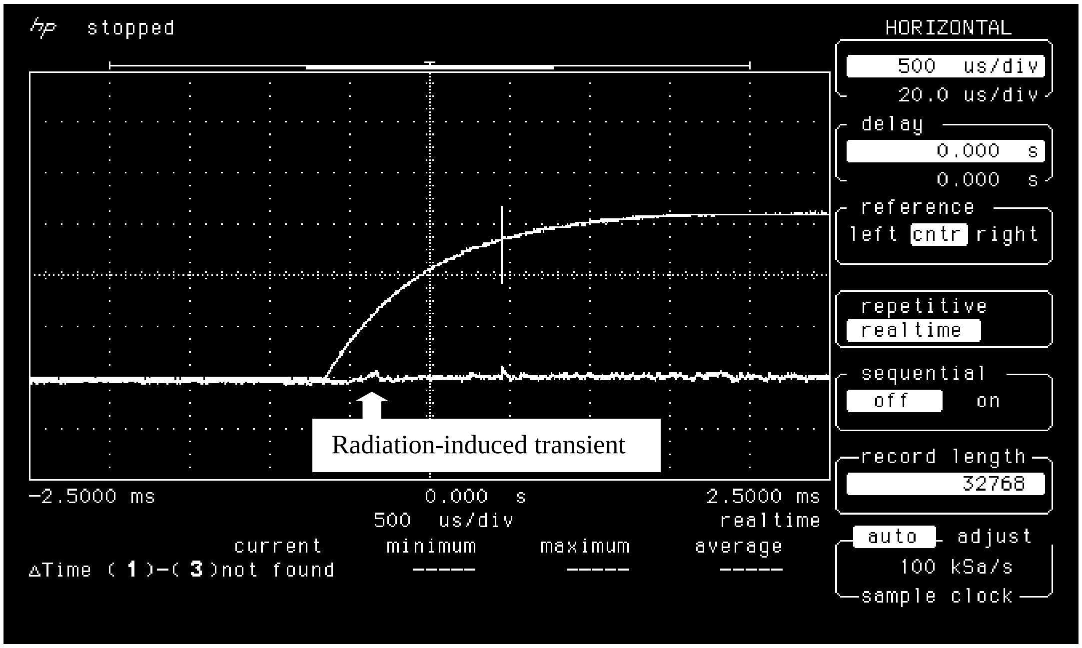


stopped

HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 32768
auto adjust
100 kSa/s
sample clock

-2.5000 ms 0.000 s 2.5000 ms
500 us/div realtime
current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 14a. Power-up transient of LAN4403 pre-irradiation.



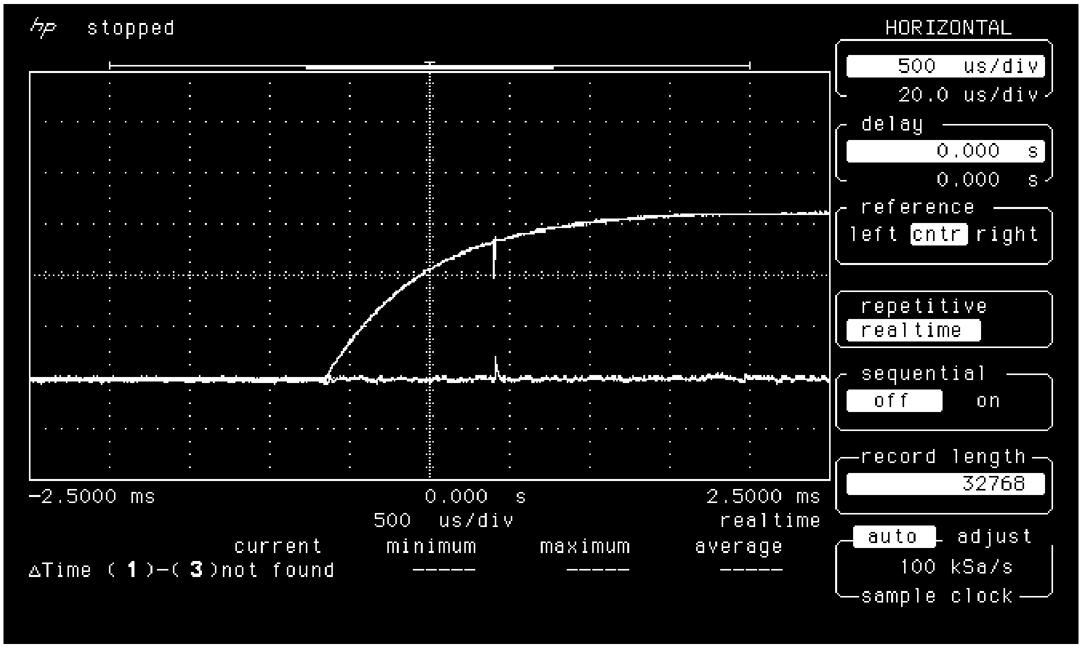
stopped

HORIZONTAL
500 us/div
20.0 us/div
delay 0.000 s
0.000 s
reference left cntr right
repetitive realtime
sequential off on
record length 32768
auto adjust
100 kSa/s
sample clock

-2.5000 ms 0.000 s 2.5000 ms
500 us/div realtime
current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Radiation-induced transient

Figure 14b. Power-up transient of LAN4403 post-annealing.

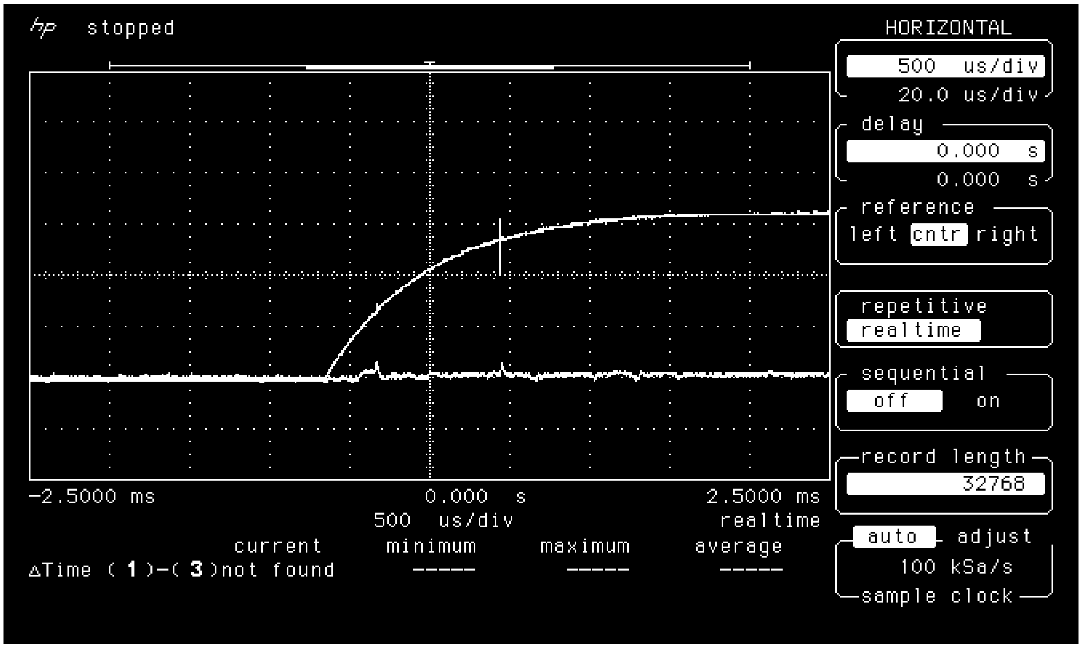


stopped

HORIZONTAL
500 us/div
20.0 us/div
delay
0.000 s
0.000 s
reference
left cntr right
repetitive
realtime
sequential
off on
record length
32768
auto adjust
100 kSa/s
sample clock

current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 15a. Power-up transient of LAN4404 pre-irradiation.



stopped

HORIZONTAL
500 us/div
20.0 us/div
delay
0.000 s
0.000 s
reference
left cntr right
repetitive
realtime
sequential
off on
record length
32768
auto adjust
100 kSa/s
sample clock

current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 15b. Power-up transient of LAN4404 post-annealing.

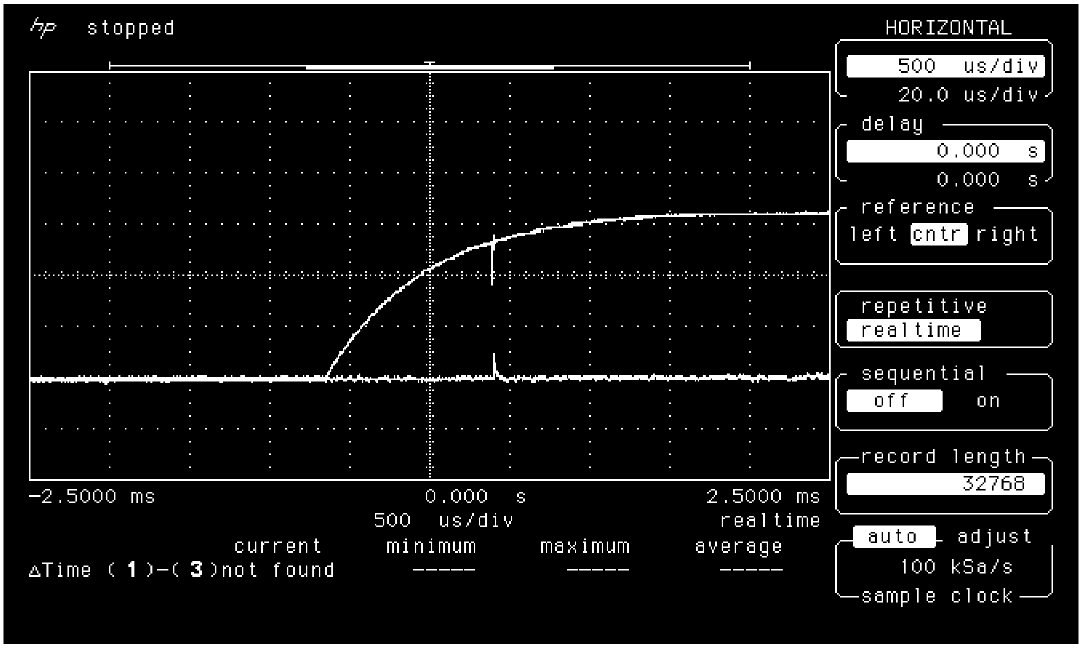


Figure 16a. Power-up transient of LAN4405 pre-irradiation.

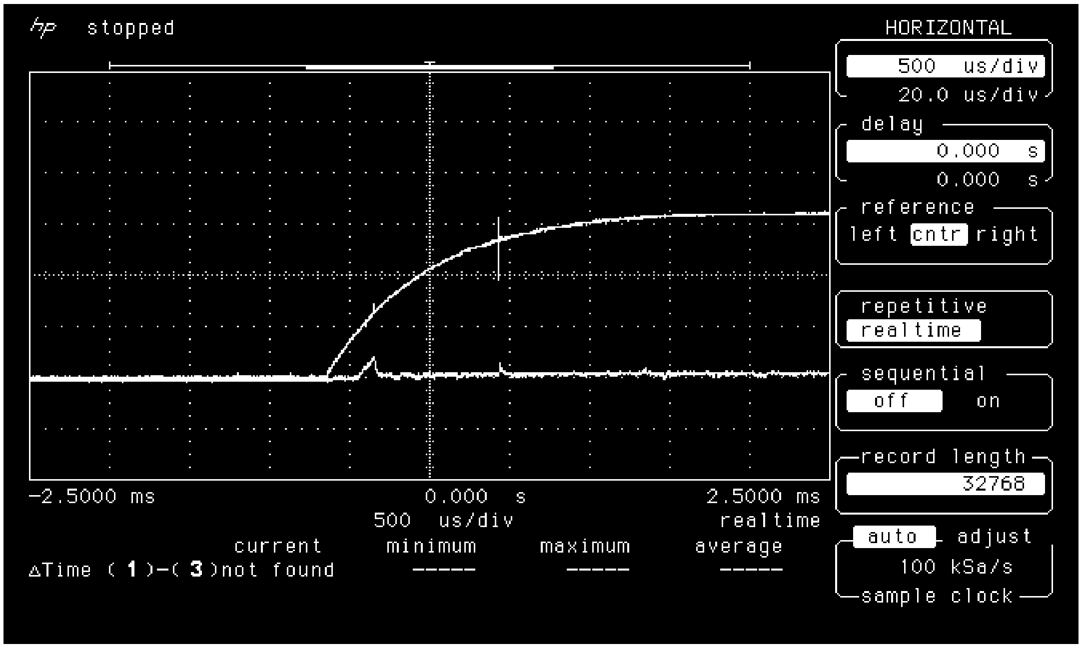
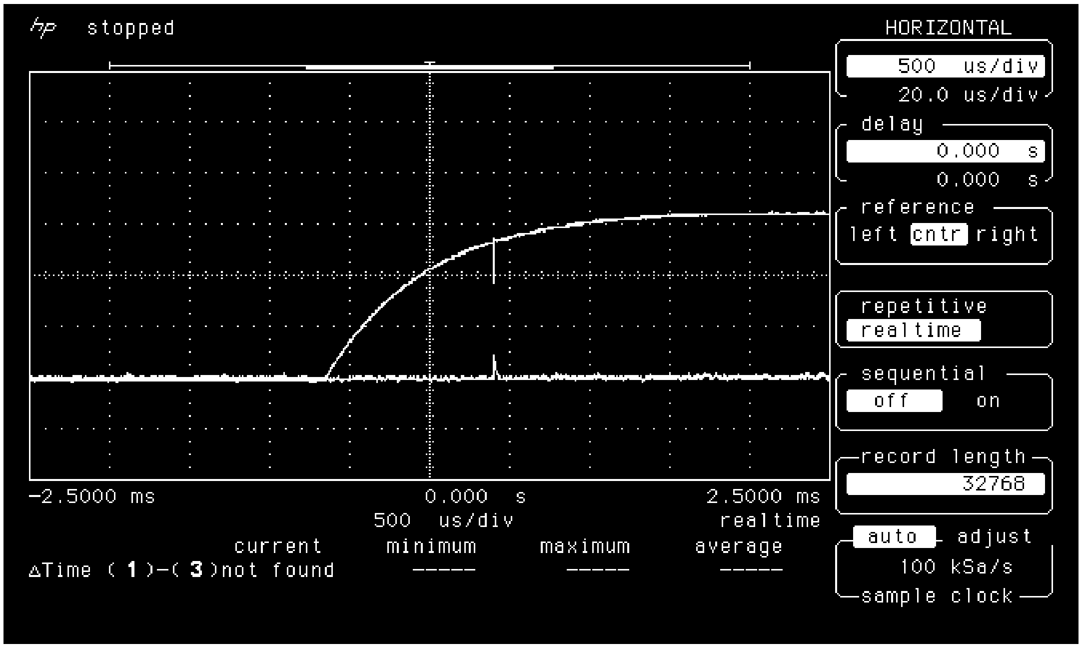
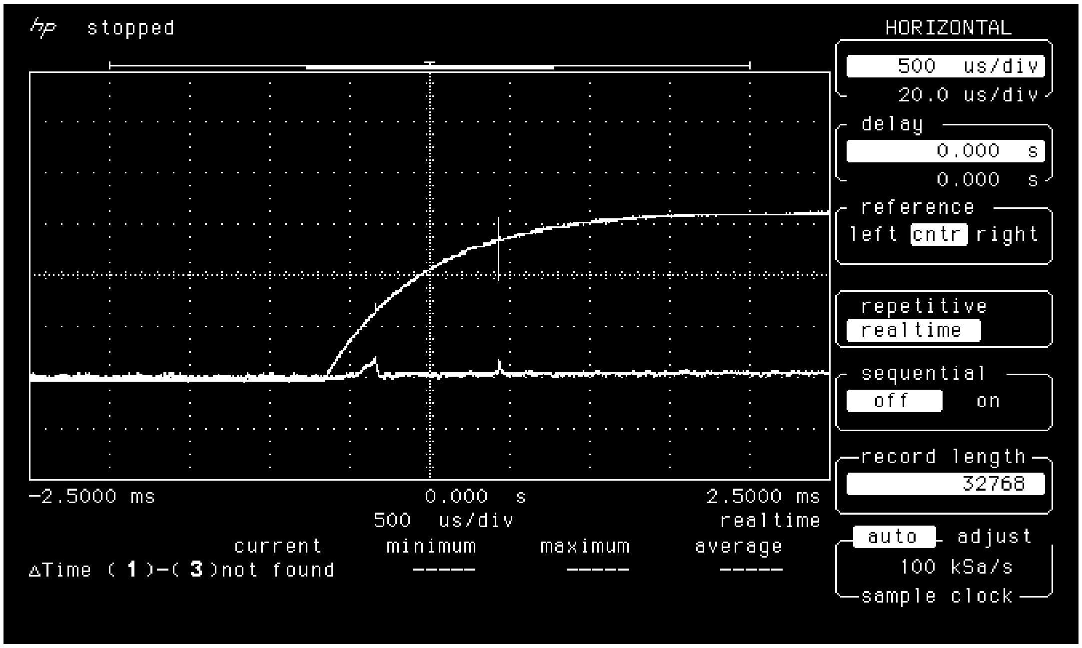


Figure 16b. Power-up transient of LAN4405 post-annealing.



stopped
HORIZONTAL
500 us/div
20.0 us/div
delay
0.000 s
0.000 s
reference
left cntr right
repetitive
realtime
sequential
off on
record length
32768
auto adjust
100 kSa/s
sample clock
-2.5000 ms
0.000 s
2.5000 ms
500 us/div
realtime
current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 17a. Power-up transient of LAN4406 pre-irradiation



stopped
HORIZONTAL
500 us/div
20.0 us/div
delay
0.000 s
0.000 s
reference
left cntr right
repetitive
realtime
sequential
off on
record length
32768
auto adjust
100 kSa/s
sample clock
-2.5000 ms
0.000 s
2.5000 ms
500 us/div
realtime
current minimum maximum average
ΔTime (1)-(3)not found ----- ----- -----

Figure 17b. Power-up transient of LAN4406 post-annealing