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TOTAL IONIZING DOSE TEST REPORT

No. 00T-RT14100-UCL082
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I. Summary Table

Parameters	Tolerance
1. Gross Functional	> 20krad(Si), exact number pending on customer's interest
2. $I_{DDSTDBY}$	Passed 20krad(Si)
3. V_{IL}/V_{IH}	Passed 20krad(Si)
4. V_{OL}/V_{OH}	Passed 20krad(Si)
5. Propagation Delays	Passed 20krad(Si)
6. Rising/Falling Edge Transient	Passed 20krad(Si)
7. Power-up Transient Current	Passed 20krad(Si)

II. Total Ionizing Dose (TID) Testing

This section describes the device(s) under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT14100A
Package	CQFP256
Foundry	MEC
Technology	0.8µm CMOS
Die Lot Number	UCL082
Quantity Tested	4
Serial Numbers	LAN3801, LAN3802, LAN3803, LAN3804

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA
Radiation Source	Co-60
Dose Rate	6krad(Si)/day (+-10%)
Final Total Dose	20krad(Si)
Temperature	Room
Bias	5.0V

C. Test Method

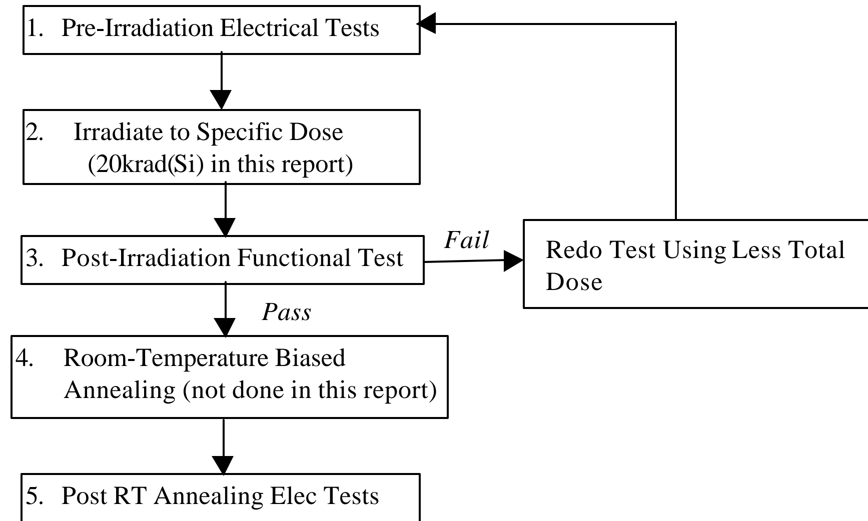

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and then parametric test. Gross functional test is included in this method. The method is in compliance with TM1019. Often biased room-temperature-annealing is used to simulate the low-dose-rate space environment. However, annealing is not performed in this report to save time. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This won't be logistically possible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. TEST RESULTS

A. *Method One: Irradiate to Gross Functional Failure*

This test was not performed in this report.

B. *Method Two: Irradiation and Parametric Test*

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post-irradiation (step 3) tests. Since $I_{DDstandby}$ is within the spec after 20krad(Si) irradiation (Figure 2), we didn't do room temperature annealing to save time.

1) Functional Test

Table 4 lists results of the functional test.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Irradiation
LAN3801	passed	passed
LAN3802	passed	passed
LAN3803	passed	passed
LAN3804	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation and room-temperature annealing. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation/annealing effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

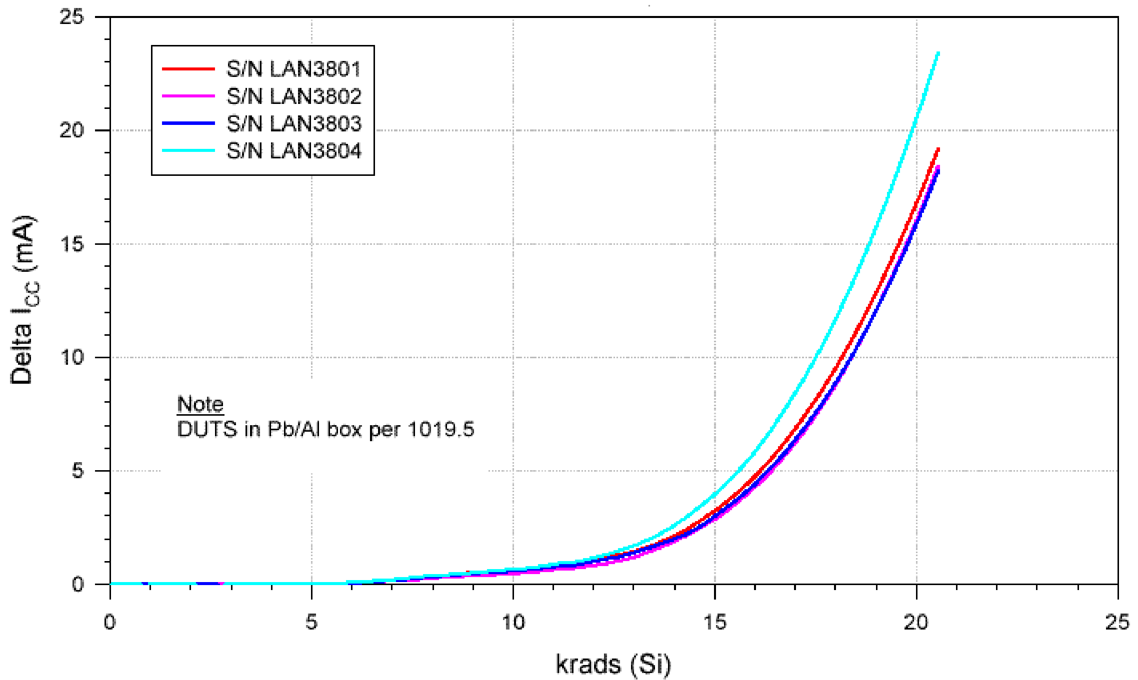

Figure 2. Delta $I_{DDstandby}$ versus total dose.

In Figure 2, DUT serialized LAN3801, LAN3802, LAN3803 and LAN3804 were irradiated to 20krad(Si). Every DUT has $I_{Ddstandby}$ below 25mA (the spec) after irradiation.

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-room-temperature annealing. The irradiated-and-annealed DUT is within the spec and the change for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results

	Pre-Irradiation	Post-Irradiation
LAN3801	1.27V	1.33V
LAN3802	1.27V	1.33V
LAN3803	1.27V	1.34V
LAN3804	1.27V	1.36V

4) Output Characteristic

Figure 3a and 3b show the V_{OL} characteristic curves for the pre-irradiated and post-irradiated DUT. All irradiated DUT are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 6mA, V_{OL} cannot exceed 0.4V.

Figure 4a and 4b show the V_{OH} characteristic curves for the pre-irradiated and post-irradiated DUT. All DUT passed the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 4mA, V_{OH} cannot be lower than 3.7V.

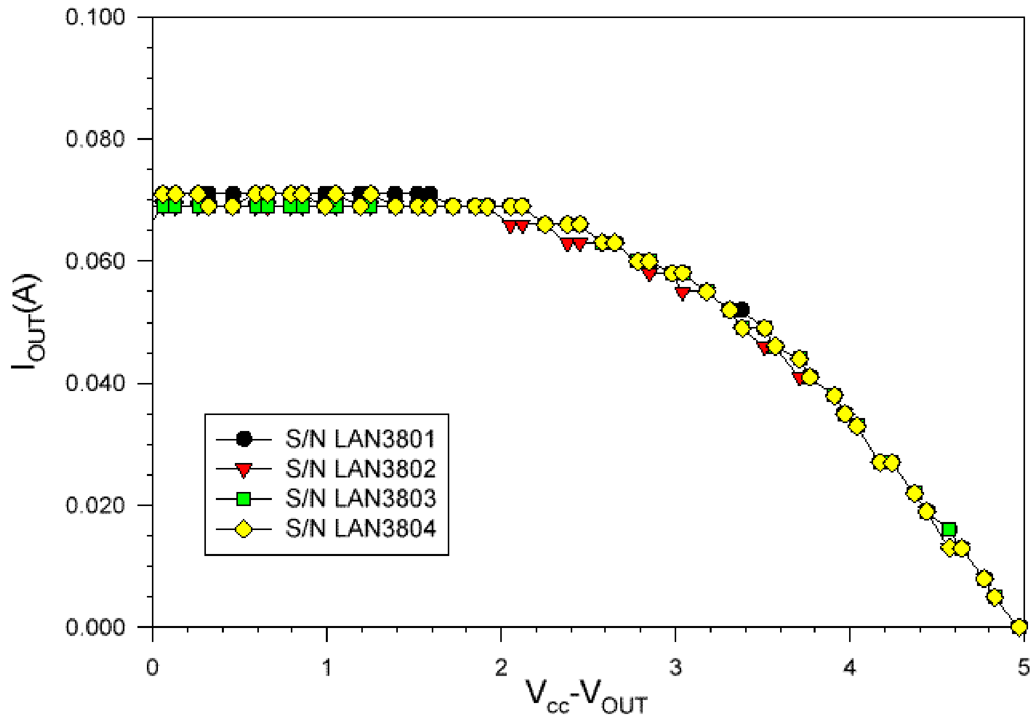

Figure 3a. Pre-irradiation V_{OL} characteristic curves.

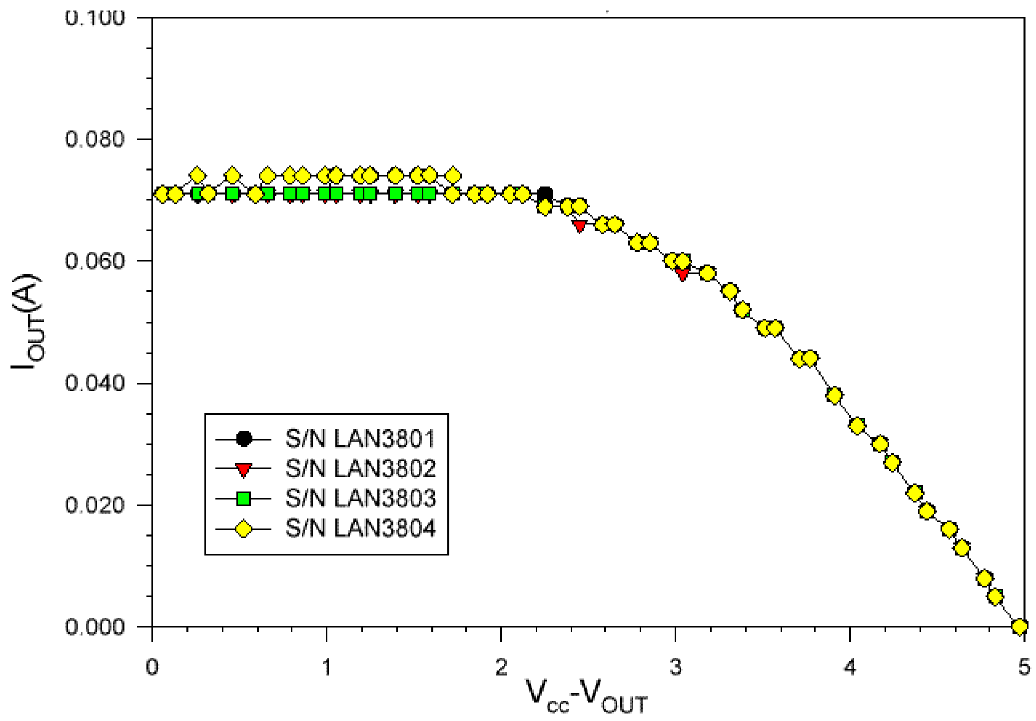

Figure 3b. Post-irradiation V_{OL} characteristic curves.

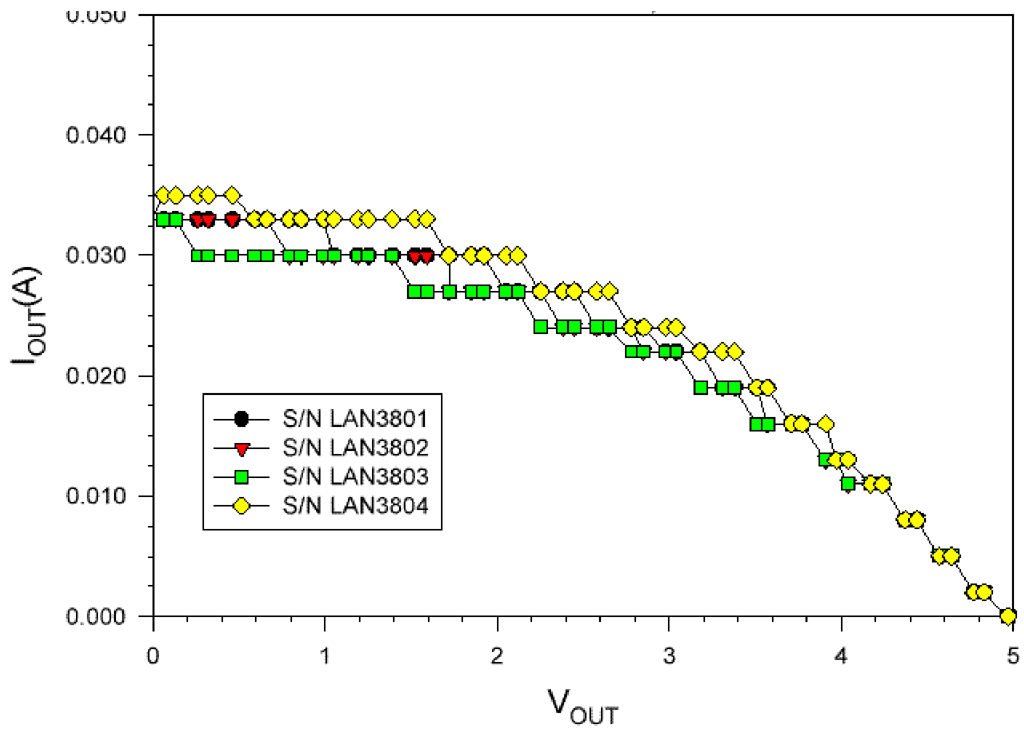

Figure 4a. Pre-irradiation V_{OH} characteristic curves.

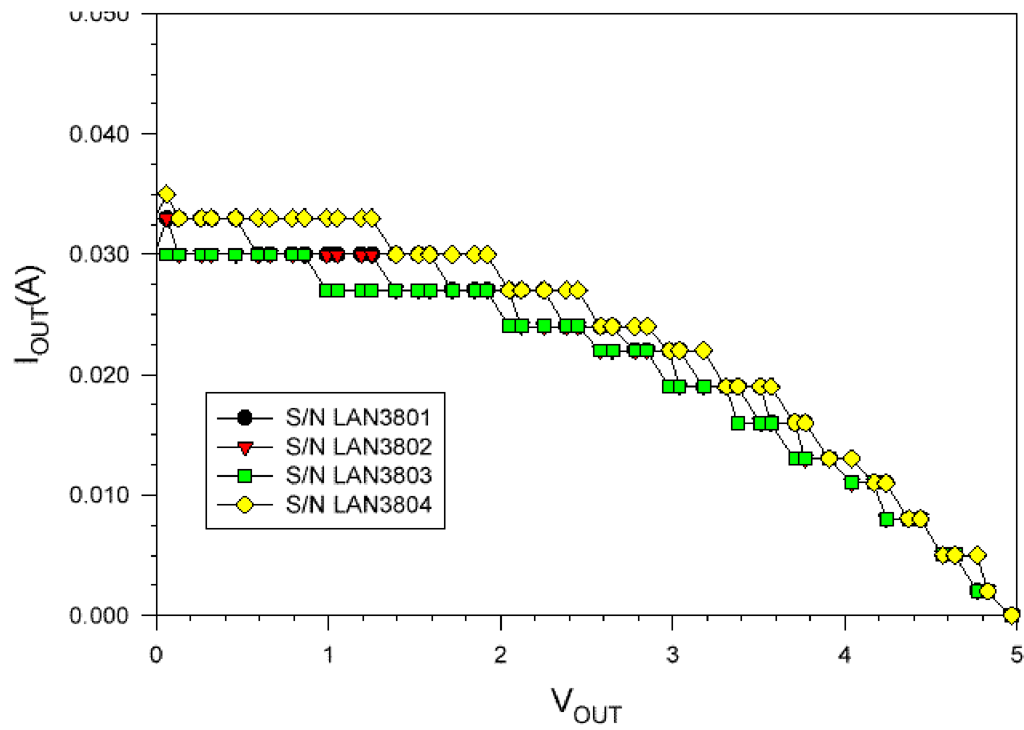

Figure 4b. Post-irradiation V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3801	903	936	903	924
LAN3802	909	946	909	933
LAN3803	913	951	912	939
LAN3804	900	936	900	923

Table 7. Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3801	<10	<10	<10	<10
LAN3802	<10	<10	<10	<10
LAN3803	<10	<10	<10	<10
LAN3804	<10	<10	<10	<10

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3801	<10	<10	<10	<10
LAN3802	<10	<10	<10	<10
LAN3803	<10	<10	<10	<10
LAN3804	<10	<10	<10	<10

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-irradiation. Figures 5-8 show the rising edge transient. Figures 9-12 show the falling edge transient. The radiation effect is basically negligible.

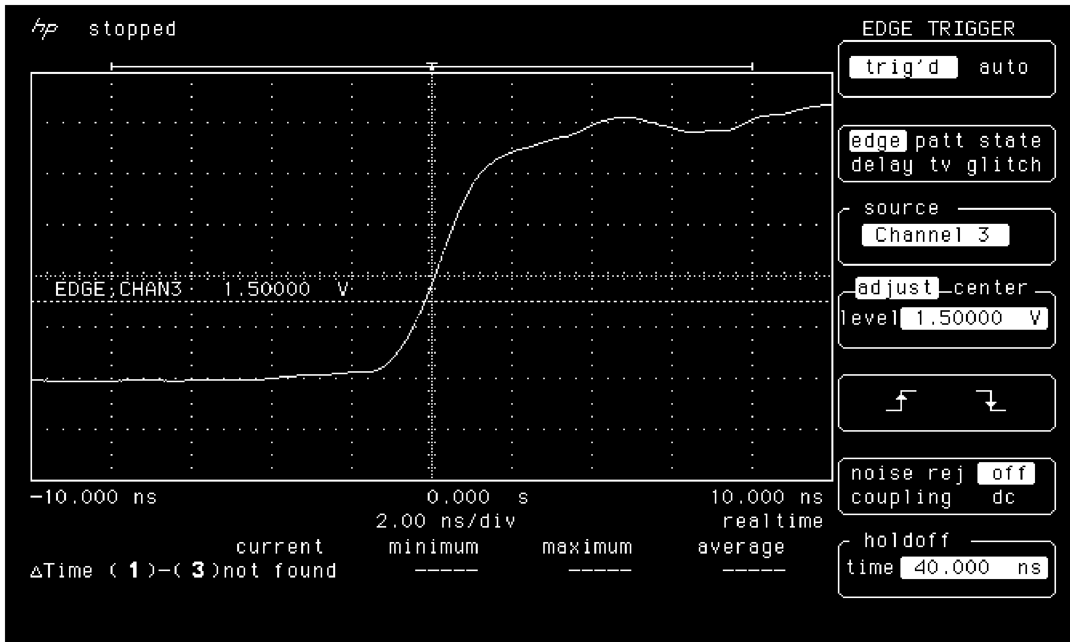

Figure 5a. Rising edge of LAN3801 pre-irradiation.

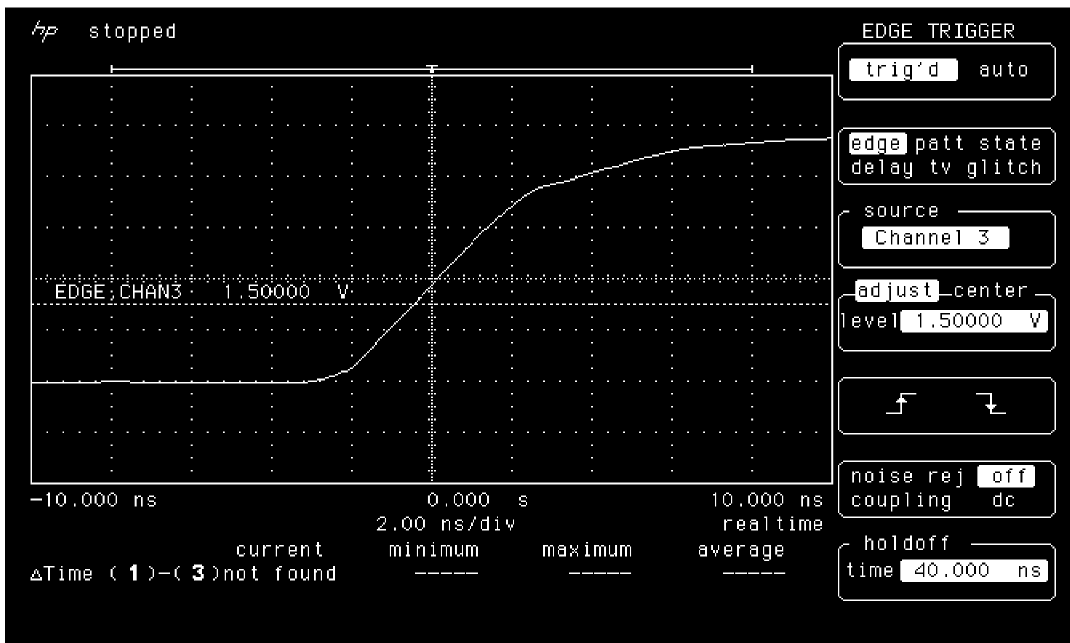

Figure 5b. Rising edge of LAN3801 post-irradiation.

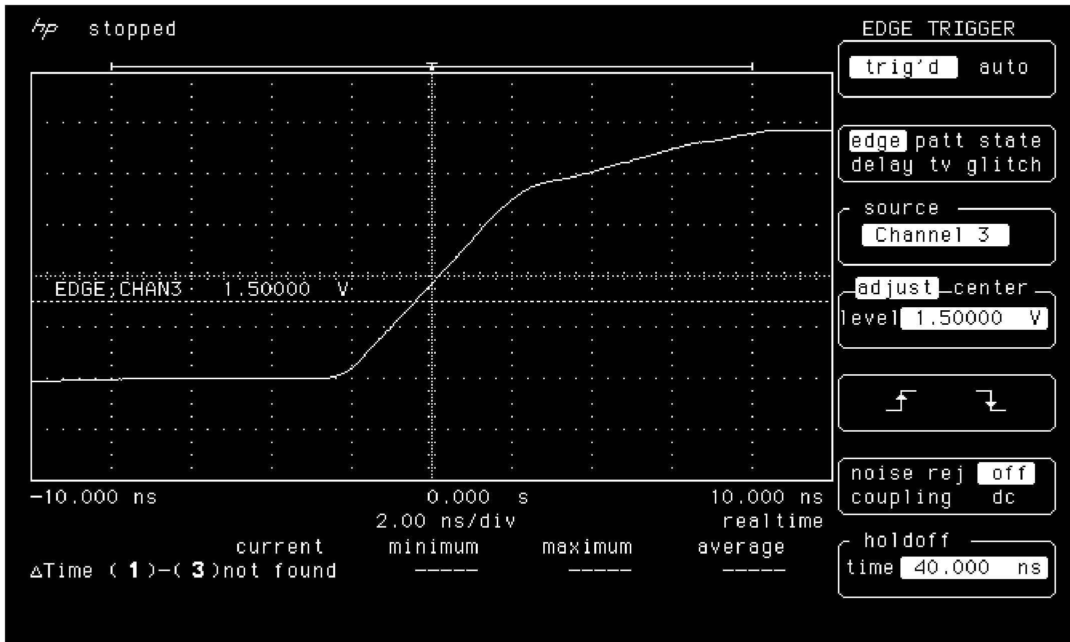

Figure 6a. Rising edge of LAN3802 pre-irradiation

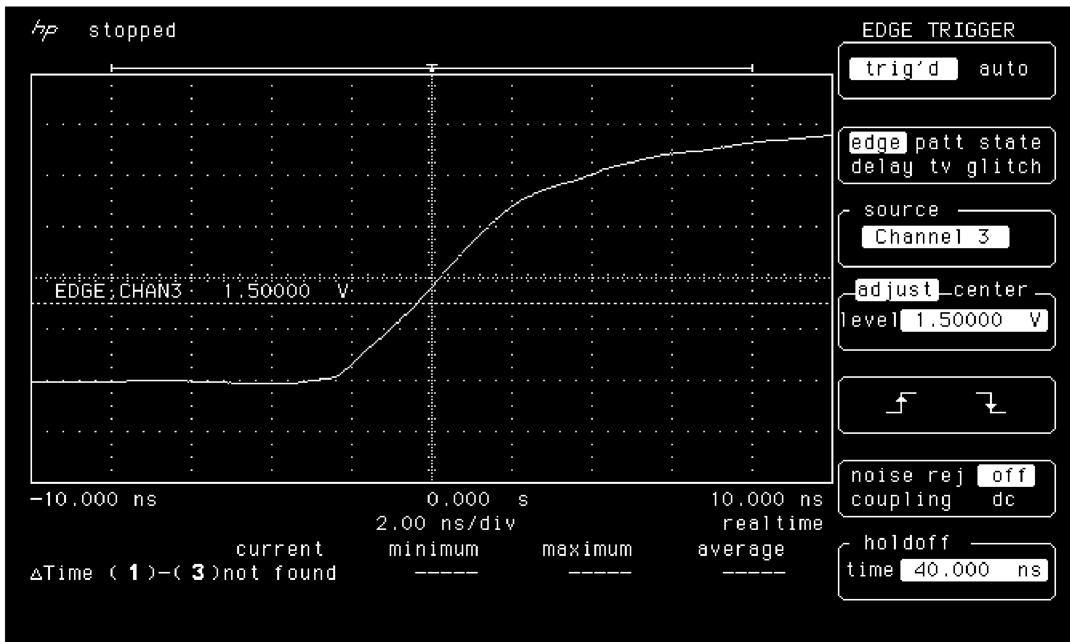

Figure 6b. Rising edge of LAN3802 post-irradiation

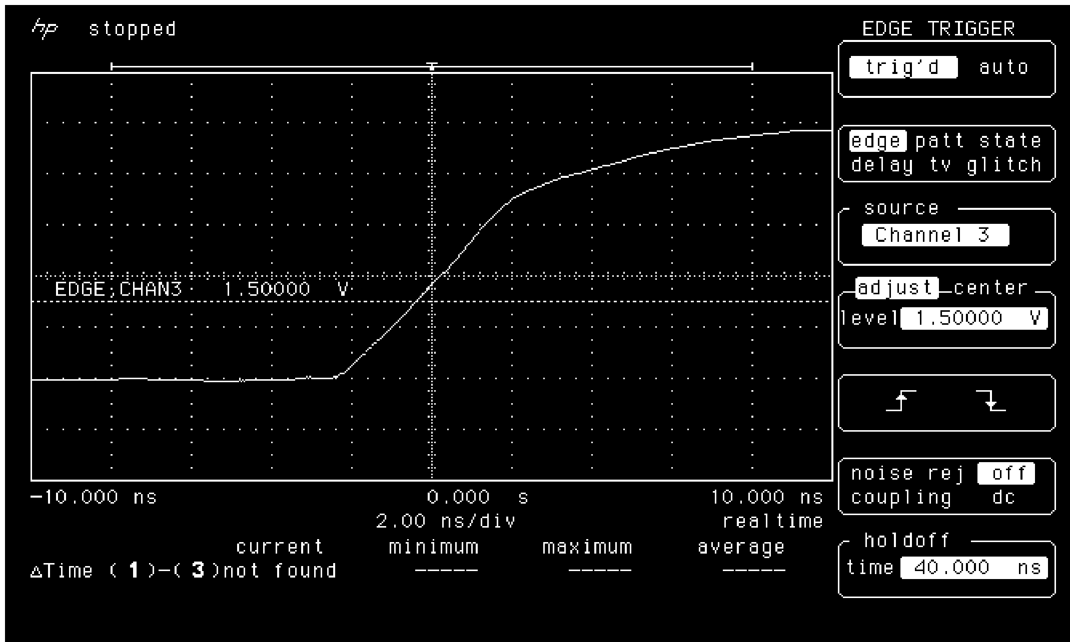

Figure 7a. Rising edge of LAN3803 pre-irradiation

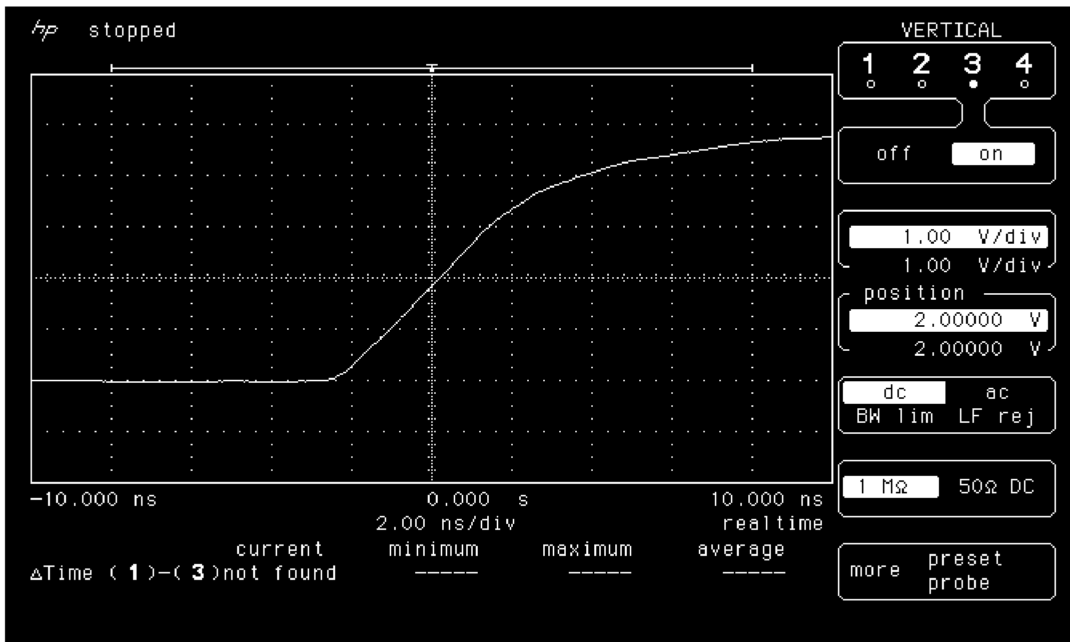

Figure 7b. Rising edge of LAN3803 post-irradiation

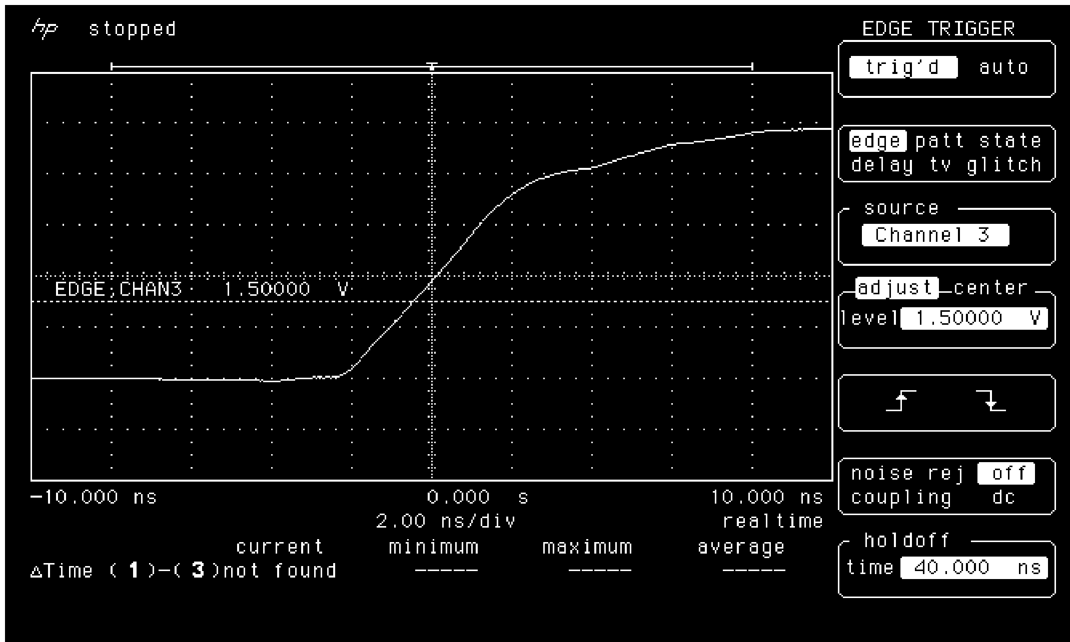

Figure 8a. Rising edge of LAN3804 pre-irradiation

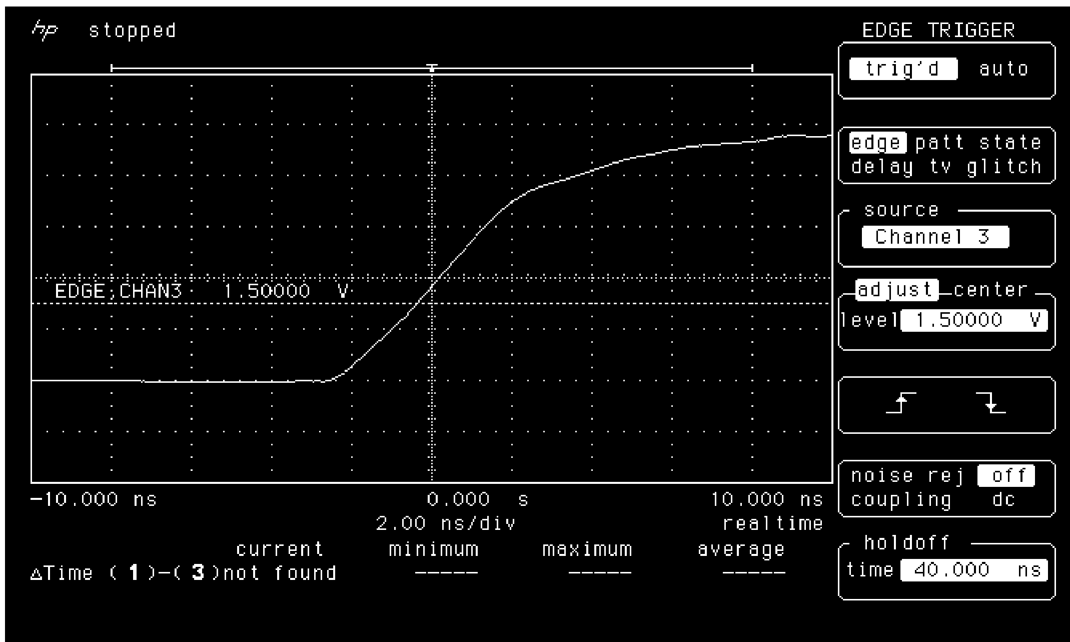

Figure 8b. Rising edge of LAN3804 post-irradiation

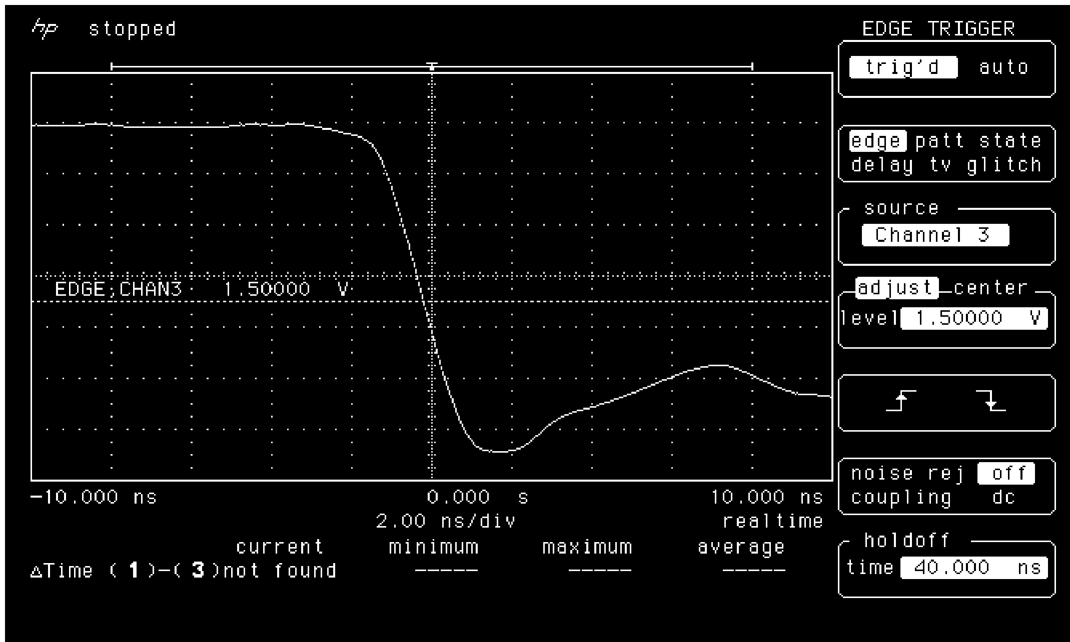

Figure 9a. Falling edge of LAN3801 pre-irradiation

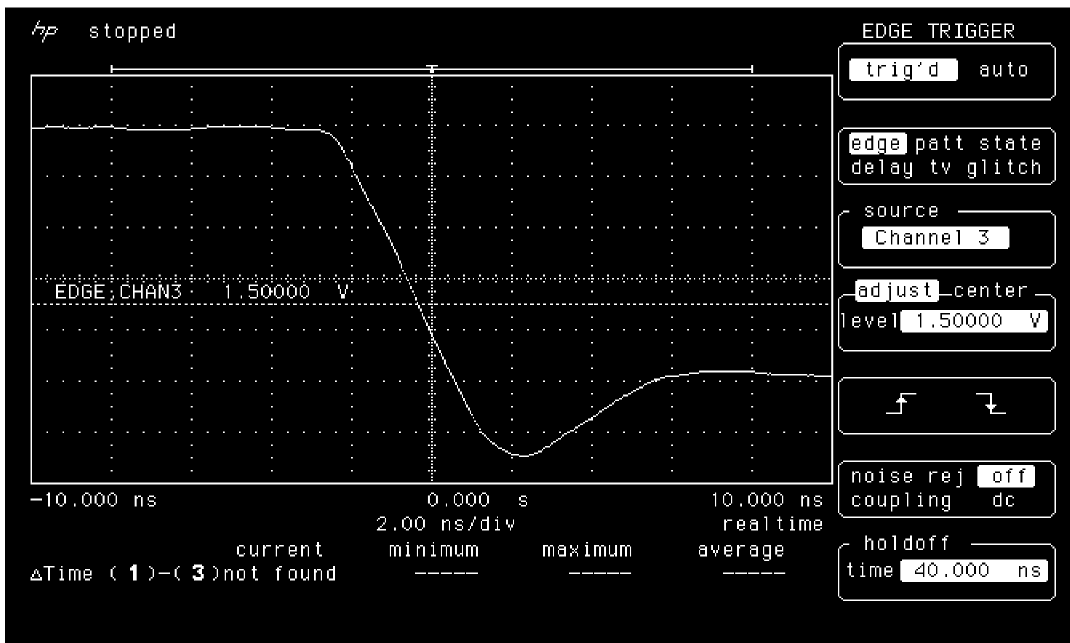

Figure 9b. Falling edge of LAN3801 post-irradiation.

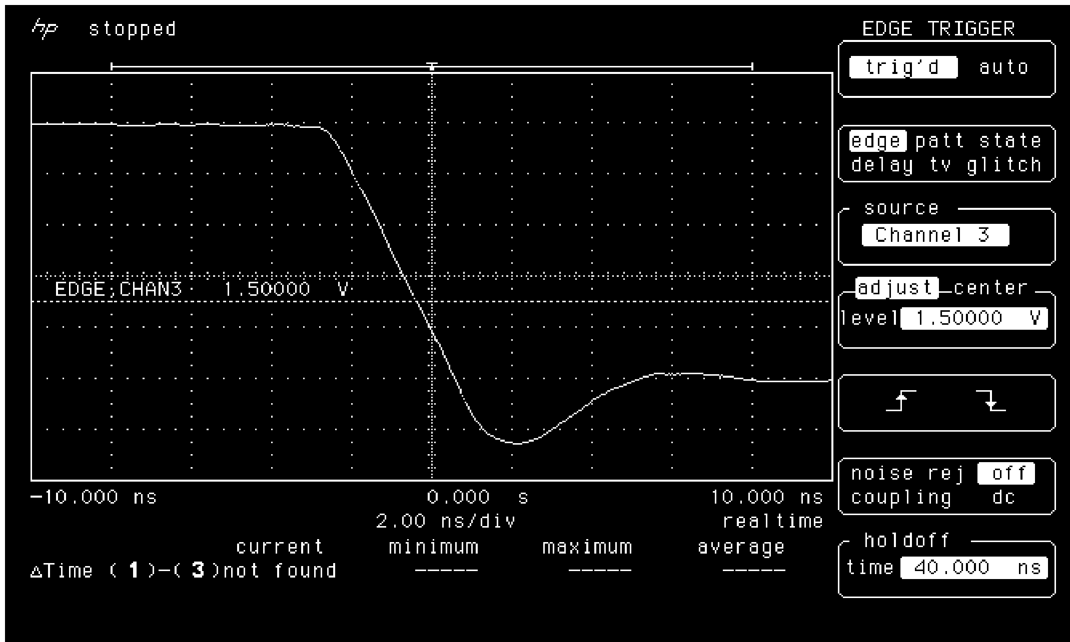

Figure 10a. Falling edge of LAN3802 pre-irradiation.

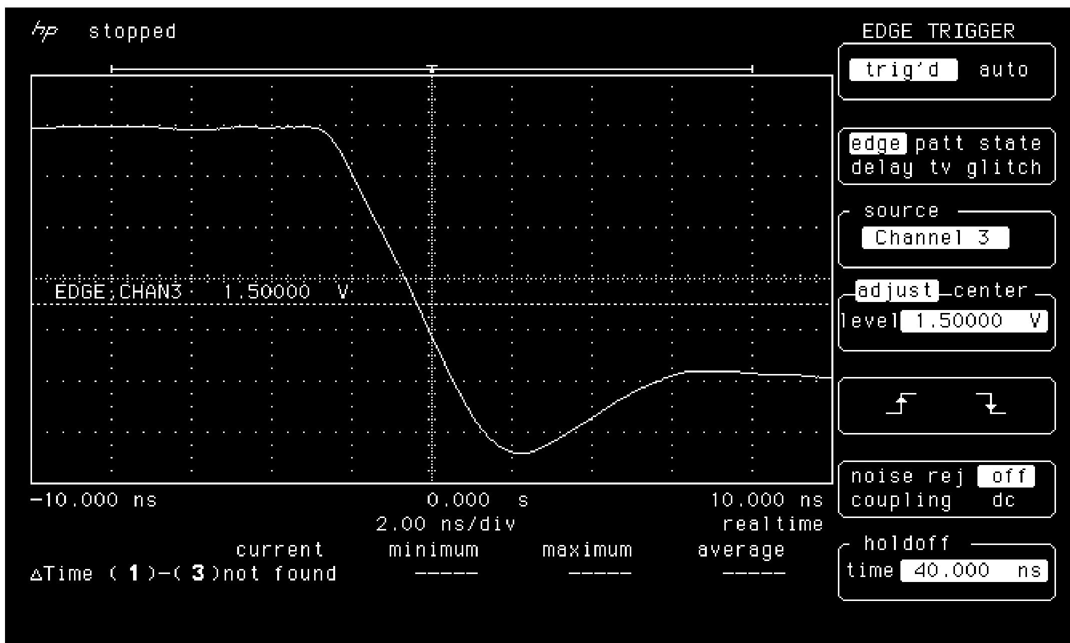

Figure 10b. Falling edge of LAN3802 post-irradiation.

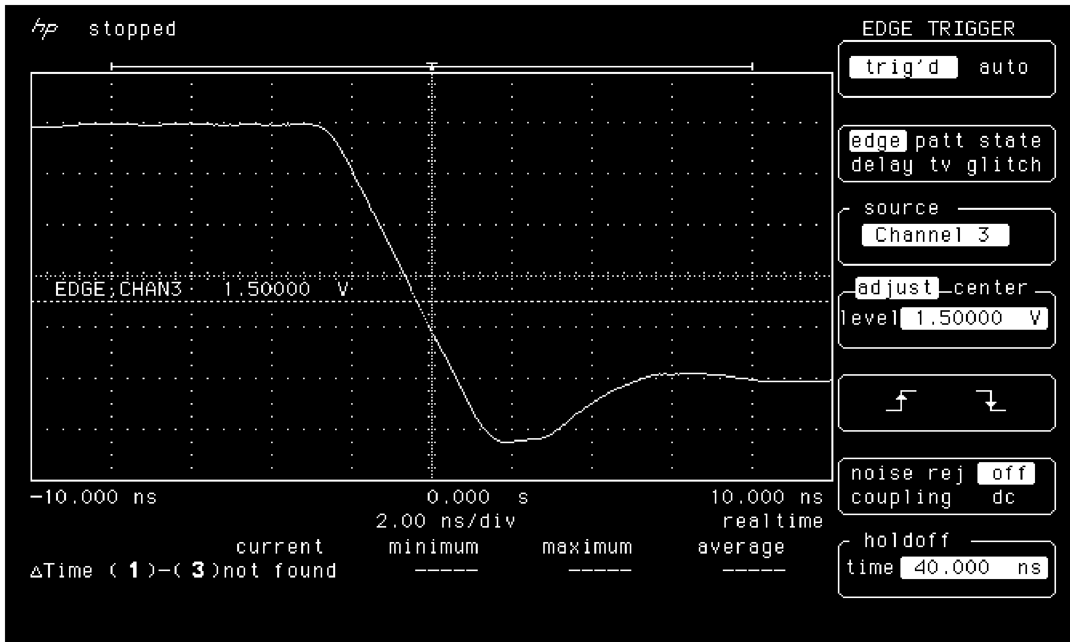

Figure 11a. Falling edge of LAN3803 pre-irradiation.

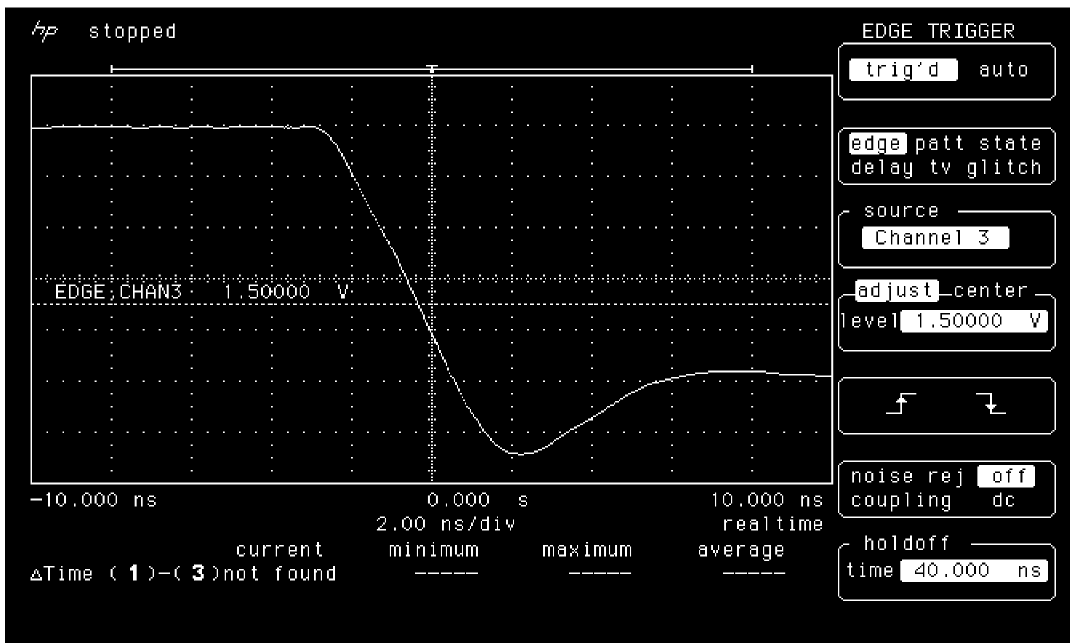

Figure 11b. Falling edge of LAN3803 post-irradiation.

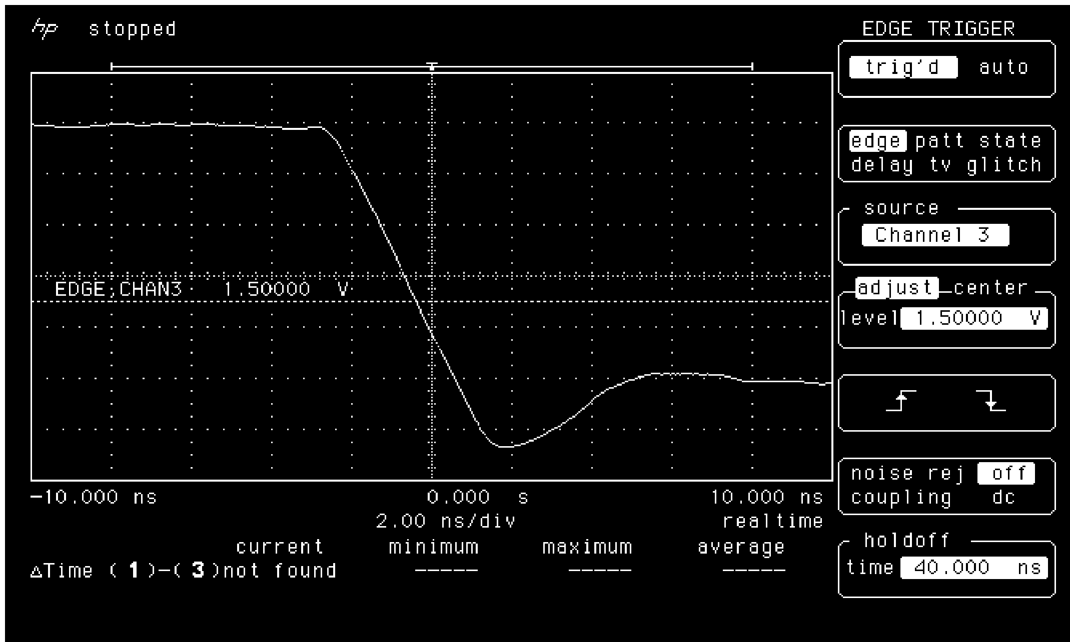

Figure 12a. Falling edge of LAN3804 pre-irradiation.

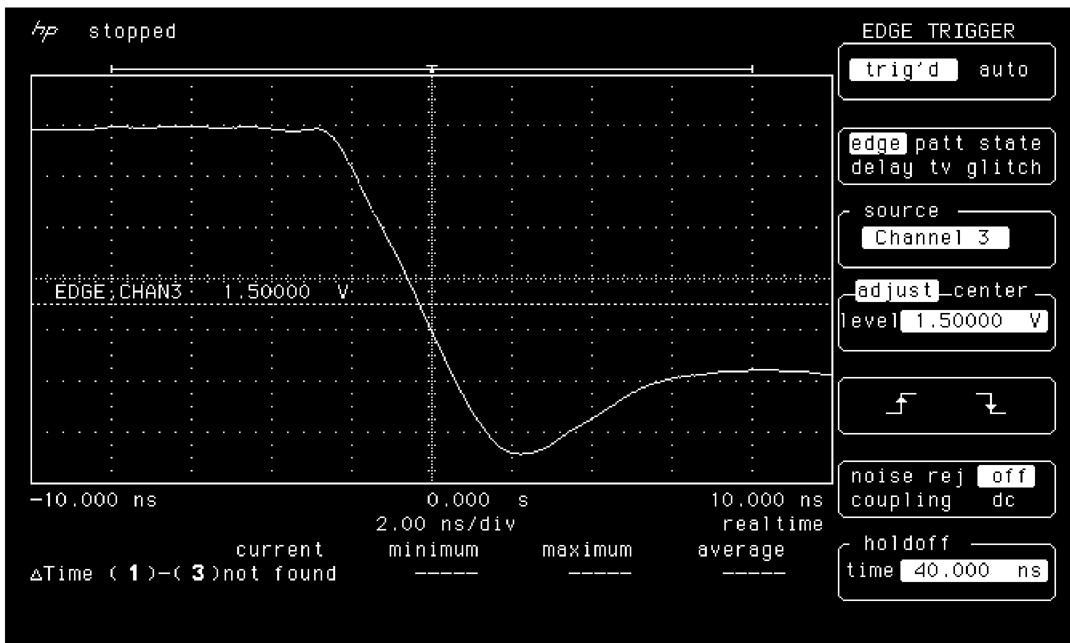

Figure 12b. Falling edge of LAN3804 post-irradiation.

7) Power-Up Transient

In each measurement, the rising time of the power supply voltage (V_{CC}) was set at 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 13-16 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 5.0V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. These pictures show that 20krad(Si) of irradiation basically has no impact on the power up.

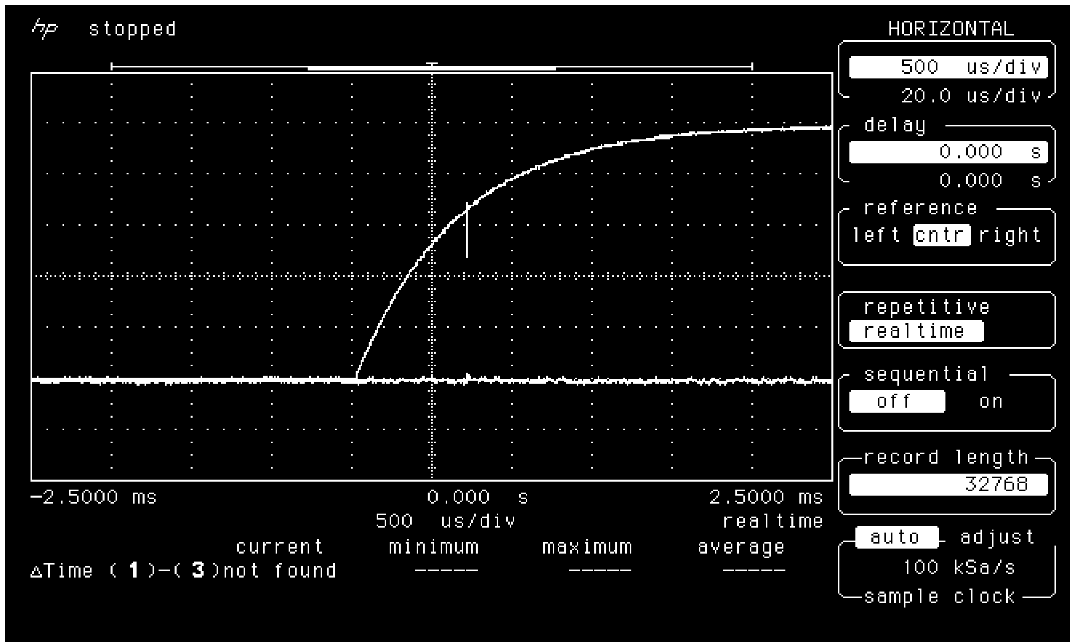

Figure 13a. Power-up transient of LAN3801 pre-irradiation.

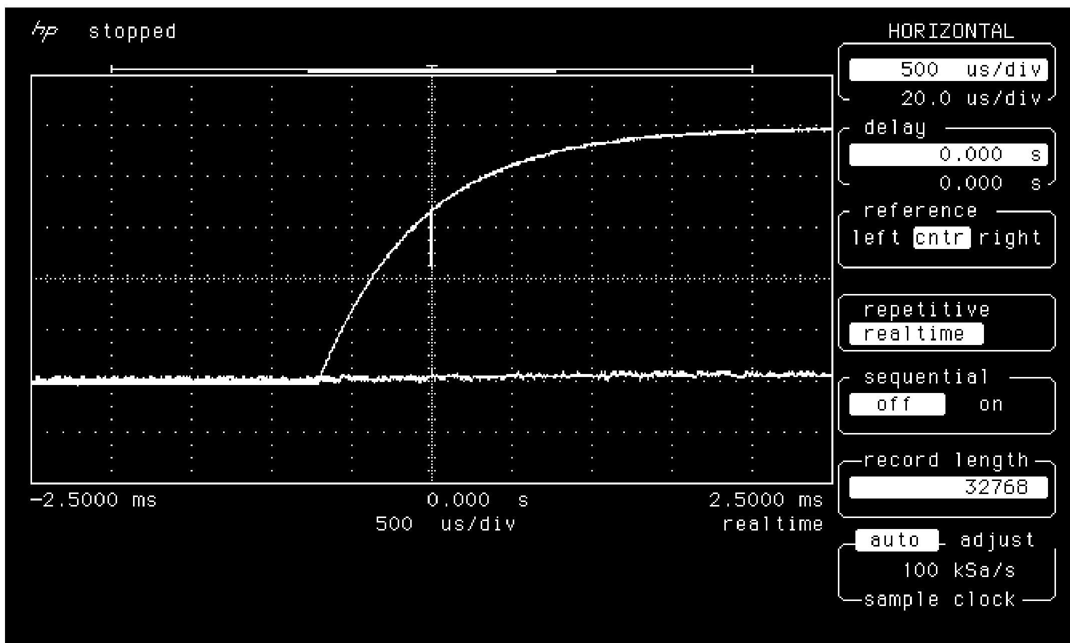

Figure 13b. Power-up transient of LAN3801 post-irradiation.

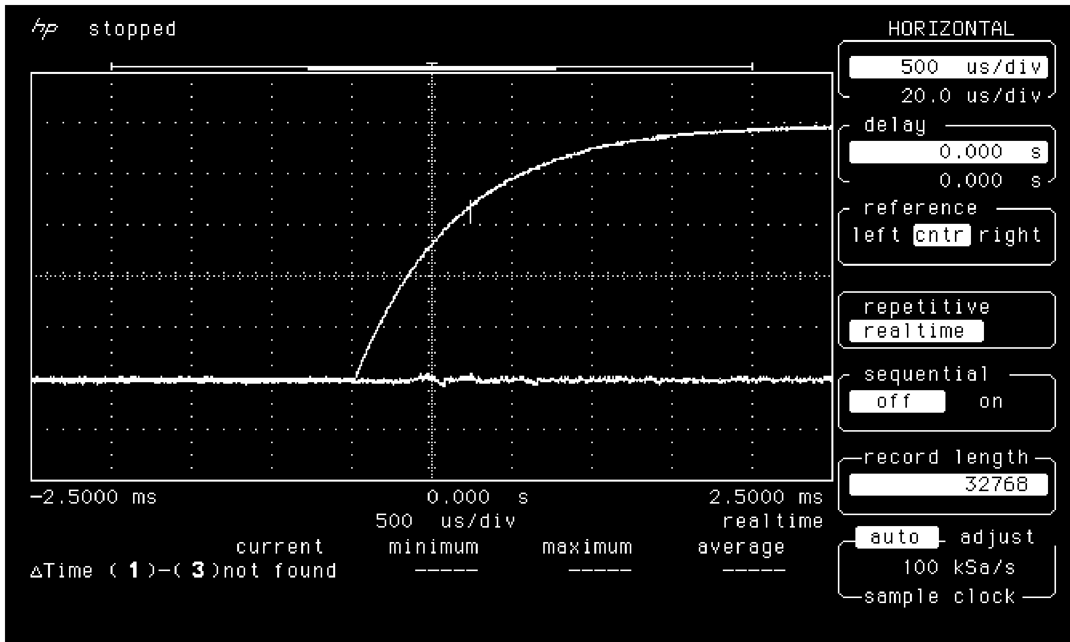

Figure 14a. Power-up transient of LAN3802 pre-irradiation.

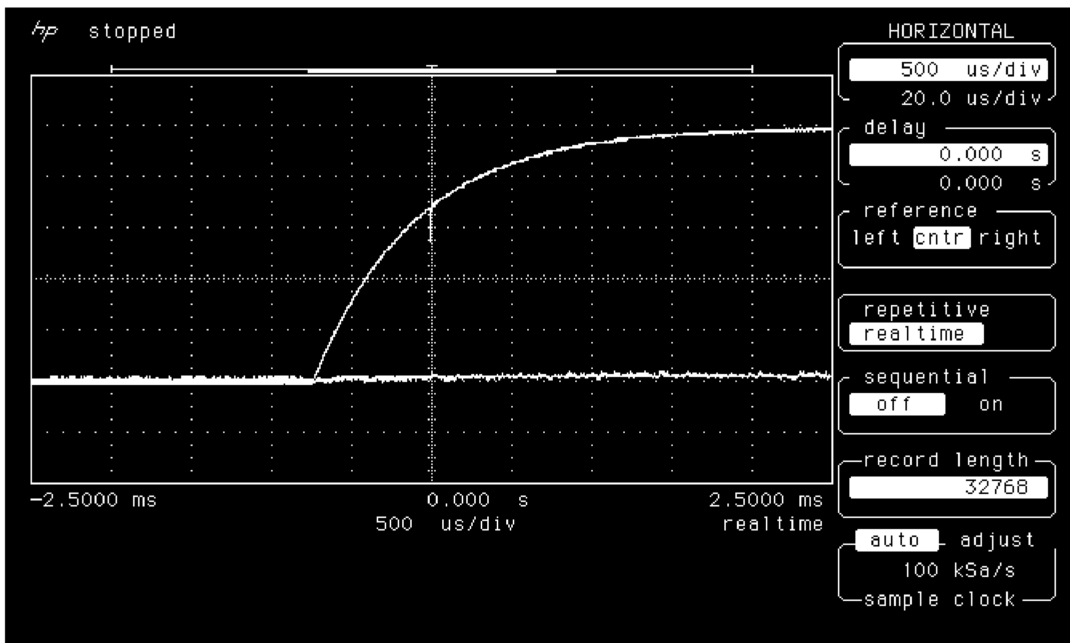

Figure 14b. Power-up transient of LAN3802 post-irradiation.

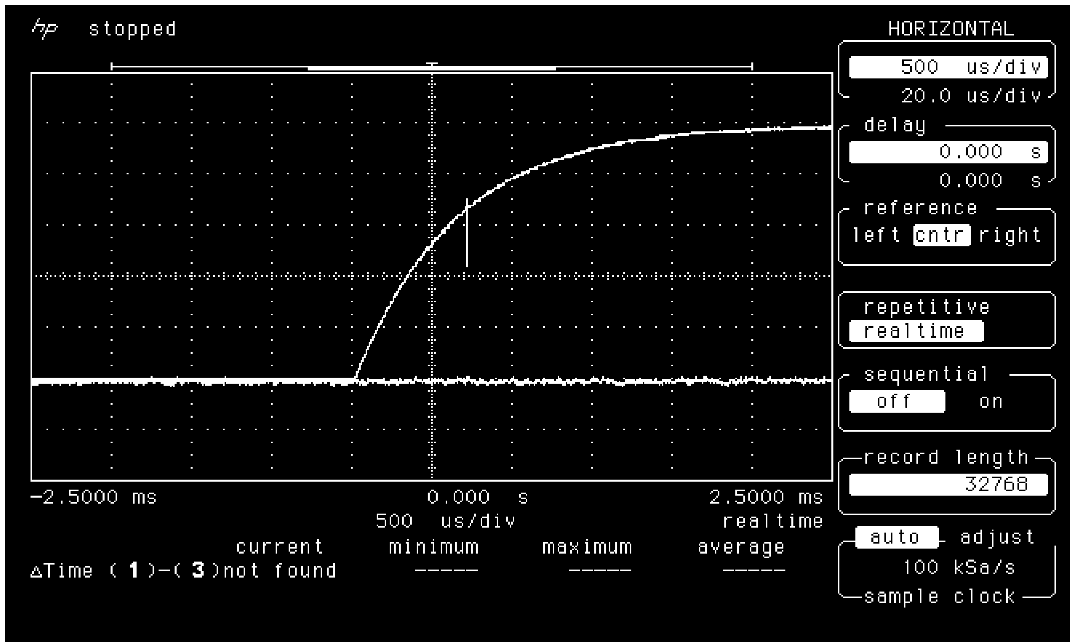

Figure 15a. Power-up transient of LAN3803 pre-irradiation.

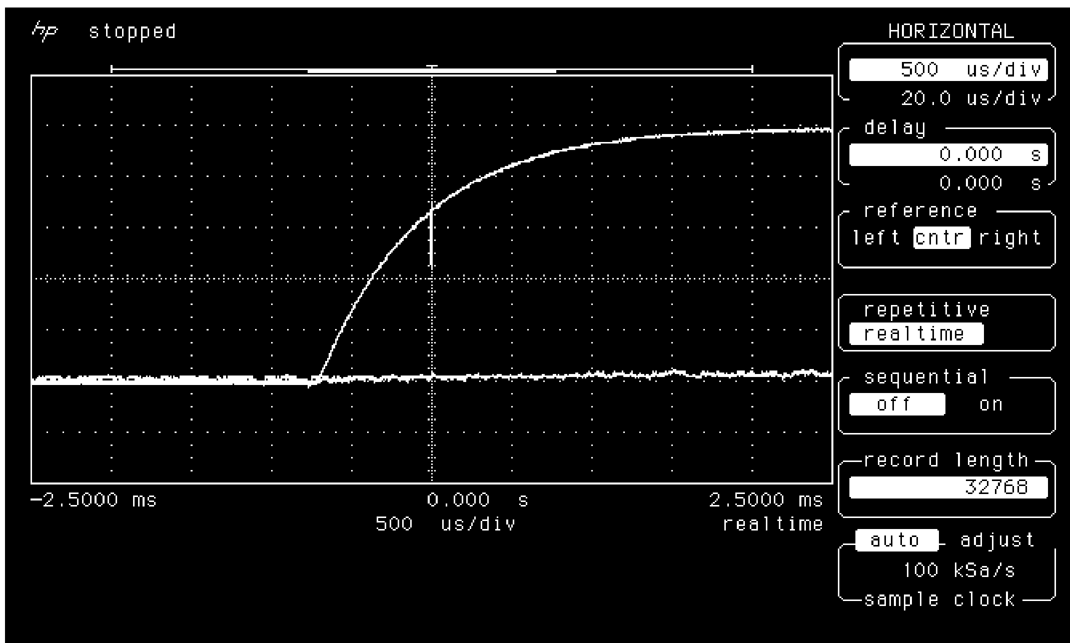

Figure 15b. Power-up transient of LAN3803 post-irradiation.

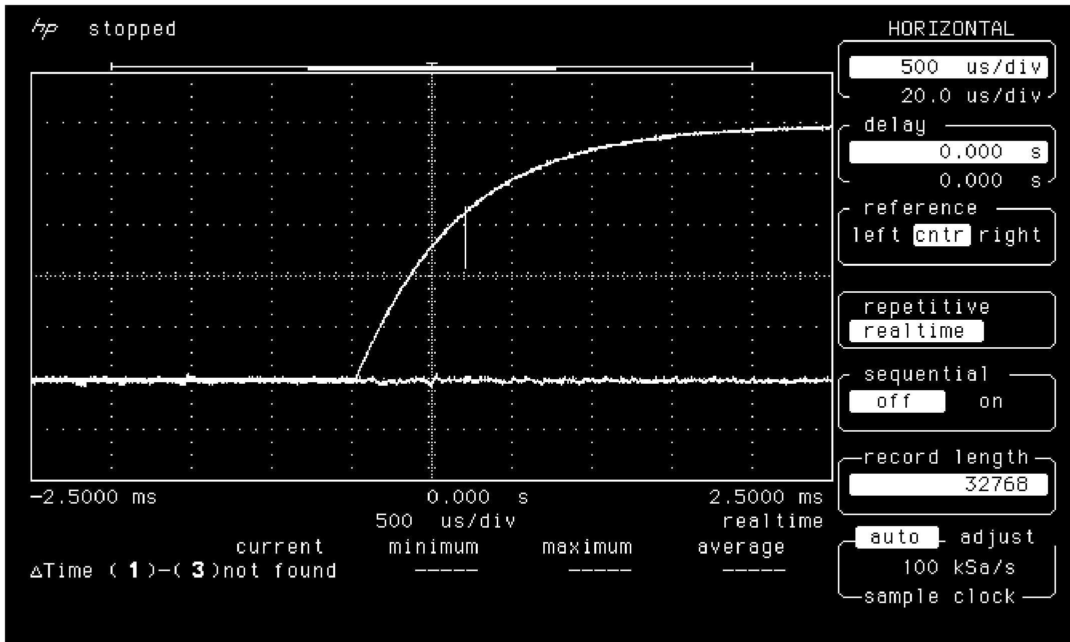

Figure 16a. Power-up transient of LAN3804 pre-irradiation

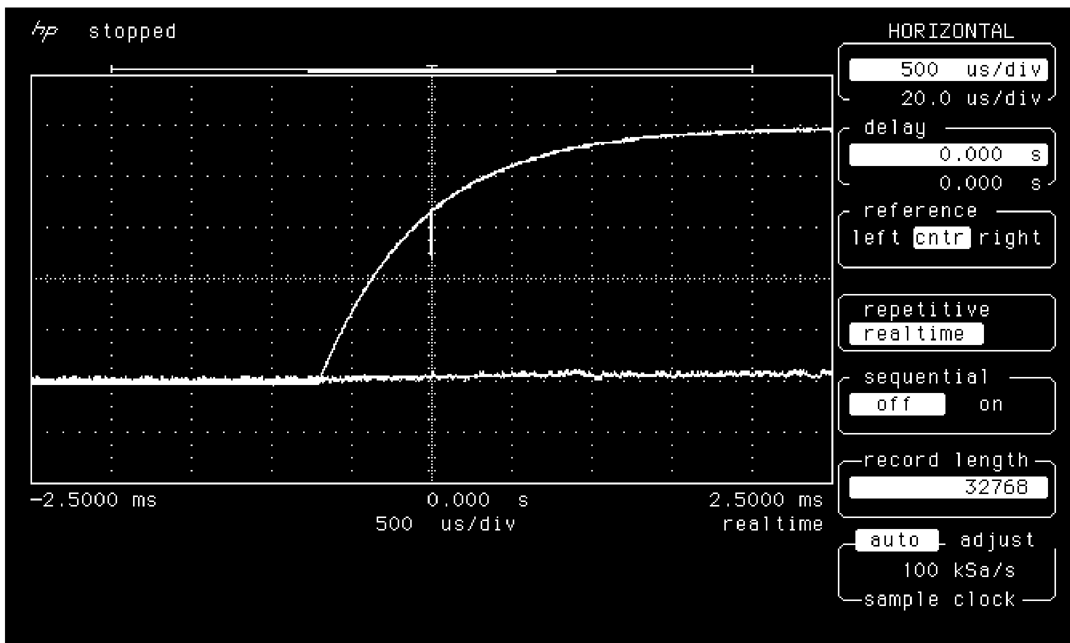

Figure 16b. Power-up transient of LAN3804 post-irradiation