TOTAL IONIZING DOSE TEST REPORT

No. 00T-RT54SX32-T6JP03
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I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	~140krad(Si)
2. $I_{DDSTDBY}$	Passed 92kard(Si)
3. V_{IL}/V_{IH}	Passed 92kard(Si)
4. V_{OL}/V_{OH}	Passed 92kard(Si)
5. Propagation Delays	Passed 92kard(Si)
6. Rising/Falling Edge Transient	Passed 92kard(Si)
7. Power-up Transient Current	Passed 92kard(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device(s) under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT54SX32
Package	CQFP208
Foundry	MEC
Technology	0.6µm CMOS
Die Lot Number	T6JP03
Quantity Tested	7
Serial Numbers	LAN3600, LAN3602, LAN3604, LAN3605, LAN3606, LAN3607, LAN3608

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA
Radiation Source	Co-60
Dose Rate	1krad(Si)/hr (+/-10%)
Data Mode	Static
Temperature	Room
Bias	3.3V/5.0V

C. Test Method

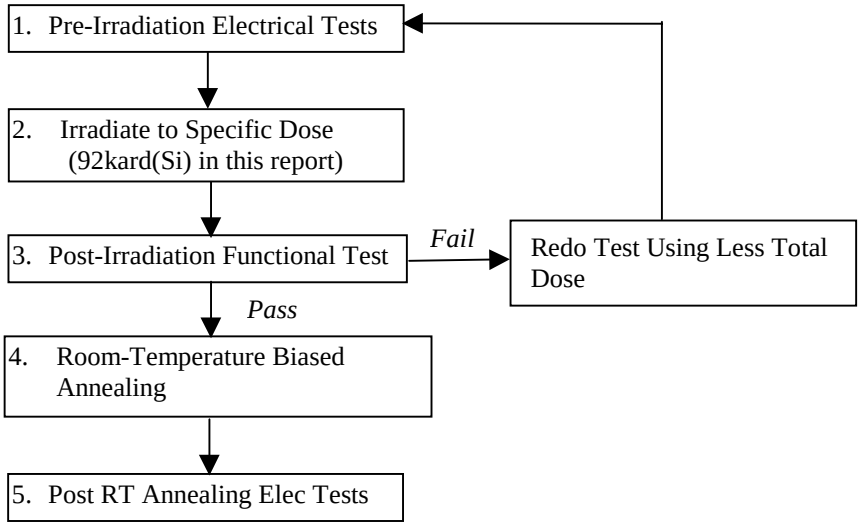

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and then parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has much less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This won't be logistically possible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. Test Results

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced I_{CC} versus total dose for DUT LAN3600, LAN3602 and LAN3604. Functionality was measured every hour on selected pins. Failure was detected by clocking out the data and comparing them with the truth table. The first failure occurred just above 140krad(Si). The sudden surge of I_{CC} when functional failure occurred is a testing artifact. This current surge is due to the synchronization of clocking all the failed nodes during measurement. The inputs were at static during irradiation for the worst case of radiation effects. If dynamic inputs (for example, we tested 1kHz) were used during irradiation, there was no sudden I_{CC} surge when functional occurred.

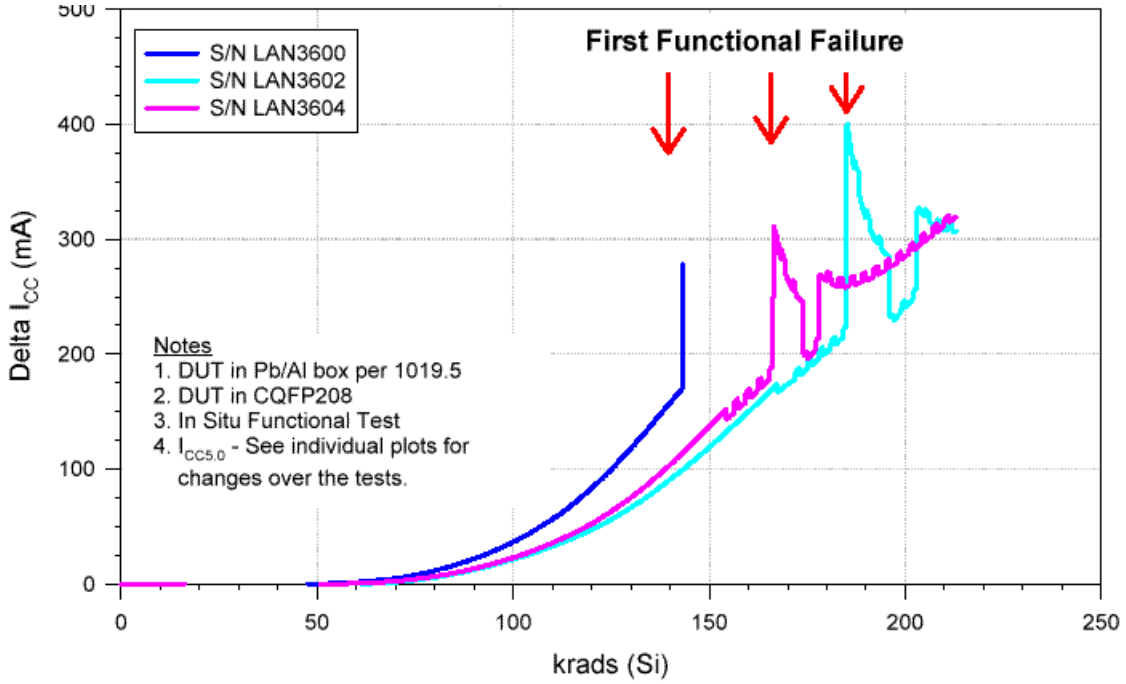

Figure 2. Radiation-induced I_{CC} (Delta I_{CC}) versus total dose for three DUTs. Note that the sudden surge of I_{CC} when functional failure occurred is an artifact due to testing setup

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post irradiation test (step 3). The room temperature annealing was considered not necessary for qualifying this particular lot at 92kard(Si). The DUTs used for this test are LAN3605, LAN3606, LAN3607 and LAN3608.

1) Functional Test

Table 4 lists results of the functional test results.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Irradiation
LAN3605	passed	passed
LAN3606	passed	passed
LAN3607	passed	passed
LAN3608	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

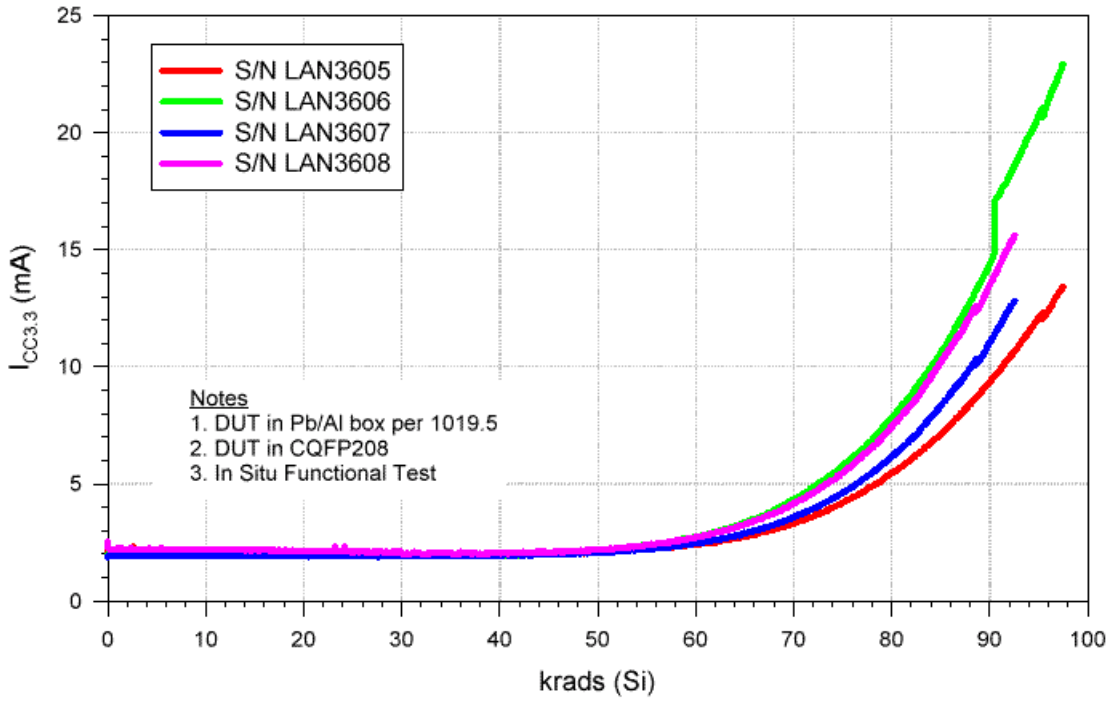

Figure 3. Radiation-induced Delta $I_{DDstandby}$ (I_{CC}) versus total dose for four DUTs.

As shown in Figure 3, LAN3605, LAN3606, LAN3607 and LAN3608 were irradiated to 92kard(Si). Every DUT has $I_{Ddstandby}$ below 25mA (the spec) after irradiation.

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-irradiation. The irradiated DUTs are within the spec and the change of this parameter for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Irradiation
LAN3605	1.35	1.24
LAN3606	1.44	1.46
LAN3607	1.45	1.48
LAN3608	1.46	1.50

4) Output Characteristic

Figure 4a and 4b show the V_{OL} characteristic curves for the pre-irradiated and post-irradiated DUTs. All irradiated DUTs are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 5a and 5b show the V_{OH} characteristic curves for the pre-irradiated and post-irradiated DUTs. All DUTs pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.

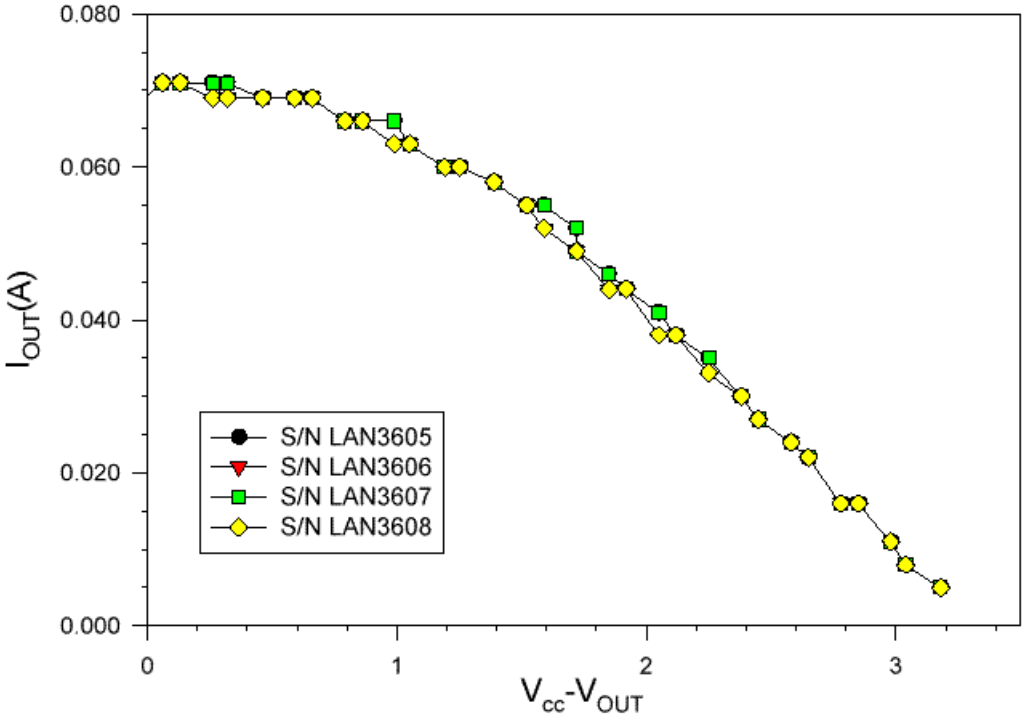

Figure 4a. Pre-irradiation V_{OL} characteristic curves.

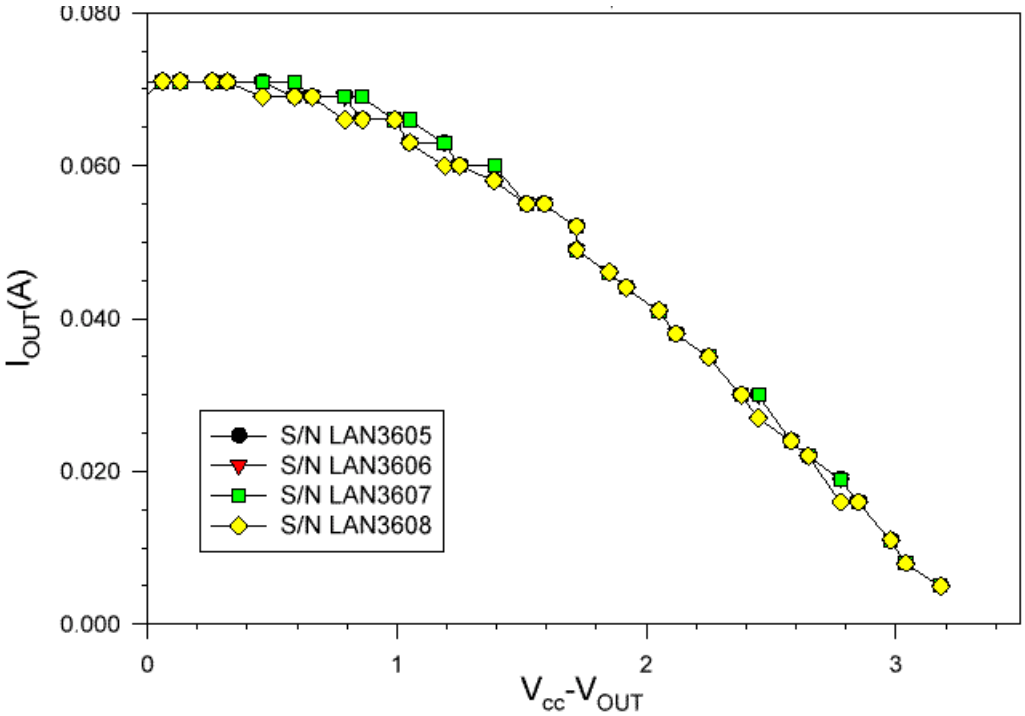

Figure 4b. Post-irradiation V_{OL} characteristic curves.

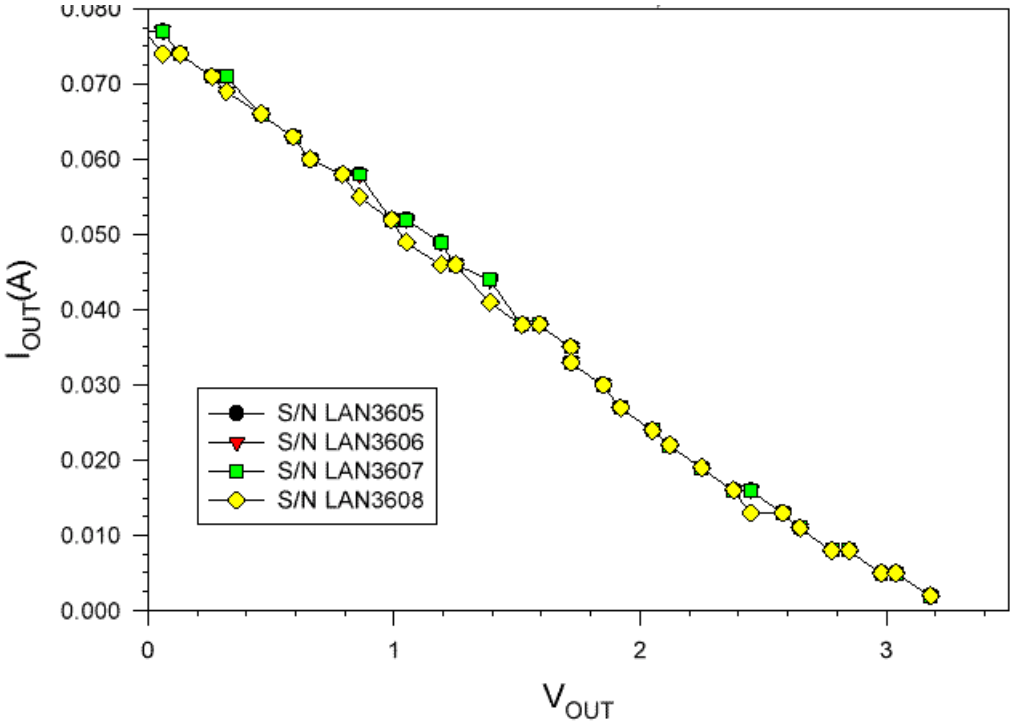

Figure 5a. Pre-irradiation V_{OH} characteristic curves.

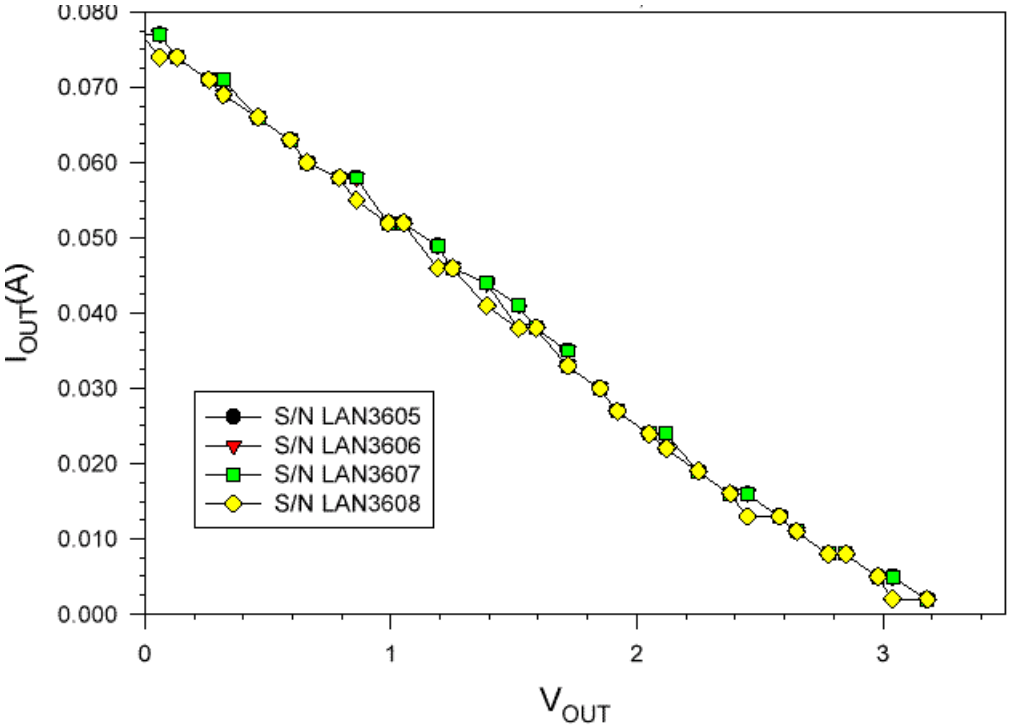

Figure 5b. Post-irradiation V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3605	1414	1413	1413	1399
LAN3606	1440	1439	1440	1422
LAN3607	1424	1422	1423	1406
LAN3608	1391	1392	1390	1375

Table 7. Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3605	57.0	56.9	57.9	57.7
LAN3606	57,7	57.8	58.0	57.7
LAN3607	57.6	57.1	57.5	57.3
LAN3608	56.7	56.5	56.6	56.2

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Irradiation	Pre-Irradiation	Post-Irradiation
LAN3605	58.1	58.0	59.7	59.5
LAN3606	58.6	58.7	59.6	59.3
LAN3607	58.5	58.4	59.5	59.2
LAN3608	57.5	57.4	58.1	57.9

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-irradiation. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The radiation effect is basically negligible.

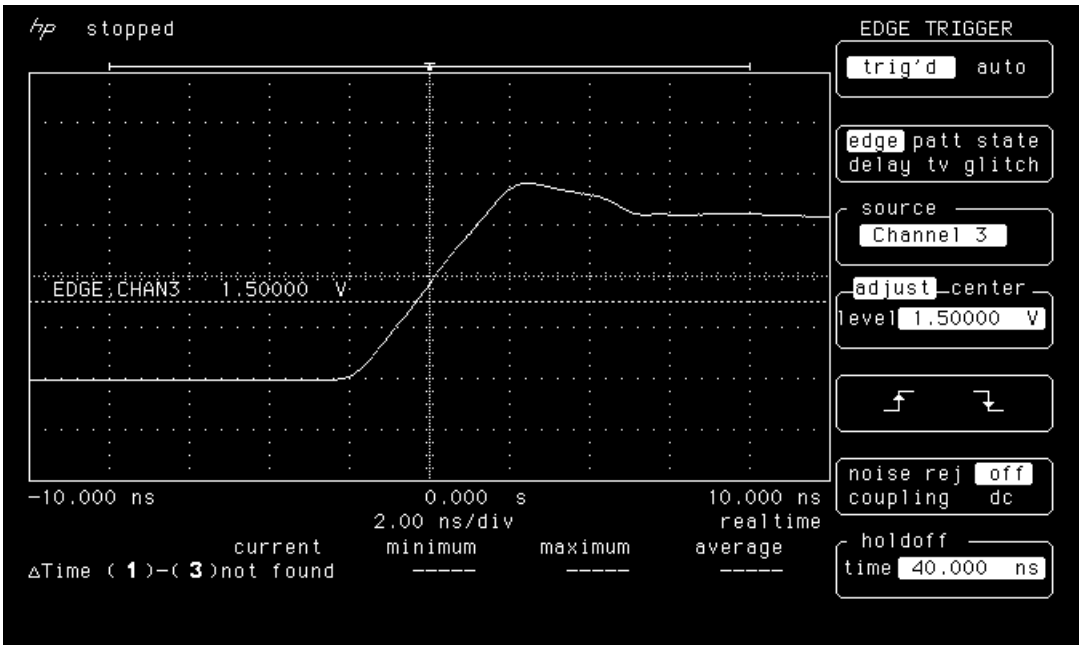

Figure 6a. Rising edge of LAN3605 pre-irradiation.

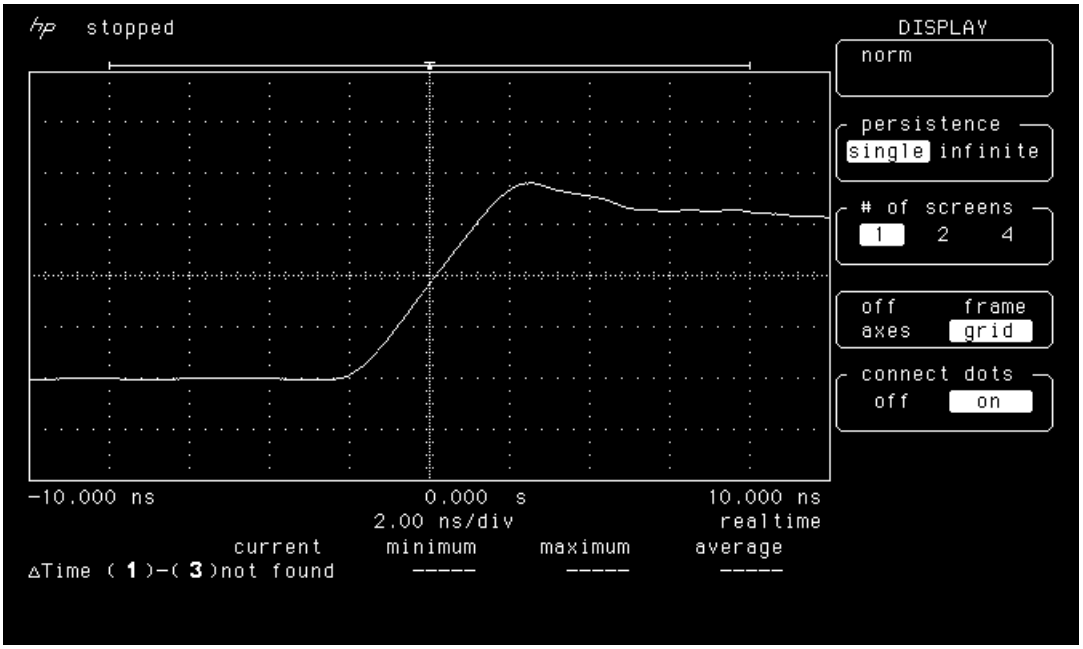

Figure 6b. Rising edge of LAN3605 post-irradiation.

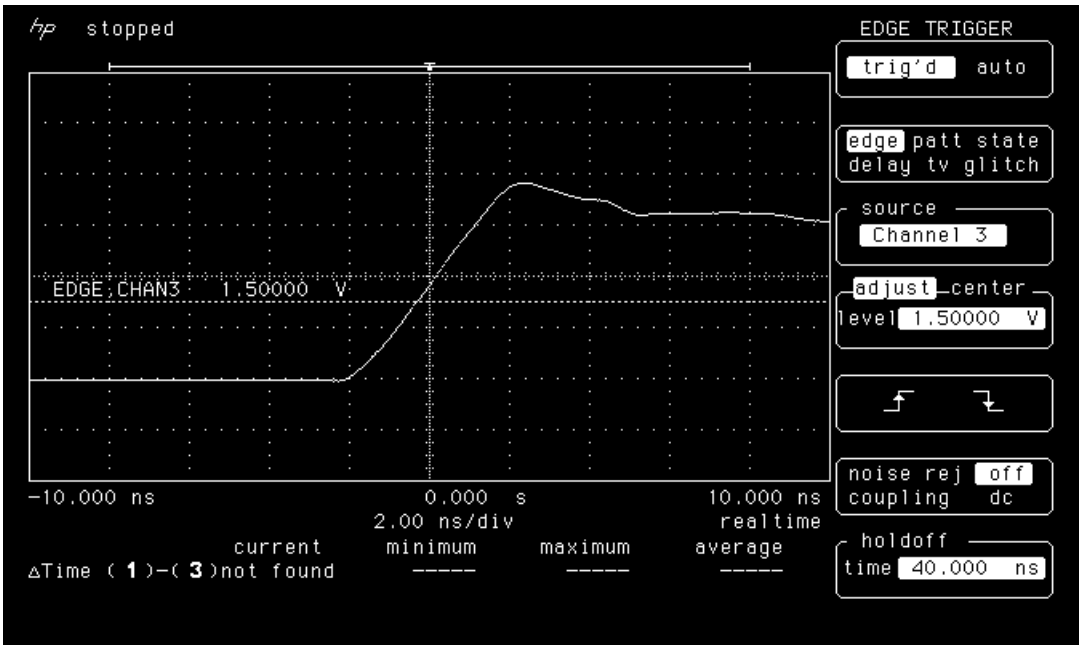

Figure 7a. Rising edge of LAN3606 pre-irradiation.

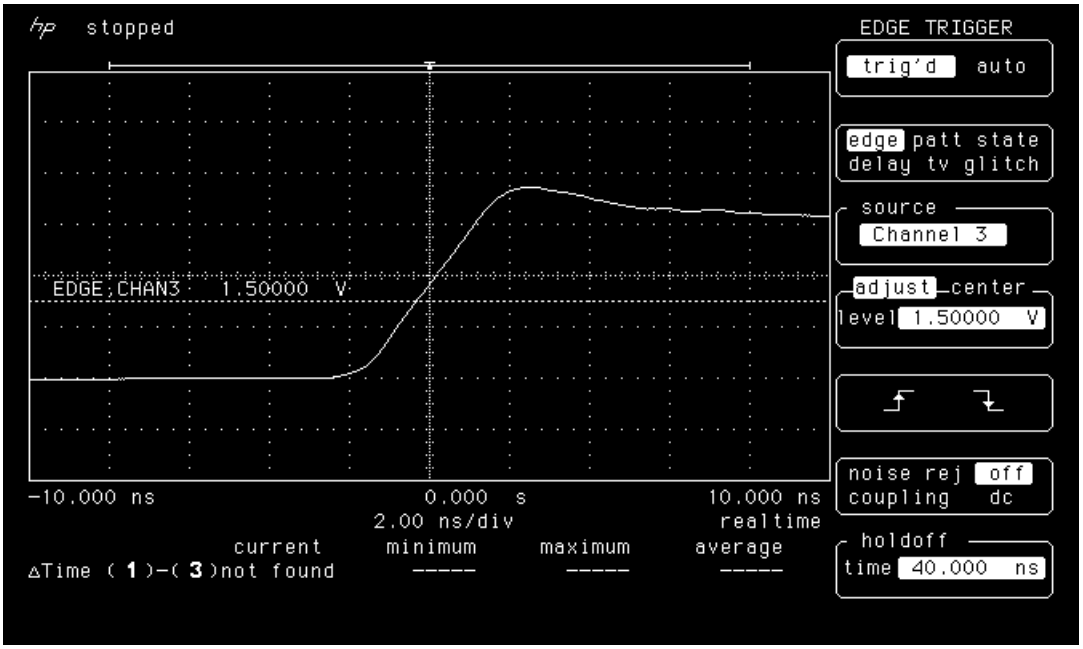

Figure 7b. Rising edge of LAN3606 post-irradiation.

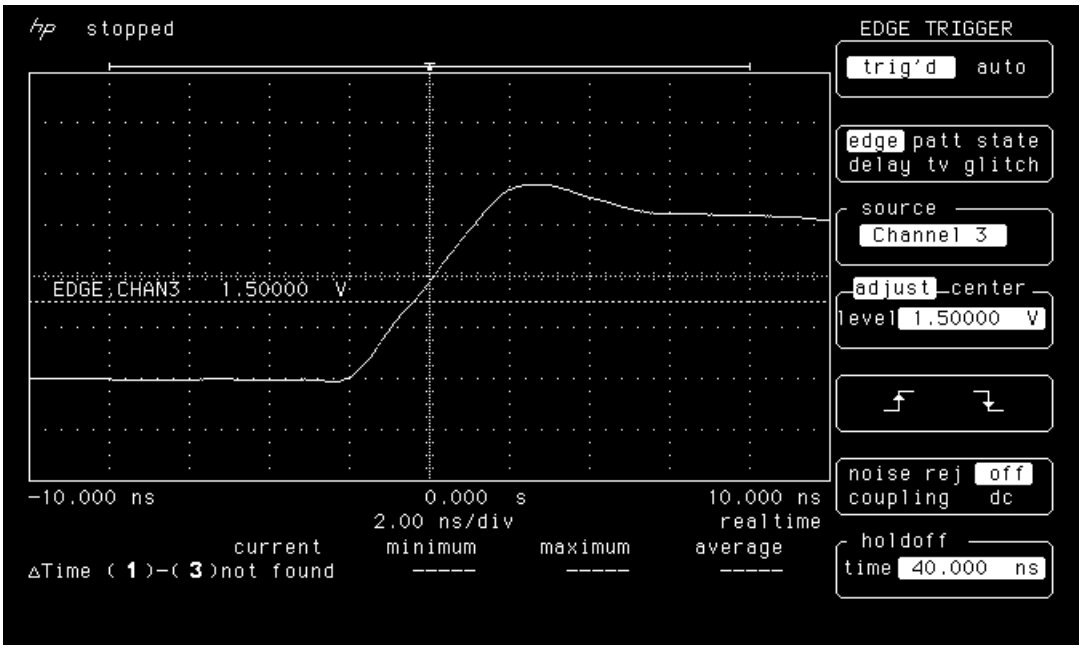

Figure 8a. Rising edge of LAN3607 pre-irradiation.

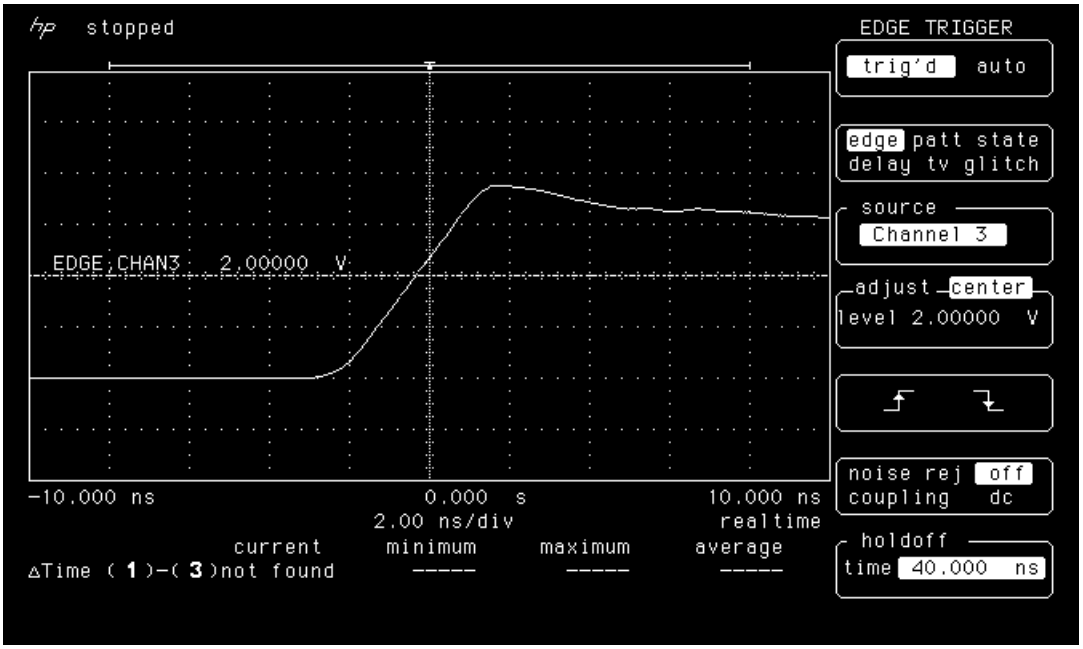

Figure 8b. Rising edge of LAN3607 post-irradiation.

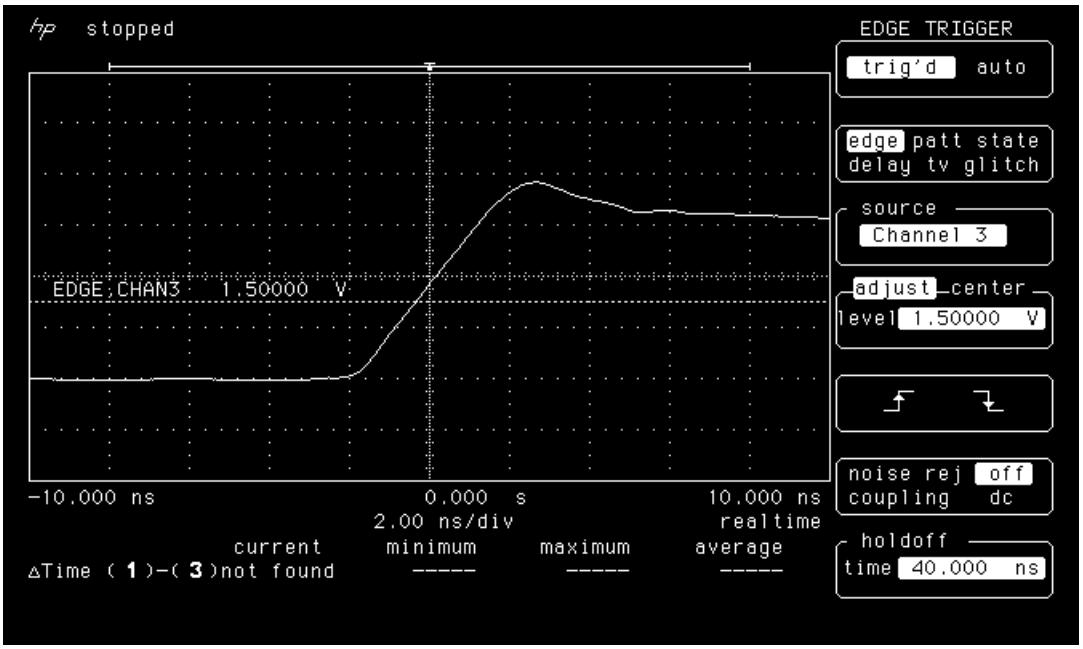

Figure 9a. Rising edge of LAN3608 pre-irradiation.

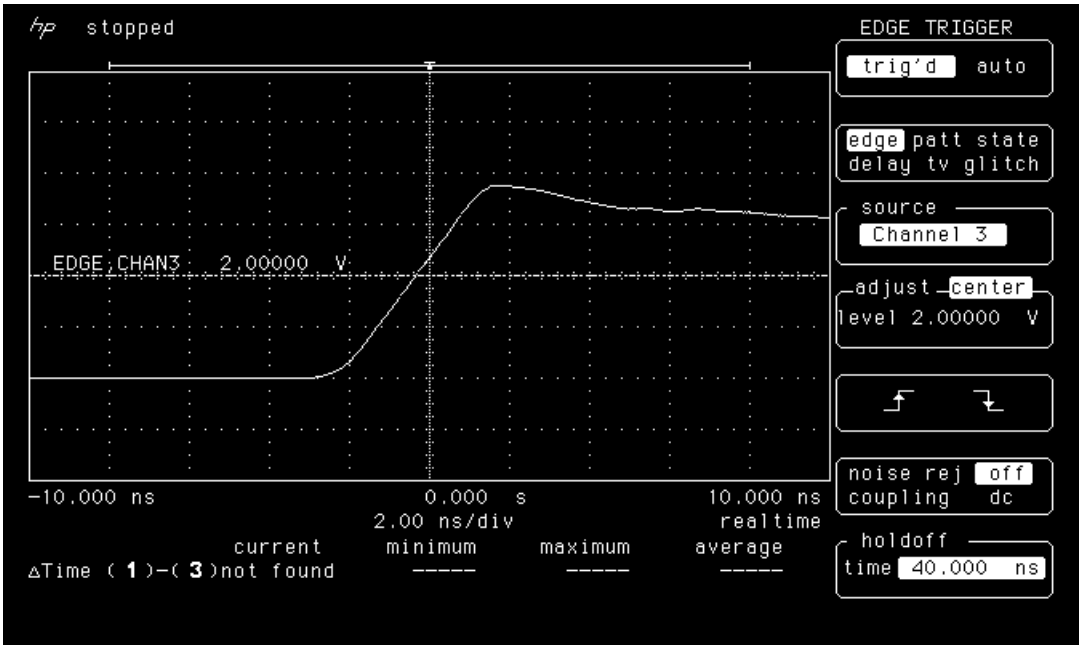

Figure 9b. Rising edge of LAN3608 post-irradiation

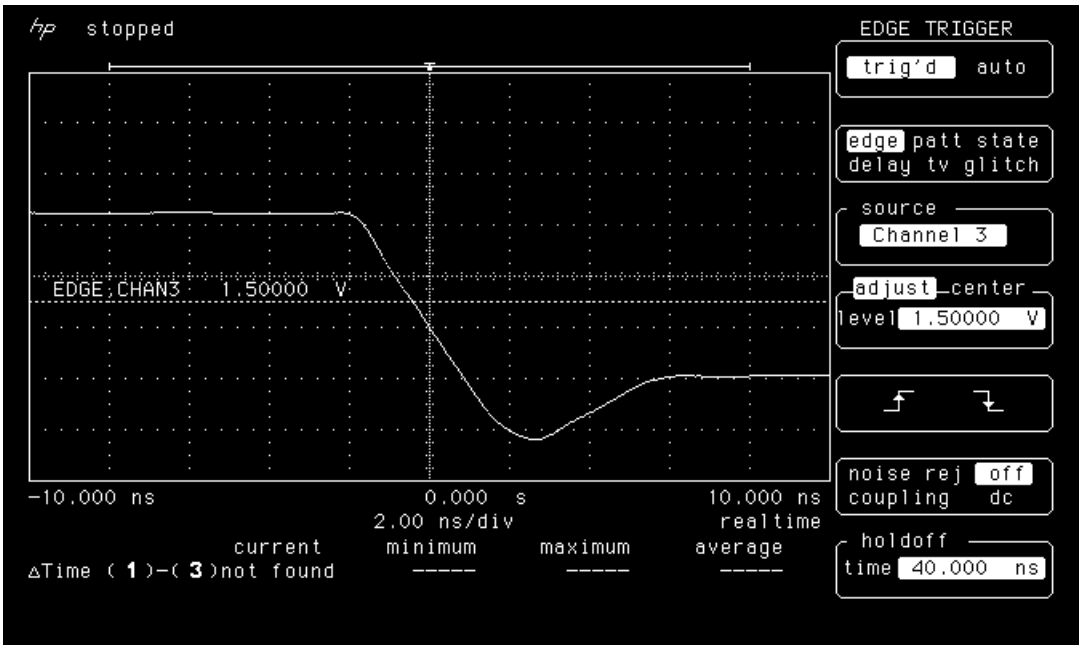

Figure 10a. Falling edge of LAN3605 pre-irradiation

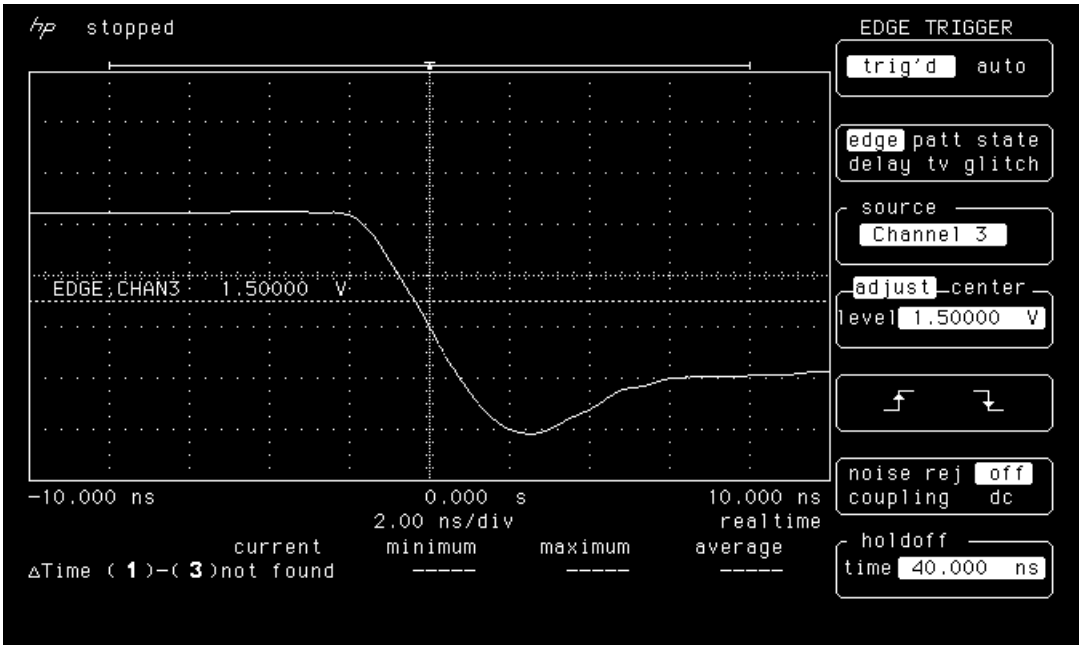

Figure 10b. Falling edge of LAN3605 post-anneal.

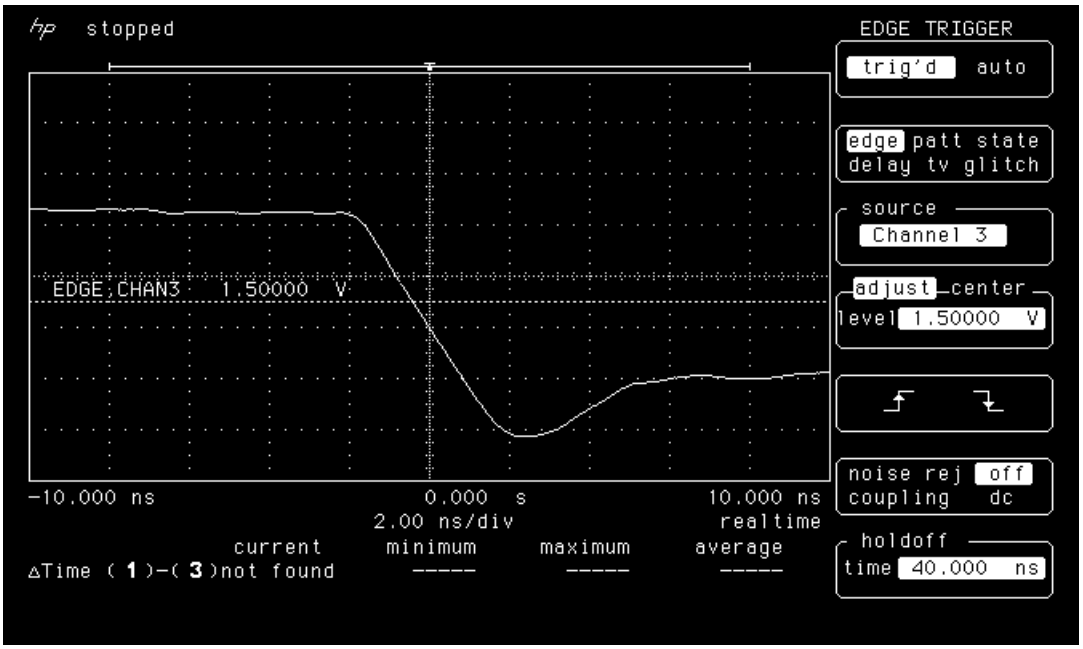

Figure 11a. Falling edge of LAN3606 pre-irradiation.

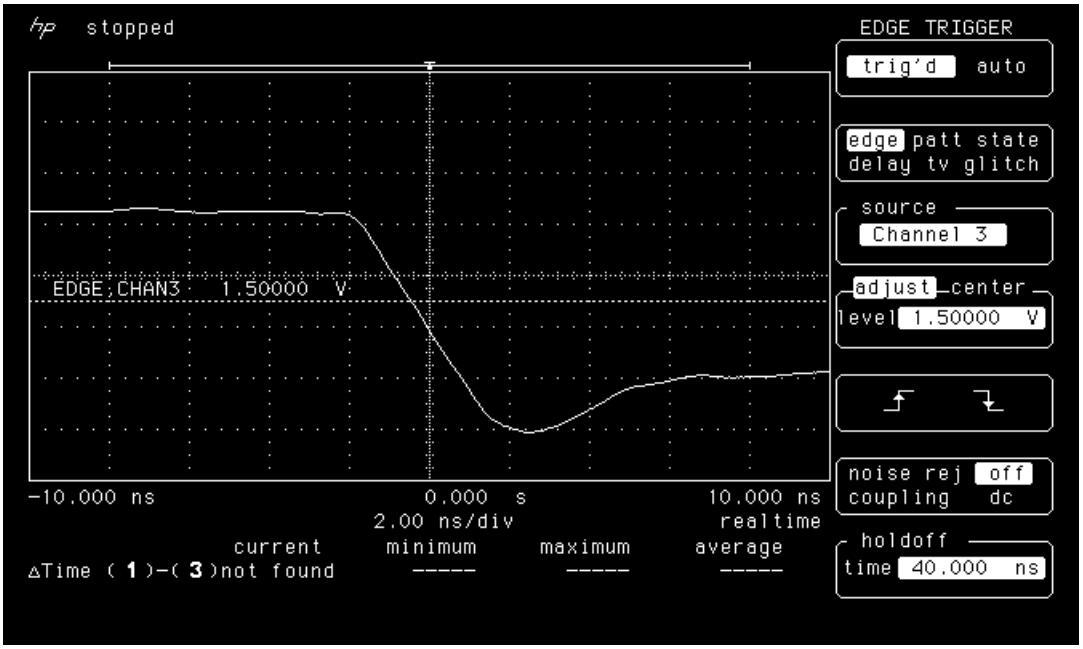

Figure 11b. Falling edge of LAN3606 post-irradiation.

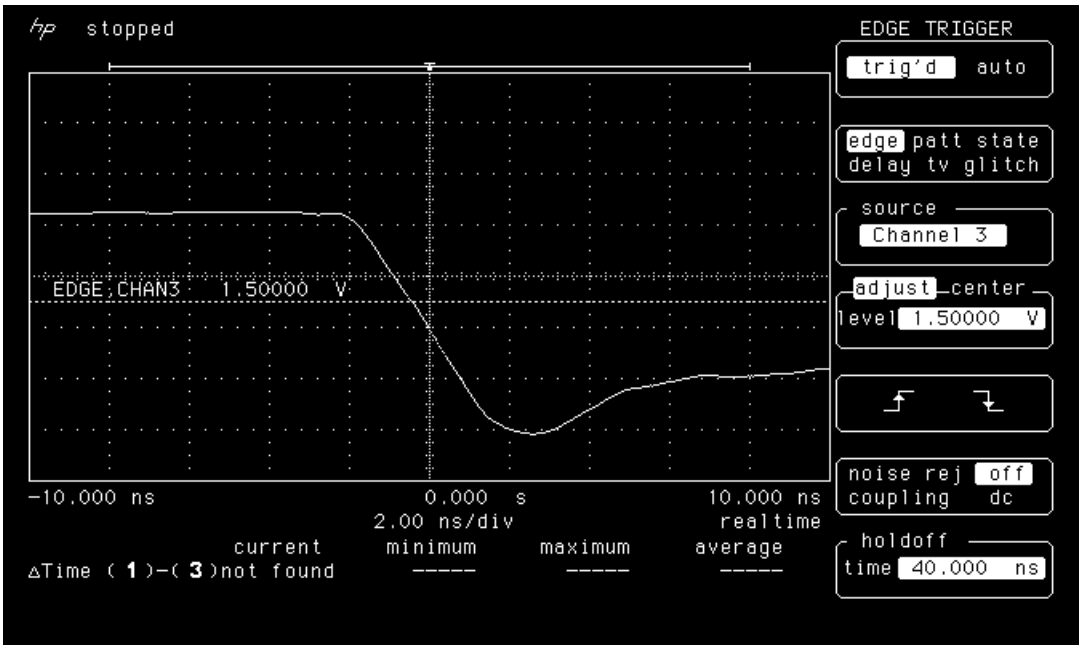

Figure 12a. Falling edge of LAN3607 pre-irradiation.

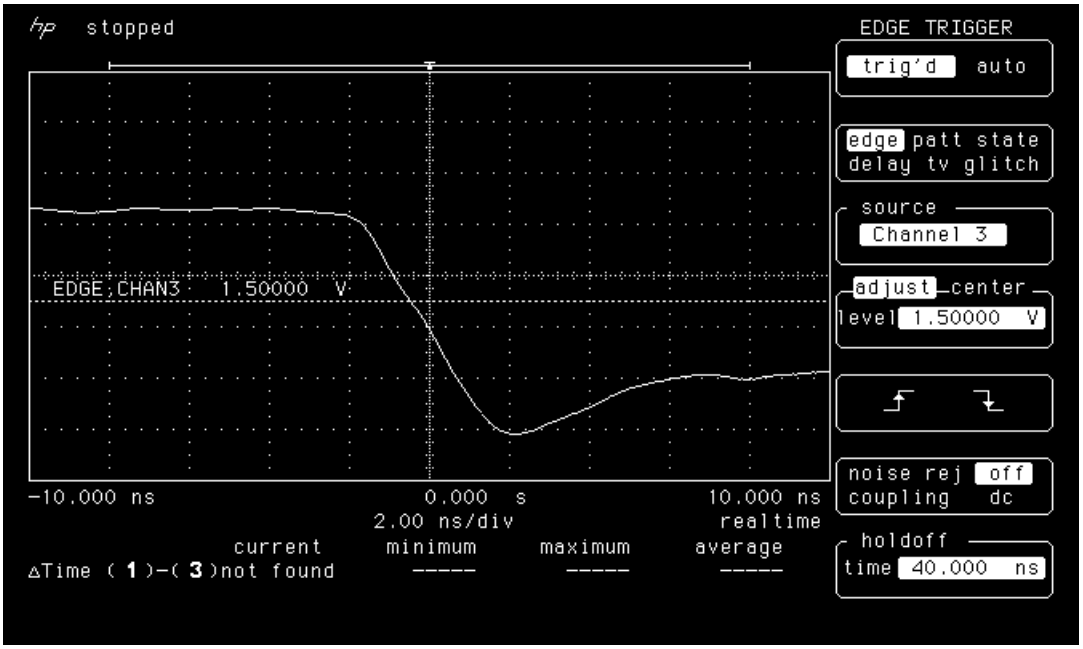

Figure 12b. Falling edge of LAN3607 post-irradiation.

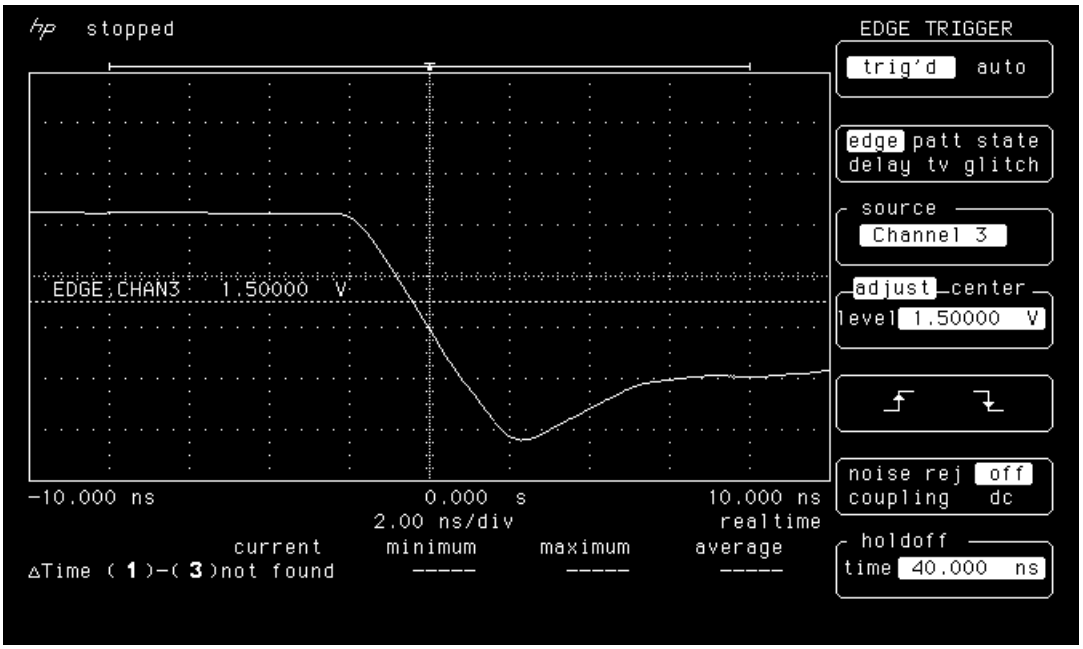

Figure 13a. Falling edge of LAN3608 pre-irradiation

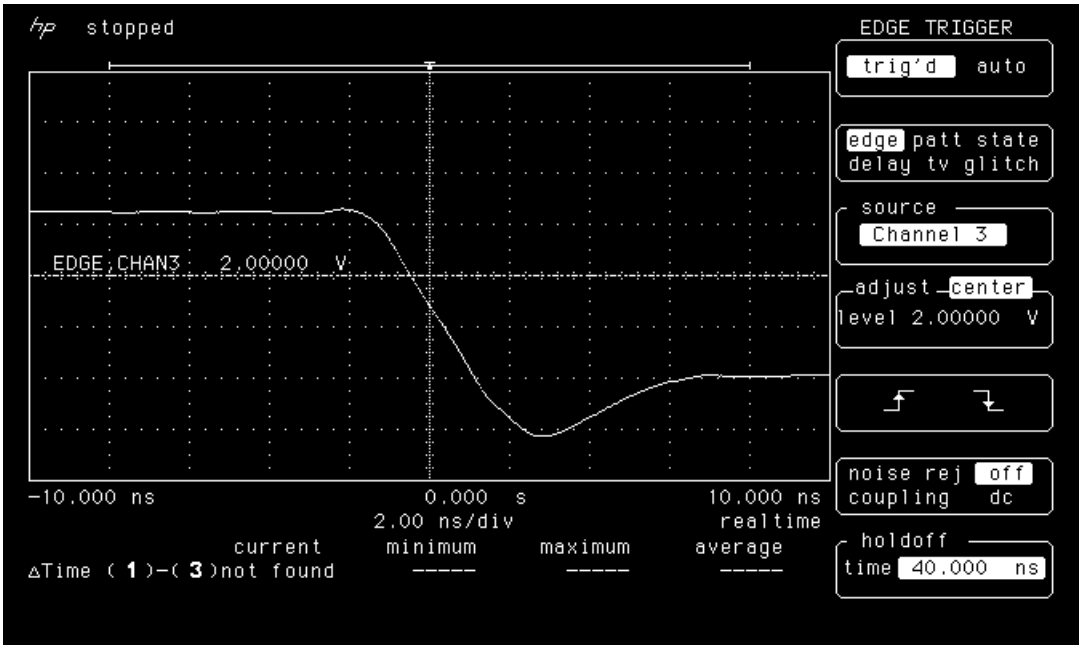

Figure 13b. Falling edge of LAN3608 post-irradiation

7) Power-Up Transient

In each measurement, the rising time of the power supply voltage (V_{CC}) was set at 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 14-17 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 3.3V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. Post 92kard(Si) irradiation DUTs have a radiation induced transient current during power up (see, for example, Figure 14b). However, this transient is very minute. Also, if annealing at room temperature is performed, this transient should be easily annealed out within very short period of time. The details can be found in a previous publication ("Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278).

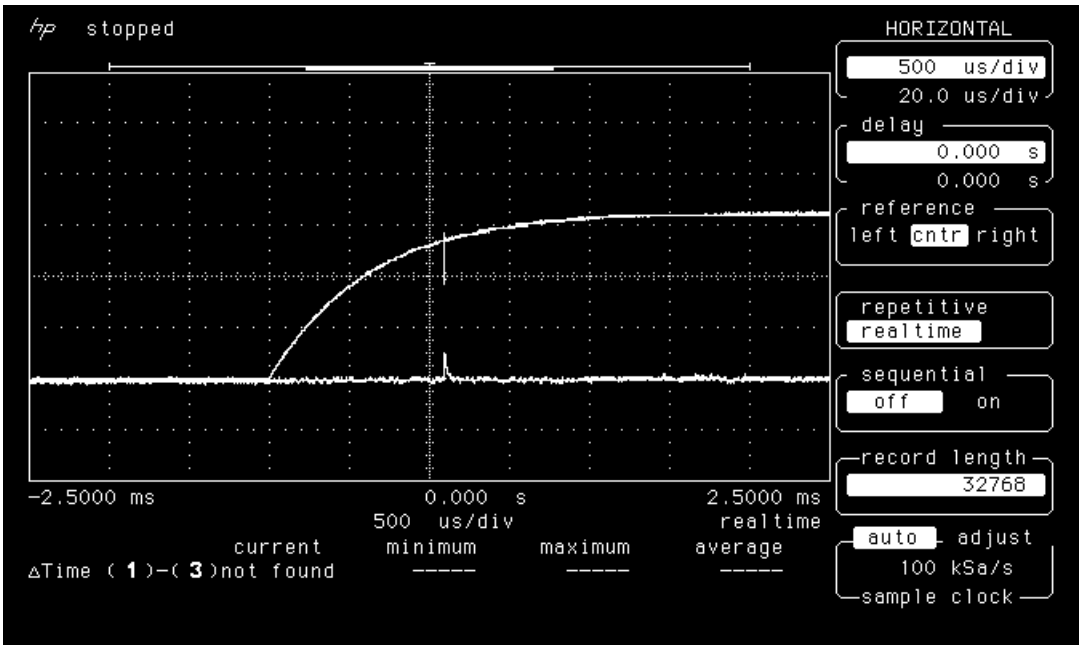

Figure 14a. Power-up transient of LAN3605 pre-irradiation.

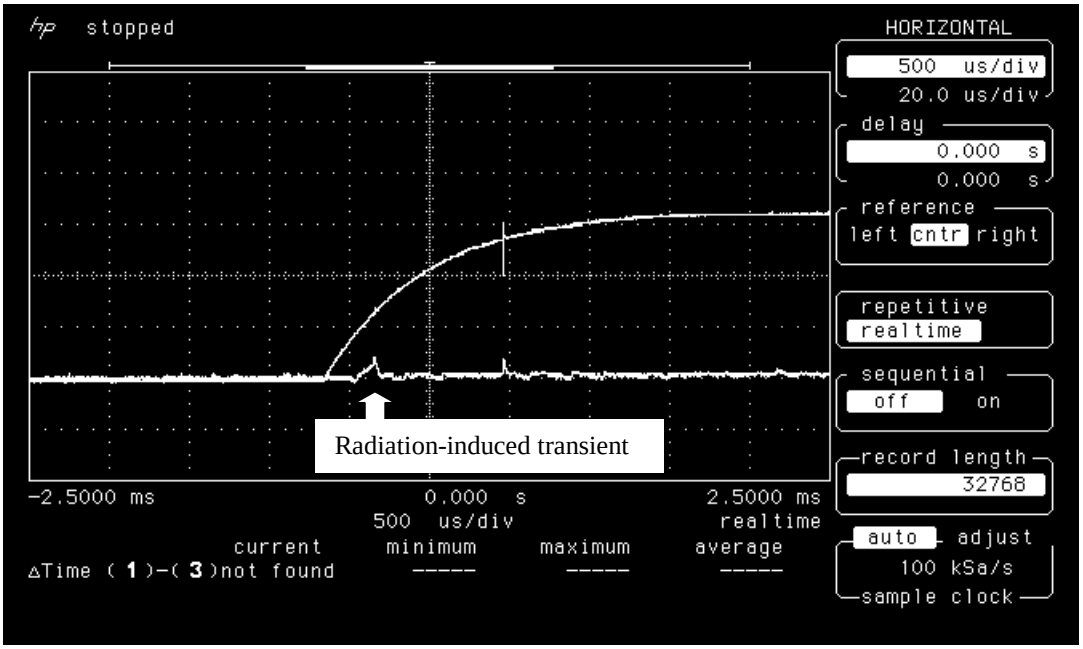

Figure 14b. Power-up transient of LAN3605 post-irradiation.

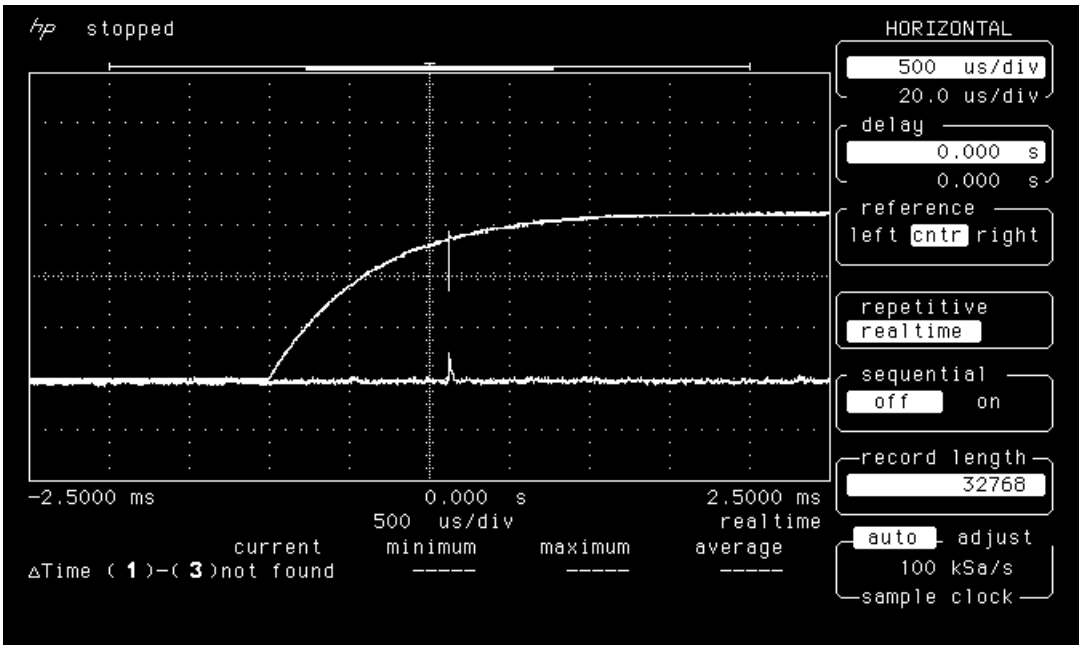

Figure 15a. Power-up transient of LAN3606 pre-irradiation.

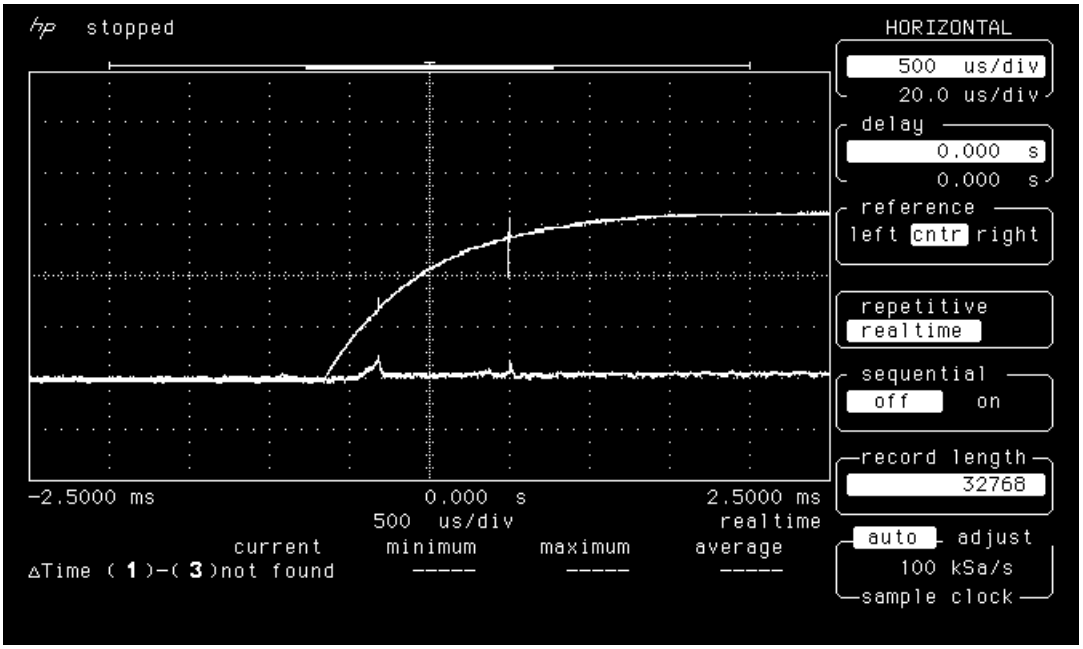

Figure 15b. Power-up transient of LAN3606 post-irradiation.

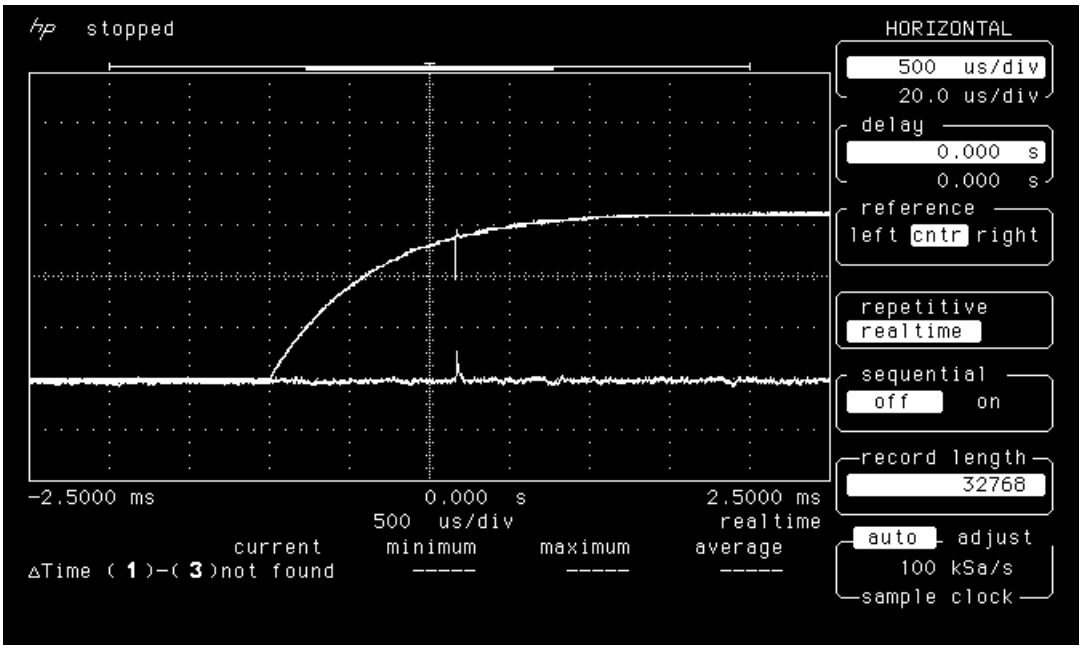

Figure 16a. Power-up transient of LAN3607 pre-irradiation.

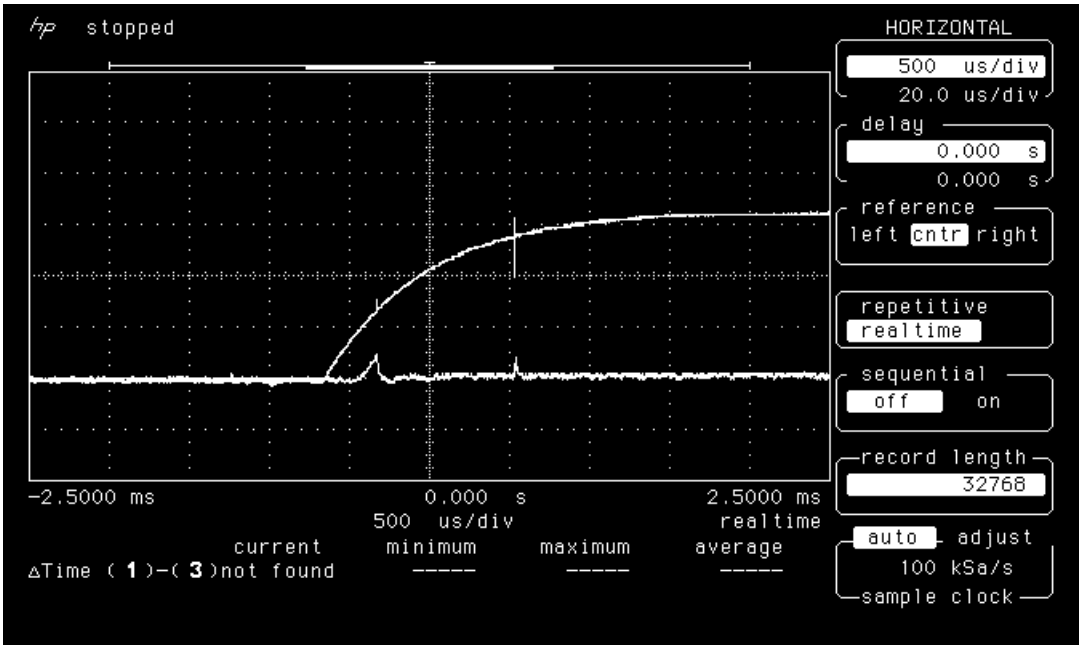

Figure 16b. Power-up transient of LAN3607 post-irradiation.

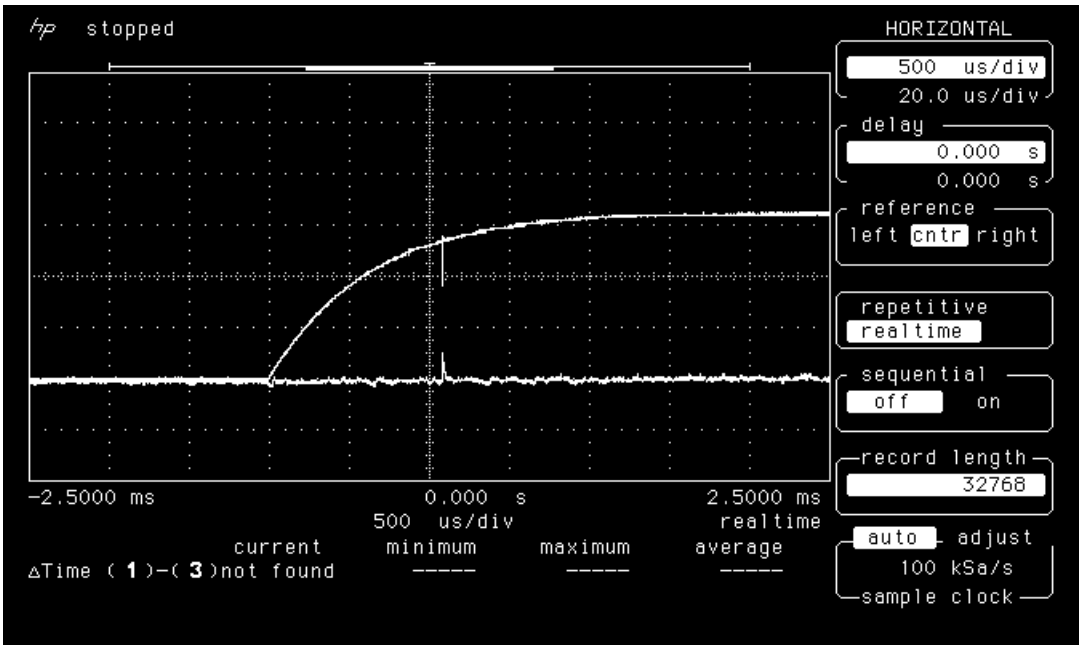

Figure 17a. Power-up transient of LAN3608 pre-irradiation

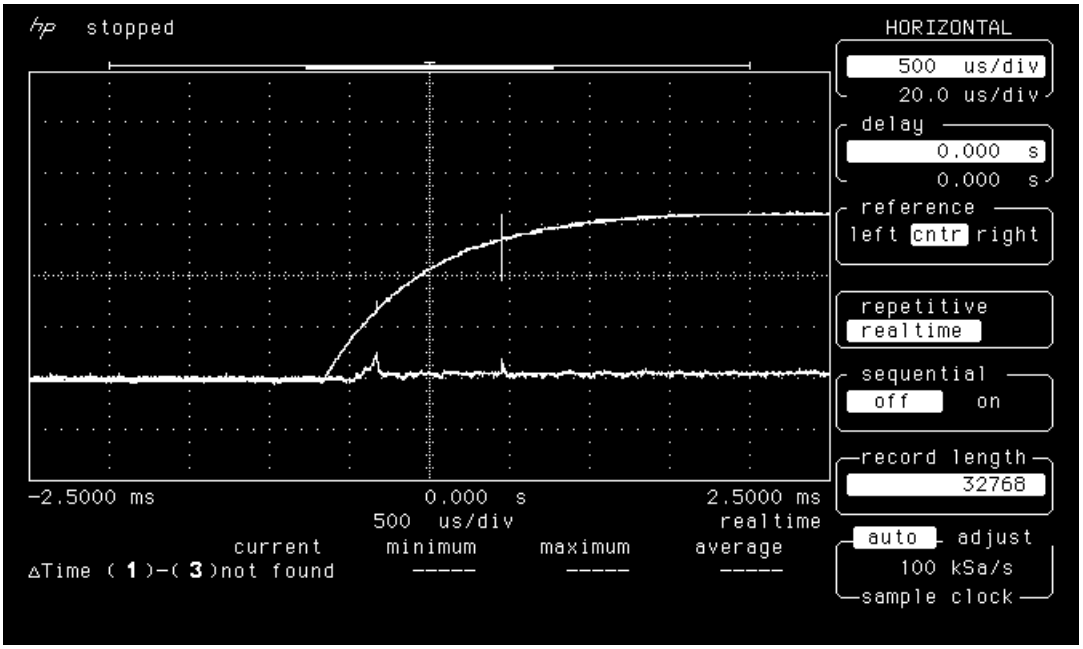

Figure 17b. Power-up transient of LAN3608 post-irradiation