TOTAL IONIZING DOSE TEST REPORT

No. 00T-RT54SX16-T6HP12D
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J.J. Wang
(408) 522-4576
jih-jong.wang@actel.com

Igor Kleyner
(301) 286-5683
igor.kleyner@nasa.gov

I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	152krad(Si) in static case, 240krad(Si) in dynamic case
2. $I_{DDSTDBY}$	Passed 80krad(Si)
3. V_{IL}/V_{IH}	Passed 80krad(Si)
4. V_{OL}/V_{OH}	Passed 80krad(Si)
5. Propagation Delays	Passed 80krad(Si)
6. Rising/Falling Edge Transient	Passed 80krad(Si)
7. Power-up Transient Current	Passed 80krad(Si)

Note: This test was performed in NASA/Goddard radiation facility following their radiation guideline.

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT54SX16
Package	CQFP208
Foundry	MEC
Technology	0.6µm CMOS
Die Lot Number	T6HP12D
Quantity Tested	6
Serial Numbers	LAN4202, LAN4203, LAN4204, LAN4205, LAN4206, LAN4207

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	1krad(Si)/hr (+/-10%)
Data Mode	Static (Except LAN4203)
Temperature	Room
Bias	3.3V/5.0V

C. Test Method

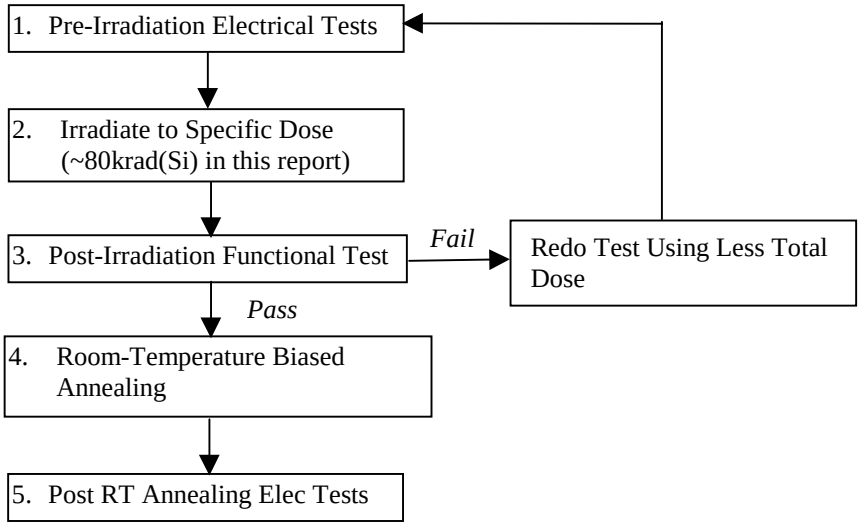

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has much less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This is almost logistically impossible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured accurately on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. Test Results

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced I_{CC} versus total dose for DUT LAN4202 and LAN4203. During irradiation, the logic states in LAN4202 were static while the logic states in LAN4203 were dynamically running at 1MHz. Failure in static case was detected by clocking out the data and comparing them with the truth table. The failures occurred at ~152krad(Si) and 240krad(Si) for static and dynamic case respectively. The sudden surge of I_{CC} at functional failure only occurred in static case. As expected from the published data on total dose effects of digital integrated circuits, the static case is worse than the dynamic case.

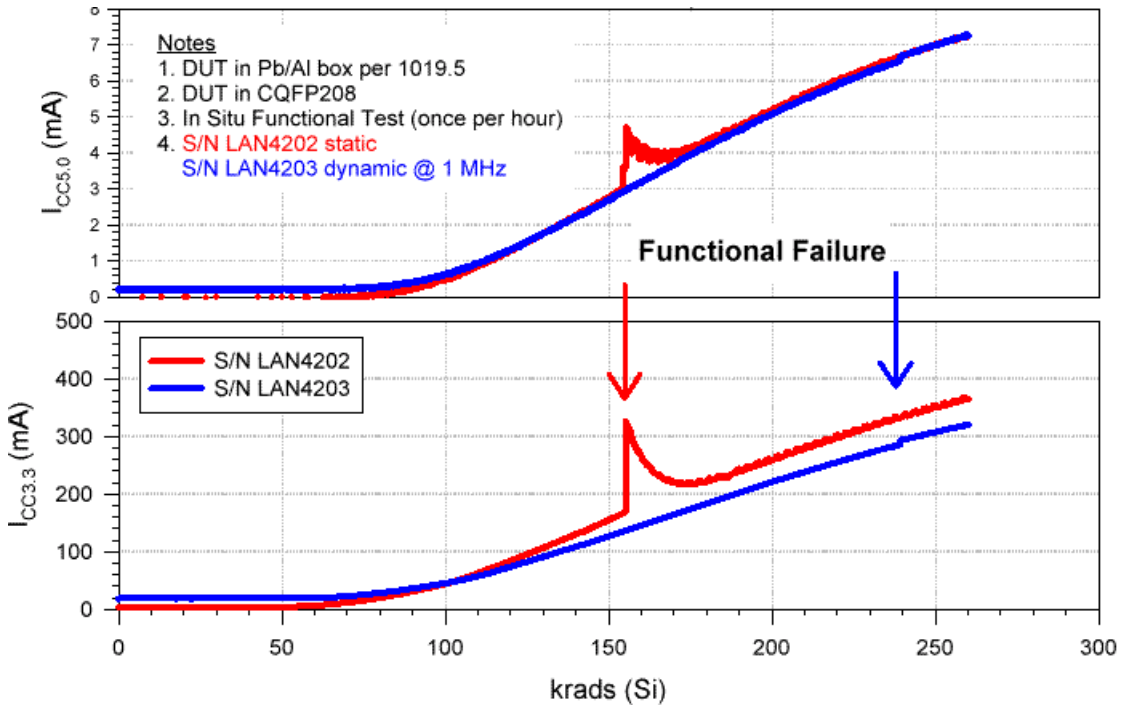

Figure 2. Radiation-induced I_{CC} (Delta I_{CC}) versus total dose for two DUTs (LAN4202 and LAN4203). Note that the static case (LAN4202) is worse than the dynamic case (LAN4203). In static case, the sudden surge of I_{CC} when functional failure occurred is an artifact due to testing setup.

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post room temperature annealing test (step 5). The room temperature annealing was performed for approximately 10 days to reduce the static leakage current and power-up transient current. The DUTs used for this test are LAN4204, LAN4205, LAN4206 and LAN4207.

1) Functional Test

Table 4 lists results of the functional test results.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Annealing
LAN4204	passed	passed
LAN4205	passed	passed
LAN4206	passed	passed
LAN4207	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

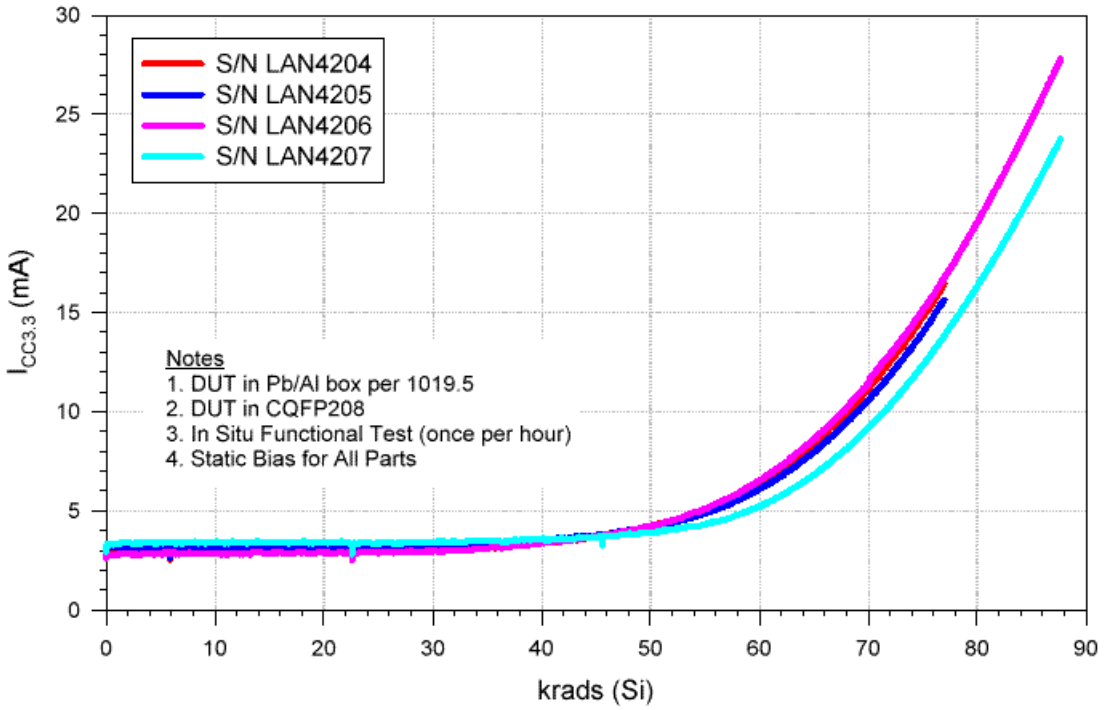

Figure 3. Radiation-induced Delta $I_{DDstandby}$ (I_{CC}) versus total dose for four DUTs (LAN4204, LAN4205, LAN4206 and LAN4207).

As shown in Figure 3, LAN4204, LAN4205, LAN4206 and LAN4207 were irradiated to approximately 80krad(Si). Every DUT has $I_{Ddstandby}$ below 25mA (the spec) after 80krad(Si) irradiation. It was observed later on that if the static state of the device during irradiation was reversed I_{CC} could increase by 100%. However, the room annealing results indicate that even with this worse condition, I_{CC} will drop within the spec in reasonable annealing time (months).

This new finding doesn't compromise the tests done so far because there are enough data for every test showing room temperature annealing effectively reducing I_{CC} to pass the target tolerance. I_{CC} versus annealing time can be predicted by a log-log plot. Using the extrapolated data from every test, we can predict the static I_{CC} will drop well within the spec (25mA).

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing. The irradiated DUTs are within the spec and the change of this parameter for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Annealing
LAN4204	1.48	1.49
LAN4205	1.50	1.45
LAN4206	1.50	1.45
LAN4207	1.50	1.44

4) Output Characteristic

Figure 4a and 4b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUTs. All irradiated DUTs are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 5a and 5b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUTs. All DUTs pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.

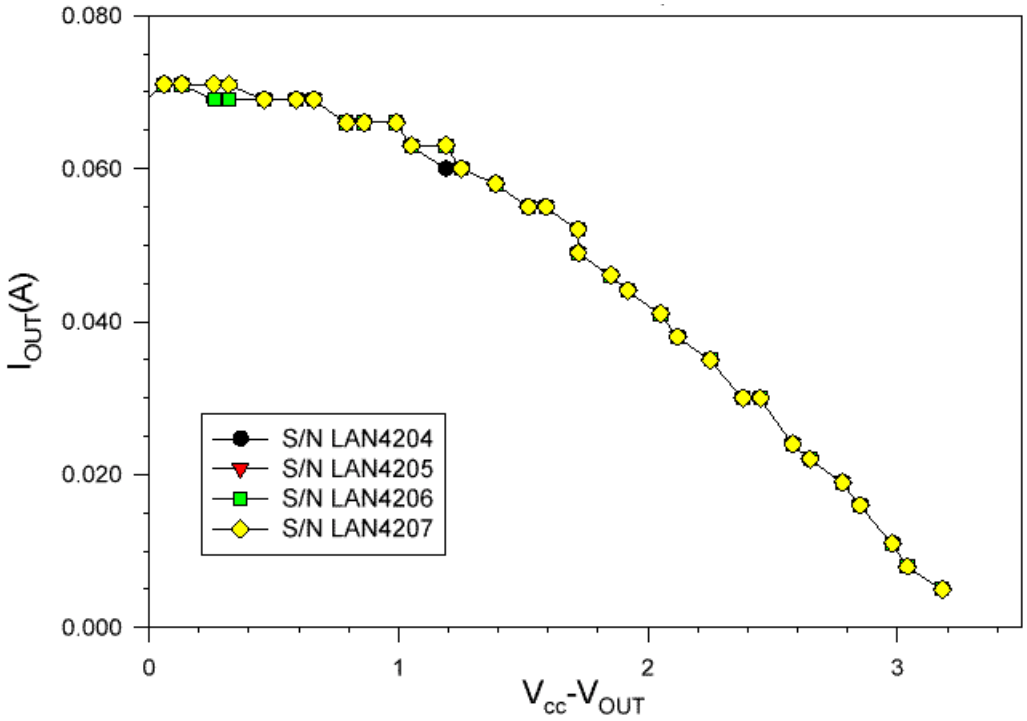

Figure 4a. Pre-irradiation V_{OL} characteristic curves.

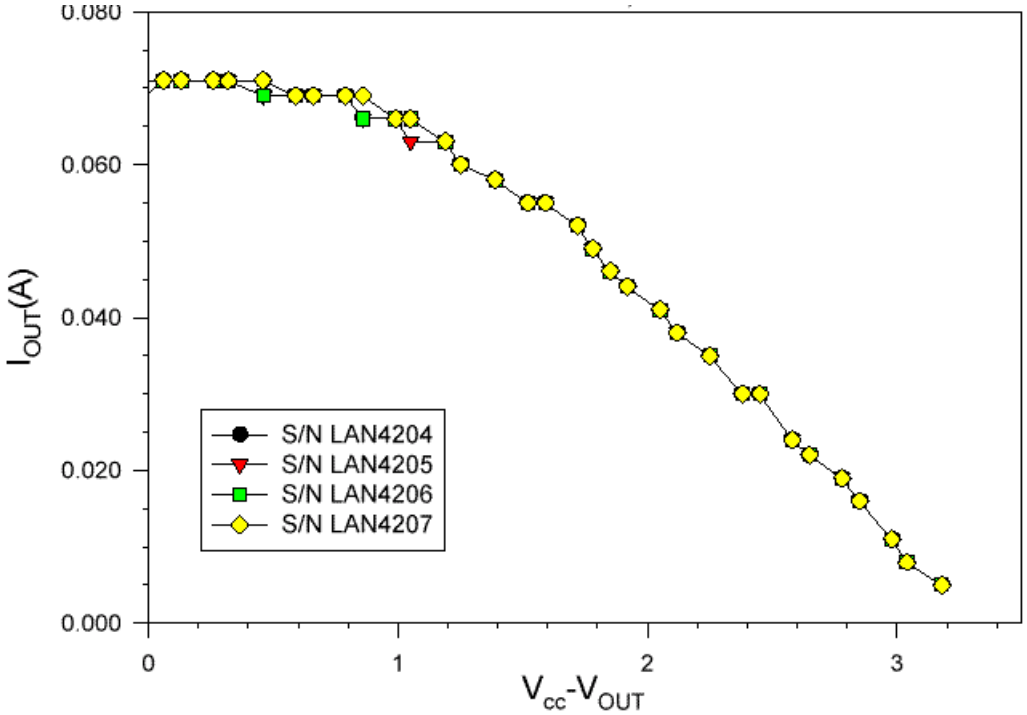

Figure 4b. Post-annealing V_{OL} characteristic curves.

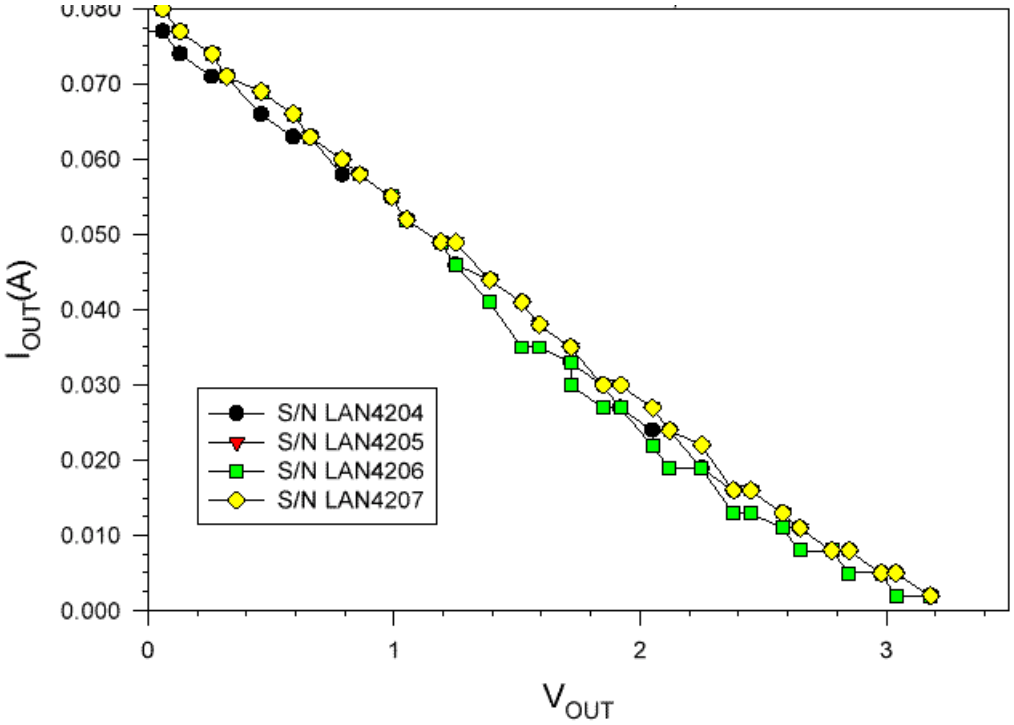

Figure 5a. Pre-irradiation V_{OH} characteristic curves.

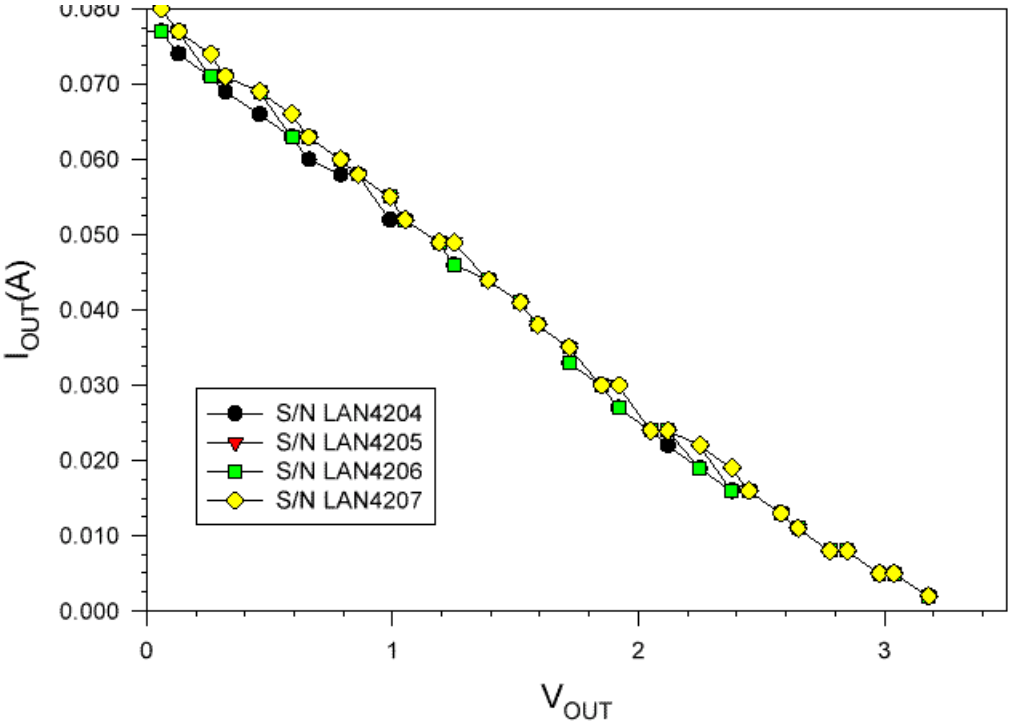

Figure 5b. Post-annealing V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4204	682	681	682	673
LAN4205	699	699	699	689
LAN4206	682	683	682	674
LAN4207	683	685	683	674

Table 7. Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4204	52.3	52.5	51.6	51.4
LAN4205	52.6	52.7	51.9	51.6
LAN4206	52.2	52.2	51.4	51.3
LAN4207	52.0	51.4	51.6	51.7

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4204	51.7	52.0	52.1	51.9
LAN4205	52.6	52.1	52.7	52.6
LAN4206	51.5	52.0	52.0	51.7
LAN4207	51.7	51.2	51.8	51.7

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The radiation effect is basically negligible.

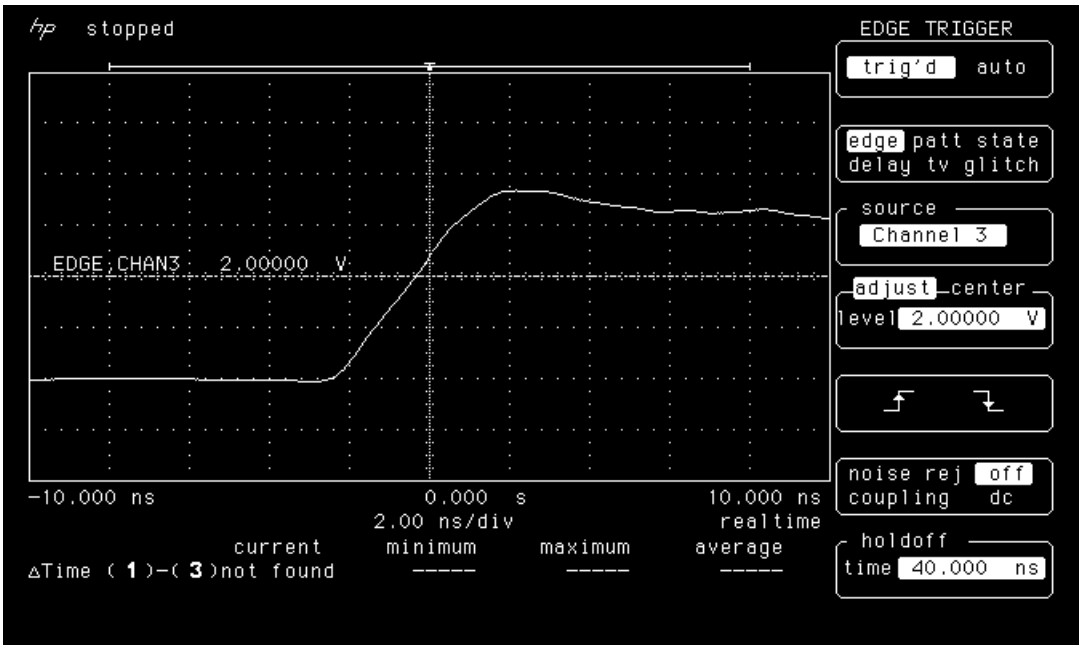

Figure 6a. Rising edge of LAN4204 pre-irradiation.

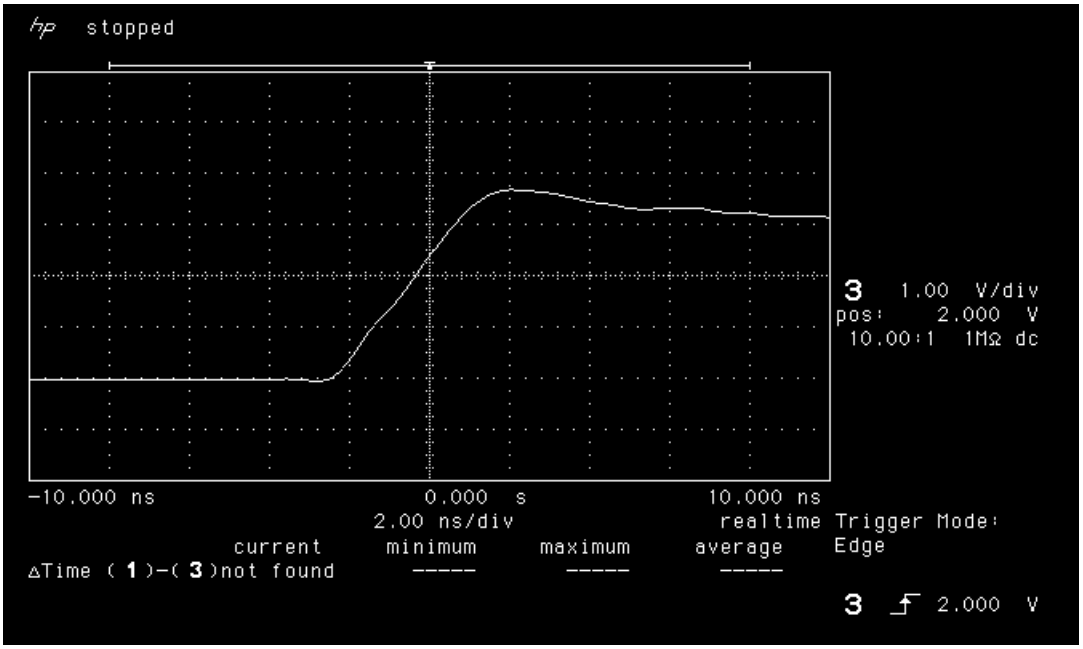

Figure 6b. Rising edge of LAN4204 post-annealing.

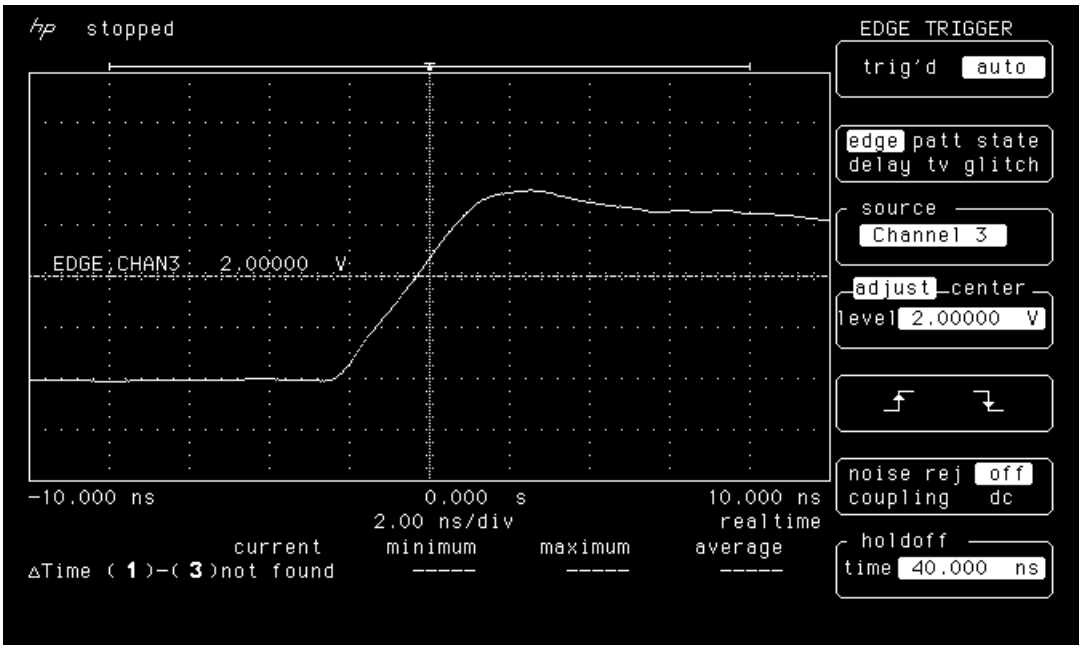

Figure 7a. Rising edge of LAN4205 pre-irradiation.

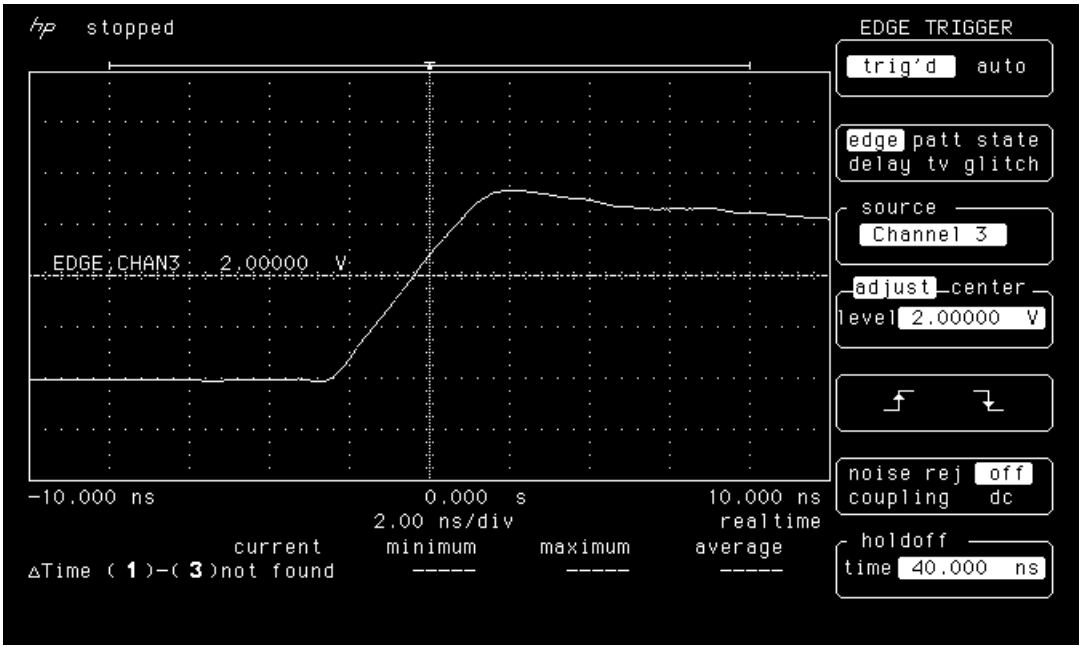

Figure 7b. Rising edge of LAN4205 post-annealing.

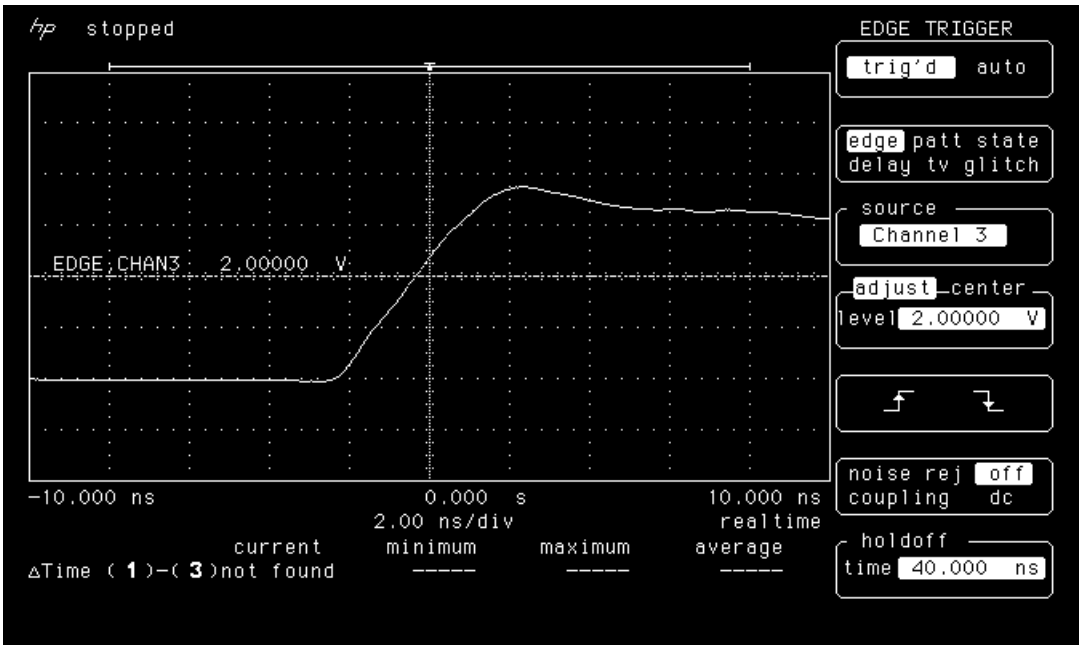

Figure 8a. Rising edge of LAN4206 pre-irradiation.

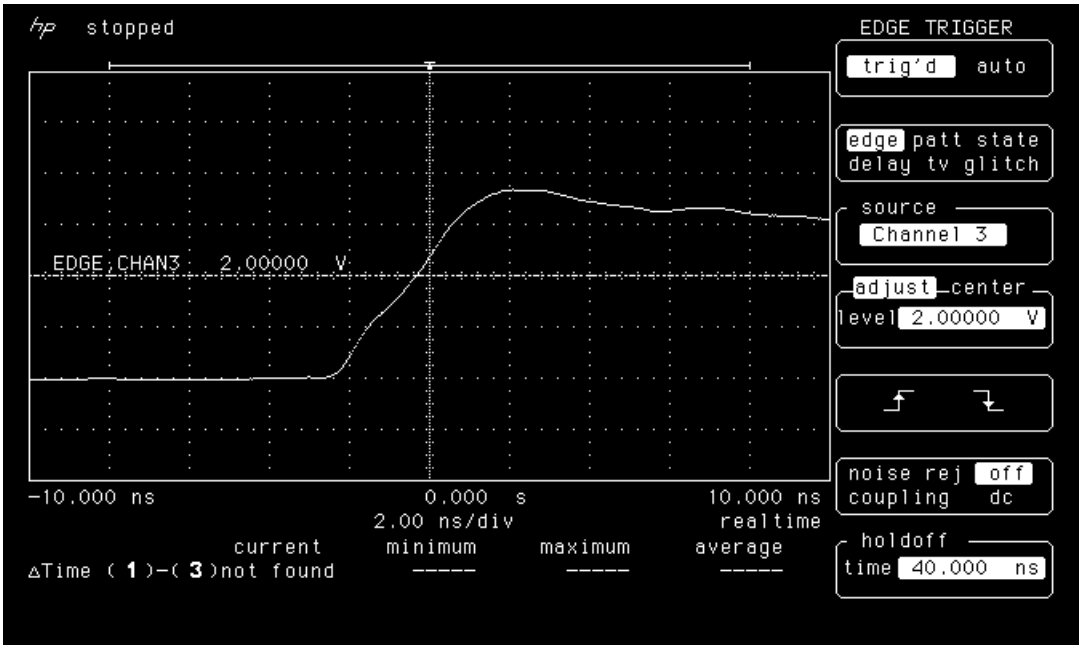

Figure 8b. Rising edge of LAN4206 post-annealing.

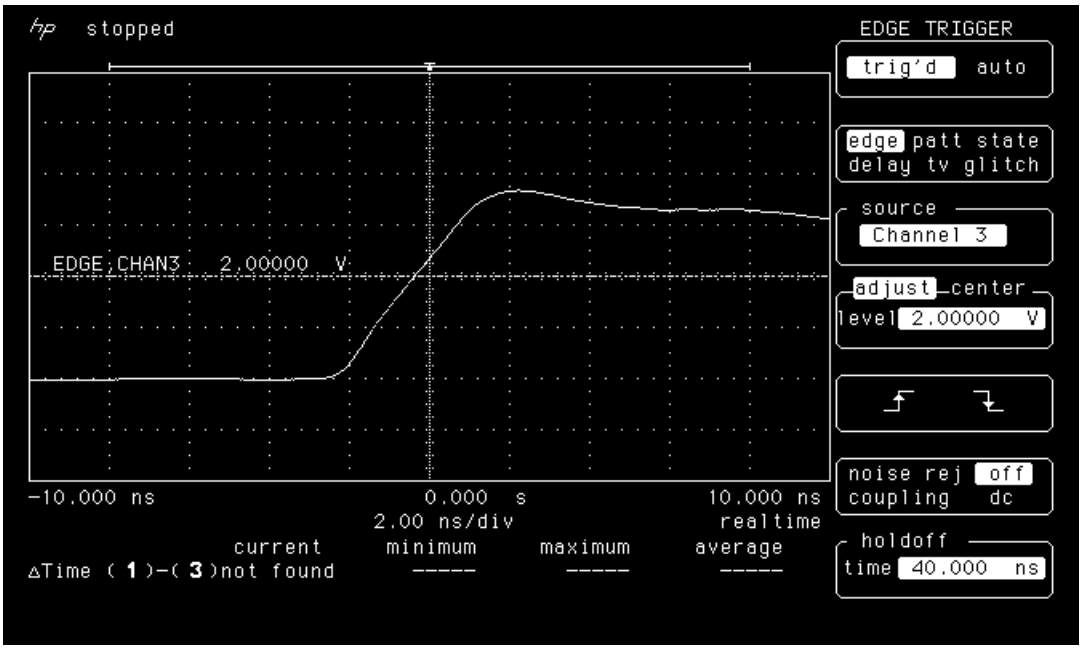

Figure 9a. Rising edge of LAN4207 pre-irradiation.

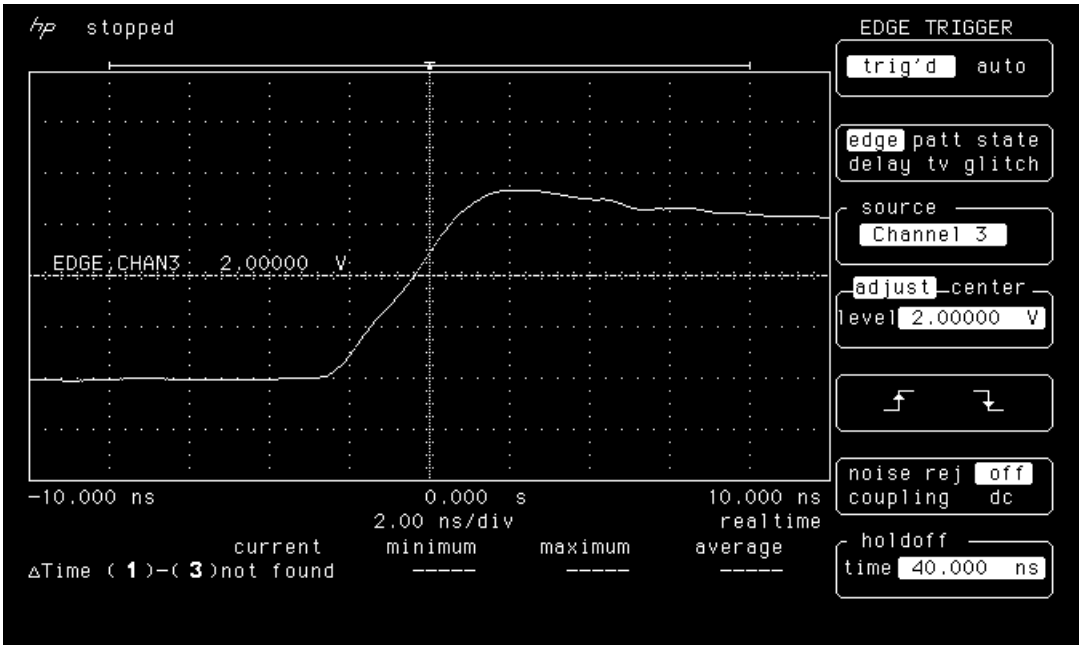

Figure 9b. Rising edge of LAN4207 post-annealing

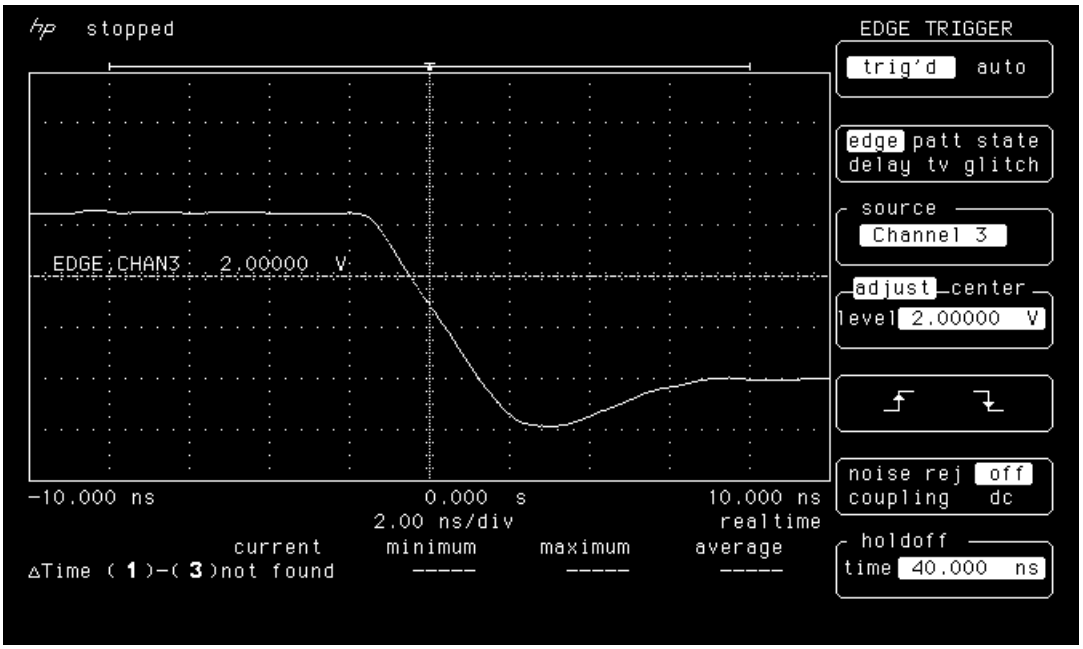

Figure 10a. Falling edge of LAN4204 pre-irradiation

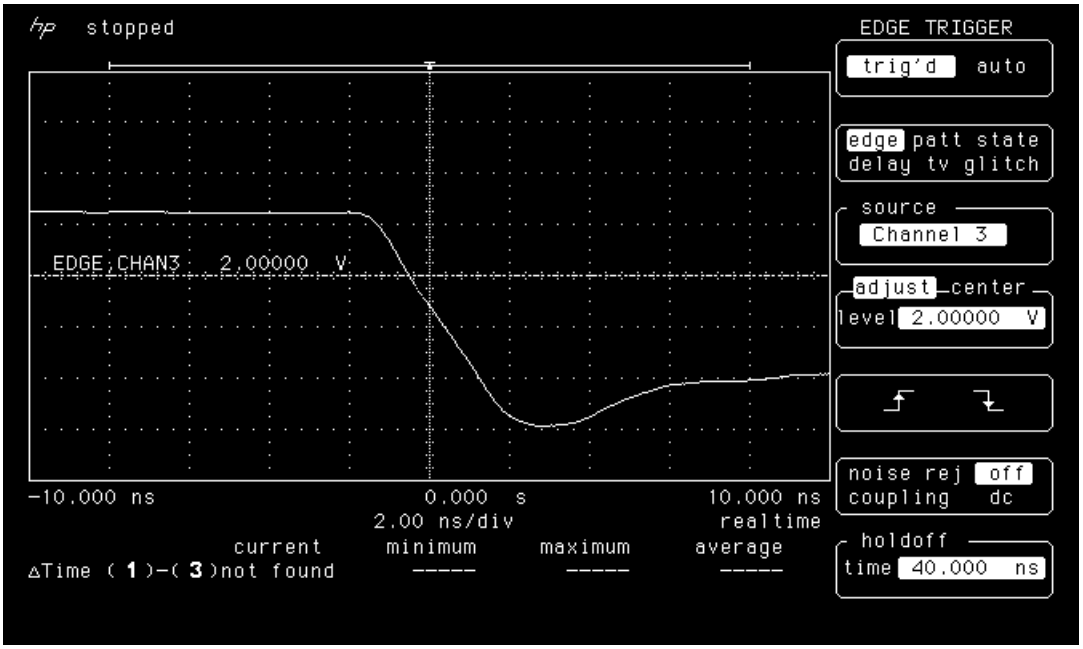

Figure 10b. Falling edge of LAN4204 post-annealing.

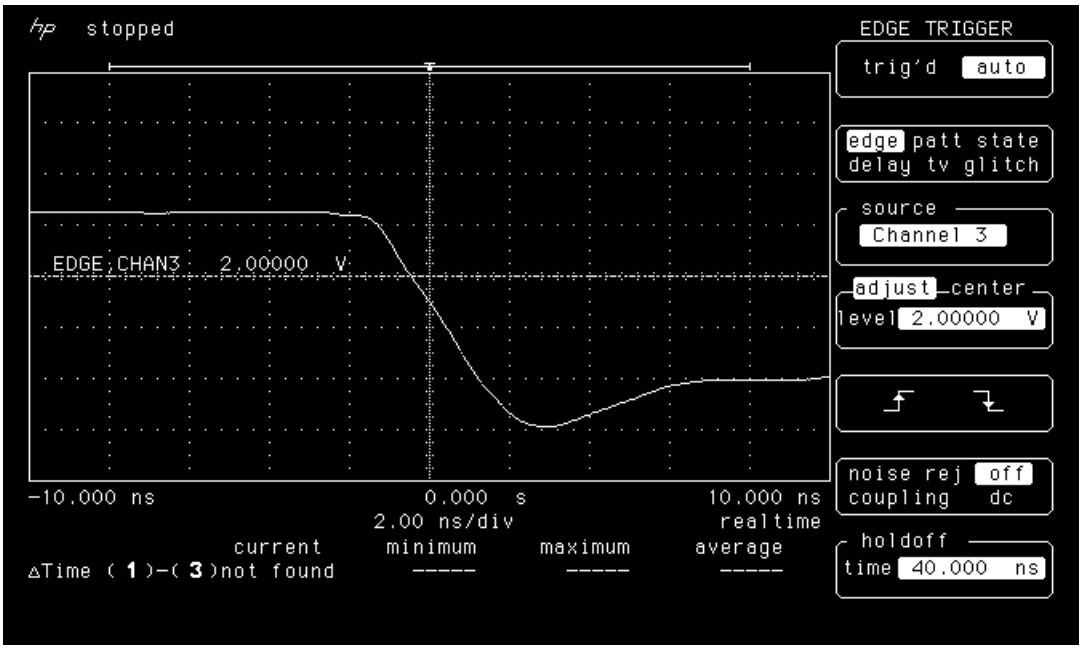

Figure 11a. Falling edge of LAN4205 pre-irradiation.

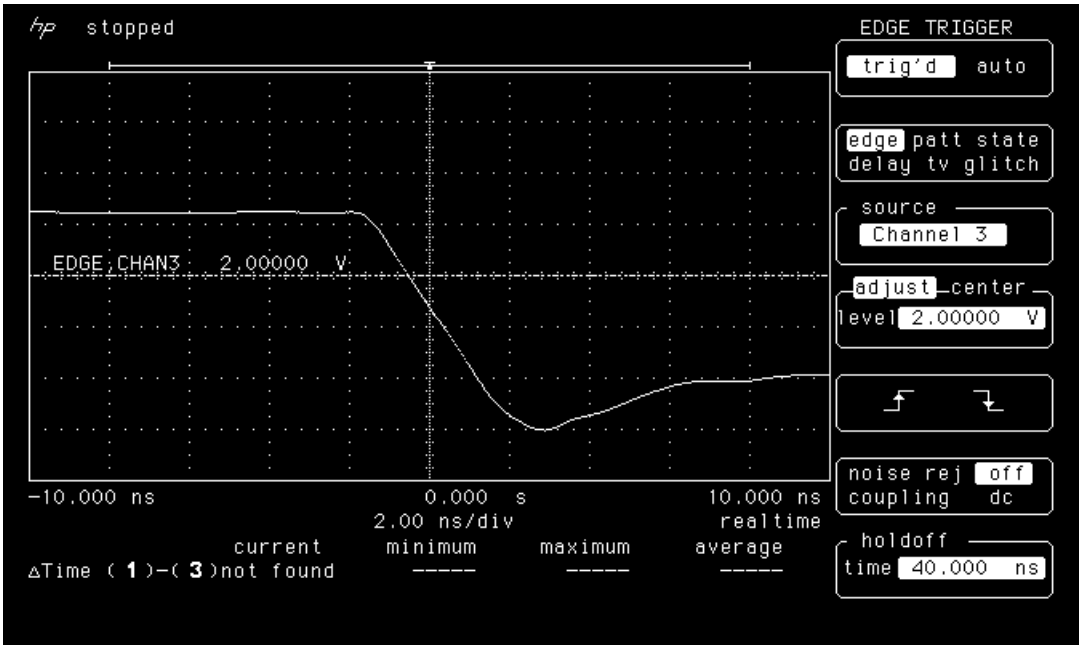

Figure 11b. Falling edge of LAN4205 post-annealing.

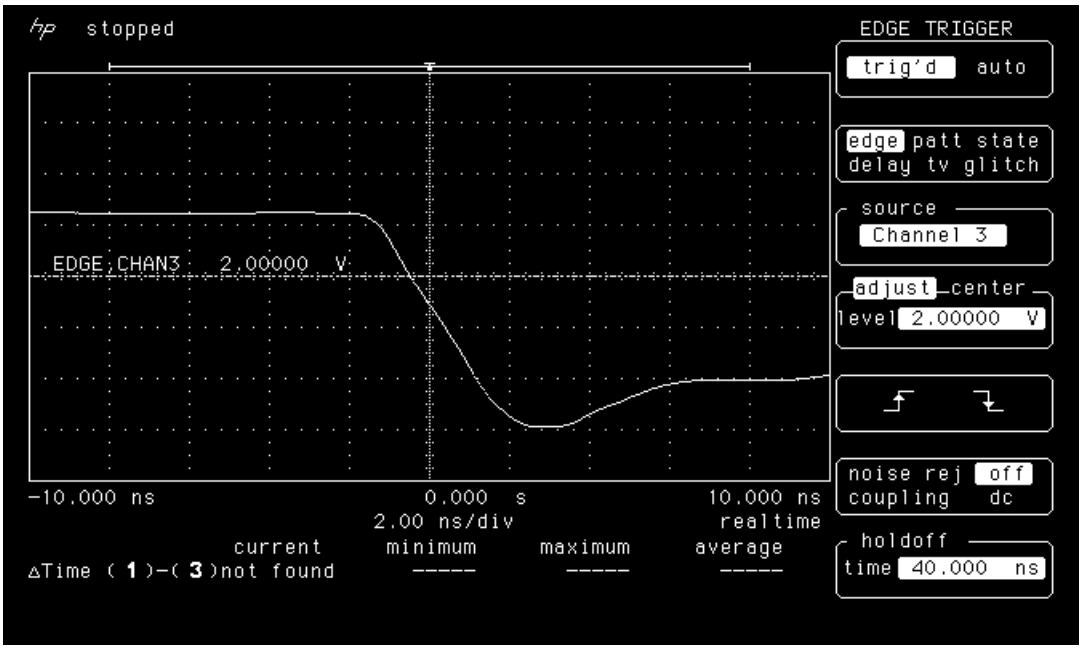

Figure 12a. Falling edge of LAN4206 pre-irradiation.

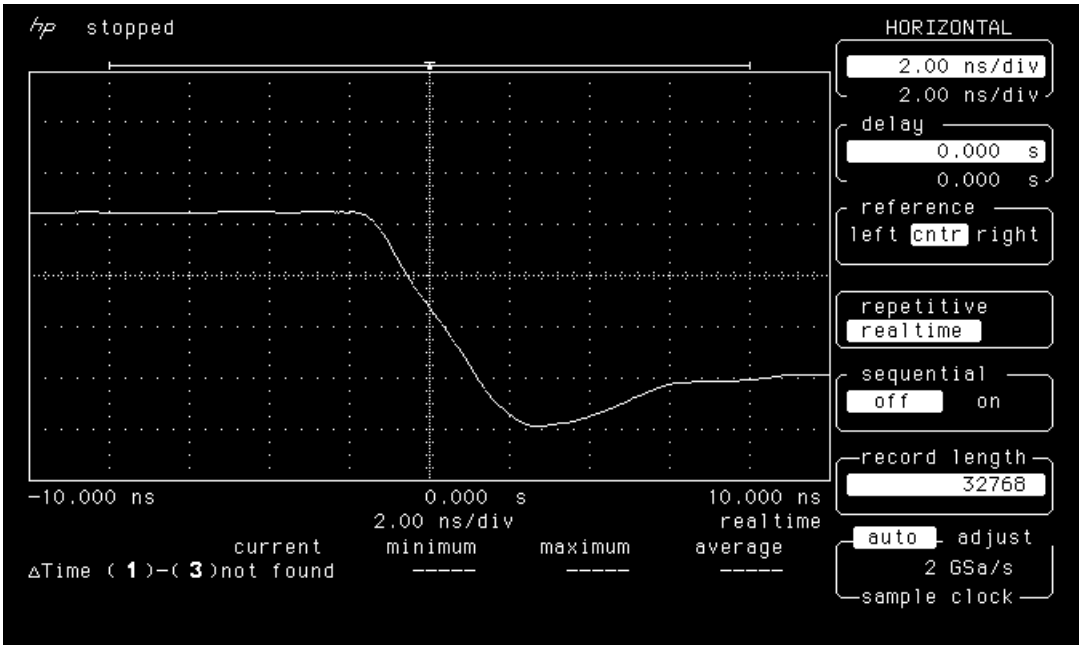

Figure 12b. Falling edge of LAN4206 post-annealing.

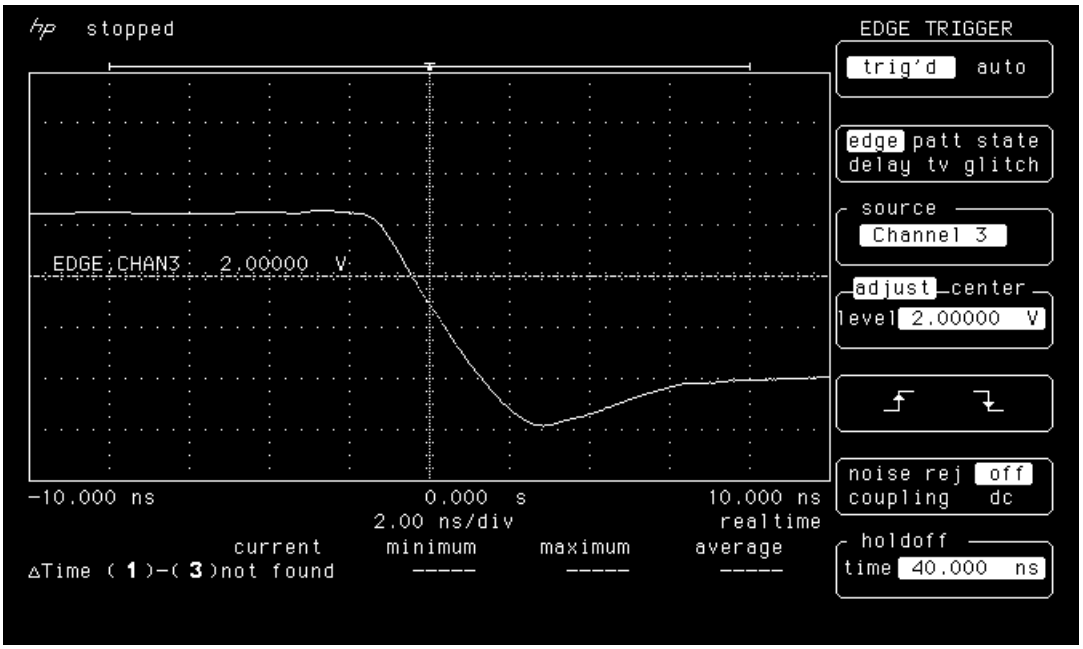

Figure 13a. Falling edge of LAN4207 pre-irradiation

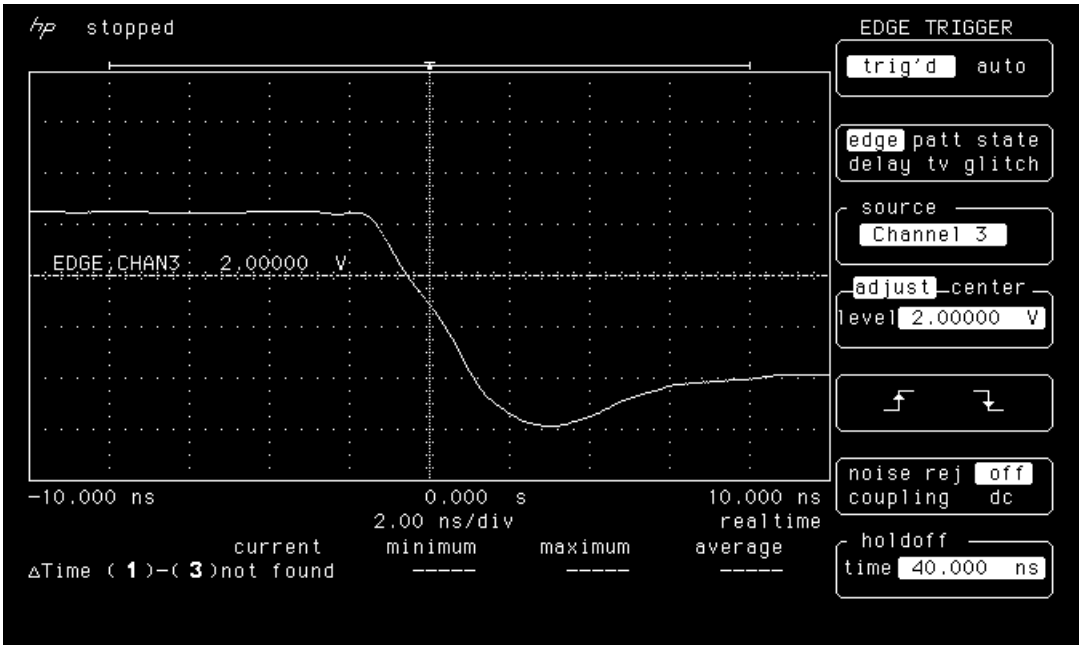

Figure 13b. Falling edge of LAN4207 post-annealing

7) Power-Up Transient

In each measurement, the rise time of the power supply voltage (V_{CC}) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 14-17 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 3.3V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. Post 80krad(Si) irradiation/annealing DUTs have a radiation induced transient current during power up (see, for example, Figure 14b). However, this transient is very minute. It can be annealed out completely, for example, in LAN4205. The details can be found in a previous publication ("Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278).

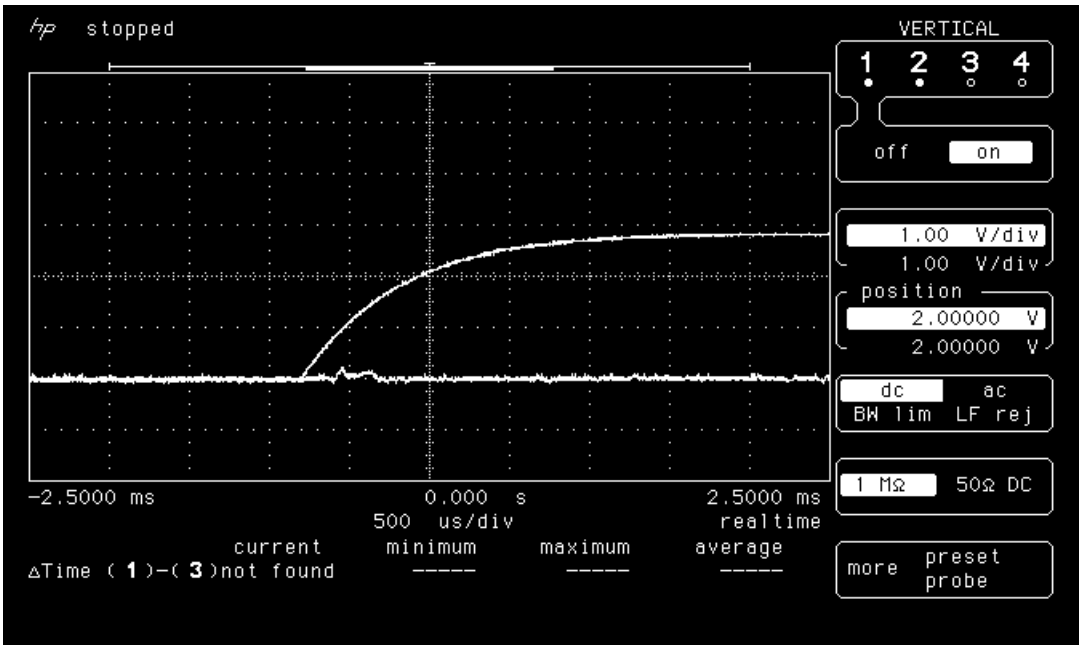

Figure 14a. Power-up transient of LAN4204 pre-irradiation.

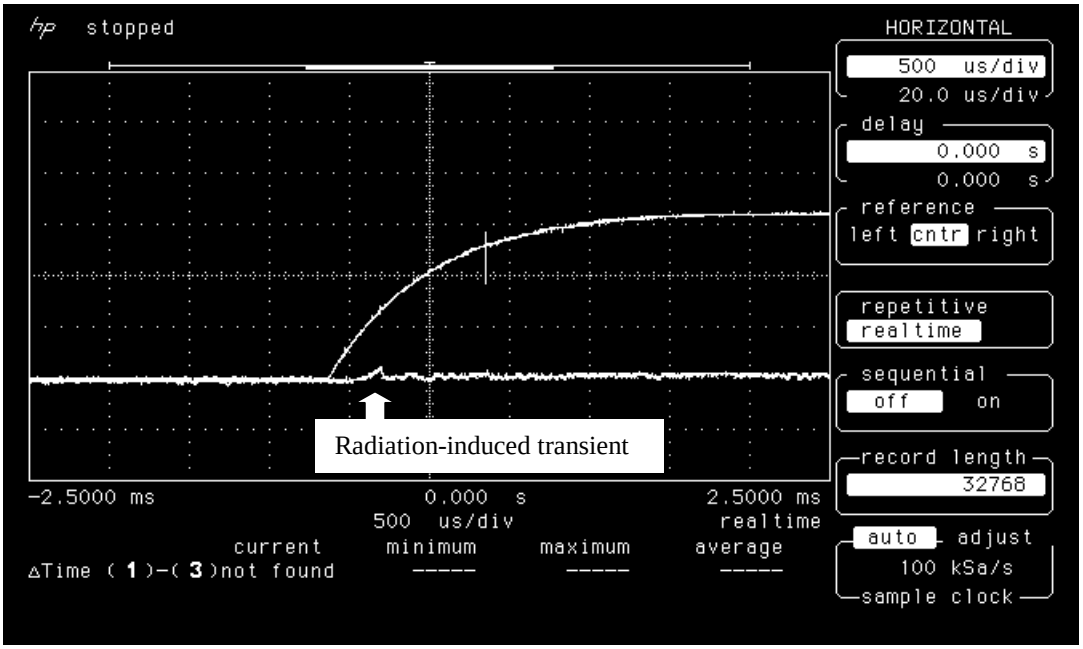

Figure 14b. Power-up transient of LAN4204 post-annealing.

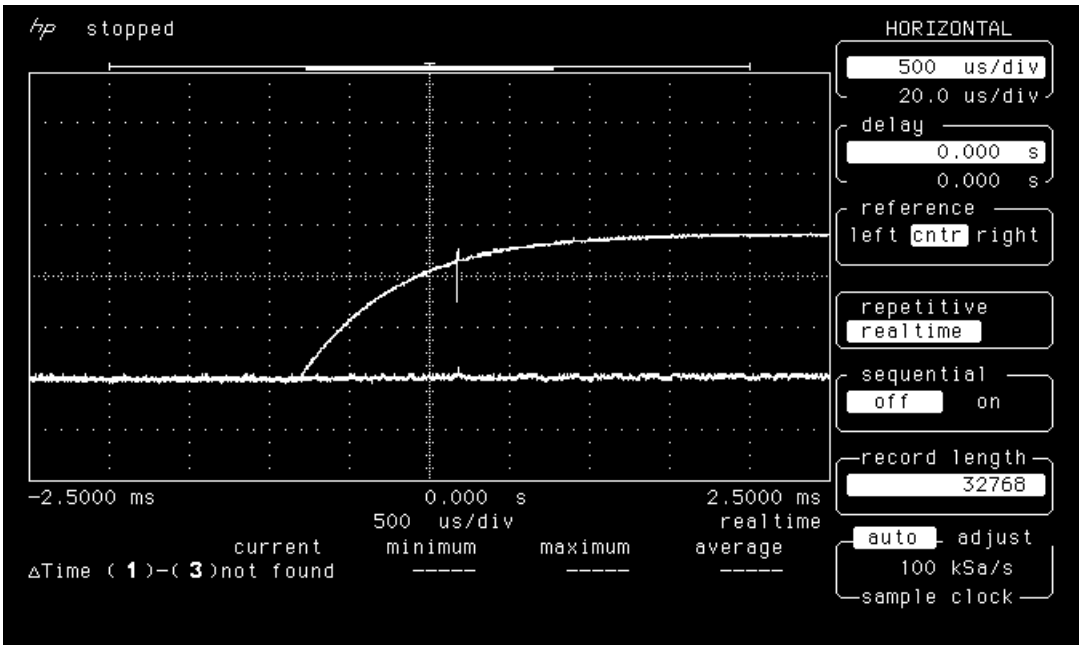

Figure 15a. Power-up transient of LAN4205 pre-irradiation.

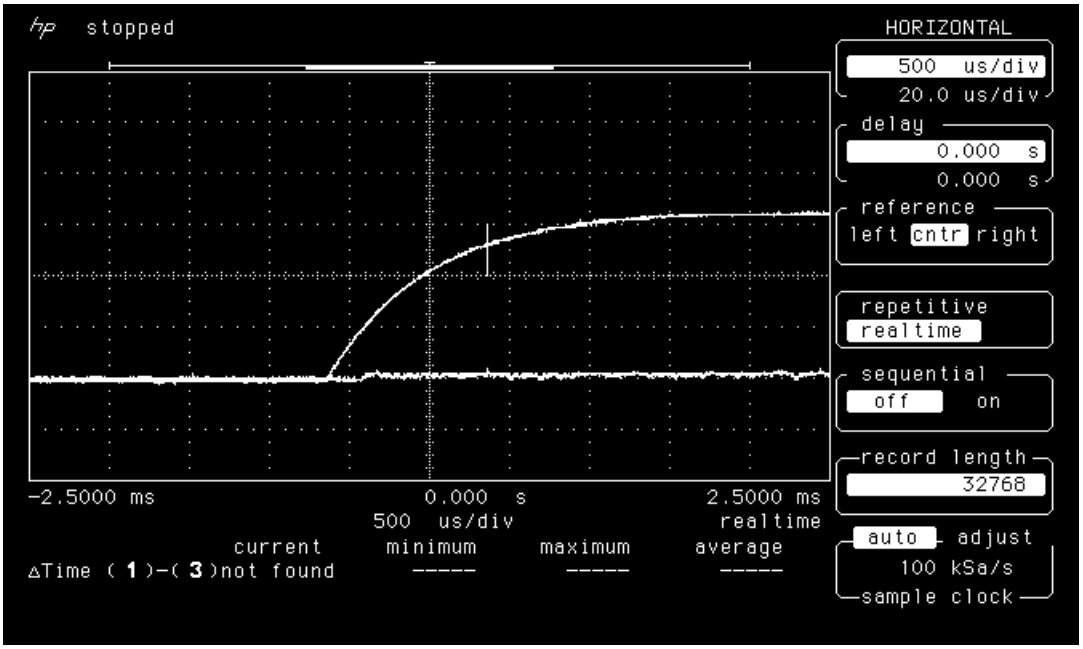

Figure 15b. Power-up transient of LAN4205 post-annealing.

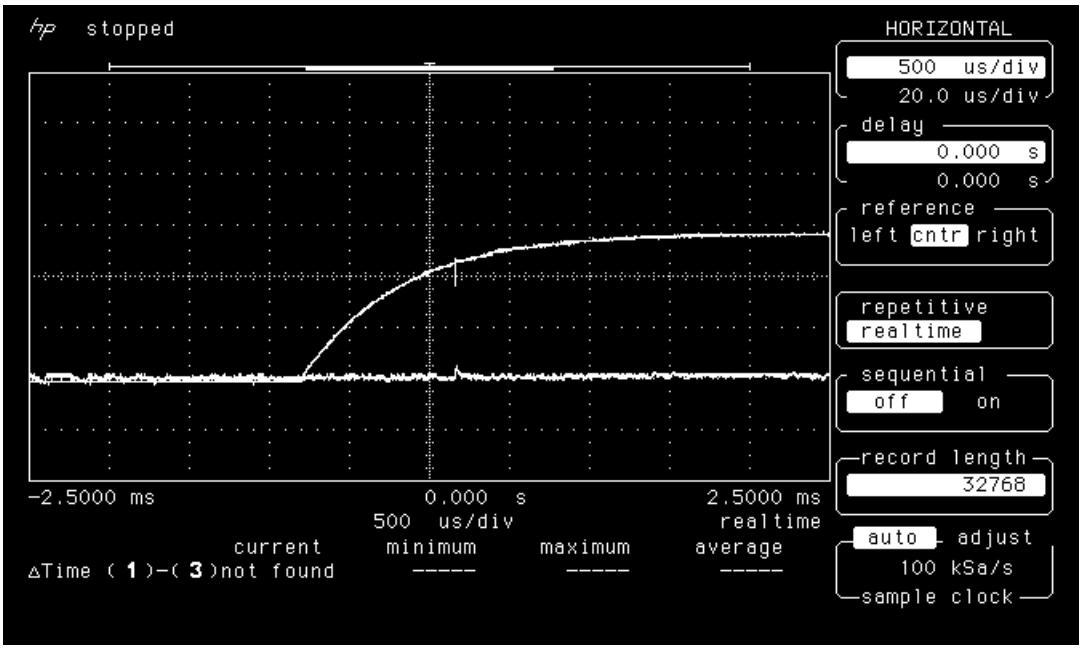

Figure 16a. Power-up transient of LAN4206 pre-irradiation.

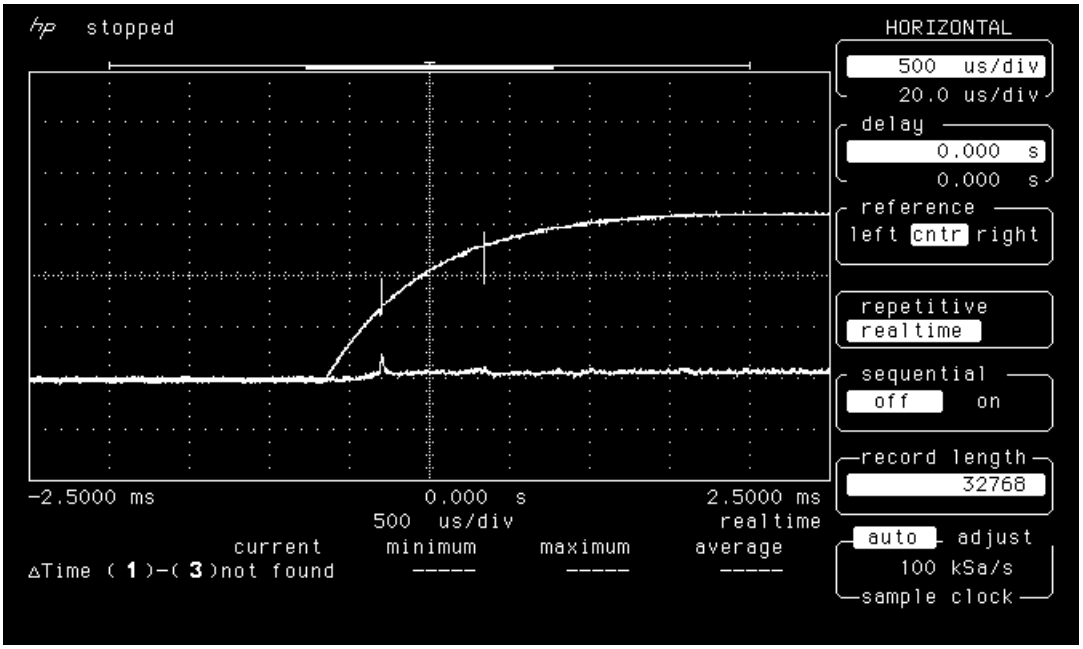

Figure 16b. Power-up transient of LAN4206 post-annealing.

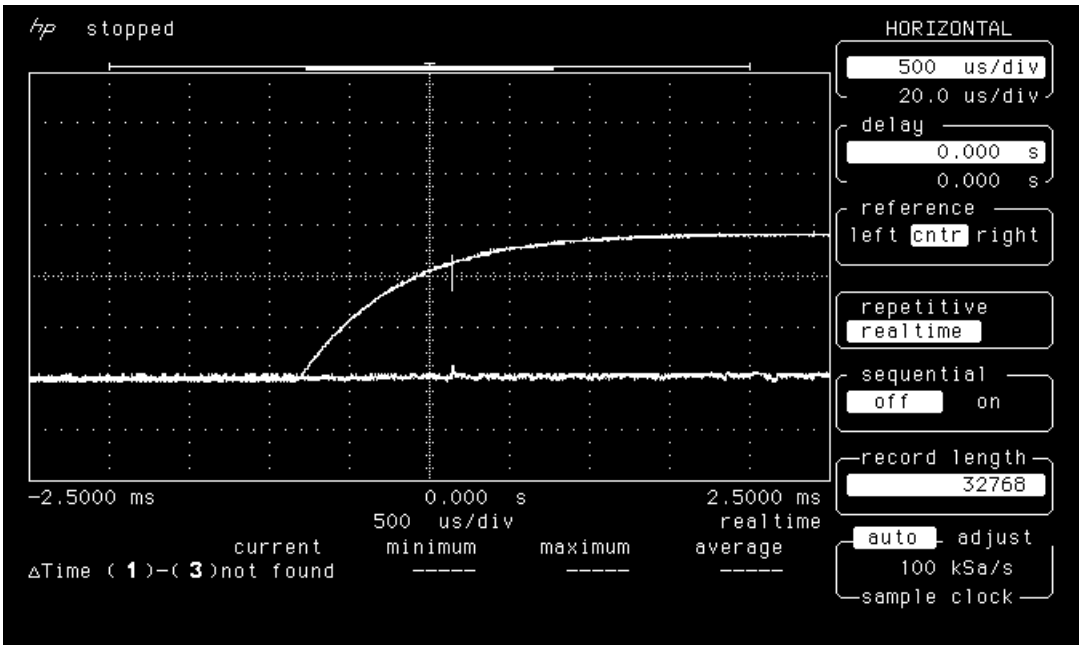

Figure 17a. Power-up transient of LAN4207 pre-irradiation

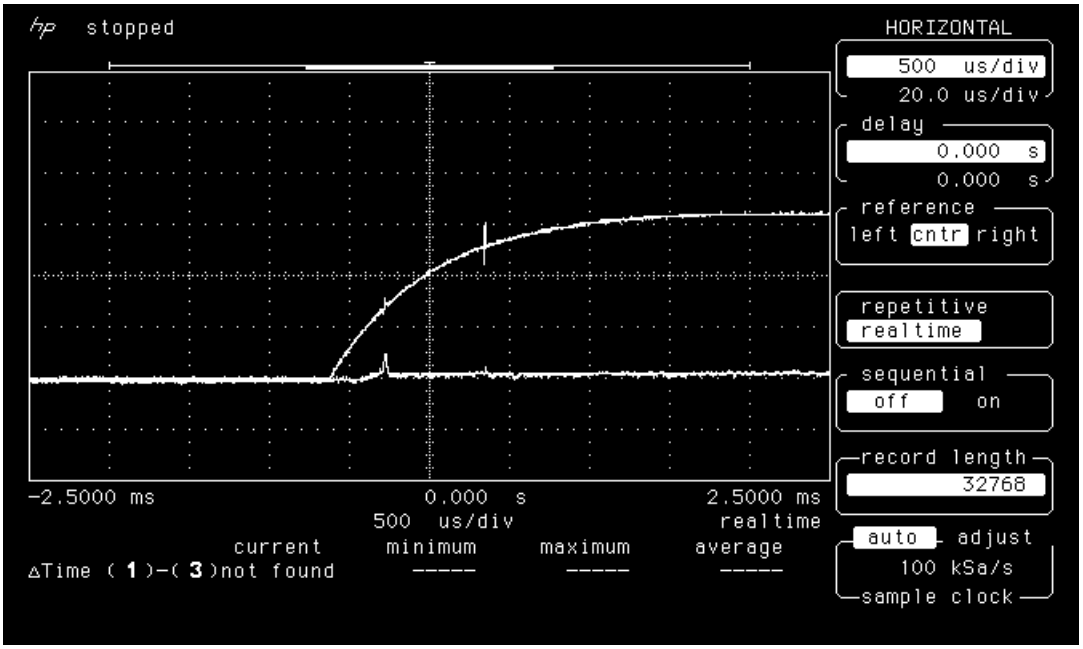

Figure 17b. Power-up transient of LAN4207 post-annealing