TOTAL IONIZING DOSE TEST REPORT  
No. 00T-RT54SX16-T6HP12D  
Dec. 13, 2000

J.J. Wang  
(408) 522-4576  
jih-jong.wang@actel.com

Igor Kleyner  
(301) 286-5683  
ingor.kleyner@nasa.gov

I. SUMMARY TABLE

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Gross Functional</td>
<td>152krad(Si) in static case, 240krad(Si) in dynamic case</td>
</tr>
<tr>
<td>2. $I_{DDSTDBY}$</td>
<td>Passed 80krad(Si)</td>
</tr>
<tr>
<td>3. $V_{IL}/V_{IH}$</td>
<td>Passed 80krad(Si)</td>
</tr>
<tr>
<td>4. $V_{OL}/V_{OH}$</td>
<td>Passed 80krad(Si)</td>
</tr>
<tr>
<td>5. Propagation Delays</td>
<td>Passed 80krad(Si)</td>
</tr>
<tr>
<td>6. Rising/Falling Edge Transient</td>
<td>Passed 80krad(Si)</td>
</tr>
<tr>
<td>7. Power-up Transient Current</td>
<td>Passed 80krad(Si)</td>
</tr>
</tbody>
</table>

Note: This test was performed in NASA/Goddard radiation facility following their radiation guideline.

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

<table>
<thead>
<tr>
<th>Table 1. DUT Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
</tr>
<tr>
<td>Package</td>
</tr>
<tr>
<td>Foundry</td>
</tr>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Die Lot Number</td>
</tr>
<tr>
<td>Quantity Tested</td>
</tr>
<tr>
<td>Serial Numbers</td>
</tr>
</tbody>
</table>

B. Irradiation

Table 2 lists the irradiation parameters.

<table>
<thead>
<tr>
<th>Table 2. Irradiation Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Facility</td>
</tr>
<tr>
<td>Radiation Source</td>
</tr>
<tr>
<td>Dose Rate</td>
</tr>
<tr>
<td>Data Mode</td>
</tr>
<tr>
<td>Temperature</td>
</tr>
<tr>
<td>Bias</td>
</tr>
</tbody>
</table>
C. Test Method

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has much less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DD\text{standby}}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DD\text{standby}}$ and functionality (of selected pins) during irradiation. This is almost logistically impossible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured accurately on the bench. Table 3 lists the corresponding logic design for each test parameter.
III. TEST RESULTS

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced $I_{CC}$ versus total dose for DUT LAN4202 and LAN4203. During irradiation, the logic states in LAN4202 were static while the logic states in LAN4203 were dynamically running at 1MHz. Failure in static case was detected by clocking out the data and comparing them with the truth table. The failures occurred at ~152krad(Si) and 240krad(Si) for static and dynamic case respectively. The sudden surge of $I_{CC}$ at functional failure only occurred in static case. As expected from the published data on total dose effects of digital integrated circuits, the static case is worse than the dynamic case.

![Figure 2. Radiation-induced $I_{CC}$ (Delta $I_{CC}$) versus total dose for two DUTs (LAN4202 and LAN4203). Note that the static case (LAN4202) is worse than the dynamic case (LAN4203). In static case, the sudden surge of $I_{CC}$ when functional failure occurred is an artifact due to testing setup.](image)

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post room temperature annealing test (step 5). The room temperature annealing was performed for approximately 10 days to reduce the static leakage current and power-up transient current. The DUTs used for this test are LAN4204, LAN4205, LAN4206 and LAN4207.
1) Functional Test

Table 4 lists results of the functional test results.

<table>
<thead>
<tr>
<th>LAN4204</th>
<th>LAN4205</th>
<th>LAN4206</th>
<th>LAN4207</th>
</tr>
</thead>
<tbody>
<tr>
<td>passed</td>
<td>passed</td>
<td>passed</td>
<td>passed</td>
</tr>
</tbody>
</table>

2) $I_{DDSTANDBY}$ (Static $I_{CC}$ or $I_{DD}$)

$I_{DDSTANDBY}$ was monitored during the irradiation. The delta $I_{DDSTANDBY}$ is the increment $I_{DDSTANDBY}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDSTANDBY}$ is negligible. The delta $I_{DDSTANDBY}$ spec is approximately 25mA and used to determine tolerance.

![Figure 3. Radiation-induced Delta $I_{DDSTANDBY}$ ($I_{CC}$) versus total dose for four DUTs (LAN4204, LAN4205, LAN4206 and LAN4207).](image)

As shown in Figure 3, LAN4204, LAN4205, LAN4206 and LAN4207 were irradiated to approximately 80krad(Si). Every DUT has $I_{DDSTANDBY}$ below 25mA (the spec) after 80krad(Si) irradiation. It was observed later on that if the static state of the device during irradiation was reversed $I_{CC}$ could increase by 100%. However, the room annealing results indicate that even with this worse condition, $I_{CC}$ will drop within the spec in reasonable annealing time (months).

This new finding doesn’t compromise the tests done so far because there are enough data for every test showing room temperature annealing effectively reducing $I_{CC}$ to pass the target tolerance. $I_{CC}$ versus annealing time can be predicted by a log-log plot. Using the extrapolated data from every test, we can predict the static $I_{CC}$ will drop well within the spec (25mA).
3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing. The irradiated DUTs are within the spec and the change of this parameter for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

<table>
<thead>
<tr>
<th></th>
<th>Pre-Irradiation</th>
<th>Post-Annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAN4204</td>
<td>1.48</td>
<td>1.49</td>
</tr>
<tr>
<td>LAN4205</td>
<td>1.50</td>
<td>1.45</td>
</tr>
<tr>
<td>LAN4206</td>
<td>1.50</td>
<td>1.45</td>
</tr>
<tr>
<td>LAN4207</td>
<td>1.50</td>
<td>1.44</td>
</tr>
</tbody>
</table>

4) Output Characteristic

Figure 4a and 4b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUTs. All irradiated DUTs are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 5a and 5b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUTs. All DUTs pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.
Figure 4a. Pre-irradiation $V_{\text{OL}}$ characteristic curves.

Figure 4b. Post-annealing $V_{\text{OL}}$ characteristic curves.
Figure 5a. Pre-irradiation $V_{OH}$ characteristic curves.

Figure 5b. Post-annealing $V_{OH}$ characteristic curves.
5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

<table>
<thead>
<tr>
<th></th>
<th>Rising Output</th>
<th>Falling Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pre-Irradiation</td>
<td>Post-Annealing</td>
</tr>
<tr>
<td>LAN4204</td>
<td>682</td>
<td>681</td>
</tr>
<tr>
<td>LAN4205</td>
<td>699</td>
<td>699</td>
</tr>
<tr>
<td>LAN4206</td>
<td>682</td>
<td>683</td>
</tr>
<tr>
<td>LAN4207</td>
<td>683</td>
<td>685</td>
</tr>
</tbody>
</table>

Table 7. Serial-In Delays (ns)

<table>
<thead>
<tr>
<th></th>
<th>Rising Output</th>
<th>Falling Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pre-Irradiation</td>
<td>Post-Annealing</td>
</tr>
<tr>
<td>LAN4204</td>
<td>52.3</td>
<td>52.5</td>
</tr>
<tr>
<td>LAN4205</td>
<td>52.6</td>
<td>52.7</td>
</tr>
<tr>
<td>LAN4206</td>
<td>52.2</td>
<td>52.2</td>
</tr>
<tr>
<td>LAN4207</td>
<td>52.0</td>
<td>51.4</td>
</tr>
</tbody>
</table>

Table 8. Serial-Out Delays (ns)

<table>
<thead>
<tr>
<th></th>
<th>Rising Output</th>
<th>Falling Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pre-Irradiation</td>
<td>Post-Annealing</td>
</tr>
<tr>
<td>LAN4204</td>
<td>51.7</td>
<td>52.0</td>
</tr>
<tr>
<td>LAN4205</td>
<td>52.6</td>
<td>52.1</td>
</tr>
<tr>
<td>LAN4206</td>
<td>51.5</td>
<td>52.0</td>
</tr>
<tr>
<td>LAN4207</td>
<td>51.7</td>
<td>51.2</td>
</tr>
</tbody>
</table>

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The radiation effect is basically negligible.
Figure 6a. Rising edge of LAN4204 pre-irradiation.

Figure 6b. Rising edge of LAN4204 post-annealing.
Figure 7a. Rising edge of LAN4205 pre-irradiation.

Figure 7b. Rising edge of LAN4205 post-annealing.
Figure 8a. Rising edge of LAN4206 pre-irradiation.

Figure 8b. Rising edge of LAN4206 post-annealing.
Figure 9a. Rising edge of LAN4207 pre-irradiation.

Figure 9b. Rising edge of LAN4207 post-annealing
Figure 10a. Falling edge of LAN4204 pre-irradiation

Figure 10b. Falling edge of LAN4204 post-annealing.
Figure 11a. Falling edge of LAN4205 pre-irradiation.

Figure 11b. Falling edge of LAN4205 post-annealing.
Figure 12a. Falling edge of LAN4206 pre-irradiation.

Figure 12b. Falling edge of LAN4206 post-annealing.
Figure 13a. Falling edge of LAN4207 pre-irradiation

Figure 13b. Falling edge of LAN4207 post-annealing
7) Power-Up Transient

In each measurement, the rise time of the power supply voltage ($V_{CC}$) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 14-17 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing $V_{CC}$ ramping from GND to 3.3V, and another curve showing $I_{CC}$. The scale is 1V per division for $V_{CC}$ and 100mA per division for $I_{CC}$. Post 80krad(Si) irradiation/annealing DUTs have a radiation induced transient current during power up (see, for example, Figure 14b). However, this transient is very minute. It can be annealed out completely, for example, in LAN4205. The details can be found in a previous publication (“Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA,” by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278).
Figure 14a. Power-up transient of LAN4204 pre-irradiation.

Figure 14b. Power-up transient of LAN4204 post-annealing.
Figure 15a. Power-up transient of LAN4205 pre-irradiation.

Figure 15b. Power-up transient of LAN4205 post-annealing.
Figure 16a. Power-up transient of LAN4206 pre-irradiation.

Figure 16b. Power-up transient of LAN4206 post-annealing.
Figure 17a. Power-up transient of LAN4207 pre-irradiation

Figure 17b. Power-up transient of LAN4207 post-annealing