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TOTAL IONIZING DOSE TEST REPORT

No. 00T-RT54SX16-T6HP12
J. J. Wang
(408)522-4576
jih-jong.wang@actel.com

I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	> 80krad(Si), exact number will be provided in a supplemental report
2. $I_{DDSTDBY}$	Passed 80krad(Si)
3. V_{IL}/V_{IH}	Passed 80krad(Si)
4. V_{OL}/V_{OH}	Passed 80krad(Si)
5. Propagation Delays	Passed 80krad(Si)
6. Rising/Falling Edge Transient	Passed 80krad(Si)
7. Power-up Transient Current	Passed 80krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device(s) under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT54SX16 (Rev 1)
Package	CQFP208
Foundry	MEC
Technology	0.6µm CMOS
Die Lot Number	T6HP12
Quantity Tested	3
Serial Numbers	LAN2901, LAN2902, LAN2903

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA
Radiation Source	Co-60
Dose Rate	1krad(Si)/hr (+-10%)
Final Total Dose	80krad(Si)
Temperature	Room
Bias	3.3V/5.0V

C. Test Method

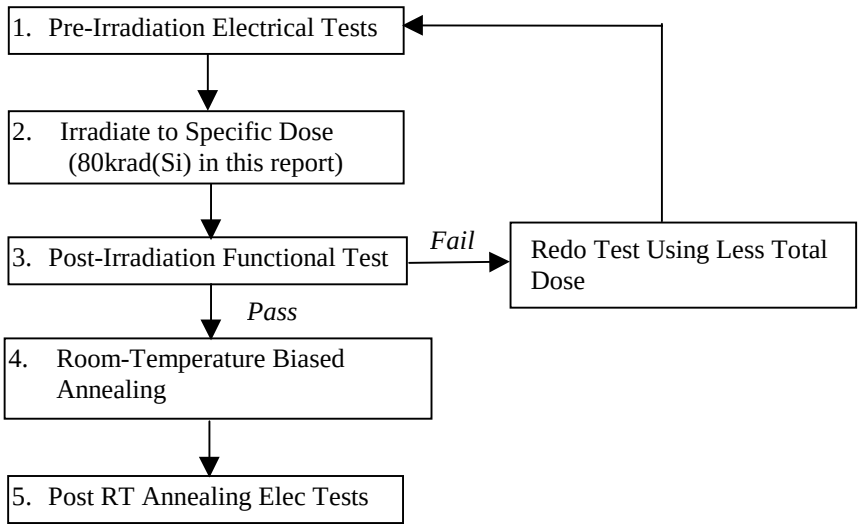

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and then parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019. Biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGAs fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has much less noise but can only sample few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This won't be logistically possible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. TEST RESULTS

A. Method One: Irradiate to Gross Functional Failure

This test was not performed due to temporary shortage of the package part. A supplemental report will be followed to provide the test results.

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation (step 1 in Figure 1) and post room temperature annealing tests (step 5). The only post-irradiation (step 3) test is the gross functional test.

1) Functional Test

Table 4 lists results of the functional test.

Table 4. Functional Test Results

	Pre-Irradiation	Post-Irradiation	Post-Annealing
LAN2901	passed	passed	passed
LAN2902	passed	passed	passed
LAN2903	passed	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation and room-temperature annealing. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation/annealing effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

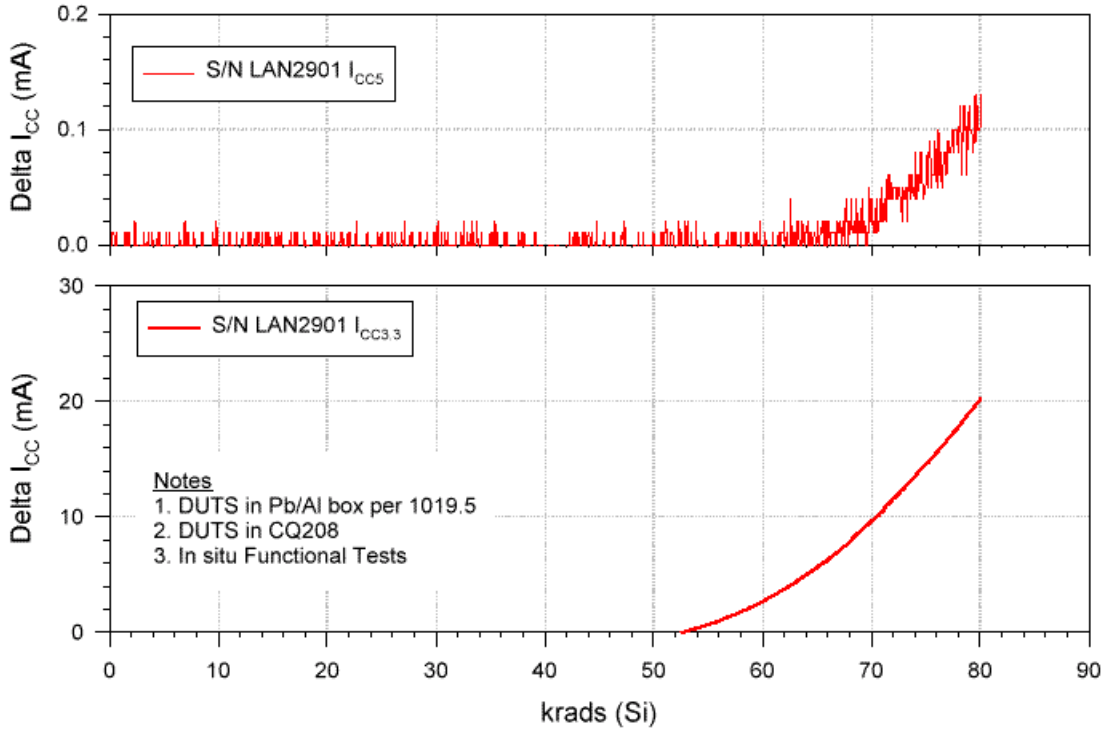

Figure 2a. Delta $I_{DDstandby}$ versus total dose, LAN2901.

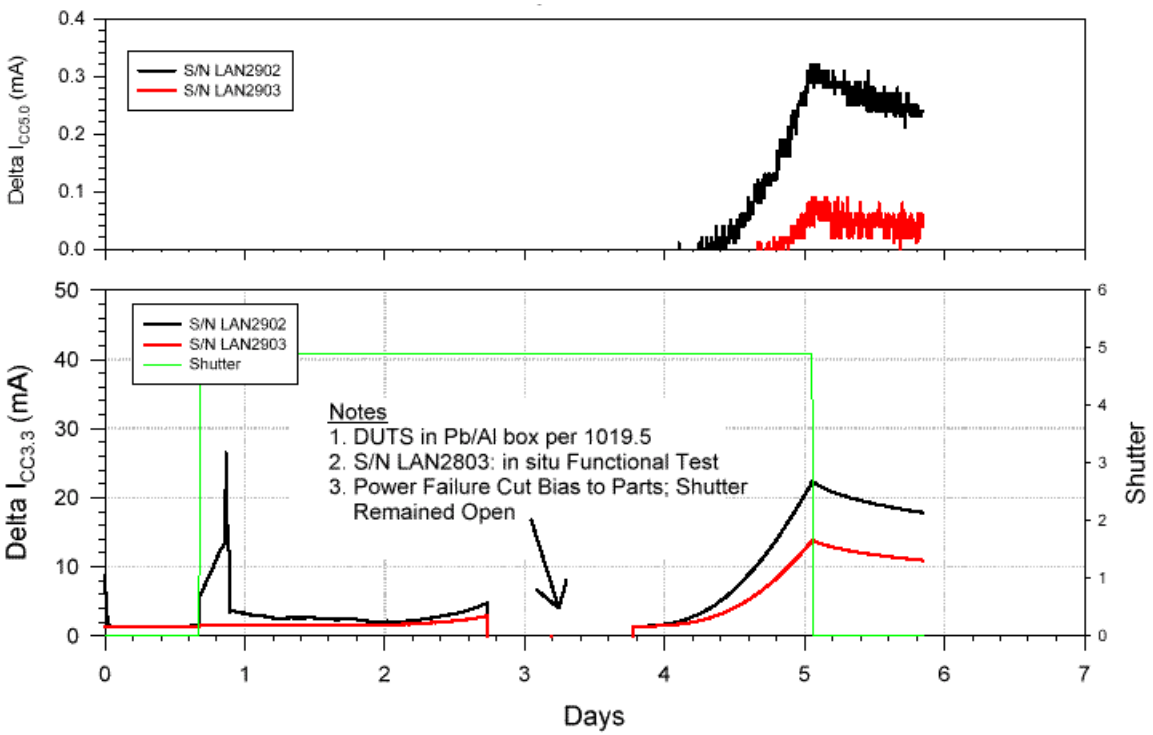

Figure 2b. Delta IDDstandby versus total dose, LAN2902, LAN2903.

As shown in Figure 2, DUT serialized LAN2901, LAN2902, and LAN2903 was irradiated to 80krad(Si). Every DUT has $I_{Ddstandby}$ below 25mA (the spec) after irradiation. In Figure 2b when LAN2902 and LAN2903 were irradiated, DUT bias was interrupted due to power failure. However, the total biased irradiation dose is no less than 80krad(Si). Since the non-biased irradiation should exert more radiation effects on the DUT, these results should be

worse than the case without interruption and continuous irradiation to 80krad(Si). The drop of current is due to stopping of the irradiation. All the DUT were biased annealed at room temperature for few days to reduce the static leakage and power up transient current.

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-room-temperature annealing. The irradiated-and-annealed DUT is within the spec and the change for each DUT is less than 10%.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results

	Pre-Irradiation	Post-Annealing
LAN2901	1.44V	1.40V
LAN2902	1.44V	1.37V
LAN2903	1.44V	1.36V

4) Output Characteristic

Figure 3a and 3b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUT. All irradiated-and-annealed DUT are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 4a and 4b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUT. All DUT passed the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.

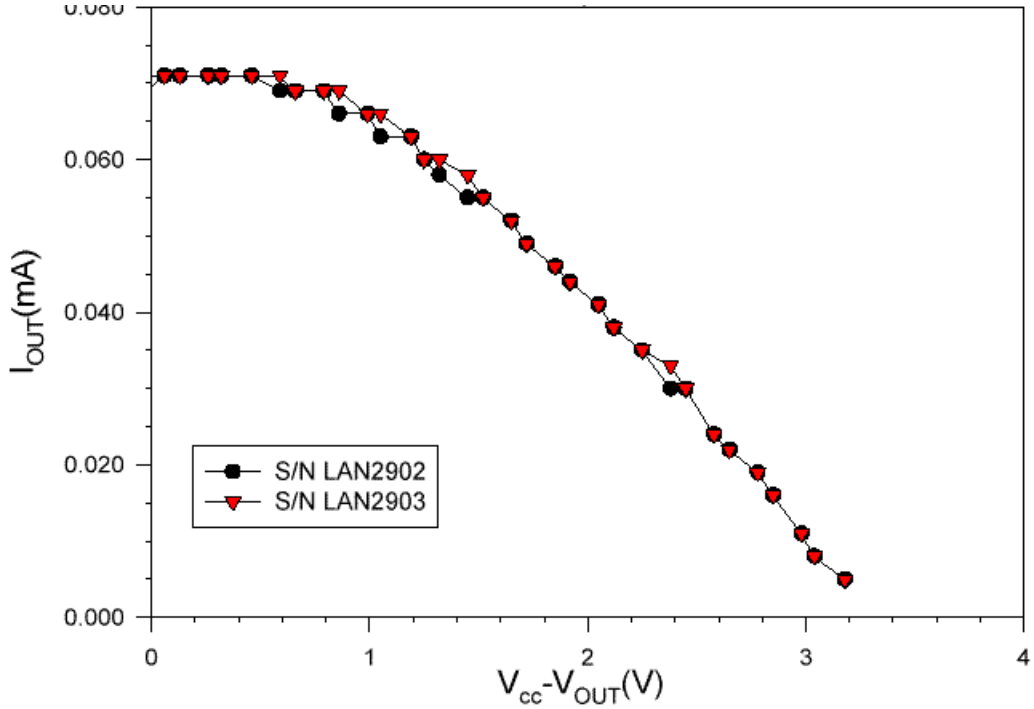

Figure 3a. Pre-irradiation V_{OL} characteristic curves.

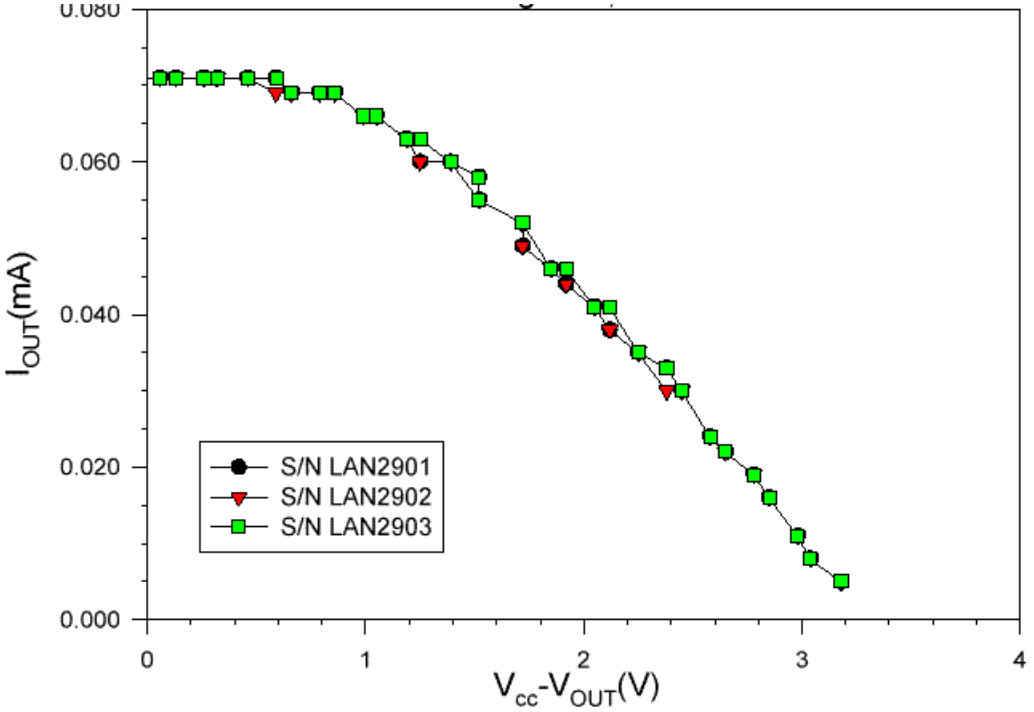

Figure 3b. Post-annealing V_{OL} characteristic curves.

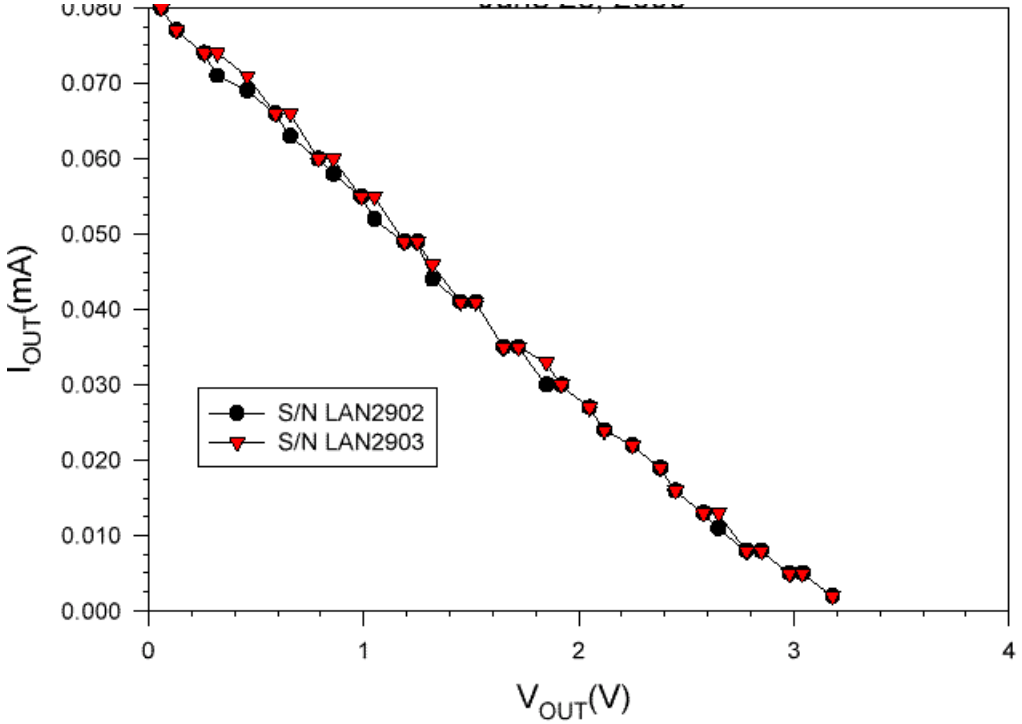

Figure 4a. Pre-irradiation V_{OH} characteristic curves.

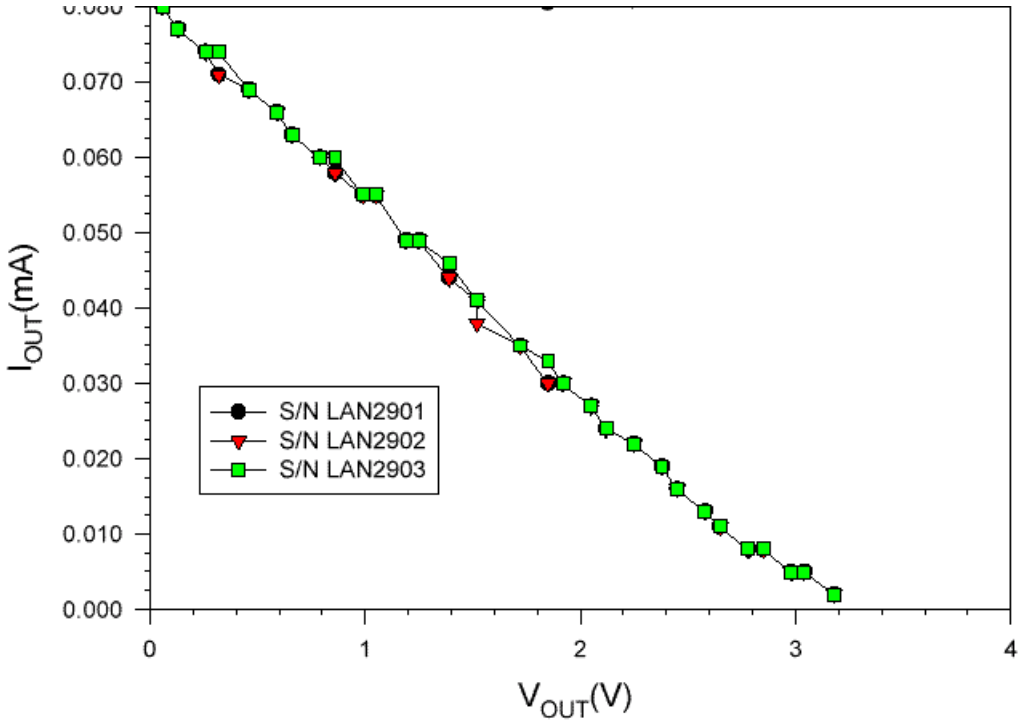

Figure 4b. Post-annealing V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is always within 10%.

Table 6. Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN2901	653	675	643	663
LAN2902	663	671	653	662
LAN2903	650	659	640	666

Table 7. Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN2901	51.4	53.1	50.3	52.9
LAN2902	50.7	52.9	50.1	52.1
LAN2903	51.3	53.0	50.4	52.5

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN2901	50.4	52.9	50.8	53.4
LAN2902	50.8	53.1	51.2	53.4
LAN2903	50.1	52.6	50.9	52.8

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 6-9 show the rising edge transient. Figures 10-13 show the falling edge transient. The radiation effect is basically negligible.

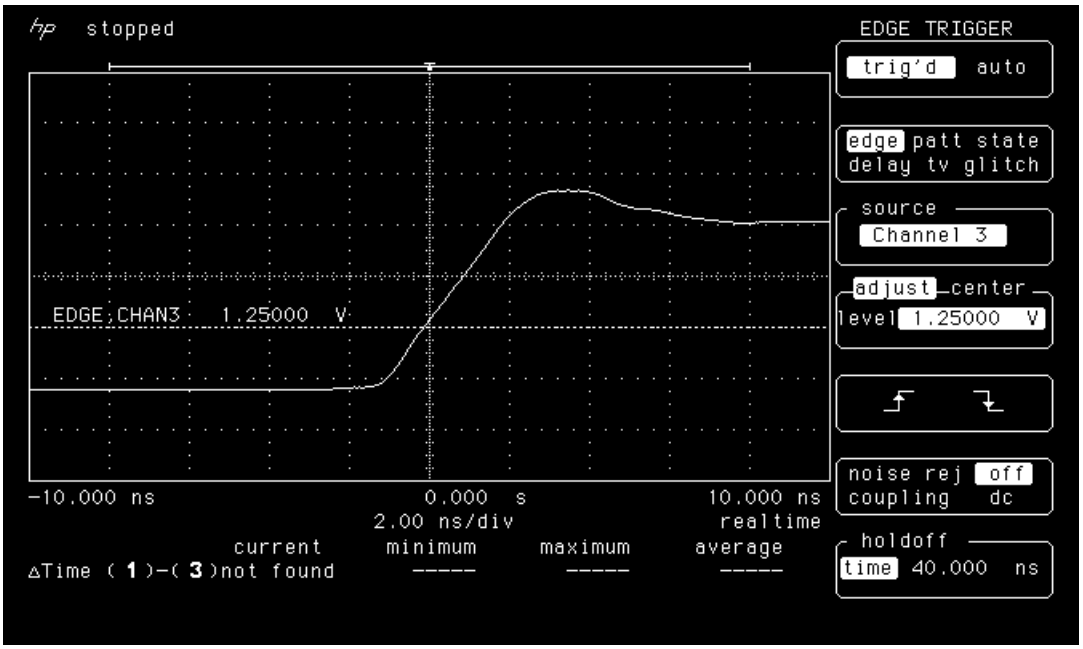

Figure 5a. Rising edge of LAN2901 pre-irradiation.

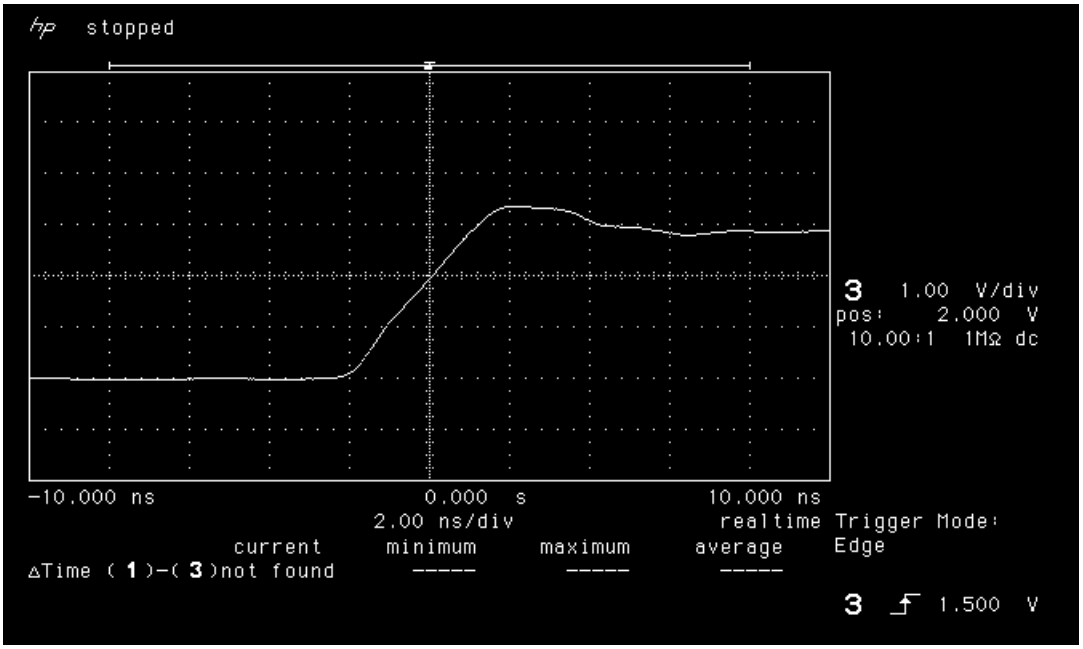

Figure 5b. Rising edge of LAN2901 post-annealing.

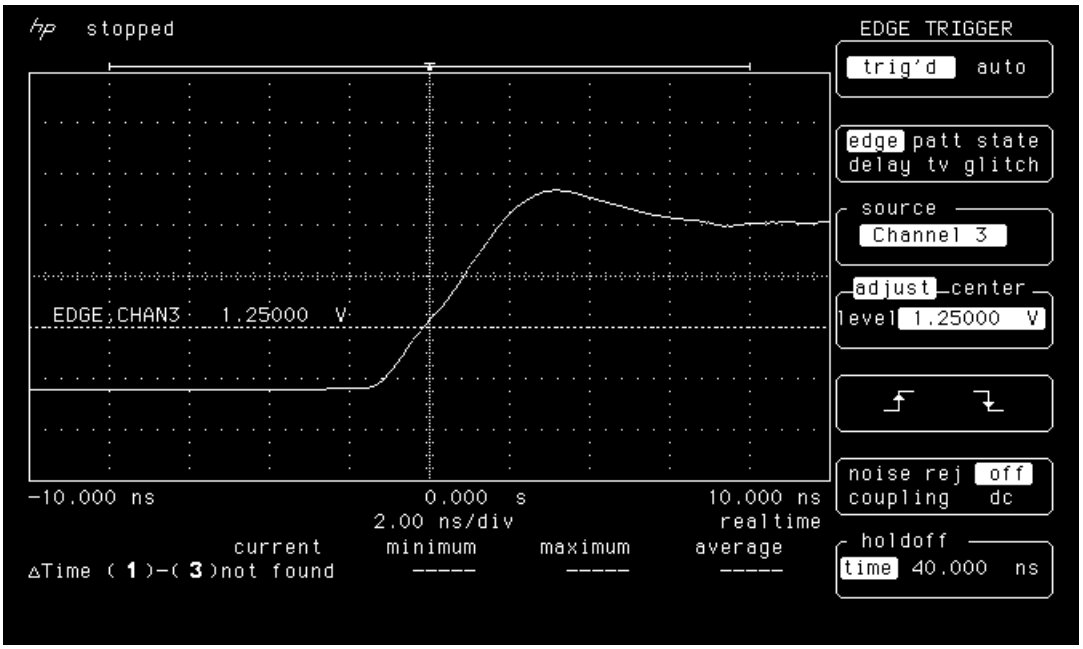

Figure 6a. Rising edge of LAN2902 pre-irradiation.

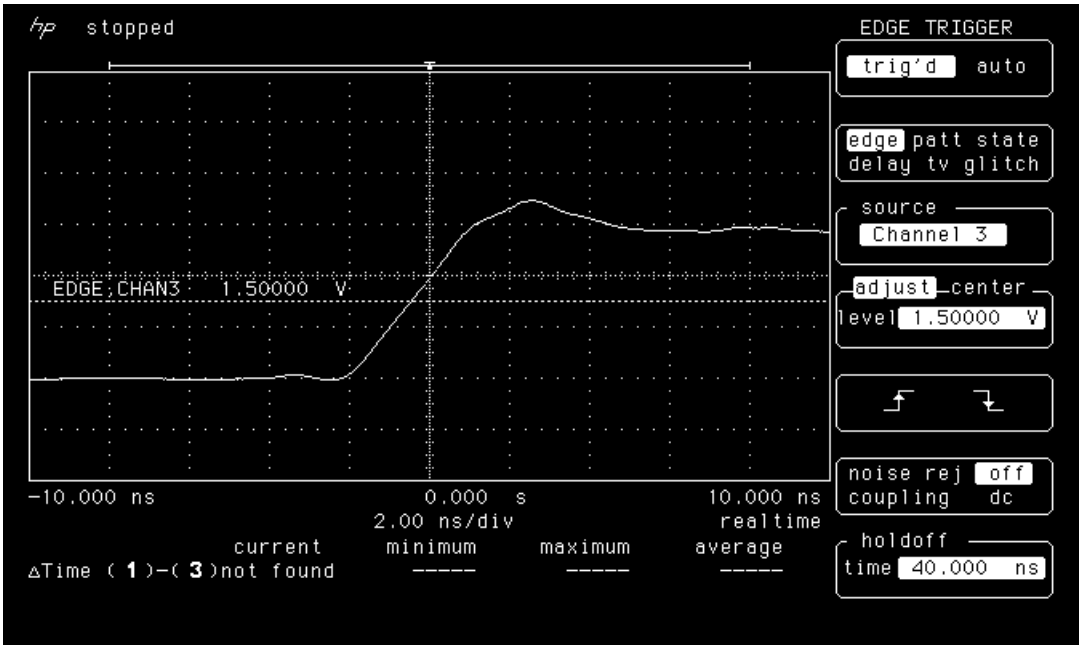

Figure 6b. Rising edge of LAN2902 post-annealing.

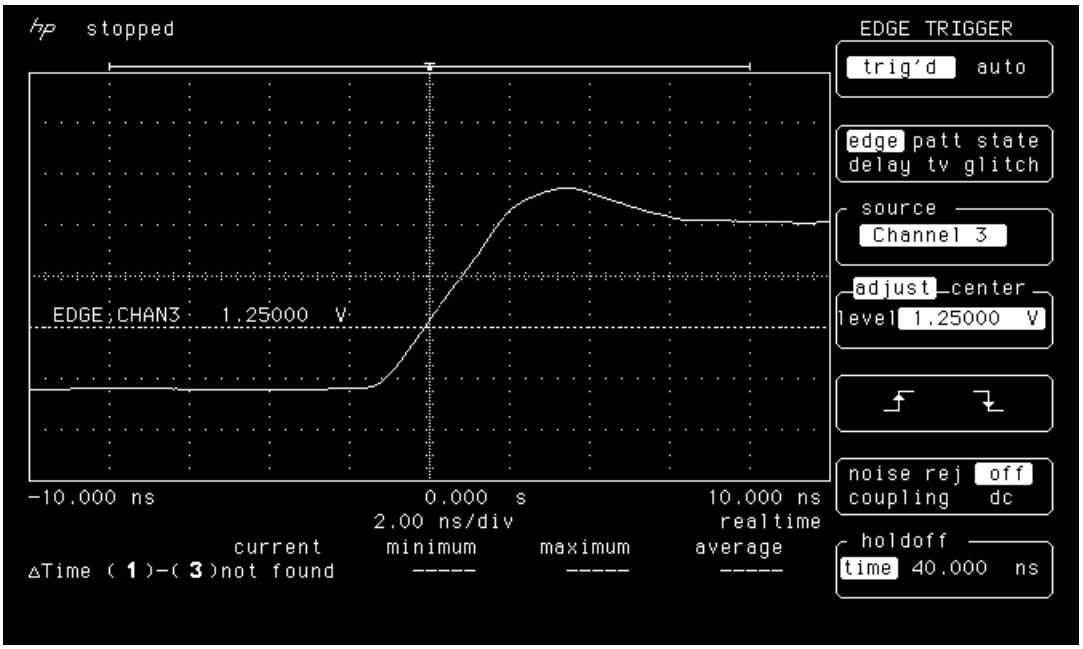

Figure 7a. Rising edge of LAN2903 pre-irradiation.

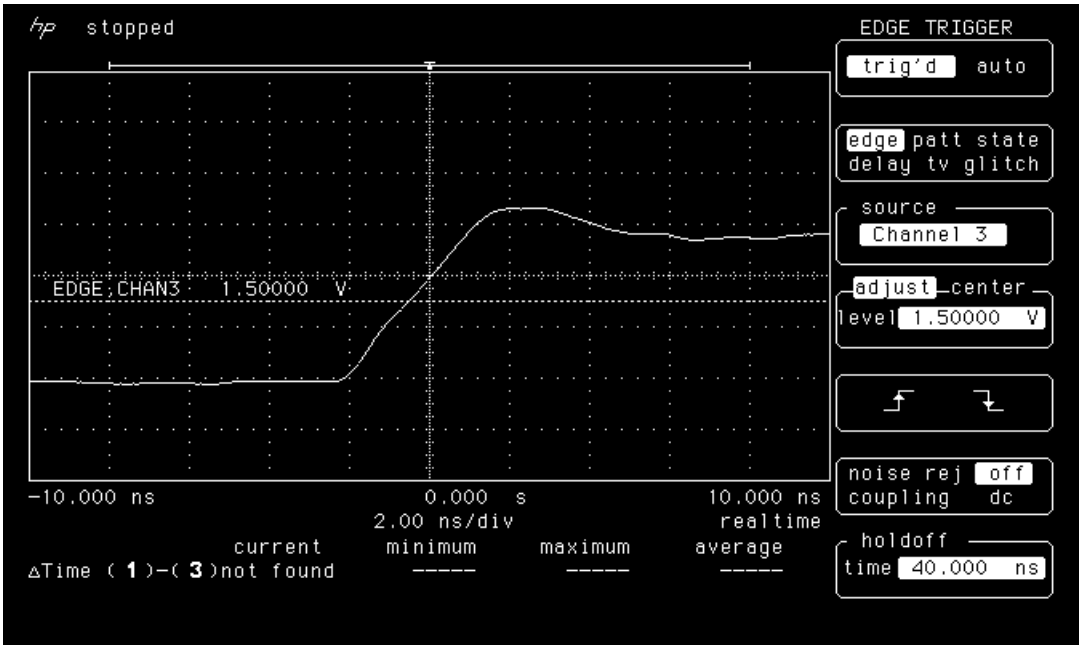

Figure 7b. Rising edge of LAN2903 post-annealing.

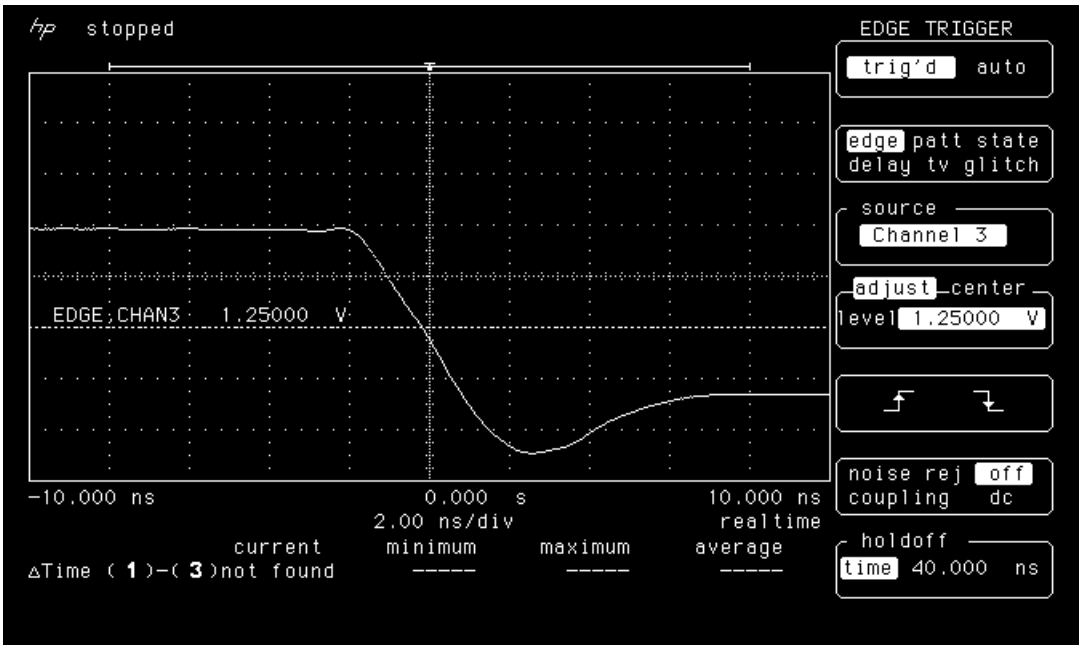

Figure 8a. Falling edge of LAN2901 pre-irradiation

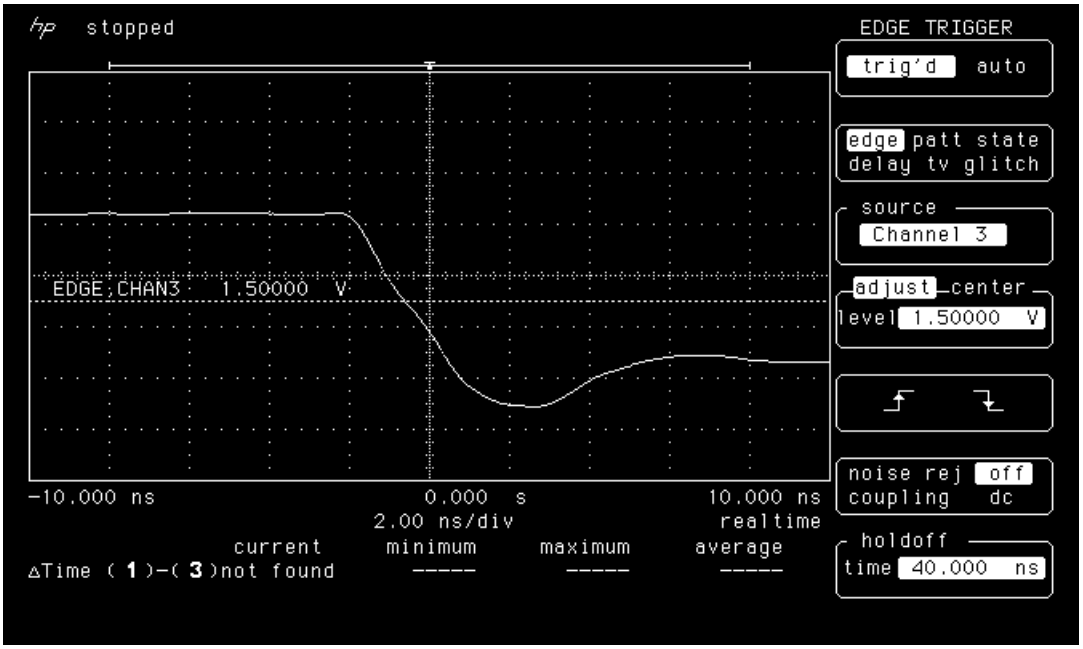

Figure 8b. Falling edge of LAN2901 post-anneal.

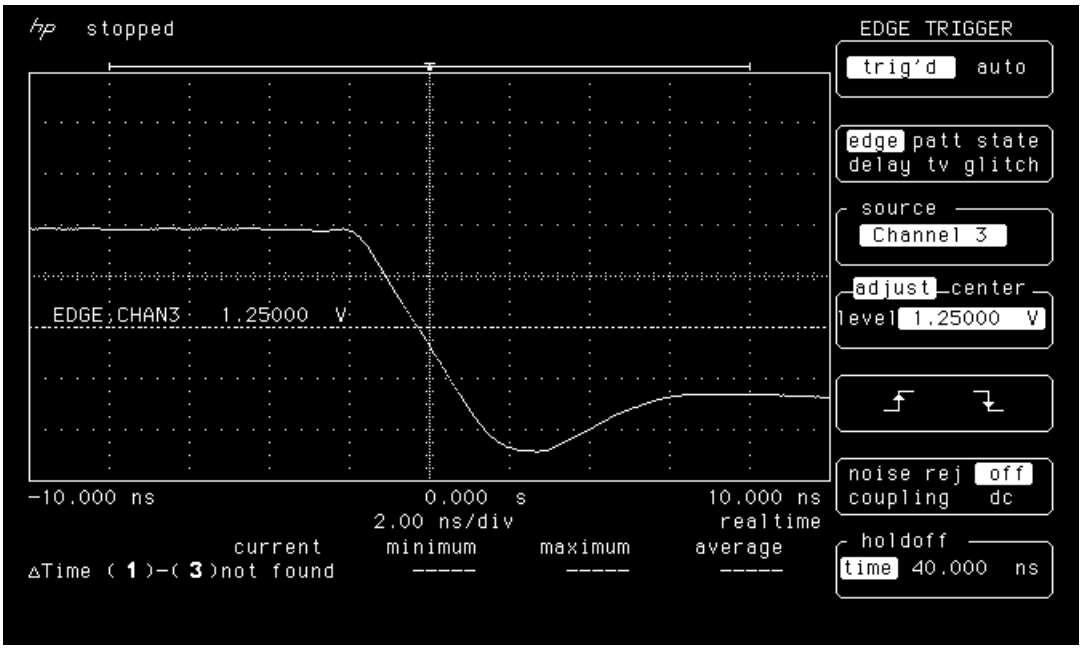

Figure 9a. Falling edge of LAN2902 pre-irradiation.

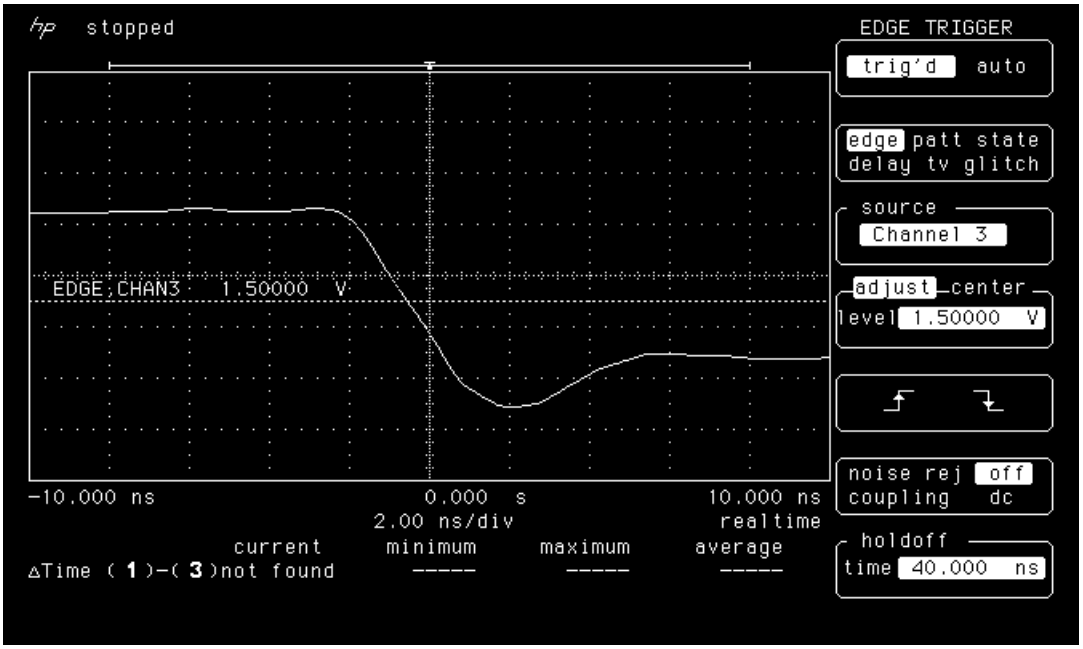

Figure 9b. Falling edge of LAN2902 post-annealing.

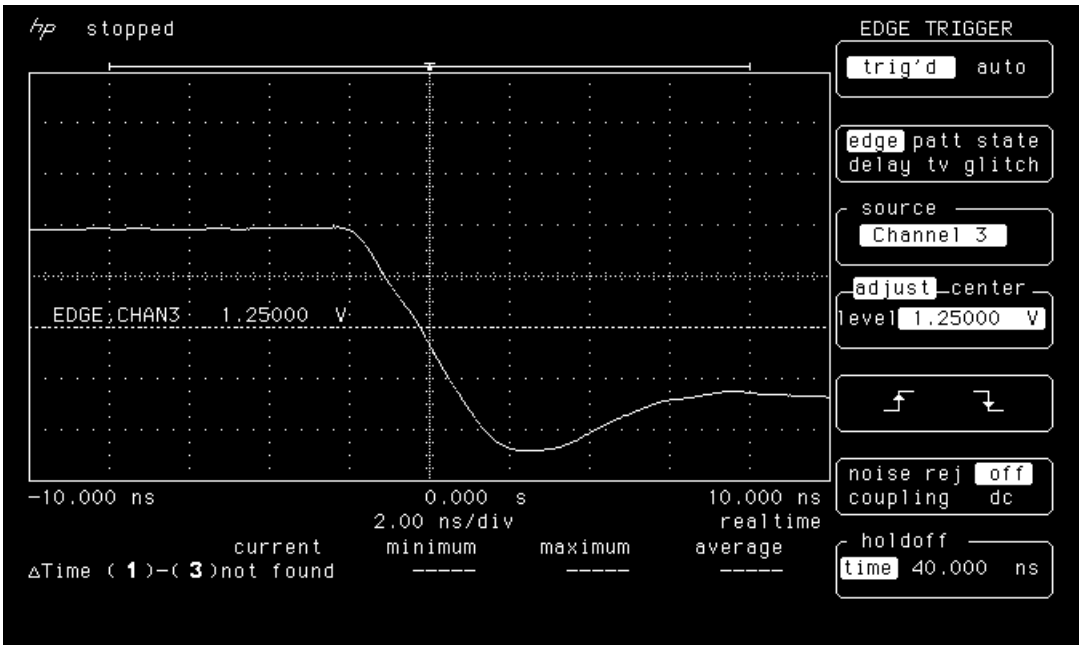

Figure 10a. Falling edge of LAN2903 pre-irradiation.

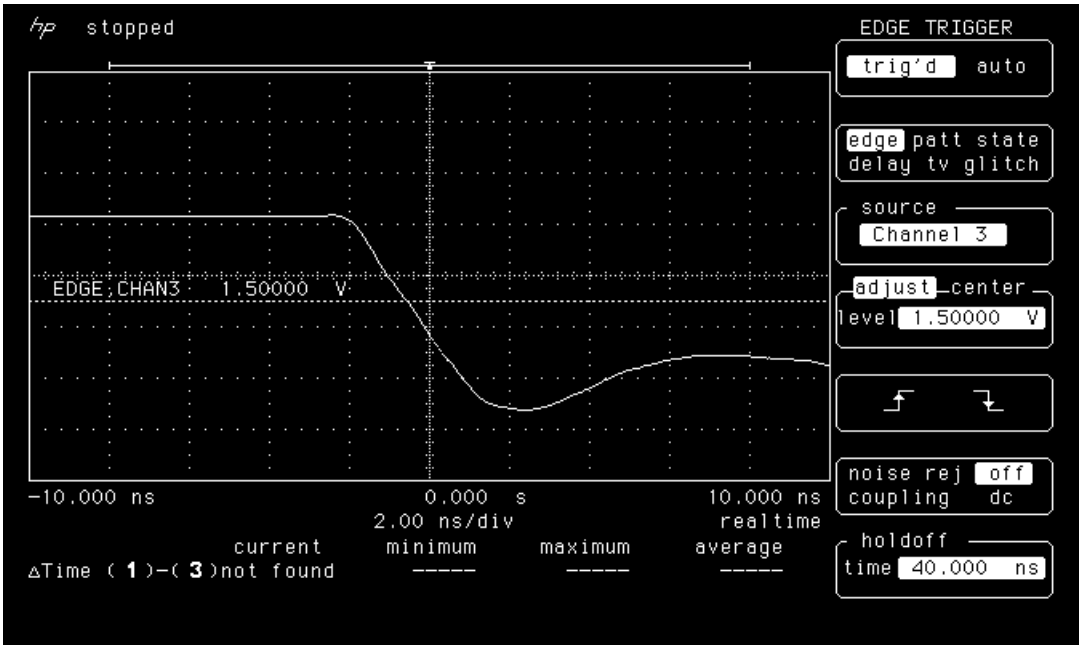

Figure 10b. Falling edge of LAN2903 post-annealing.

7) Power-Up Transient

In each measurement, the rising time of the power supply voltage (V_{CC}) was set at 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 11-13 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 3.3V, and another curve showing I_{CC}. The scale is 1V per division for V_{CC} and 100mA per division for I_{CC}. These pictures show that 80krad(Si) of irradiation basically has no impact on the power up.

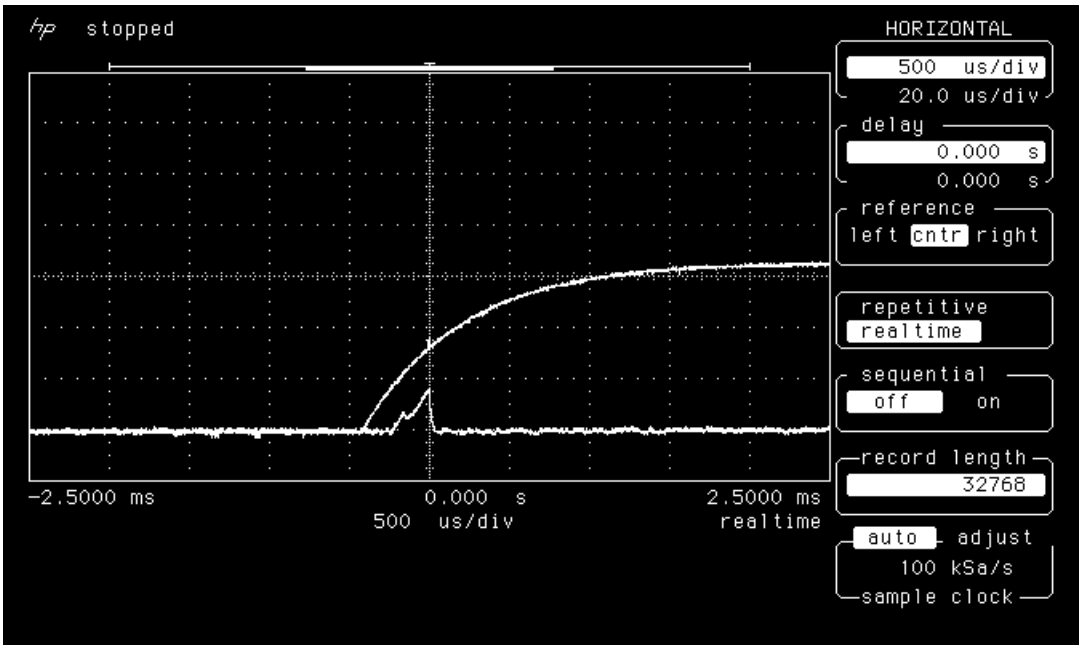

Figure 11a. Power-up transient of LAN2901 pre-irradiation.

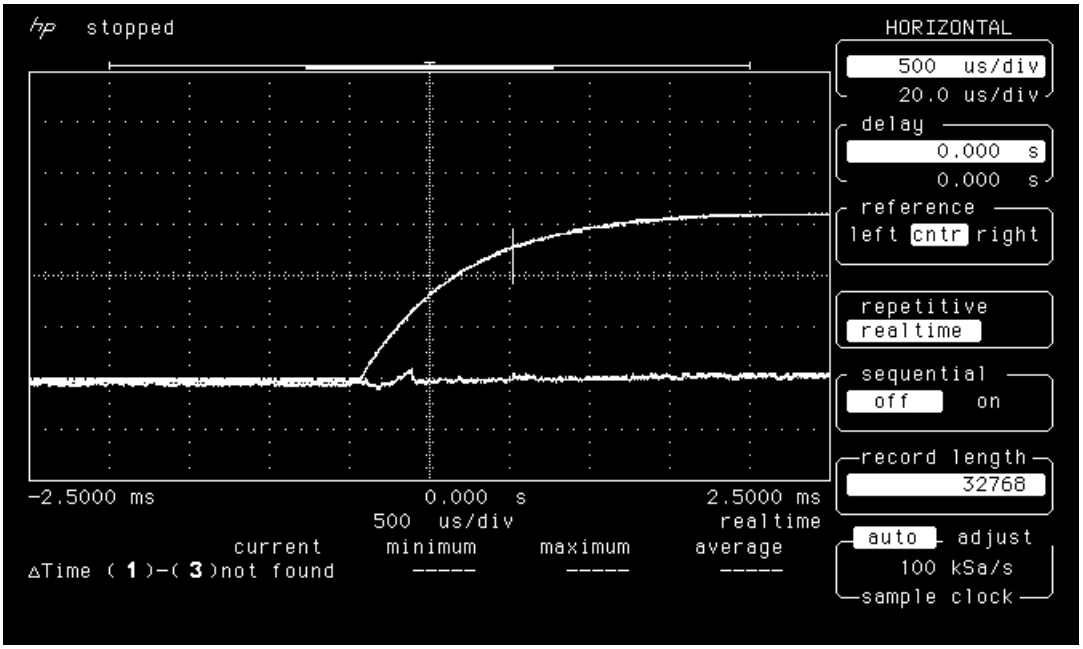

Figure 11b. Power-up transient of LAN2901 post-annealing.

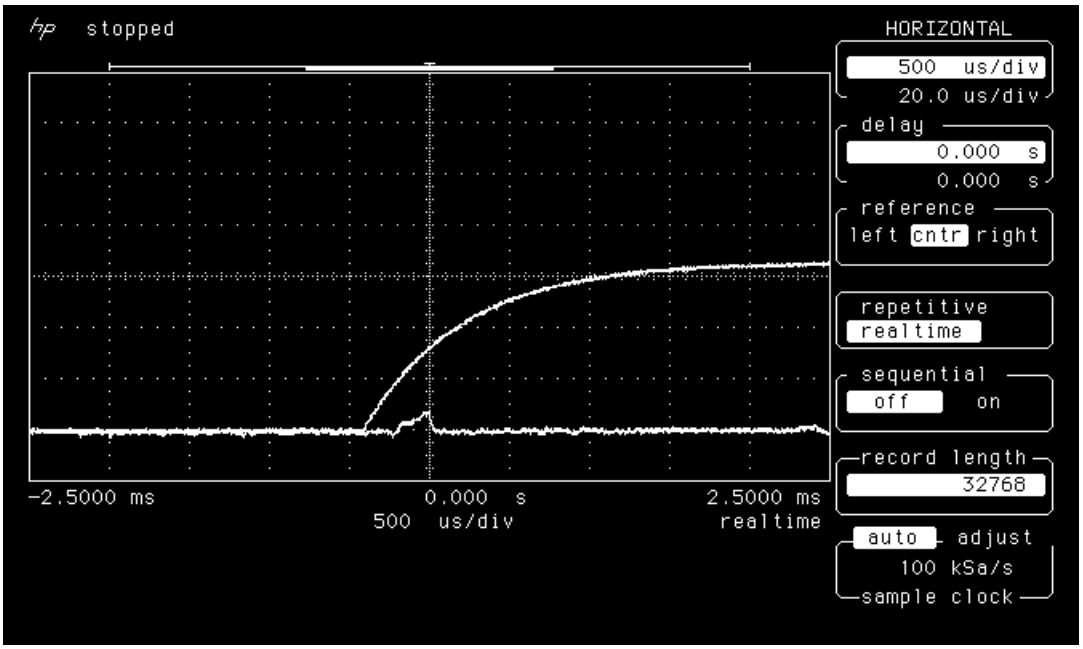

Figure 12a. Power-up transient of LAN2902 pre-irradiation.

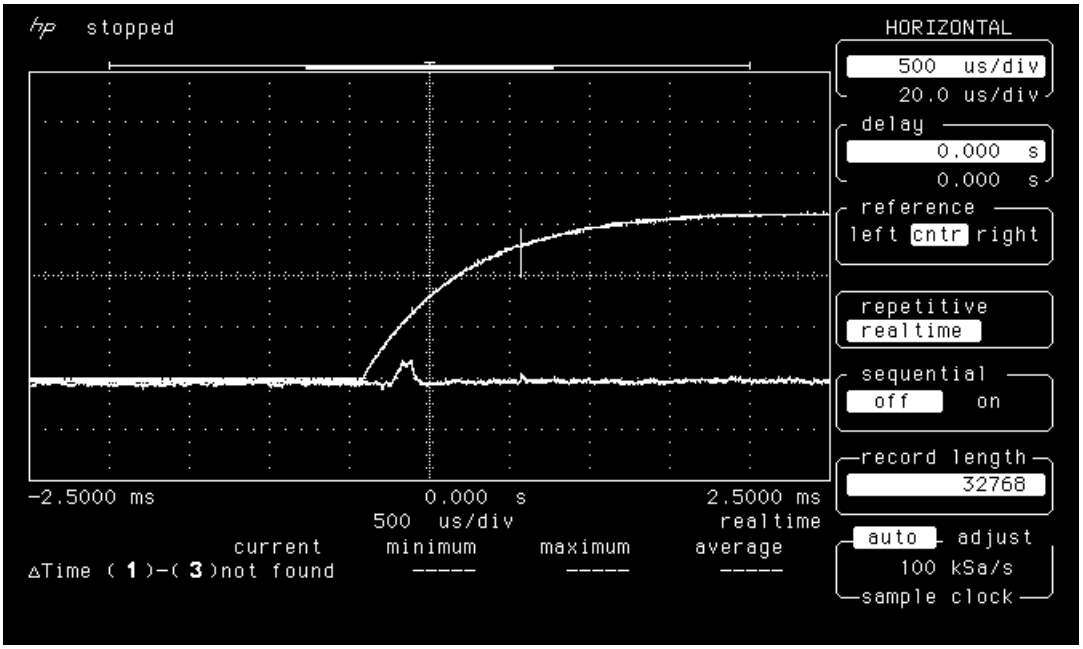

Figure 12b. Power-up transient of LAN2902 post-annealing.

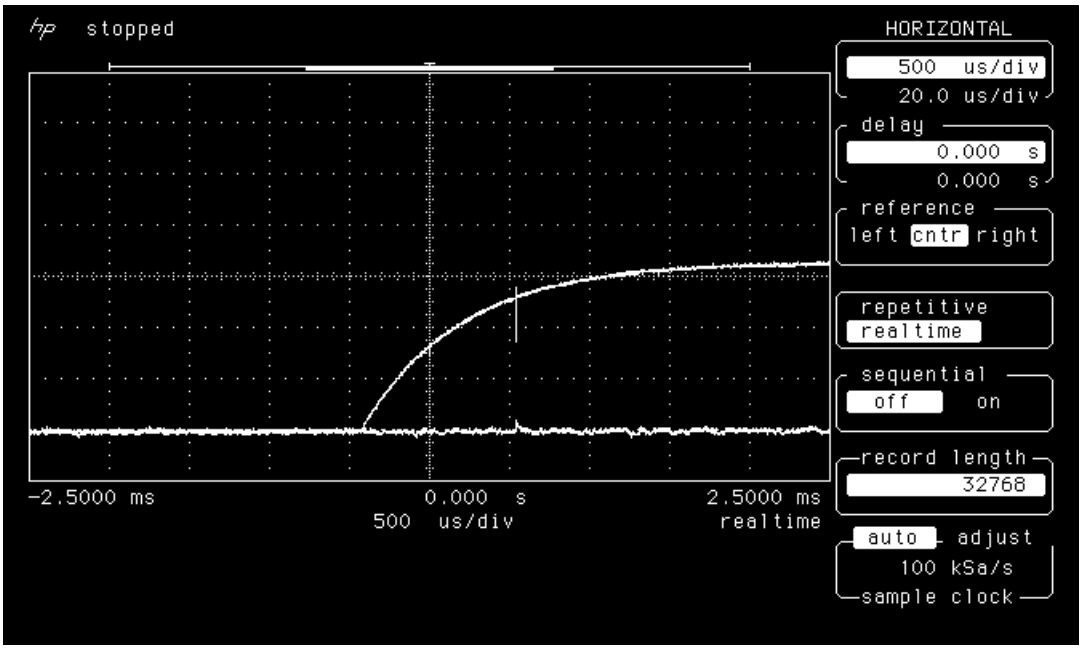

Figure 13a. Power-up transient of LAN2903 pre-irradiation.

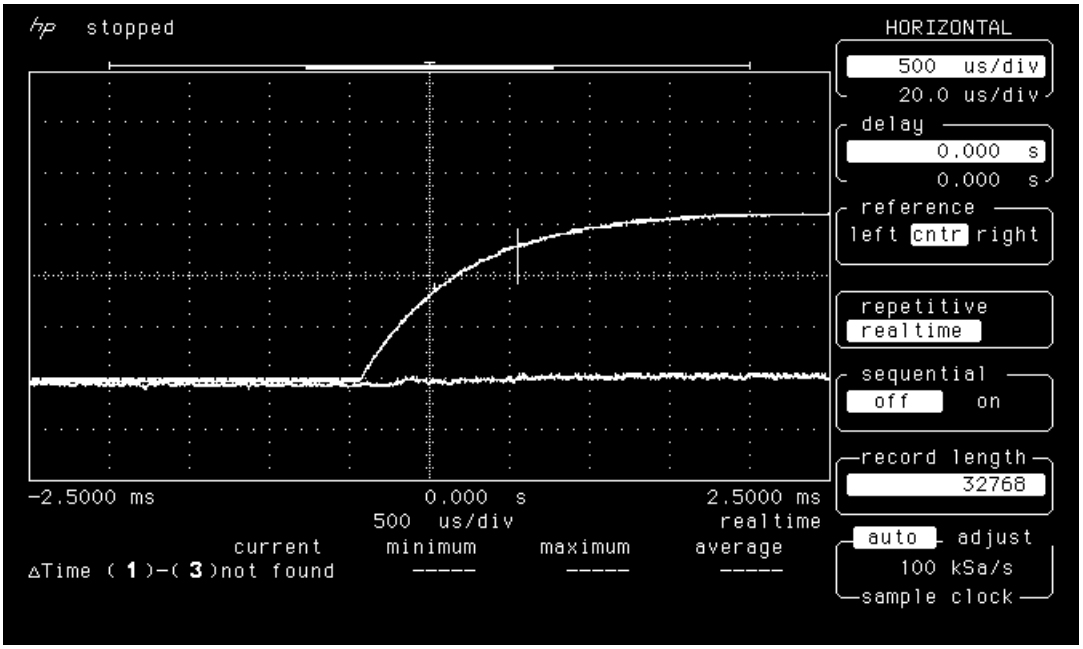

Figure 13b. Power-up transient of LAN2903 post-annealing.