POST PROGRAMMING BURN IN (PPBI) FOR RT54SX-S AND A54SX-A ACTEL FPGAS

By

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ABSTRACT

Burn-in (BI) for programmed FPGAs (Field Programmable Gate Array) is a growing concern in the space community. This paper addresses these concerns in regard to the RT54SX-S and A54SX-A Actel FPGAs in the un-programmed versus programmed mode. Discussion in this paper will include architecture and testing methodologies of devices in an un-programmed state. Pre and Post BI methodologies for un-programmed units will be covered for Dynamic and Static BI conditions. This will be compared to the programmed conditions for Dynamic BI. Actel's internal Quality Control (QC) design will be analyzed and Ongoing- Reliability-Testing (ORT) results will be discussed in detail.

All this data in summary will demonstrate that Post Programming Burn In (PPBI) for Actel RT54SX-S and A54SX-A products is not required nor recommended.

Introduction

The RT54SX-S and A54SX-A devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility in Japan. It's a 3 layer metal process for the RTSX32S and A54SX32A versus 4 metal layers for the RT54SX72S and A54SX72A devices. The architecture of the RT54SX-S devices is an enhanced version of Actel's A54SX-A device. The RTSX-S devices offer levels of radiation survivability far in excess of typical CMOS devices.

The main difference between the RTSX-S and A54SX-A is in the design of the R-cell. Triple Module Redundancy (TMR) is a well-known technique for SEU mitigation. Instead of a single FF, TMR uses three FFs hardwired to a majority gate voting circuit. If one FF is flipped to the wrong state, the other two override it and the correct value is propagated to the rest of the circuit. The RT54SX-S family has a self-refreshing TMR built into every register thereby eliminating the need to TMR every FF using software techniques. The A54SX-A family does not have this built in TMR feature. Though there are distinct differences between the two product families, they share the identical antifuse design, composition, structure and process. For the purpose of this paper we will make use of data from both families to explain why PPBI is not required.

Architecture

The RT54SX-S Datasheet and Hi-Rel A54SX-A Datasheet describe in detail the architecture for the two M2M (Metal-2-Metal) families. The main differences between the two families are listed in Table 1 below.

Feature	RT54SX-S	A54SX-A
Technology	0.25	0.25
Built In TMR	Yes	No
Radiation Survivability	Yes	No
TRST Pin	Dedicated	User Defined
5VCMOS I/O	Yes	No
PCI, TTL	Yes	Yes
Charge pump enhancement	Yes	No
Military Flows	B, E	B
SEL Immune	Yes	No

Table 1: Difference between RT54SX-S and A54SX-A

Antifuse devices have isolation transistors to keep high programming voltages out of the logic circuits. During normal operation a charge pump drives these gates high to pass a logic signal. The devices put all modules in a predetermined state until the charge pump has reached operating voltage and then all modules will immediately switch to the user state. The outputs are tri-stated until the correct state is reached and then enabled. Slew rate control is available on the general purpose I/Os to minimize switching noise. The JTAG TRST pin, which should always be grounded in space, is a dedicated input pin for the RT54SX-S devices and user selectable for the A54SX-A devices.

The unique architecture of the FPGA allows for testability of the device in an un-programmed state via the JTAG interface. All routing tracks can be addressed and driven to a "0" or "1" state. The state of any track can be sampled and read back. The output of any logic module can be observed using the patented Actel Action Probe circuitry.

Test Modes of Actel FPGAs

Several of the tests that ensure 100% test coverage are outlined below:

1. A shift register circles the periphery of the chip which can be loaded and read back during testing. A pattern of all 0, all 1 and alternating 0 and 1 is loaded and read back. The various shift register patterns are used to ensure that different portions of the internal circuits are fully functional. BSR (Boundary Scan Register) is included in testing since it is used in several different patterns for testing.
2. All vertical and horizontal tracks are tested for continuity and shorts.
3. All horizontal and vertical pass transistors are tested for leakage and functionality.
4. The clock buffers, modules and drivers are fully tested by driving with the clock pins and reading the proper levels.
5. There exist two special pins noted as Probe A and Probe B (Actel Action Probes), which by use of the shift register, can address the output of every logic module inside the array to ensure functionality. Every logic module in the blank FPGA is fully tested.
6. Through Probe A and Probe B, numerous other functional tests are allowed on a blank FPGA such as verification of the routed clock modules.
7. The JTAG BSR can drive all output buffers to low, high or tri-state for testing. Thus Vol, Voh, Iol, Ioh and output leakage tests are performed. The limits for all output modes are tested.
8. All input modes like PCI, TTL and CMOS are configured and tested for Vih, Vil and input leakage.
9. There exists **a dedicated column** on the FPGA which is transparent to the customer and allows Actel to program antifuses connecting inputs and outputs of modules into what is known as the

"binning circuit". The programming is performed at conditions identical to those utilized by the programmer (Silicon Sculptor) while programming a customer design. This allows Actel to ensure functionality of the programming circuitry, programmed antifuses and guarantees speed performance of the FPGA.

10. The device has special circuitry and high voltage devices to isolate low voltage logic from the elevated voltages during programming. There are specific tests to verify the functionality of this circuitry.
11. There are tests to ensure that all antifuses are un-programmed and to ensure reliability and quality of the antifuse in the FPGA. These proven electrical screens are performed prior to and after the tests that exercise the programming conditions of the FPGA.
12. Standby current measurement testing is done for Vpp, Vcci, Vcca, Vks and Vsv.
13. Every unit in the wafer lot is 100% tested with the above mentioned tests. Each test is completed at the following temperatures: **125°C, –55°C and Room temperature.**
14. Antifuse stress tests are done only at wafer sort and commercial test to screen out weak antifuses. After the stress tests, an antifuse shorts test is done to detect any failures.
15. All lots go through B or E-flow per the MIL-STD-883E. One of the major differences is that B flow units go through Dynamic Blank Burn-in only whereas E-flow units go through both Dynamic and Static Burn-ins. All tests mentioned above are performed (except antifuse stress tests) at Military temperatures both pre and post burn-ins. Table 2 shows the two flows:

Actel MIL-STD-883 Class E Product Flow	Actel MIL-STD-883 Class B Product Flow
Destructive In-Line Bond Pull3	NA
Internal Visual	Internal Visual
Serialization	NA
Temperature Cycling	Temperature Cycling
Constant Acceleration	Constant Acceleration
Particle Impact Noise Detection	Particle Impact Noise Detection
Radiographic	NA
Seal	Seal
a. Fine	a. Fine
b. Gross	b. Gross
Visual Inspection	Visual Inspection
Pre-Burn-In Electrical Parameters	Pre-Burn-In Electrical Parameters
Dynamic Burn-In	Dynamic Burn-In
Interim (Post-Burn-In) Electrical Parameters	Interim (Post-Burn-In) Electrical Parameters
Static Burn-In	NA
Interim (Post-Burn-In) Electrical Parameters	NA
Percent Defective Allowable (PDA)	Percent Defective Allowable (PDA)
Final Electrical Test	Final Electrical Test
Static Tests : 25°C, –55°C and +125°C	Static Tests : 25°C, –55°C and +125°C
Functional Tests : 25°C, –55°C and +125°C	Functional Tests : 25°C, –55°C and +125°C
Switching Tests at 25°C	Switching Tests at 25°C
External Visual	External Visual

Table 2: Actel Mil-STD-883 Flows

Burn-In of Actel FPGAs

The un-programmed antifuse infant mortality failures are sufficiently screened out during blank device electrical testing; therefore, it is unnecessary to do a burn-in to screen out failures of this type in standard commercial production units. Voltage stress testing of semiconductor devices is a much more effective screen than a temperature burn-in (**Reference from JM**). Additionally defect densities have significantly dropped as semiconductor technology has matured as shown in Figure 1 below.

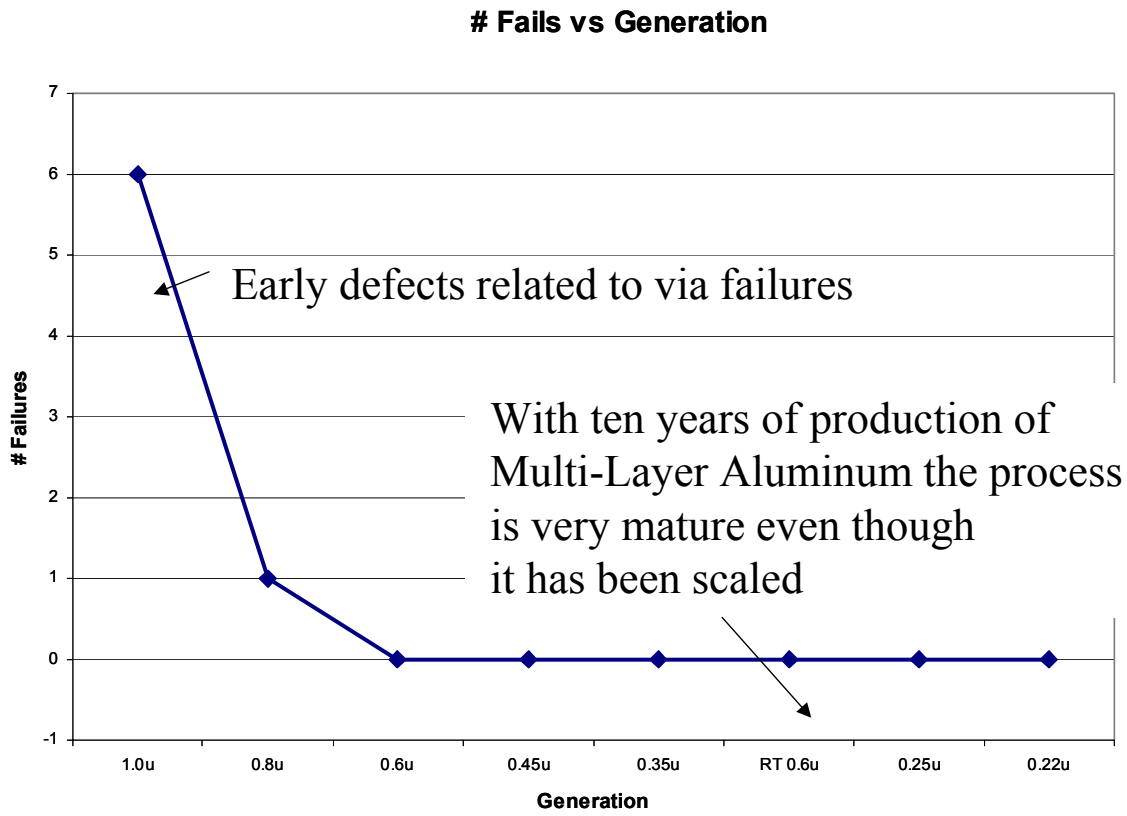

Figure 1 : Failure Rate Versus Technology generations

During blank device electrical testing, Actel devices are subjected to controlled voltage stress conditions significantly higher than the maximum operating conditions specified in the data sheet. Because of the lower defect densities and the voltage screening that Actel performs, infant mortality failures have not been an issue. The fallout seen during the burn-in test phases have been due to handling and improper burn-in conditions, not defects.

However, burn-in is required for all military 883E products. MIL-883E Method 1005, allows several types of burn-in screens, which can be divided into two categories: dynamic and steady-state (static). Dynamic burn-in applies AC signals to device inputs. These signals are selected so that the device receives internal and external stresses similar to those it would experience in a typical application. A properly designed dynamic burn-in can effectively stress inputs, outputs, and internal circuits. Dynamic burn-in of ASICs can get very expensive because each unique ASIC design will require a customer-specific burn-in pattern and burn-in boards must be designed and built to properly stress the device. This results in large NRE costs and long lead times. A programmed FPGA is exactly the same as a mask-programmed ASIC from the standpoint of burn-in. Both require custom burn-in circuits to do the dynamic burn-in. However, Actel takes advantage of the testability features of its FPGA products to provide effective dynamic burn-in of un-programmed devices. This blank dynamic burn-in enables the FPGA circuits to be stressed in a way that a programmed dynamic burn-in is incapable of duplicating.

Dynamic Blank Burn-In (DBBI)

Actel performs DBBI for three main reasons:

- Stress the un-programmed antifuses
- Stress inputs, outputs and internal circuits
- Stress I/Os

During a DBBI stress test, the blank FPGA units are inserted onto a Burn-in Board (BIB) and the IEEE 1149.1 JTAG device pins are driven from an EPROM on the burn-in system driver board. The HCLK, CLKA, CLKB, QCLKA-D(on A54SX72A and RT54SX72S devices) inputs are driven with a 500KHz 50% duty cycle clock driver. During the blank device electrical test program which stresses the un-programmed antifuses the Vpp pin is biased at 4.5V for the Actel SX-S and SX-A devices. However, due to the accelerated temperature stress on the device during the Dynamic Blank Burn-in, the Vpp is reduced to 4.1V. The supply pins for the A54SX-A and RT54SX-S products during the DBBI are as follows:

- Vcci = 5.5V ± 0.25V
- Vcca= 2.75V ± 0.25V
- Vsv = Vpp = 4.10V ± 0.25V

The EPROM provides stimulus to exercise the device through the following sequence.

1. Load the Actel internal Long Scan Register via JTAG extension command to drive all vertical tracks in the device to '0' and all horizontal tracks to '1'.
2. Load the Actel internal Mode Register with settings appropriate to setup the cross antifuse stress condition.
3. Load the Mode Register to enable antifuse stress.
4. Load the I/O pattern for bonded out pins via the Boundary Scan Register (BSR)
    a. Each pin is configured using the BSR to be in one of the following three states:
        i. tri-stated 'Z'
        ii. driving '0'
        iii. driving '1'
    b. To minimize the simultaneous switching outputs during the burn-in, the BSR pattern loaded at step 4 will be done such that only one pin in each group of four pins switches between the driving '1' and '0' state on any given TCK cycle. Non-switching pins are left in the 'Z' state. An example of the pattern can be seen in Table 3:

Cycle	Pin 1	2	3	4
0	**1**	Z	Z	**Z**
1	**0**	Z	Z	Z
2	**Z**	**1**	Z	Z
3	Z	**0**	Z	Z
4	Z	**Z**	**1**	Z
5	Z	Z	**0**	Z
6	Z	Z	**Z**	**1**
7	Z	Z	Z	**0**

Table 3: Pattern used during DBBI

5. Switch the antifuse stress direction by reversing the drive state on vertical and horizontal tracks. This will also cause all input and output tracks of the logic modules to toggle, stressing the internal devices of every logic module.
6. Toggle the I/O pins using the BSR
7. Return to Step 3.

Unlike a typical programmed design where only a percentage of logic modules and antifuses are stressed, in the blank dynamic burn-in 100 percent of all logic modules, routing tracks and antifuses are stressed. Additionally, switching noise is reduced by toggling 25% of the I/Os at any time.

Static Blank Burn-In (SBBI)

Actel products processed to the E-flow are screened with a static burn-in of the blank device. The DBBI process step is followed by a static blank burn-in. Static burn-in applies DC voltage levels to the pins of the device under test. The device will be powered up. Static burn-in is easier to implement. By choosing appropriate biasing conditions and load resistors, it is possible to design a single BIB for both un-programmed and programmed devices. With a properly designed BIB the pattern programmed into the device does not matter. Static burn-in can be an effective screen for mobile ionic contamination failure modes, which affect device inputs or outputs. Effective design of seal ring barriers and device passivation makes this type of contamination highly unlikely. Static burn-in is not very effective at stressing internal device circuits. Most internal nodes will be biased at ground without receiving any voltage or current stress. The supply pins for the A54SX-A and RT54SX-S products during the SBBI are as follows:

- Vcci = 5.5V ± 0.25V
- Vcca= 2.75V ± 0.25V
- Vsv = Vpp = 2.75V ± 0.25V

After burn-in, post read and record testing is performed as specified by MIL-STD-883E. The Percent Defect Allowed (PDA) is calculated for units subjected to both the DBBI and SBBI (E-Flow only) screening to ensure that the combined fallout is less than 5%.

Programming

It has been reported in literature[4] that an amorphous silicon based antifuse PROM requires a post programming temperature bake to cull out infant mortality of programmed antifuses which are subsequently reprogrammed. This is not the case with Actel amorphous silicon antifuse FPGAs. PROMS by their very nature have one transistor per switch element (antifuse) as shown in Figure 2. The antifuse is small and sits above the silicon, hence the die size is directly affected by the size of the programming transistor. Thus the designer is forced to use the minimum required size for the programming transistor in order to fit in a reasonable die size.

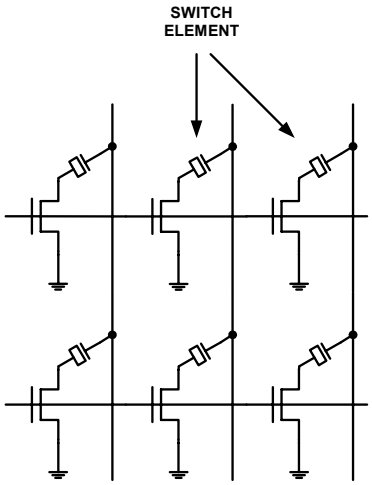

Figure 2: PROM Schematic

This means that the programming currents will be limited to only a few milliamps. The sense currents in such a device can be made small enough (assuming speed is not an issue) so as not to affect the antifuse

during read. Such a small link, however, is very susceptible to the mechanical stress placed on the link by temperature variations. Hence an antifuse programmed at low currents can open up during a bake or temperature cycle stress.

Actel FPGAs require one programming transistor per metal track, which can have as many as 1000 antifuses, as shown in **Figure 3** . Also, due to the high speed nature of these metal tracks, the interconnecting antifuses must have low resistance (typically 20 to 100 ohms) requiring the programming currents to be much higher than in a PROM. This makes the programmed metal filament much larger and stronger, such that high temperature bakes and cycle stress have no effect on the integrity of the antifuse.

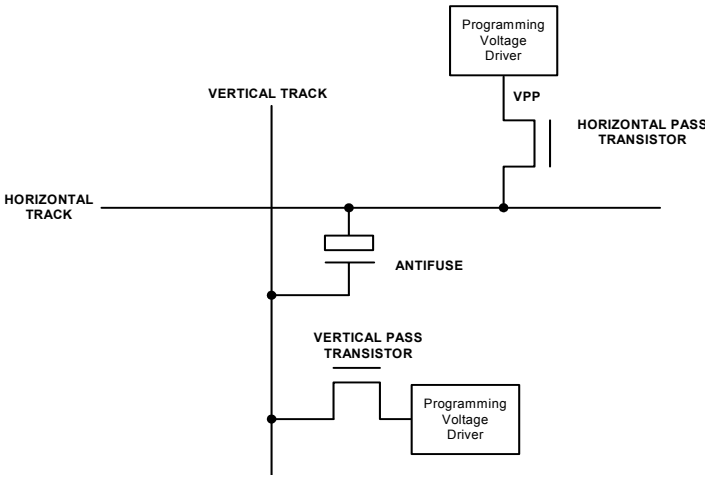

Figure 3: Schematic of Actel FPGA

As mentioned in section 2, all transistor, metal lines and antifuses have been tested except for the programmed state of the antifuse, which obviously needs to be done at programming. The programming algorithm runs serially and identifies the antifuse to be programmed per the customer generated "AFM (Actel Fuse Map)" file which uniquely identifies each antifuse that needs to be programmed per the design.

Programming and Testing

In this step the antifuse to be programmed is addressed and pulses are applied until current is sensed. Additional checks are done at a lower voltage to ensure that the correct antifuse has been addressed and programmed. Soak is done after programming to ensure that a low resistance antifuse link has been established. Additional tests are done before the algorithm moves to the next antifuse.

Several checks are done by the programmer to verify that only the correct antifuses have been programmed, else it is identified as a programming failure. Numerous tests are done after each antifuse, each channel, and column to ensure the correct nets have been generated such that functionality of the part is guaranteed after programming is complete. Following is a list of some of these tests:

1. **Icc measurement**

   The programming algorithm performs a pre Icca measurement before the programming of the part begins. Icca is monitored before any programming begins. Once the programming of the part has completed, the algorithm now verifies the post Icca measurements. Comparisons are made to pre Icc measurements and if the delta exceeds the pre determined delta value it is deemed a programming failure.

   This measurement ensures that the electrical characteristics of the device have not changed after programming.

2. **Net Short Test:**

This test verifies that any un-programmed antifuses are indeed un-programmed after programming is complete to ensure that no sneak paths have been established.

3. **EOC (End of Channel**): Following the array antifuse programming several EOC tests are performed. The primary tests check for shorts on the input, output, horizontal and vertical tracks within the channels.

4. **EOP (End of programming):** Once the array antifuse programming, EOC, net short tests are done then EOP tests are performed. Some of these are listed here:
    - VCC to GND short
    - Output to Horizontal and Vertical routing tracks.
    - Output to Output Short between different columns
    - Output to Output Short in the same column
    - Clock tracks to VCC or GND
    - Clock to Clock
    - Other

These tests ensure that all nets are 100% tested for continuity and shorts. Samples of units are programmed to a Quality Control (QC) design from each wafer lot prior to shipment of blank units from that lot. All units are 100% tested for functionality and no failures are allowed prior to shipment. No functional failures have been reported to date for processed A54SX-A and RT54SX-S wafer lots.

Following the EOC and EOP, the silicon signature and the checksum antifuses are programmed which are unique to each design. Finally, the P-fuse is programmed which enables the charge pump and allows the device to function as intended.

DPPBI (Dynamic Post Programming Burn In)

Actel devices are tested with 100% fault coverage testing and screened via Dynamic Blank and Static Blank Burn-in. This section addresses customer concerns regarding post-programmed device reliability. This section will cover the testing methodology and reliability data that has been collected by Actel with programmed units. Based on this data it is Actel's position that customers should not perform their own DPPBI.

QUALIFICATION:

In the qualification process of the RTSX-S and A54SX-A product families, a sample of 77 units were programmed and subjected to the Group C testing per Mil-Std-883E TM1005 for each family.

1. HTOL (High Temperature Operating Life):

The purpose of HTOL is to check for CMOS related failures such as gate oxide breakdown and BVII type of issues. Group C testing is equivalent to HTOL. Serialized blank units to be used for the Group C testing are processed through the B-flow and then programmed to an internal Quality Control Monitor (QCM) design. This design has greater than 95% utilization of the logic modules. The design uses all of the available combinatorial macro cells in the Actel library. All of the available user I/Os are exercised. The design uses a scheme, which toggles 25% of the device I/Os per cycle. The design implements built in self-test (BIST) blocks that utilize techniques to manage power consumption, but at the same time maximize all the features in the product. All the low-skew clock resources in the device are used in the design to ensure the stress of these global networks.
All units are tested for functionality and DC parameters (tri-state leakage, continuity, shorts, standby currents). Pre and post burn-in measurements are performed to check for parametric shifts. Once all pre burn-in tests are completed, units are loaded onto the burn-in board with conditions as specified below. Units are tested post burn-in to check for functional failures or drifts.

Table 4 summarizes the qualification and HTOL data that was collected for the RT54SX-S and A54SX-A programmed units. All programmed unit burn-in testing is performed at 150°C.

MEC 0.25 um FPGA Reliability Summary								
High Temperature Operating Life (HTOL)								
				Test Hours/Failures				
PRODUCT	**PACKAGE**	**Test time**	**#UNITS**	**168**	**500**	**1000**	**2000**	**Unit Hrs**
A54SX32A	PQ208	500	50	**0**	**0**	**-**	**-**	25000
A54SX32A	PQ208	1000	80	**0**	**0**	**0**		80000
A54SX72A	PQ208	1000	28	**0**	**0**	**0**		28000
A54SX32A	PQ208	1000	88	**0**	**0**	**0**		88000
A54SX72A	PQ208	1000	88	**0**	**0**	**0**		88000
A54SX72A	PQ208	1000	77	**0**	**0**	**0**		77000
RT54SX32S	CQ208/256	1000**	76	**0**	**0**	**0**		76000
RT54SX72S	CQ208/256	1000**	77	**0**	**0**	**1* (see Note 1)**		77000
RT54SX32S	CQ208	2000	8	**0**	**0**	**0**	0	16000
A54SX72A	CQ208	1000**	77	**0**	**0**	**1*(see Note2)**		77000
TOTAL Units for MEC 0.25um FPGA =			**649**	**Total test time Hrs.**				**632000**
TOTAL Failures for MEC 0.25um FPGA =						**2**		

Table 4: Summary of HTOL for the 0.25um

Note 1: During the RT54SX-S qualification 1 of the 77 units failed with excess Icca. Failure analysis of this unit indicated the root cause of the failure to be EOS (Electrical Over Stress) on the Vcca power supply. A voltage spike on Vcca >5V caused a N-channel transistor to get damaged, thus resulting in high Icca. The cause for this electrical failure was traced to EOS in the burn-in system.

Note 2: Failure analysis in progress

** Device hours in test equivalent. Devices tested at 150°C for 184 hrs

2. LTOL (Low Temperature Operating Life):

Normally LTOL screens for hot electron effects. Actel runs programmed units through LTOL during qualification also to check for programmed antifuse integrity at low temperatures. The transistor drive currents increase by ~20% at –55ºC and antifuses are more sensitive to current stress than high temperature stress[2]. For the qualification, 45 programmed units were subjected to LTOL and no failures were observed. Table 5 summarizes all the LTOL data collected to date for the 0.25µm technology.

MEC 0.25 um FPGA Reliability Summary								
Low Temperature Operating Life (LTOL)								
				Test Hours/Failures				
PRODUCT	**PACKAGE**	**Test time**	**#UNITS**	**168**	**500**	**1000**	**2000**	**Unit Hrs**
54SX32A	PQ208	500	50	**0**	**0**	**-**	**-**	25000
54SX32A	PQ208	1000	80	**0**	**0**	**0**		80000
54SX72A	PQ208	1000	28	**0**	**0**	**0**		28000
54SX32A	PQ208	1000	88	**0**	**0**	**0**		88000
54SX72A	PQ208	1000	88	**0**	**0**	**0**		88000
RT54SX72S	CQ208	1000	45	**0**	**0**	**0**		45000
TOTAL Units for MEC 0.25um FPGA =			**379**	**Total test time Hrs.**				**354000**
TOTAL Failures for MEC 0.25um FPGA =				**0**				

Table 5: Summary of LTOL data for the 0.25um

Improper Burn-in

Over the course of Actel's history in the HiRel and Aerospace business, Actel has encountered several customer issues related to incorrect burn-in conditions. Thus, it is very important to understand the reasons for performing burn-in under proper conditions. This section describes the demerits of performing burn-in without complete understanding of the inherent risks.

Actel has run several experiments for burn-in to establish acceptable burn-in criteria. During the course of these experiments, devices have been damaged when incorrect testing or vectors, systems and procedures were used. Systems include board design, voltage protection circuits, bypass capacitors, burn-in ovens, fans, heaters, driver boards, cable lengths, power supplies, power lines, sockets, accurate monitors, etc.

Incorrect design of any of the above mentioned parameters could result in device failures. Over voltage or under voltage spikes on power supplies or device inputs can result in CMOS (transistor related) failures. During the course of burn-in acceptable criteria development experiments showed spikes on the power supply due to turning ON the heater for the burn-in oven in Figure 4 below. Example of overstress on an input pin can result in damage at the I/O buffer as shown in Figure 5.

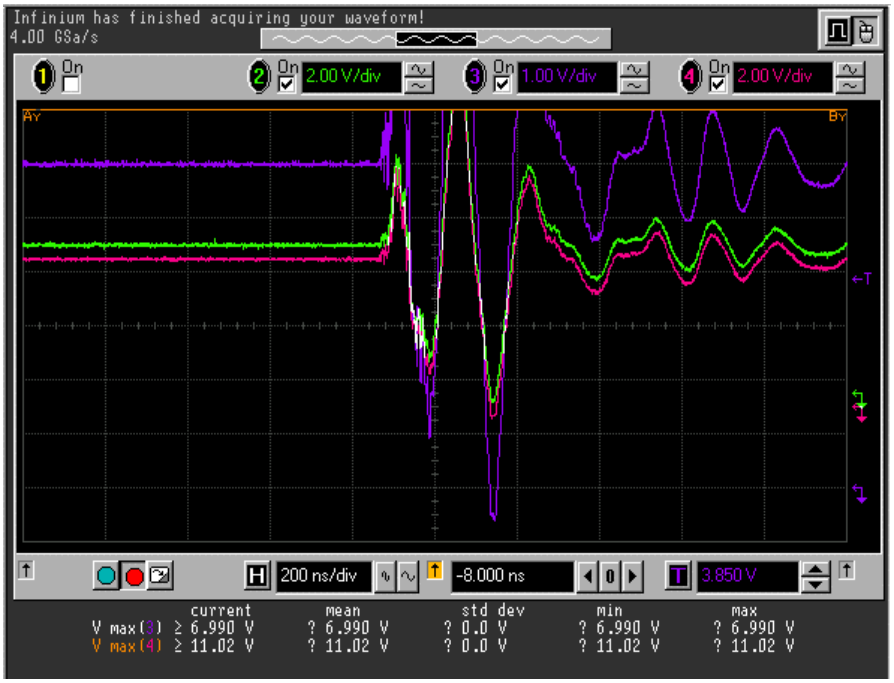

Figure 4 : Spike on Vcca and Vcci in a Burn-in oven

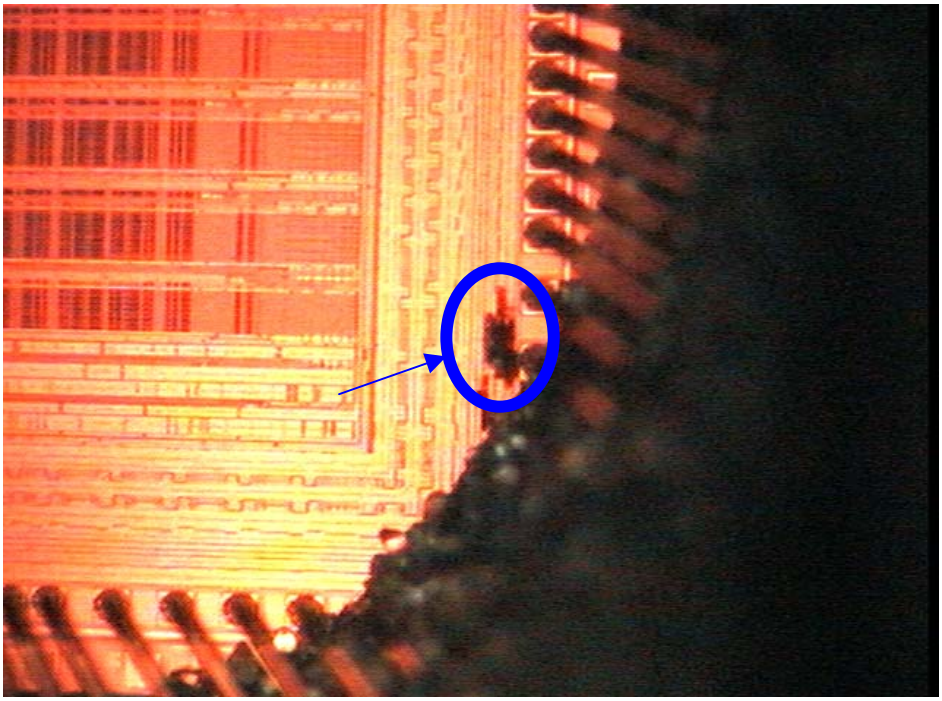

Figure 5: Damage to an input pin due to EOS

Detailed attention must be paid to the design of these burn-in boards in terms of number of DUTs under test, and the number of capacitors per DUT power supply. Capacitors to filter out high and low frequency noise have to be appropriately chosen based on device operating frequency and PCB trace impedances. Voltage regulator circuits to detect spikes need to be carefully incorporated. Driver boards, cable lengths,

proper terminations, oven conditions, sequence of turning on and off of fans, heaters, power line regulation and filtering etc must be taken into account while designing systems for burn-in.

Antifuse related failures have also been observed in an incorrectly designed burn-in system. Root cause has been traced to an overstress condition on the Vcca power supply. A spike on Vcca when coupled with a toggling net can result in pulsed DC currents in excess of the safe operating limits of the antifuse element as shown by the red arrow in the figure below.

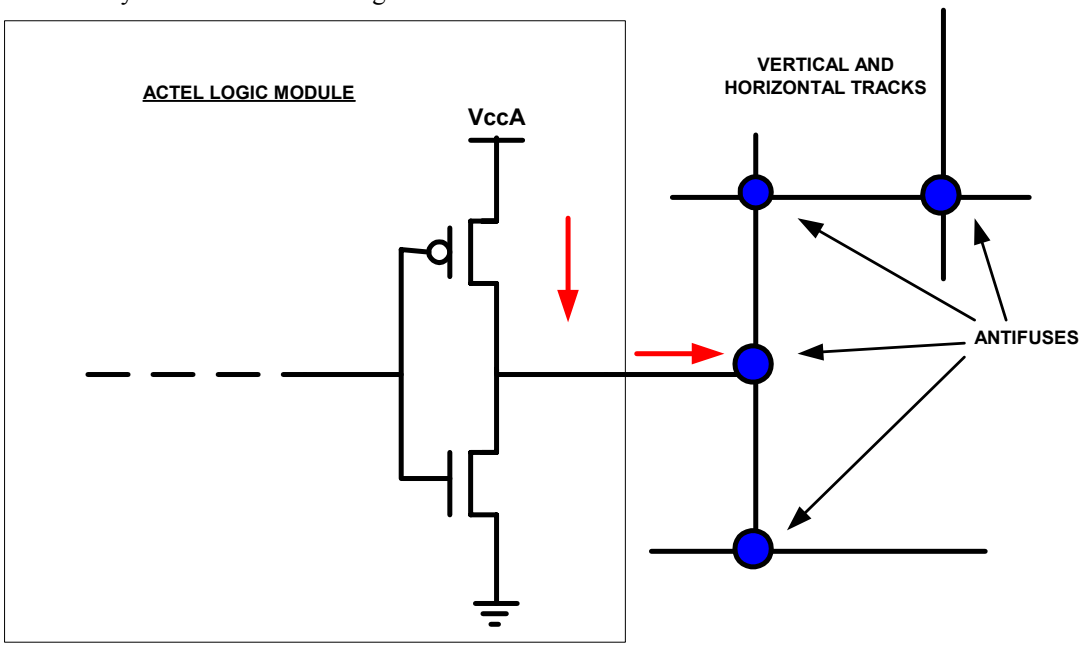

Figure 9: Schematic of LM and fuses

Improper design of any of the above mentioned conditions could result in failures of the device during burn-in. Customers have reported burn-in with incorrect power supplies and lack of capacitors on the boards. A spike on the power supply or the DUT inputs of a very short duration (ns) is enough to cause units to be damaged. As the semiconductor industry goes to smaller process technologies and lower power supplies, the new technologies are increasingly sensitive to out of specification transients. For example:

2.5V spike (for a 5V part) = 50% overstress
2.5V spike (for a 2.5V part) = 100% overstress
2.5V spike (for a 1.5V part) = 167% overstress !!!

Conclusion

As shown in the sections above, the unique architecture of the Actel FPGA allows Actel to test with 100% coverage. 100% of the devices go through the blank burn-ins (DBBI and SBBI-for E-flow only) which stresses un-programmed antifuses, logic modules, routing tracks and I/O's. Many verifications are performed during programming which ensures that a robust antifuse link has been established and no unwanted antifuses are programmed. Programmed Burn-in at Actel shows highly reliable devices as indicated by the data below:

- 632,000 hours of burn-in at HTOL
- 354,000 hours of burn-in at LTOL
- **NO** antifuse related failures have been reported

Thus great care must be exercised in testing and designing of burn-in systems. Considering the complexities and cost of these devices, it is not recommended that customers perform their own burn-in. Actel has effectively shown that that Post Programming Burn In (PPBI) for Actel RT54SX-S and A54SX-A products is not required nor recommended.

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