

Design and Layout Effects on SET Propagation in 90-nm ASIC and FPGA Test Structures

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Abstract—SET propagations in ASIC-like and FPGA-like digital circuits are investigated, using 90-nm test structures, by fault injection and radiation tests. SET fault injection tests are used to show the dependence of the final SET-pulse on the design and layout of the logic circuit.

Index Terms—SET Characterization, Propagation and Mitigation, reprogrammable and non-volatile Flash-based FPGAs, radiation tests, Fault Injection.

I. INTRODUCTION

As the feature sizes of the new-advanced Field Programmable Gate Array (FPGA) circuits have scaled down, their critical charge for Single Event Effects (SEE) has scaled down as well. As a consequence, in highly scaled circuits, an SEE caused by an ion strike can affect both sequential and combinational logic elements.

To induce a Single Event Upset (SEU) in the logic circuit, the Single Event Transient (SET) has to propagate through the data path and finally be latched into a storage device. Therefore, only the final SET pulse at the input of the storage device counts. The formation of the final SET can be separated into two stages: the initiation of an SET at the ion-strike node and the subsequent propagation of the SET to the input node of the storage device. In the past, the initiation stage was considered as the most important. If the initial SET can propagate through few logic stages without attenuation, the SET shape is considered fixed; it can propagate forever without further distortion. However, recent experiments show a strong SET pulse-width modulation throughout the propagation stage, and often the final SET pulse-width depends more on the propagation [1-3].

Many questions have been raised for the best suited test methodology for SET pulse-width measurements. One major controversy is that this phenomenon is very different in ASIC and FPGA circuits. Previous work has shown that in ASICs, for example, the SET is widened by 1.25 ps per inverter-stage when it propagates through an inverter-chain [1], while in FPGAs, the SET pulse width doesn't change after propagating 486 stages of FPGA-inverter [4].

The resulting SET pulse width in front of the storage device (usually a flip-flop) significantly impacts the selected SET hardening technique. Indeed, when SETs are hardened by pulse filtering [5], the SET filter threshold should be set as small as possible to optimize for performance. A typical 90-nm junction node, struck by an ion with a LET of 40 MeV-cm²/mg, will have an SET with width well below 1 ns. Filtering SET with this pulse width and still achieving above hundred-MHz speed is apparently feasible. But propagation can widen the SET to a few ns and cause very expensive trade-offs between the error-rate and speed of the FPGA. Hence the studying and understanding of the mechanisms of the SET propagation in ASICs and FPGAs are very important for applying filter-hardening in these ICs.

An ASIC comprises a set of CMOS logic gates designed to perform a specific function. An FPGA, however, comprises a programmable logic block with a number of initially uncommitted logic modules arranged in an array along with an appropriate amount of initially uncommitted routing resources. Logic modules are circuits, which can be configured to perform a variety of logic functions, such as AND, OR, NAND, NOR, XOR, XNOR, invert, multiplex, add, latch, and flip-flop. Routing resources include elements of wires, switches, multiplexers, and buffers. Other programmable elements also found in modern FPGAs are peripheral circuits such as I/O buffers and embedded components such as memory blocks. The detailed circuit implementation of the logic modules and routing resources can vary from one circuit to another and can impact the SET propagation significantly.

Based on the differences between ASIC and FPGA, the parameters to analyze the SET pulse width during initiation and propagation can be separated into two classes. The first class is generic to both ASIC and FPGA: 1) the shape and width of the initial ion's hit, 2) the ratios of the PMOS and NMOS transistors affecting the rise and the fall times of the SET, 3) the path of the SET-pulse through the logic cells in terms of fanout, load, the types of CMOS gates (inverters, buffers, OR-gates, etc.), 4) the organization of P and N transistors in these gates, 5) the layout of the circuit. The second class is specifically related to FPGA: 1) the routing switches and 2) the user's design-configuration of the FPGA. This paper will quantify SET pulse width modulation caused by these parameters in 90-nm test structures. Extensive SPICE simulations are performed to correlate with radiation test results.

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II. STUDIED TEST STRUCTURES

The applied technique for the measurement of SET cross-section on the combinational logic is derived from a technique used previously [5-7]. As shown in Fig. 1, conceptually the design utilizes an inverter-string connected to a latch to capture SET in the inverters. In normal operation, the input of the inverter-string and the Reset of the latch remain at '0'. The application of a momentary '1' to the Set-input potentially can switch the latch to the set state with an output of '1'. Resetting the latch would recover the output to '0'. Indeed, any SET having a pulse width wider than the latch setup time will trigger the state transition from '0' to '1'. This SET-detection technique will generate a true combinational logic SET cross-section; its result doesn't depend on the clock speed.

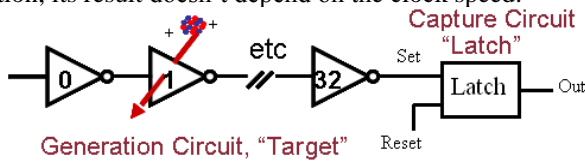


Fig. 1: SET Characterization Circuit

The same technique can be enhanced to measure the SET pulse width and also to mitigate SET effects. Fig. 2 shows a conceptual design of three basic components: 1) a combinational logic, represented by an inverter-string, called target (for SET generation), 2) an SET filter, which controls the minimum detectable pulse width of an SET, and 3) an asynchronous latch to capture and register the occurrence of an SET as a static state. The SET filter uses an inverter string to delay the signal along one path and uses a guard-gate to pass only those transients with widths exceeding the delay. Fig. 2 shows a guard-gate of four transistors; it functions as an AND gate when the two input-signals agree, or as a dynamical storage of the previous state when input signals differ.

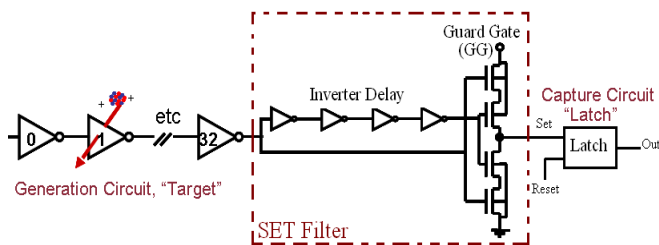


Fig. 2: SET Pulse-width measurement and SET mitigation circuit. It uses an inverter string to delay the signal along one path and a guard-gate to pass only those transients with widths exceeding the delay.

Similarly, the SET detection and mitigation circuit, depicted in Fig. 3, is implemented for all the tested structures. The output of each test structure is connected to an adjustable SET filter, whose filtering strength is controlled by a delay (an inverter-string). Any SET with a pulse-width narrower than the delay time will be filtered. To implement the adjustable delay, a few multiplexors have been added to the traditional SET filter used in [4-5]. Because of these additional gates, only

SET pulses wider than 600 ps can be detected by the SET-Filter circuit.

For all the tested structures, the filter threshold, which is determined by the number of inverters in the delay chain, ranges between 0.6 ns and 15.8 ns. The target circuit is then varied to investigate the effects of the circuit elements on the propagation of the induced transient in the target circuit.

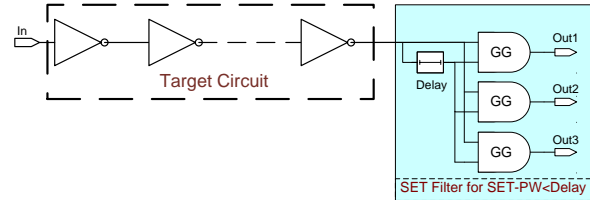


Fig. 3: SET Detection and Mitigation Circuit. The output of each test structure is connected to an adjustable SET filter, whose filtering strength is controlled by a delay (an inverter-string). The guard-gate (GG) is tripled to avoid counting SET errors in the GG itself.

The two types of test circuits are named ASIC-like and FPGA-like. The ASIC-like includes mainly inverter-strings with various stages, different layout spacing, loads and routing; while the FPGA-like includes various logic cells used in FPGAs, such as LUTs, carry-chains and adders.

Fig. 4 depicts the ASIC-like test structures and they are as follows:

- *T1a* also called *Inv-500*: a 500 inverter-string. R1 and C1 are parasitic resistance and capacitance, whose values depend on the layout.
- *T1b* or *InvS-500*: a 500 inverter-string, where an N pass transistor is inserted between each two adjacent inverters. Again, R2 and C2 are also parasitic. This will show some of the routing effects on the SET propagation.
- *T1c* or *InvSL-500*: a 500 inverter-string, where an N pass transistor, and external resistance and capacitance loads (RL and CL) are inserted between each two adjacent inverters.
- *T1d* or *InvSL-50*: This test structure is similar to the case 1c except that the number of stages (inverter + switch + external load) has been reduced to 50 and the layout spacing between adjacent stages has been increased to 10 μm , resulting in additional parasitic capacitance and resistance as shown in Table 2. The purpose of this case is to show layout variations.

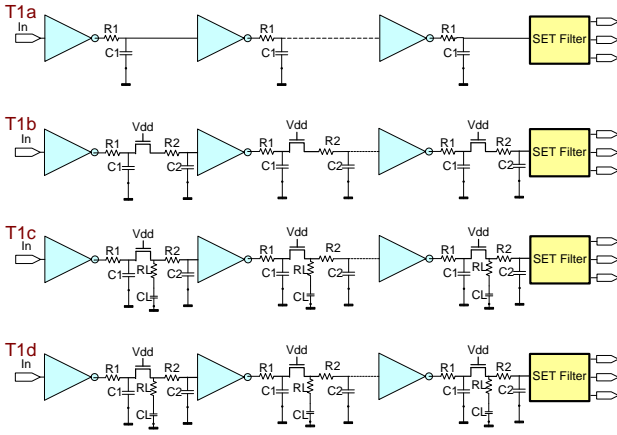


Fig. 4: ASIC-Like Test Structures. R1, R2, C1 and C2 are parasitic resistance and capacitance; RL and CL are externally applied loads.

Furthermore, tables 1 and 2 show the features of these test structures (channel width and length of each transistor) as well as the parasitic resistance and capacitance estimated from the layout of the circuits. In table 1, Wp and Wn are respectively the channel-widths of the P and N transistors and Lp and Ln are their channel-lengths. In this case, the ratio of the P and N channel-widths is equal to one. In the remainder of this paper, this ratio is called R1 or “N-dominant” test structure.

Table 1: Channel Widths and Lengths of Transistors

TS	Inverter	Inverter	Switch	Switch
	Lp, Ln	Wp, Wn	Ln	Wn
1a	Inv-500	0.1	0.22	-
1b	InvS-500	0.1	0.22	-
1c	InvSL-500	0.1	0.22	0.16
1d	InvSL-50	0.1	0.22	0.455

Table 2: Capacitances and Resistances in the ASIC Structures

TS	R-Sw	R1	R2	RL	C1	C2	CL
	(Ohms)	(Ohms)	(Ohms)	(Ohms)	[fF]	[fF]	[fF]
1a	-	50	-	-	0.49	-	-
1b	2.6K	38	50	-	0.54	0.84	-
1c	2.6K	38	80	32	0.48	0.10	1
1d	2.6K	38	88	32	0.49	2.19	1

The FPGA-like Test Structures are shown in Fig. 5. They are Look-Up Tables (LUTs) configured as buffers, carry-chains, and adders. A LUT is a set of CMOS logic circuits and routing switches that can be configured to perform any combinational logic function using a given number of inputs and one output. In this case, it is a LUT4, i.e. it using up to 4 inputs.

- T2a or LCB-500: a chain of 500 LUTs each one of them configured as a buffer (LCB) to show the maximum lengthening of an SET pulse width without the compensation effects as demonstrated in the previously published data [3].
- T2b or CC-500: a 500 carry-chain. The same type of circuit might exist in an ASIC.

- T2c or SUM-500: a 500 adder-string, where each LCB is combined with a carry-chain.

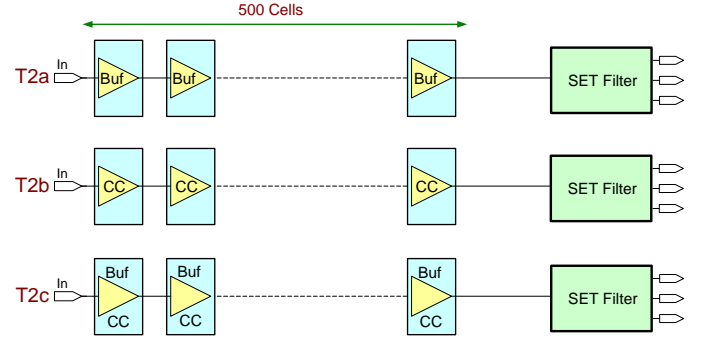


Fig. 5: FPGA-Like Test Structures

III. RADIATION TEST RESULTS

The radiation test experiments were performed at the Lawrence Berkeley National Labs (LBNL). The aforementioned SET filter was implemented with three delay options: “No-Delay”, “Delay 1” (6 inverters) and “Max. Delay” (36 inverters). For the “No-Delay” option, the delay circuit is bypassed; however, only SET wider than 600 ps can be detected. This is due to the setup times of the multiplexers and the guard-gate circuits between the latches and the target logic-circuit. For the “Delay 1” option, only SET wider than 1.8 ns will be detected, and only SET wider than 15.8 ns will be detected for the “Max. Delay” option. The data is shown in Fig. 6 for the ASIC-like test structures and in Fig. 7 for the FPGA-like test structures. No errors were observed in all the ASIC-like test structures when mitigated with the “Delay 1” option. Therefore, Fig. 6 shows only the data obtained for the non-mitigated cases. In the FPGA test structures, even with the “Max. Delay” option, errors were still observed on the test structures T2a and T2c but not with the test case T2b (the carry-chains). To simplify the presentation, Fig. 7 shows only the data with the “No-Delay” and the “Max. Delay” options.

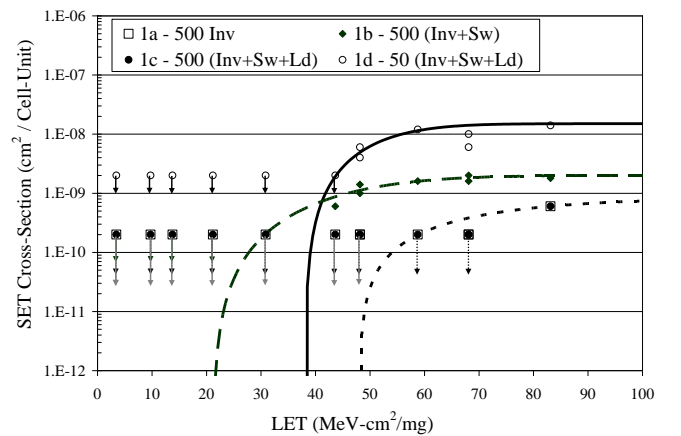


Fig. 6: Beam Test Results for the ASIC Structures

The radiation data show no SET sensitivity for the 500 inverter-chain till an LET of 83.13 MeV.cm²/mg. This means that all the SET pulse widths were shorter than 600 ps. However, based on the data published in Ref. 1, the average widening per inverter is 1.25 ps. From this, it would be

expected that an ion-hit on the first inverter of this chain would have been widened with 625 ps ($500 * 1.25$) and so the absence of a widened pulse at the output would mean the inverter is SET immune. We know that they are not and therefore this data contradicts the previous published data in [5]. Instead it provides evidence that if there was SET pulse-widening, the LET_{th} should have been much lower and the saturation cross-section higher.

Furthermore, the radiation data obtained for the test structure InvS-500 showed that the LET_{th} was reduced to 22 MeV.cm²/mg and the saturation cross-section increased to 2 E-9 cm²/logic-cell. This means that the switches are contributing to the SET cross-sections and consequently reducing the LET_{th} of a logic cell or that the N pass transistors are widening the initial SET pulses (caused by the heavy-ion hits). With this test structure (T1b), the RC parasitic circuits have been increased and consequently the asymmetry also increases between the rise and fall times of any signal that will propagate through its logic cells, including SETs. SET simulation in the next section will study the effects of the inserted RC circuits.

Furthermore, the test case InvSL-500 exhibited errors at an LET threshold around 50 MeV.cm²/mg while the saturation cross-section is reduced to 8 E-10 cm²/logic-cell almost as if the switches and the load capacitances have not been added. This data shows that the SET widening caused previously in the test structure 1b was compensated for by the added load. Most importantly, it demonstrates that with the right load and routing, all SET can be filtered. Moreover, despite what would be predicted by [1], the test case InvSL-50 exhibited errors at LET_{th} around 40 MeV.cm²/mg while the saturation cross-section was increased to almost 2 E-8 cm²/logic-cell. Therefore, the added spacing in the layout to avoid the MBU effects instead increased the SET-broadening in the test structure 1d. One should remember that this layout spacing should result in more resistance and capacitance inserted in series between each two logic cells.

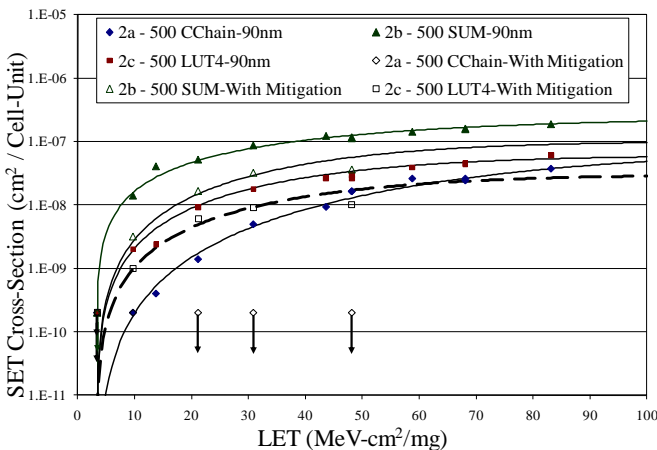


Fig. 7: Beam Test Results for the FPGA Structures

For the FPGA-like test structures, the LET_{th} was about 4 MeV.cm²/mg even with the “No-Delay” and the “Max. Delay” option and the saturation cross-section did not vary much between the non-mitigated and the mitigated versions. This

means that the initial SETs were certainly widened to higher than 15.8 ns, which was expected and well explained in [4]. Indeed, since all the tested structures are not inverting the input signal, a positive SET pulse on the first cell (carry-chain (CC), LCB or LCB+CC) will be widened from one cell to another. All of these test structures are not representative of a real FPGA test design, because no compensation effects are taken in consideration between the positive and negative pulses [3]. Test structures with LUTs configured as inverters will be added and tested in future work to demonstrate these effects.

In the remainder of this paper, SET fault injection by SPICE simulation are performed on the extracted netlists of most of the tested structures to better understand the radiation test results.

IV. SET FAULT INJECTION BY SPICE SIMULATION

SPICE simulation tests were performed by means of HSPICE, version 2007.09. The netlists of the same circuits tested in beam were extracted with the layout parasitic capacitances and resistances. For each test structure, consecutive positive and negative pulses are injected at its input (*Din*) and its SET pulse width is measured at its output (*Dout*), as shown in Fig. 8. The measurements are made with trigger levels for each input/output pulse set at $V_{dd}/2$ (0.6 V).

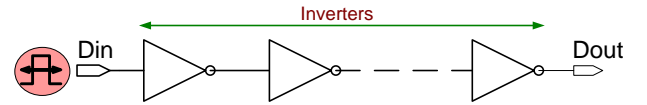


Fig. 8: Scheme of the Fault Injection Test Points

The rise and fall times of the positive pulse are named *trp* and *tfp*, and of the negative pulse *trn* and *tfn*. Based on the test condition used, the width of the flat part (*tw*) of the injected pulse (at V_{dd} if the pulse is positive or at 0 V if the pulse is negative) could be variable or fixed. Four test conditions were simulated with positive and negative pulses as shown graphically in Fig. 9, with the temporal parameters listed in Table 3.

Table 3: Rise and Fall Times of the Injected Pulses

Pulse	<i>Trp</i> (ps)	<i>Tfp</i> (ps)	<i>Trn</i> (ps)	<i>Tfn</i> (ps)	<i>Tw</i> (ps)
1	200	200	200	200	variable
2	28	200	28	200	variable
3	28	variable	28	variable	0
4	variable	28	variable	28	0

- *Pulse 1*: A perfectly symmetrical positive or negative pulse is injected at the input of each test structure and the pulse at the output of each test case (1a, 1b, etc.) is measured. In this case, *trp* equals *tfp*, *trn* and *tfn*. Digital simulators such as ModelSim allow only this type of SET fault injection and does not account therefore for the ion’s diffusion time in the sensitive transistor node.
- *Pulse 2*: An asymmetrical pulse is injected at the input of each test structure (*Din*), more similar to SET resulting from

an ion-hit, except that the SET diffusion time is almost instant. This type of SET pulse simulates only the ion's drift in the sensitive transistor node, and mimic its impact on the SET pulse width change. The rise and fall times of the pulses are fixed while t_w is variable.

- *Pulse 3*: The t_{rp} and t_{fn} of the injected pulse are fixed, t_w equals 0, and t_{fp} and t_{rn} are equal to each other but variable. This pulse most closely resembles the SET resulting from an ion's hit and mostly the SET diffusion part in the strike transistor.
- *Pulse 4*: The t_{fp} and t_{rn} are fixed, t_w equals 0 and t_{rp} equals t_{fn} . This specific fault injection will show the effects of the SET pulse shape on its propagation and whether opposite signal pulse shapes will lead to opposite effects.

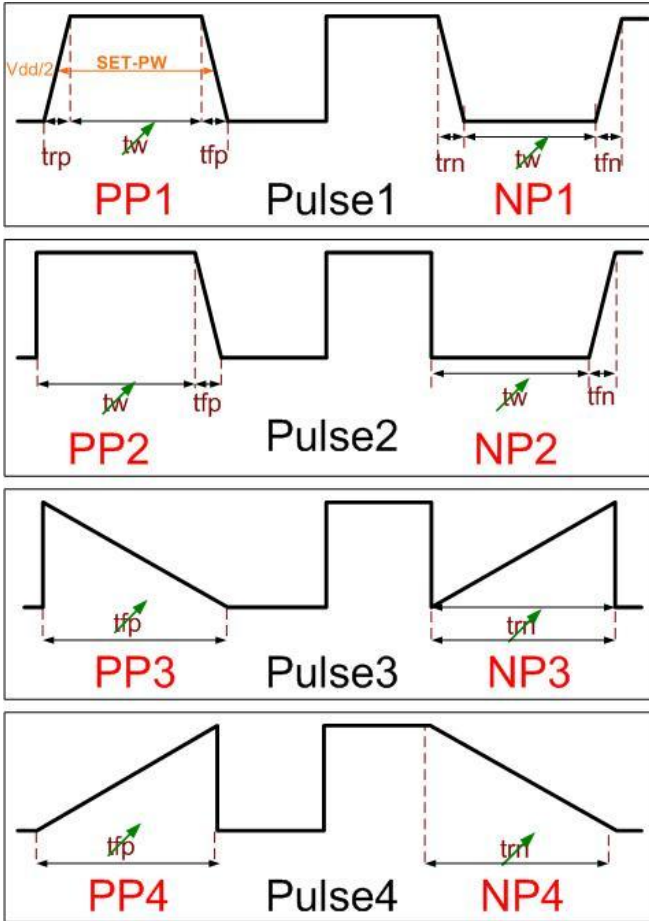


Fig. 9: Simulated SET Pulse Shapes and Widths

V. SET FAULT INJECTION SIMULATION RESULTS

To better understand the major parameters affecting the SET propagation in a given circuit, SPICE SET simulations were performed first on the netlists of ideal test structures. The ideal test structures are composed of inverter-strings, with various numbers of inverters but without resistances or capacitances in the layout. Although these ideal test structures cannot be implemented in a real-circuit, they are mandatory for the understanding of the SET propagation mechanism in integrated circuits (ICs).

A few parameters were varied and their effects on the SET propagation were studied. These parameters are 1) the number of inverters, 2) the ratio of the channel-widths of the PMOS and the NMOS transistors, called also P/N ratio and 3) the SET pulse shape and width. The PMOS and NMOS ratio is equal to the P transistor channel-width divided by the N transistor channel-width (Ratio = W_p/W_n). In this paper, it is also named P/N ratio or simply R.

Furthermore, three different P/N ratios: N-dominant ($R=1$), balanced ($R=2.59$) and P-dominant ($R=4$) are selected for the SET simulation tests. For clarity purposes in this paper, the N-dominant type, P-dominant and balanced are named R1, R4 and RB respectively. RB is the ratio where the rise and the fall times of the P and N transistors are equal, hence the name balanced.

A. Impact of the Number of Inverters, the Pulse Width, and the P/N Ratio

Pulse 1 type SETs (Fig. 9) were injected on the ideal test structures shown in Fig. 8, where the number of inverters and the P/N ratios were varied. With the SET pulse shape (P1), the simulation results displayed in Fig. 10 show that the variation of the number of inverters and the P/N ratio has minor effects on the propagated SET pulse width in ideal inverter-strings. For instance, with the balanced test structure (RB), SET pulses propagated with almost the same SET pulse width (± 2 ps). However, with *Pulse 3* SET types, the SET pulse width has varied of ± 20 picoseconds for all inverter-strings.

In addition, the variation of the P/N ratio has almost no effect on the SET widening or filtering with both pulse shapes. Its effect is very minor, varying between ± 10 picoseconds for inverter-strings of 50 inverters or less. This variation is slightly augmented to (± 20 ps) when the number of inverters is increased to 500 cells. The augmentation of the SET pulse width with the number of inverters could be related to the increased load, forcing the transients with the short pulses to reduce their amplitude while widening their pulses. In the following, the balanced test structure is selected to study the impact of the SET pulse shape on the resulting pulse width.

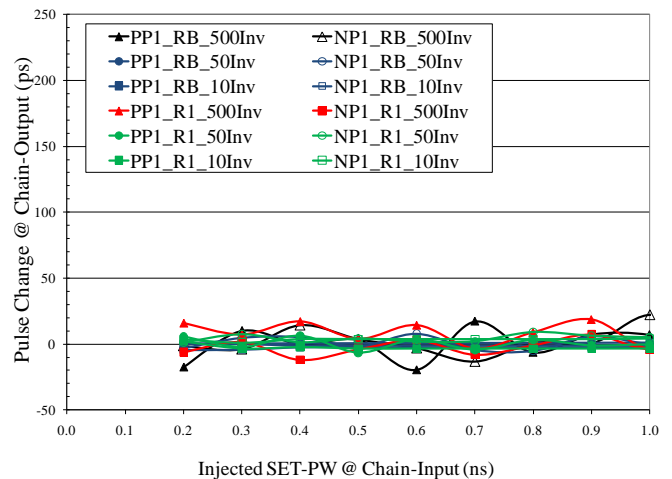


Fig. 10: Impact of the # of Inverters, the pulse width and the P/N Ratio

B. Impact of the Number of Inverters and the SET Pulse Shape and Width

Pulse 1 and *Pulse 3* type SETs were injected at the inputs of the 10, 50 and 500 balanced ideal inverter-strings (with no resistances or capacitances). As displayed in Fig. 11 and for all the simulated test structures, the width of the propagated SET-pulse varied mostly with the shape of the injected SET-pulse but not with the number of inverters used. In addition, SETs of 1 ns pulse width like *Positive-Pulse 3* (PP3) increased by approximately 80 ps in width at each output of the simulated inverter-string, compared to 10 ps for SETs like PP1. While, SETs of 1 ns like *Negative-Pulse 3* (NP3) increased by approximately 120 ps, compared to 20 ps for *Negative-Pulse 1* SET type. As the balanced ratio (RB) was calculated based on the rise and the fall times of a symmetrical pulse like *Pulse 1*, the asymmetry of a pulse-shape like *Pulse 3* was not taken in account. Both of the PP3 and the NP3 pulses have been widened.

An I.C. designer should readjust the channel-widths of the P and N transistors to account for the additional asymmetry caused by the initial pulse shape. This should result in the slight decrease of the PMOS channel-width, so SETs will be less widened. As ions' hits result in SET-pulses closely resembling to *Pulse 3*, the asymmetry of the SET pulse-shape is most likely one of the main reasons behind SET broadening and filtering in ICs.

Fig. 11 shows also that the SET pulse-widening is linearly proportional to the injected SET pulse width that can be approximated by the function ($y = Ax + B$). In the following, A is called the amplification factor. In the case of the simulated inverter-strings, A equals 84 and B equals 33.5 ps. As the slope of the SET-pulse increases, the meta-stability region of the very first inverters (less than 10) is augmented and with it the SET pulse-widening. Since this SET pulse-shape is more resembling to the SET resulting from ions' strikes, new fault injection tests are needed to study the effect of the P/N ratios, this time with SET-pulses like PP3 and NP3.

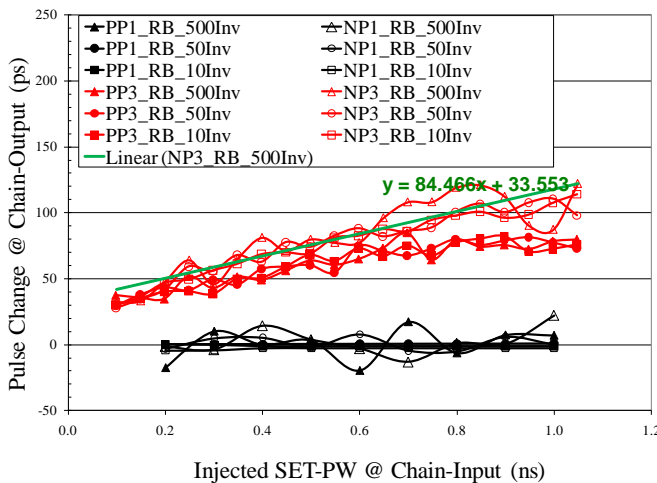


Fig. 11: Impact of the # of Inverters and the SET pulse width and SET pulse shape

C. Impact of the P/N Ratio with Asymmetrical SET-Pulses

Three 50-inverter-strings were tested, each with a different P/N ratio (R1, RB and R4). The N-dominant (R1) inverter-string showed the highest SET broadening, approximately 170 ps for an initial SET pulse width of 1 ns (shown in Fig. 12), while the P-dominant (R4) inverter-strings showed the most broadening of the negative pulses. Positive SET-pulses are then broadened with inverter-strings that have wider P transistors than the N transistors and vice versa for the negative SET-pulses in test structures, whose N transistors are wider than their P transistors. This result shows the impact of the P/N ratio on the propagation of SETs like ions' hits, which resemble to *Pulse 3*.

The data was fitted with a straight line to determine the implied amplification factors. It is interesting to see that the ratio of these slopes appears to be related to the ratio of the P/N ratios. That is $A(R1)/A(RB)$ for the PP3 data equals 2.86 (145.17/50.67), which is very close to $RB/R1$ (2.59). For NP3, $R4/RB$ is 1.59 and the $A(R4)/A(RB)$ is 1.56. Consequently, we can approximate the amplification factor $A(Rx)$ of the initial positive SET-pulse to be:

$$A(Rx) = A(RB) / (RB/Rx) \quad (1)$$

where $A(RB)$ is the amplification factor for the positive pulses in the balanced inverter-strings. Conversely, the amplification factor $A(Ry)$ can similarly be approximated as:

$$A(Ry) = A(RB) * (Ry/RB) \quad (2)$$

Although these two formulas are not very accurate, the simulation results show a dependency suggesting these relationships. This needs to be explored.

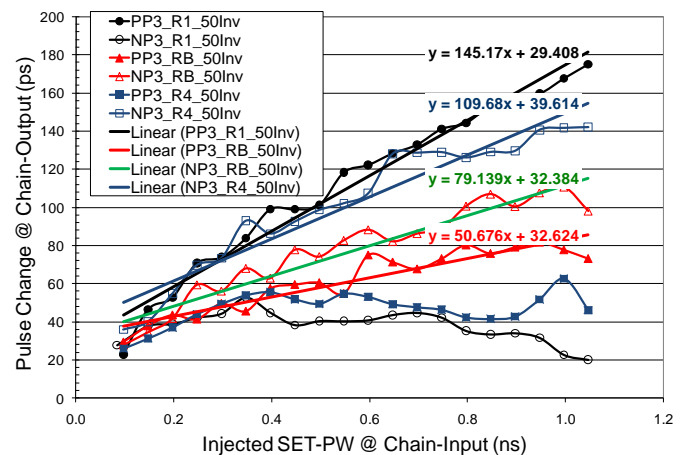


Fig. 12: Impact of the P/N Ratio with Asymmetrical SET pulse shape

Finally, it has been shown again that the SET widening and broadening is related to the polarity of the injected SET pulses (positive or negative) and to the P/N ratio of the simulated test structure. This behavior is more observable with SET-pulses like *Pulse 3* that amplify the meta-stability region of the first inverters leading them to operate as a linear amplifier. It is also clear that the SET-pulse changes are controlled by the initial SET-pulse rather than by the number of inverters: the higher the positive or negative slope of the SET pulse is, the greater the SET pulse-change.

It is also clear that the notion of average widening and filtering per inverter cannot be used here because the change in the pulse width is rather dependant on the pulse shape than on the number of inverters used. In the remainder of this paper, the SET fault simulations will target the netlists of the irradiated test structures, showing the impact of the design and the layout of a test circuit on the SET propagation. The studied test structures are 1) the ASIC-structures *T1a* (500 inverters) and *T1d* (50 inverters with load and routing switches) and 2) the LUT-Buffers.

VI. IMPACT OF THE DESIGN & LAYOUT OF A TEST CIRCUIT

A. SET Simulation in the ASIC Structures

As both of the test structures *T1a* and *T1d* were manufactured with the ratio R1 (N-dominant), SET pulse-widening is very much expected. Figures 13 and 14 show the simulation output for the test structures *T1a* and *T1d*, obtained with different injected SET-pulses (*Pulses 1, 2, 3 and 4*).

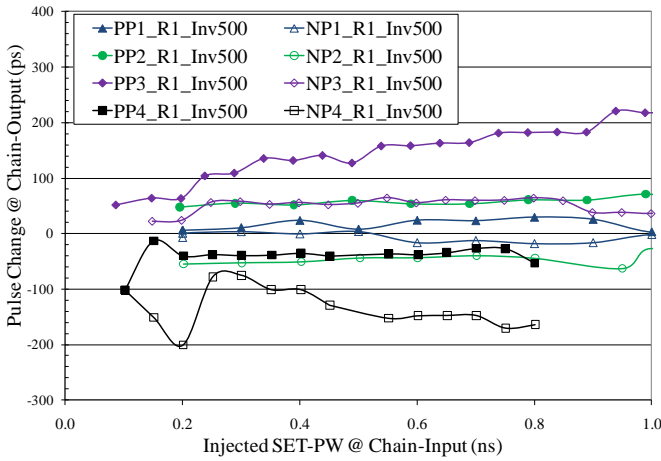


Fig. 13: Pulse Changes vs. Injected SET Pulse Widths for the 500 Inverters' String Test Structure

The simulation results for the test case 1a (500 inverters) show that the pulse widths of the injected-SETs like *Pulse 1* and *Pulse 2* were very little changed at the outputs. The changes are within ± 50 ps for the *Pulse 2* and ± 20 ps for the *Pulse 1*. This result is very similar to what has been presented in Fig. 10, where no amplification of the SET pulse width was observed, as opposed to with the injection of SETs like *Pulses 3 and 4*. This shows that most of the SET broadening is not due to the SET drift in the sensitive transistor node but rather to its diffusion. The longer the diffusion time, the stronger the changes in the SET pulse width are.

Moreover, because of the added layout resistances and capacitances between the inverters, the SET pulse width amplification is higher for the simulated structure *T1a* compared to the ideal inverter-string. For instance, for a *Pulse 3* with an initial width of 1 ns, the pulse-widening has increased from 120 ps for the ideal test structure to 200 ps for the *T1a* inverter-string. Because of the real asymmetry of SETs (closely resembling to *Pulse 3*), this result indicates a potential issue for ICs and particularly for FPGA circuits using long

routing. It will get only worse with higher-scaled technologies (90 nm and below).

As no SET was detected in the *T1a* till an LET of 83.3 MeV.cm²/mg, and knowing that all SET that are shorter than 600 ps are filtered by the added guard-gates, SET at the latches' inputs (Fig. 3) are certainly narrower than 600 ps. The simulation results presented in Fig. 13, indicate then that an SET on a single inverter is most likely to be narrower than 450 ps, since its widening was only 150 ps. Such widening of 150 ps should not make a huge difference in FPGA circuits unless other considerations are taken in account such as the layout parasitic capacitances and resistances. This will be shown for the case 1d. Finally, as shown in Fig. 13, the simulation results from the *Pulse 4* injections show the opposite effect compared to the results issued from the injections of *Pulse 3*, as expected.

For the test case 1d (*InvSL-50*), the injected SET pulse widths like *Pulses 1, 2 and 3* were all widened even more (± 300 ps), due to the additional layout resistances and capacitances inserted in the test structures. As a result, although the number of used logic cells was reduced from 500 to 50, the output SET pulse width was higher in the *T1d* simulated structure. Indeed, because of the added spacing (10 μ m) between each two inverters, resulting in increased resistances and capacitances (Table 2), the asymmetry of the propagated SET at the output of the first inverters was increased and with it the amplification factor of the SET pulse width. The increased number of inverters will not change the resulting SET pulse width but rather will increase the probability of having asymmetrical nodes in the circuit design.

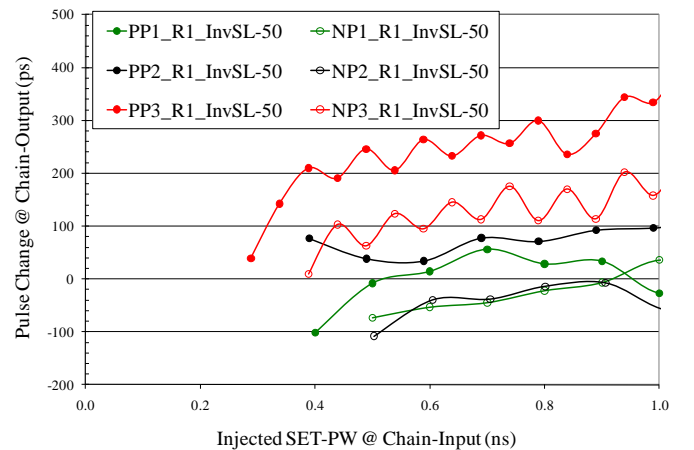


Fig. 14: Pulse Changes vs. Injected SET Pulse Width for the Test Structure of 50 Inverters' String with Load and Routing Switches

It is then clear that SETs in the test structure *T1a* were at the edge of the minimum SET pulse widths that could trigger the SET detection circuit and therefore an increase of few hundreds of picoseconds would make a difference in the LET_{th} and the saturation cross-sections. This is evidently a critical case for ASICs, in which asynchronous circuits designed for high speed-applications in space, avionic, or even in the atmospheric environments, may be implemented. This result can indicate the reason behind the high pulse-widening

observed in [1], where lengthening of the SET pulses could simply be due to the shape of the laser pulse or the layout spacing that they have used in the beginning to avoid MBUs but resulted in the lengthening of the SET pulses.

B. FPGA-like Test Structures

Because of the long hours required for SPICE simulations with the big netlists, the test structure 2b was reduced to 50 LCBs but the simulation data was extrapolated to 500 LCBs. The data displayed in Fig. 15 show that a 1 ns SET pulse width (positive or negative) will increase with approximately 200 ps at the first LCB-output (y1) and then becomes independent of the initial injected SET pulse width. The average increase in its initial SET positive pulse width is 35 ps after ten LCBs (y10). Conversely, the average change in a 1 ns negative injected SET pulse remains very small.

Note that the greater the number of LCBs used; the smaller the average pulse width increase per LCB. Finally, as the increase per LCB stage is about 35 ps after 500 consecutive LCBs, the SET pulse width will be increased by 17.5 ns, which explains why SETs were not mitigated with an SET filter of 15.8 ns.

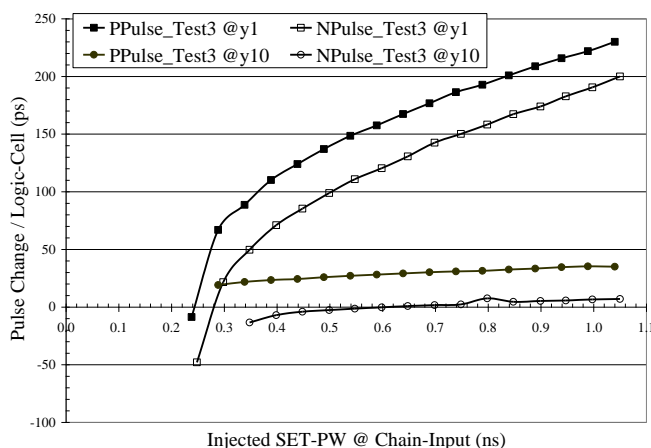


Fig. 15: Pulse Changes vs. Injected SET Pulse Width for the LUT-buffers string. It shows that a 1 ns SET pulse width (positive or negative) will increase with approximately 200 ps at the first LCB-output and then becomes almost independent of the initial injected SET pulse width.

Finally, this result agrees with what was presented previously in [3]. The SPICE simulations should be extended to the LCI test cases (LUTs configured as inverters), with variable load, switches and layout spacing, to demonstrate the compensation effects for real designs. These SPICE SET fault injections were performed with discrete signals to show purposely the rise and fall times and intrinsically the P/N ratio effects on the SET propagation. But, other SPICE simulation tests are ongoing to show the SET fault injection with the real forms of the ions' hits (double exponential) as previously published in [8-12]. The different possibilities of configuration and routing of an FPGA design can increase the probability of asymmetrical nodes in an FPGA and with it the SET pulse width. FPGA designers should then be very careful with the

routing and configuration of their designs implemented on the high-scaled FPGAs (90 nm and below).

VII. CONCLUSION

SET propagation in 90-nm test structures like ASICs and FPGAs was investigated. Radiation results and SET fault injection tests show a clear distortion of the SET pulse widths related to the design and layout of each test structure. For pure inverter-chains with a balanced P/N ratio, the broadening effects are minor as shown by our SPICE fault injection and the radiation test results. However, if the layout spacing between the inverters is increased, the changes in the SET pulse widths will become clearer and dependent on its initial pulse shape.

The asymmetry of the SET pulse shape combined with a non-balanced P/N ratio (P-dominant or N-dominant) and layout variations result in differences in the SET propagation such as its filtering or broadening. For ASIC-like test structures, this issue might become a concern and should be addressed and accounted for in high-scaled technologies.

It is clear though that because of the basic FPGAs' design based on logic modules such as LUTs, SETs will be reshaped from the first logic-cells into a rectangular shape. Actually, the more LUTs inserted in a chain, the lower is the average increase of the SET pulse width per LUT. It is also clear that any number of LUT-inverters can be used to measure the SET pulse widths, if the design, the architecture, the configuration and the layout are well accounted for in an FPGA. SET fault injection by ModelSim and SPICE are mandatory before any beam test experiments for SET characterization.

Considerable work in automating SET fault injection in circuits to simulate the radiation effects has been published and has resulted in tools that are commercially available [13]. This paper is the first in a new research area to model and simulate SET effects on the netlists of real circuits and study their propagation through the circuit's logic gates. Ultimately, the objective is to automate a fault injection tool to simulate SETs in the netlists of novel products such as Actel's next generation of radiation-tolerant Flash-based FPGAs and prevent the increase of SET pulse widths due to variations in design, architecture, layout and configuration. SPICE SET fault injection will be recursive and interactive with the simulated circuits so rise and fall times of the injected current pulse will be taking into account the circuit's parasitic capacitances and resistances.

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