Configuration and Routing Effects on the SET Propagation in Flash-Based FPGAs

Sana Rezgui, *Member, IEEE*, J.J. Wang, *Member, IEEE*, Yinming Sun, Brian Cronquist, *Member, IEEE*, and John McCollum

***Abstract*—New insights on SET propagation in Flash-Based FPGAs are investigated, with regards to their technology and unique non-volatile architecture. By means of SET fault injection tests, the broadening and the filtering of SET pulse widths were demonstrated and are related to the SET pulse transition and data-path in the studied FPGA design. These basic mechanisms result in a clear dependence of the SET pulse width on the design's configuration and routing that would favor spontaneous SET filtering in most real life designs.**

***Index Terms*—SET Characterization, Propagation and Mitigation, reprogrammable and non-volatile Flash-based FPGAs, radiation testing, Fault Injection.**

I. Introduction

Low Power Flash-based Field Programmable Gate Arrays (FPGA) are gaining interest in the radiation community due to their re-programmability feature while being non-volatile, and the possibility of their full mitigation to Single Event Effects while being a single-chip solution [1]. If hardening to Single Event Upsets (SEU) is incorporated into such a non-volatile circuit's sequential logic, Single Event Transients (SET) in combinational logic can become the primary source of observable errors, while being "transient" if not captured by a memory cell [1-7]. To avoid SET capture by any memory element (Flip-Flop (FF), latch, SRAM, etc.), SET could be filtered at its input. While the SET filtering techniques described and validated in [1-3] are applicable to all integrated circuits, they are of particular interest to non-volatile FPGAs (NVFPGA), which provide a convenient measurement and experimentation vehicle for the investigation of radiation effects as demonstrated in this paper.

In [1], new SEE characterization and mitigation techniques, based mainly on SET filtering, were described and validated on a Flash-based FPGA core, called ProASIC3 (also A3P). The SET characterization consisted mainly of SET Pulse Widths (PW) and cross-section measurements for a Logic Cell (LC) configured as an Inverter (LCI) followed by a Floating Gate (FG) switch. The assumptions were that all used LCIs have the same SET sensitivity, the routing structures are identical between two LCIs and have the same SET sensitivity, and an SET would keep the same PW from one LCI to another.

Obtained Heavy-Ion (HI) beam results showed that in an A3P FPGA, a technology of 0.13-µm, an SET could last longer than 3 ns, which raised many questions in the radiation community suggesting that such wide SET could only be due to the long used LCI-chains (486 of them). Indeed, in [8], where experiments for SET characterization were performed by means of laser Fault Injection (FI) experiments, it was demonstrated that SET-PW could get wider in long inverter-chains, with each consecutive inverter, and therefore an overestimation of SET-PWs in our case [1] could have easily been obtained. Hence, the first main idea of this paper is to trace the SET propagation in each LCI-string and to make certain that no SET pulse-width change from one LCI to another has occurred, which otherwise could lead to a wrong estimation of the maximum SET-PWs or SET cross-section per LCI. Since there was previously no continuous checking of the SET-PW propagation in a given LCI-string in-beam to confirm that, FI experiments are applied in this case.

This work will evaluate the previous HI beam results, by employing new SET FI approaches, first by simulation and second on the silicon itself, showing the SET signal propagation in an FPGA design through its LCs and diverse routing structures. Indeed, as detailed in [10], an A3P FPGA core comprises a programmable logic block with any number of initially uncommitted LCs arranged in an array along with an appropriate amount of initially uncommitted routing resources. While each LC can be configured to perform a variety of combinational or sequential logic functions, routing resources can include a mix of components such as long or local wires, FG switches, multiplexers, and buffers. As each given circuit implementation of the LCs and routing resources can vary greatly, it is advised to check if an SET-pulse would propagate differently in various routed designs with various configurations.

Hence, these are the main questions that this paper will address: How do SETs propagate in non-volatile FPGAs, particularly the Flash-based FPGAs? Is the first measurement of SET-PWs in [1], an overestimation of the initial SET-PW

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caused by an ion hit? Should a separation between the measurement of the first SET caused by the ion hit and the way this SET propagates in the FPGA design be made? How does the routing and configuration of an FPGA design affect the SET-PW?

In this paper, we will study the FPGA design's implementation effects on the SET propagation with respect to the number of used LCs, the LC configuration-function, the SET resulting negative ('1' to '0') or positive ('0' to '1') pulses, and the variation of routing structures. These findings should allow us to construct a few standard recommendations for an accurate SET-PW and cross-section measurement on a single LC as well as a better understanding of the configuration and routing effects on the SET propagation in a real life design.

II. SET Characterization in Flash-Based FPGAs

In previous work [1, 7], two flash-based FPGAs have been characterized for SETs: the ProASIC3 FPGA and the Low-Power IGLOO FPGA, called also AGL. They both have almost the same internal architecture, except for the process, leading the IGLOO to be a very low-power FPGA with a power consumption in the microwatts. To allow a better understanding of the SET characterization, both of the DUT internal architectures and the beam test designs are described in the following.

A. Devices Under-Test: ProASIC3 & IGLOO FPGAs

Both of the 0.13-µm *ProASIC3/E* and the very low-power FPGA *IGLOO/E* product families have up to 3 million system gates, 504 kbits of true dual-port SRAM, 616 single-ended I/O, and 300 differential I/O pairs. They also include 1 Kbits of on-chip, programmable, nonvolatile Flash ROM (FROM) memory storage as well as up to 6 integrated Phase Locked Loops (PLLs), as shown in Fig. 1. The FPGA core consists of a set of logic tiles (called "VersaTiles") and routing structures. Each logic tile is a combination of CMOS logic and flash switches and can be configured as combinational or sequential logic by programming the appropriate flash switch interconnections [10]. The logic tiles are connected with each other through routing structures and FG switches.

Furthermore, both of the A3P and the AGL FPGAs are pin to pin compatible and identical at the architectural level except for the new feature called "flash-freeze" added to the AGL parts. Indeed, by simply asserting a single input, the device enters a low-power mode in 1µs, in which case, clocks are frozen, I/Os are tri-stated, and core registers and memories maintain state. In the freeze mode, power consumption ranges from 5µW on the smallest (AGL030) device to 289µW on the largest (AGL3000E) device [10]. In addition, the AGL parts operate with a core voltage varying from 1.2V to 1.5 V, on the contrary of the A3P product is designed to operate only at 1.5V.

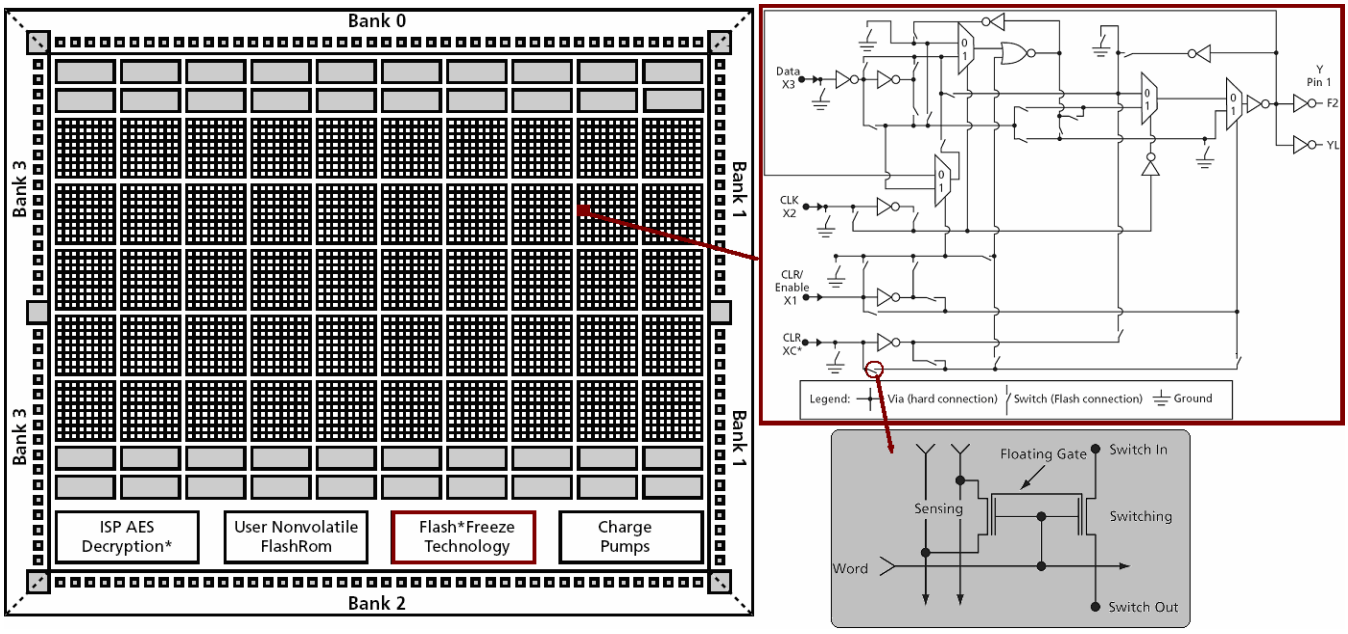

Fig. 1: ProASIC3 FPGA Core, VersaTile (Logic Tile) and Flash-Based Switch

B. Test Designs

ProASIC3: To correlate the previous HI beam results performed on the A3P250-PQ208 at Lawrence Berkeley National Laboratories (LBNL) on 2006 and 2007, and those that are obtained from FI tests, the exact same test design described in [1] and shown in Fig. 2, was selected for this new study. This design is a set of 12 sub-designs, which are a non-mitigated sub-design, and eleven mitigated sub-designs. Each one of them consists of 486 connected LCIs in series w/o SET filter at its output to an SET detection circuit (three latches). So, except for sub-design (1), which measures the SET cross-section per LCI, a sub-design (i) allows filtering of SETs that are shorter than (i-1) ns. More details about the used SET

filter could be found in [1]. In the following and for clarity purposes, each sub-design (i) is also called Chi.

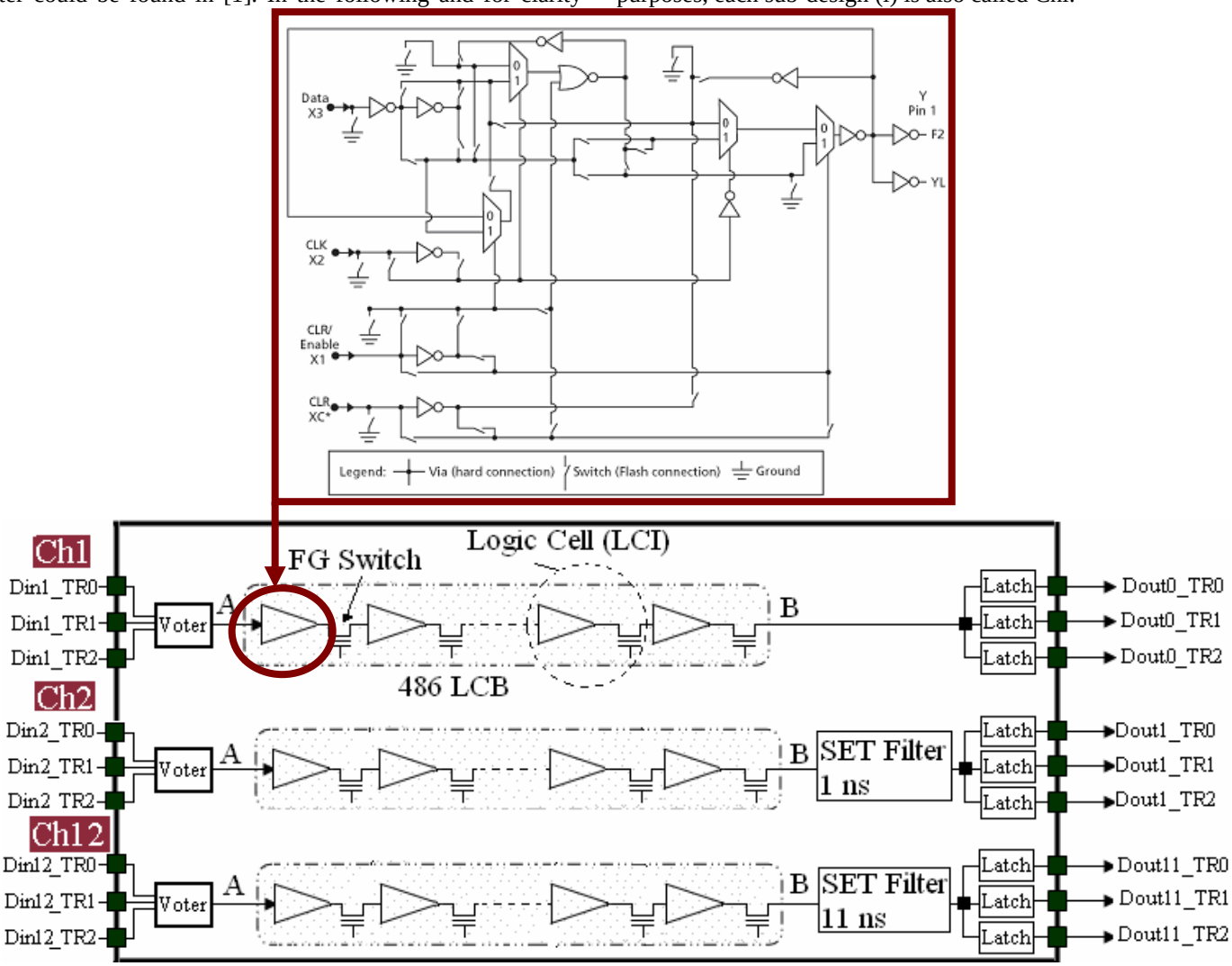

Fig. 2: Non-Mitigated and Mitigated Test Designs with Various SET Filters

In addition, all LCIs in each LCI-string were placed as close as possible to each other thereby minimizing routing structures so that each one will have identical SET cross-sections. This design uses also 100 % of the FPGA LCs in order to not miss Multiple Bit Upsets. All sets of inverters implemented in this test design are very different from the chain of inverters that have been tested in [8]. Indeed, as shown in Fig. 2 and mentioned above, each LCI is a set of CMOS logic and FG routing switches, combined to create the inverter function, in addition to the routing structures to link two LCIs. In contrast, the test structure of [8] is a set of inverters, with no additional routing or other CMOS logic gates included.

In addition, although this test design was very carefully placed and routed so most of the routing structures are minimized to the fewest tracks and two FG switches at most, both of the tested circuits (this test design and the chain of inverters used in [8]) should lead to very different pulse width measurements. Because of the internal setup time for an A3P logic tile, all SET-PW that are shorter than 550 ps won't be propagated, while for the ASIC test structure, even at the same technology node (0.13-µm in this case), all of the SET that are wider than the ASIC internal setup time (around the tens of ps) will certainly propagate. Therefore, one SET cross-section on an ASIC or an ASSP should certainly be higher than for FPGAs.

IGLOO: The same test design was implemented on the IGLOO AGL600-FG484 part, except that the number of LCIs has been increased from 486 to 1350, so most of the FPGA logic tiles are used and randomly placed and routed by the ACTEL Designer software tool. Therefore, the main assumptions mentioned in section I for keeping the SET-PW identical from the first LCI till the last one in a given chain, such as the very close placement of all the LCIs to each other to minimize the number of the routing FG switches and the careful timing analysis so SET would not change their waveforms from one LCI to another, were not kept. This should allow us to see the impact of the placement and the

routing of a given design on the SET propagation. The beam test experiments have been performed at LBNL on August 2007 [11].

C. Beam Test Results

Previous HI beam test results performed on the A3P FPGA (provided in Fig. 3), showed that all SET were filtered starting from Ch5, which means that the maximum SET-PW is between 3 and 4 ns. In addition, data on Ch4 showed that all SET occurring on an LCI or a routing structure, are shorter than 3 ns for LET > 43 MeV-cm^2/mg. However, although both of the A3P and the AGL parts have given similar SET cross-sections, as shown in Fig. 4, the AGL part exhibits very wide SET pulse widths. In the AGL test case, errors were observed from Ch1 to Ch9, which is mitigated with an SET filter of 9 ns. This means that SET-PW of 9 ns have occurred on the AGL FPGA, which is very unexpected or that the initial SET-pulse caused by the HI hit was widened and did not propagate uniformly in the FPGA design, which is more logical.

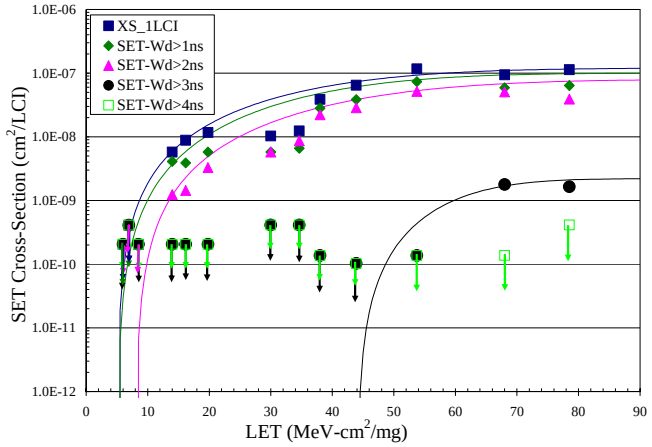

Fig. 3: A3P SET Cross-Sections for Non-Mitigated and Mitigated Test Designs (Arrows indicate that no errors were observed at the tested fluence)

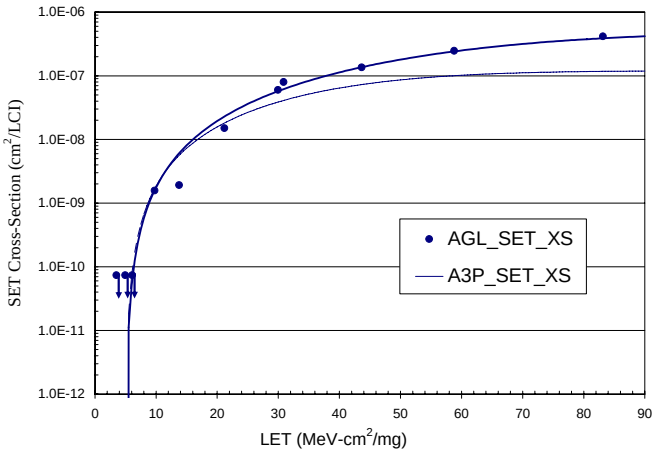

Fig. 4: A3P and AGL SET Cross-Sections

Hence, the first main idea of this paper is to trace by means of fault injection the SET propagation in each LCI-string and to make certain that no SET pulse-width change from one LCI to another has occurred. Two major types of SET FI approaches by simulation and by means of ad-hoc FI tests on the part are proposed and discussed. FI data will be compared to the beam results.

III. Proposed Fault Injection Test Approaches

A. SET FI by Simulation

FI techniques based on timing simulation of the design's gate description file known as *netlist* or spice modeling can provide us with a good understanding of the SET propagation in the FPGA core. Their predictions are still within ±5% from the real silicon case, due to the temperature, supply voltages, process variations in the FPGA product itself. SET-FI by means of simulation tools should then allow a direct relationship between the SET signal propagation and the specific FPGA-design's implementation.

In addition, it has the advantage of simplicity and the possibility of fault-simulation in any part of the design without modification of the beam test design, as well as immediate localization of the LC or routing structure causing the change of the SET-PWs. This SET simulation method could also be performed without the need for additional ad-hoc test setup and with available software simulation tools. Note that temperature and voltage variation effects on the SET-PWs as shown in [9] are not considered in this paper but could be taken in account when FI is implemented on the silicon.

Fig. 5 shows the block diagram of the FI experiments performed by simulation. An SET injected at the IO pads (Din pins) will be called external fault injection. SET injected at the insertion point A (Pt. A), after the IO voters for each channel will be called internal FI. During these experiments, there are two main observation points: Pt. A if the SET was injected on the IO pads and Pt. B if the SET was inserted at Pt. A. Note that many insertion points could be added in the design to run fault injection tests with no hardware overhead or any changes to the current timing specifications.

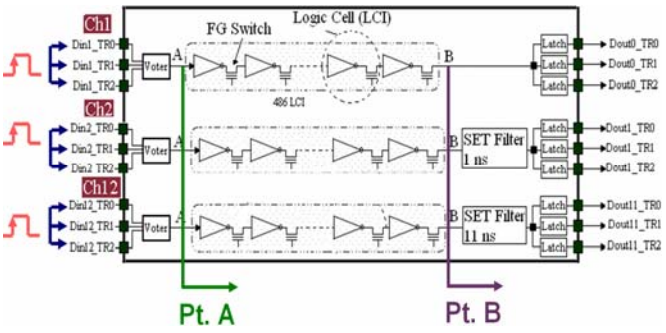

Fig. 5: Block Diagram of the Fault Injection Test Design (by simulation or on the silicon)

B. Ad-hoc FI Test Approaches

Novel ideas of ad-hoc SET FI experiments could be implemented internally or externally to the DUT. External SET-FI tests would involve sending short positive and negative pulses on each channel-input-pads or intermediate LCIs, by adding routing lines and multiplexers between the targeted LCs and additional input-pads. However, it would require detailed knowledge of the routed design and assumes that the SET-PW and shape would remain the same, from the input-pad to the targeted LCI.

This type of FI should take into consideration the SET signal-propagation between the input-buffers and the target LCI. But, to avoid distortion of SET shapes due to the input buffers or to termination resistors placed next to the DUT inputs, SETs could be injected internally. The SET FI core could be implemented in RTL and should occupy a few LCs where timing requirements could be fixed. This is known in ACTEL software routing and placement tools (LIBERO) as a "block". That block could be inserted anywhere and everywhere in the design while preserving its exact timing constraints. It is clear that this would require reduction of maximum design-sizes. Since our test design uses 100 % of the LCs, only external FI tests on the IO pads were considered in this paper.

Furthermore, laser FI could be a very good substitute to all FI techniques described above and particularly the ad-hoc SET FI, requiring absolutely no changes to the test designs and any part of the circuit. This was clearly demonstrated in [12]. However, FI tests performed on the designer's PC or in its laboratory offers certainly more flexibility and practicality to the experiment. In future work, we will attempt to obtain a correlation between the results of the above described SET-FI approaches and those obtained with laser FI experiments.

In the following, because of its simplicity and ease of use, only FI-based internal or external simulation will be used for the study of the SET propagation in the FPGA's design while the ad-hoc SET external FI will be used only for verification on the silicon.

IV. Routing Effects on the SET propagation

A. *Fault Injection on the Input Pads*

FI experiments based on simulation were performed using the *ModelSim* simulation tool from Mentor Graphics on each channel-input-pad, first with 3 ns positive SET pulses simulating the beam effects, and then with 3 ns negative SET pulses. The black line indicates the first SET-PW at the inputs of the 12 channels (the reference point). As shown in Fig. 6, positive SET pulses were always narrowed by 200 ps from each channel-input-pads till each inputs' voter (as shown in circles) and even narrower (with 200 to 2000 ps as shown in full circles) depending on the routing between the inputs' voter and a channel-LCI1 (point A in Fig. 1).

When injecting negative SET-pulses, the exact opposite case happened. SET-PWs were widened from each channel-input-pad till the voters' inputs (always with 200 ps as shown in triangles) and even wider (with 200 to 2000 ps as shown in full triangles) at the voters' outputs of each channel. This is a first observation of the SET transitions' effect on the SET signal propagation in the FPGA routing structures. We call that the *Butterfly* effect, due to its symmetry. Note that this does not contradict in any way the beam results since the test design was tested when the FPGA's inputs were grounded and all input buffers were tripled and voted and therefore their SET cross-sections were not considered in these calculations.

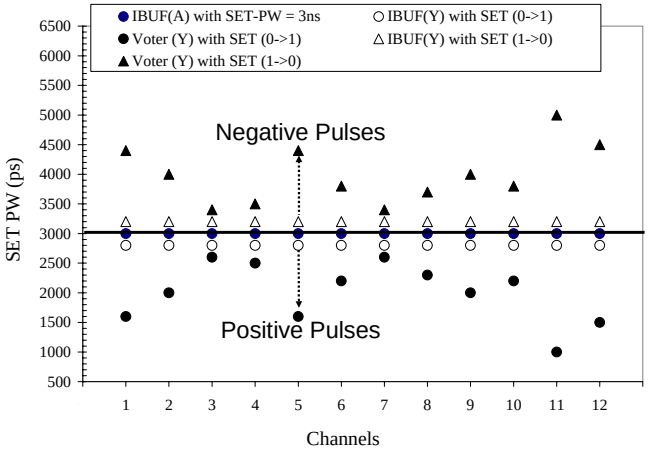

Fig. 6: Measured SET-PWs on Each Ch-Input-Voters (inputs and outputs) after Positive and Negative SET-FI

Furthermore, since each of the three utilized inputs for a given channel was placed on three separate IO banks, their routing lines were naturally very long and using more than one FG switch, buffers and multiplexers, etc. This long routing greatly affects the time-delay of the SET signal, its pulse width much less. The changes of SET-PWs, resulting from negative and positive SET pulse injections are both higher than 100 ps. In this case, they were mostly due to the voters, since each three input signals arrive to the voters at different times and might overlap or not, to create wider or shorter SET-PWs. This result justifies our choice of placing the SET detection circuit in the DUT itself rather than on the controller FPGA that counts the SETs, so they won't be filtered at the DUT outputs. In the remainder of this paper, all the SET-FI tests by simulation will be done on the inputs of the LCI1, to avoid the voters' impact on the SET-PWs.

B. *Fault Injection on the LCIs*

To avoid the variation of SET-PWs between the input-pads and the LCI1-inputs of each channel on the SET-PWs, SETs of 1, 2, and 3ns PWs were directly injected at the inputs of LCI1 of each channel. Except for channels 3 and 5, Fig. 7 shows that all SETs of 1 ns positive-PWs (circles) have been filtered in all channels after propagation through a certain number of LCIs (for instance after 15 LCIs for Ch1 and 76 for Ch2). The data shows also that among the three injected positive SET-PWs (1, 2 and 3 ns), only an SET of 3 ns-PW propagated to each LCI486 in each sub-design, as shown in full circles. For this reason and knowing that our first intention is to prove that SET as wide as 3 ns could occur in such a technology in HI beams, the remainder of this paper uses data from tests injecting mainly 3 ns SET-PWs.

The results given in Fig. 7 show that, although using the same number of LCIs in the 12 channels, the SET-PWs could get wider or shorter at the last inverter-output of a given chain. Indeed, the data point corresponding to Ch1 in Fig. 7 shows a widening of the SET-PW from 3 to 3.9 ns and suggests that an LCI SET cross-section could have been overestimated. But this is not true, because the latches in the SET detection circuit would have caught any SET wider than

the latch setup time (600 ps). Therefore, widening the SET PW from 3 to 3.9 ns does not really matter in this case.

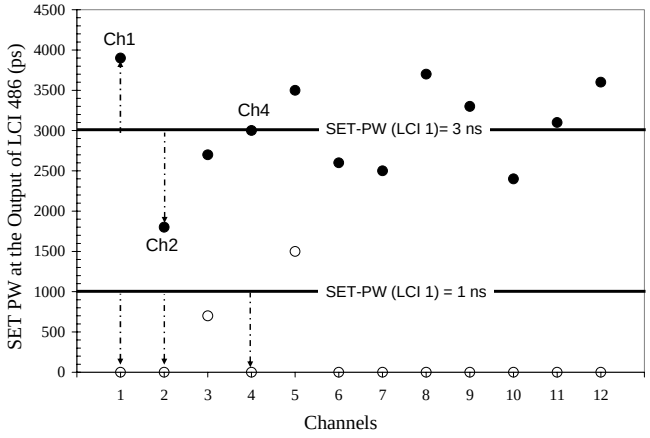

Fig. 7: Measured SET-PWs at LCI486 (pt. B) of each Channel after SET-FI of Positive PWs (1 and 3 ns) at LCI1

However, it will allow detection of narrower SET-PWs. In addition, the data point depicted in Fig. 7 as Ch4 corresponding to the most important channel in this study, shows at first impression, no distortion on the SET-PW and a first agreement with the HI beam results. However, it does not prove that an SET wider than 3 ns has occurred at LET > 43 MeV-cm^2/mg. In the following and to confirm such results, the SET propagation of the initial injected SET at the LCI-string-input will be traced and measured at each LCI-output of the three channels (Ch1, Ch2, and Ch4). The obtained results are shown in Fig. 8. For clarity purposes, the SET-PWs in this figure are shown only for LCI which ranks in the chain are multiples of ten (LCI10, LCI20, etc.).

Fig. 8 shows that the SET trajectory in Ch1 (depicted in triangles), where the SET-PW was the most widened, Ch2 (circles) where the SET-PW was the most narrowed and Ch4 (squares) where the SET pulses at the LCI1-input and LCI486-output had the same widths (3 ns).

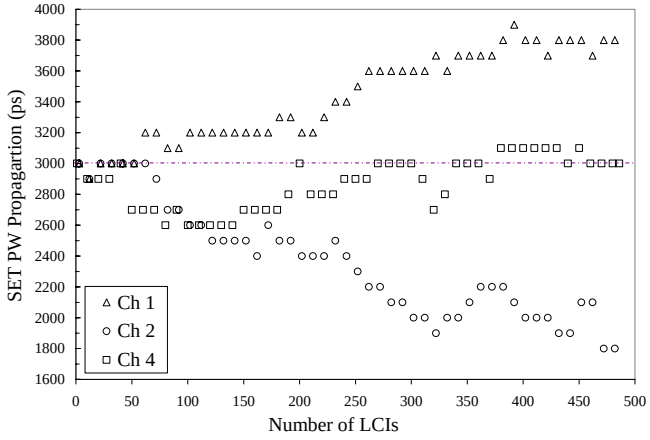

Fig. 8: SET Propagation in Sub-Designs 1, 2 and 4

Such data suggests that SET at least wider than 2.6 ns have most likely occurred at LET > 43 MeV-cm^2/mg for the SET detection of the Ch4 to trigger. Indeed, since the initial injected SET-PW in Ch4 was narrowed after 100 of LCIs from 3 to 2.6 ns, an SET of 3 ns PW injected at LCI100 could have been widened to 3.4 ns. This result is quite acceptable for such measurements, since a maximum SET pulse width of 2.6 or 3ns would probably result in the same delay element of the SET filter described in [1].

Furthermore, by looking carefully at the SET-PW distortion points for SET narrowing or widening, we've noticed that all SET filtering was of 100 ps (200 ps only on one net) and occurred only with negative SET-pulses while each SET pulse-widening was always of 100 ps and observed only with positive SET-pulses between two LCIs. Note that 100 ps was the *ModelSim* time resolution. On silicon or with spice simulation, this value could vary relatively to the 100 ps resolution time. To tackle the discrepancies between the different routing paths of each sub-design in filtering or widening the SET-PW, it is mandatory to first eliminate the compensation effects due to the LCIs. Therefore, in the following section, new configuration options are selected: Logic Cell-like Buffers (LCB) to eliminate the compensation effects due to the use of inverters, Logic Cell-like NOR (LCNO), and Logic Cell-like NAND gate (LCNA) to study the impact of the configuration of the logic tiles on the resulting SET-PWs.

V. Configuration Effects on the SET Propagation

A. Logic Tiles Configured as Buffers (LCBs)

To eliminate all compensation mechanisms due to opposite signal transitions, we have replaced all LCIs of the beam test design by Logic Cell-like Buffers (LCB), with absolutely no change to the design's routing or placement. Although such a design is unrealistic in flight applications, it should clarify if the SET-PW change is really dependant on its pulse transitions. And as expected, an SET injected on LCB1, with a 3 ns positive PW, was widened from 3 to 49.6 ns on each LCB486 of the 12 channels, with 100 ps almost after each LCB. On the contrary, with negative SET-PWs of 45 ns at each LCB1 of each of the 12 sub-designs, all SET did not propagate to any LCB486. These results prove again the *Butterfly* effect.

To explain the dependence of the SET propagation on the SET pulse polarity, spice simulations allowing a better correlation with the silicon (±2% compared to ±5% previously) have been performed on the same LCI test design. Because of the huge number of nets between the LCIs (over 10,000), spice simulations were performed only on nets where a modification of the SET-PWs was previously observed with timing simulations. The obtained results confirmed the previous statements showing the relationship between the resulting SET-PWs and the polarity of the injected SET pulse. Indeed, each SET-PW was increased at each inverter with 30 to 100 ps if the SET-PW was positive and vice-versa. Fig. 10 depicts the signal propagation between each two inverters and routing structures, including at least a FG switch (Fig. 9). Knowing that the P transistor is faster than the N transistor in the A3P FPGA family, the rising time is always less than the

falling time. Hence, a positive pulse is always widened while a negative pulse is always narrowed.

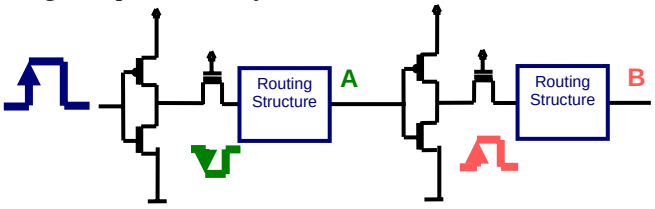

Fig. 9: Test Design Simulated by Spice Simulation

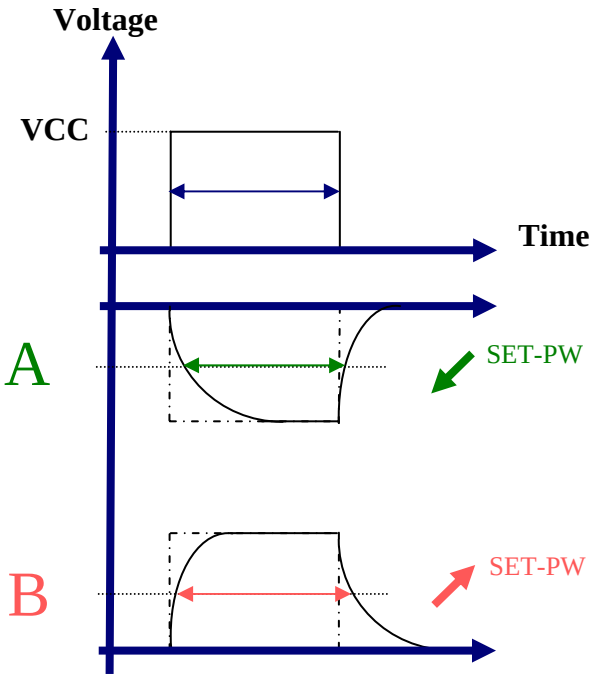

Fig. 10: Basic Mechanism of SET Propagation in an Inverter

If there is no silicon variation and no routing was involved between the two LCIs (as in the case of ASICs), or the exact routing is included between the two LCIs, there should be a perfect compensation between the rising and falling times, to propagate always the same SET-PWs at the output of each pair of LCIs. However, because of the silicon and routing variations, this is not always the case and leads frequently to different pulse widths at the output of a chain. Clearly, timing analysis is a requirement prior to any SET characterization that desires to measure correctly the maximum SET pulse width as well as the SET cross-section in the FPGA. Note that the probability of widening or shortening an SET-PW should always be equivalent. In addition, because of the small number of the logic gates inserted usually between each two sequential gates, the SET broadening phenomenon should not be very high. On the other hand, if the number of combinational gates is increased, the frequency of the design is reduced and therefore the probability of catching the SET is lowered.

For designs that highly favor many consecutive positive transitions when an SET must occur (although unlikely), SET mitigation solutions based on its filtering will not be advised and a TMR implementation would be more appropriate. However, most designs are exercised by approximately equal numbers of negative and positive signal-transitions; otherwise, they would have been optimized by software synthesis tools and include sequential elements that should stop any major change on the signal-PWs.

Although timing and spice simulations provided a good prediction and understanding of the silicon response to SET, ad-hoc SET FI are desired since they use the DUT itself. For verification on the silicon, external FI tests on the design's inputs were implemented with three different PWs (6, 20 and 100 ns). All injected positive and negative SETs were observed at all the outputs of the 12 LCI-strings (Pt. B of Fig.1), with almost the same injected SET-PWs. However, all SET-PWs have changed at all of the LCB-string-outputs. Indeed, all positive SET pulses in the buffer-strings were widened by approximately 45 ns except for the 100 ns negative SET-pulses which have been filtered by approximately 45 ns. All (6 and 20 ns) negative SET pulses were not detected at the outputs of all the LCB-strings. This confirms the previous FI results based on simulation and proves the effects of negative/positive SET pulses, the routing structures, the LC-configuration on the SET propagation in the FPGA core.

Note that these external FI-experiments were performed on a single A3P board, using a pulse generator to inject SETs (limiting the SET-PWs to 6 ns) and a scope to view the outputs of the LCI and LCB-strings, similar to what has been presented in [12]. This explains why our measurements were not as accurate, which justifies the need for internal FI tests or better instrumentation tools. More data with automated internal and external FI tests, using the beam test setup will be given in future publications.

B. Other LC- Configurations (OR3 and AND3 Gates)

The logic tiles configured as inverters (LCIs) were very convenient for the SET pulse widths and cross-section measurements in an A3P part, while the buffer-cells (LCBs) were useful for the understanding of the SET propagation in a given design. However, both the LCI and the LCB are using the smallest area of a given logic tile, which could lead to an under-estimation of the SET cross-section or the maximum SET-PW. To simulate SET effects on a Logic Tile at its maximum allowed usage when still configured as a combinational gate, two additional LC-configurations have been selected: NOR3, and NAND3 gates, where the input signal is connected simply to one input signal of the LCNO3 (NOR3) or LCNA3 (NAND3) gate and their two other inputs grounded, as shown in Fig. 11.

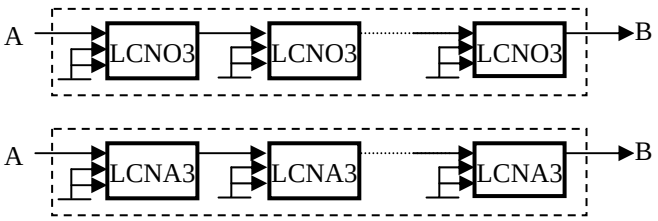

Fig. 11: LC-Configuration Impact on the SET Propagation

Results showed that both the LCNO3 and the LCNA3 have a filtering effect on the SET-PW. First, because of a logic tile (Fig. 2) intrinsic capacitances and the additional number of CMOS gates that are used to code a NAND3 or NOR3 gates, both of the gates had an internal setup time higher than the one needed for the LCI or the LCB. Therefore, all SET-PWs that are shorter than 1 ns are filtered and not seen at Pt. B. Second, because of the architectural implementation of the LCNO3 or the LCNA3 on an LC, none of the injected SET having a PW shorter than 3.5 ns propagated to Pt. B (LCNA3 [486] or LCNO3 [486]).

It should be mentioned though that this is somewhat dependent on the specific routing of this design, which is exactly the same as for the LCI and LCB, so a relative comparison could still be done. Furthermore, the high number of used LCs in this design is not a realistic case and was previously used to demonstrate the concept. Although SET pulses shorter than 3.5 ns were filtered, it should not be considered as a definitive major advantage for this architecture. Indeed, by tracing the data-path of the SET at the LC-outputs, all SET that are wider than 1 ns did propagate at least to the first 20 logic tiles, which is usually the number of LCs inserted between two sequential memory cells.

This shows clearly that SETs propagate differently in designs with different routing and logic-configurations. LC-configurations other than LCI, such as LCNA3 and LCNO3, showed lower susceptibility to the increase of the SET propagation because of the logic tiles' setup time. Other configurations will be studied to find the worst case to favor SET broadening. These results show the importance of differentiation between two SET phenomenons: the measurement of SET-PWs per LC and the smallest routing structure, and the SET propagation dependant on the FPGA design's implementation. The former is mainly related to the device technology while the latter is dependant on the FPGA architecture and layout.

In summary, these findings highlight the filtering effects of this unique architecture and the high potential for this part and such type of architecture to naturally filter SET due to the high number of capacitances and the routing lines acting as resistors placed in and between the logic tiles, acting globally as RC filters. If a smart place and route tool is implemented to favor the SET filtering based simply on the architectural knowledge of this circuit and thorough timing analysis, complete SET mitigation could be achieved with no hardware overhead and consequently with minimal time penalty. More research studies are in process to verify this novel SET mitigation solution and explore this advantage for the designer. These studies can only be done with the precise knowledge of the routing (design's netlist) and the physical parameters of the routing structures (capacitances, resistors, etc.) from the vendor, since the physical placement and the logical view provided from the ACTEL software tools (Designer) are very different. Being able to precisely estimate the SET propagation in a given design requires good knowledge of this physical placement, where the software tool can be modified to allow SET filtering. Such SET filtering techniques will be tested and validated on Flash and Antifuse based FPGAs and the resulting data should be available in future publications.

VI. Conclusion

Studies of the SET Propagation in Flash-based FPGAs showed a clear dependence of the SET-PW on the FPGA design's routing and configuration as well as the SET polarity. These analyses were based on fault injection data compared to previous and new heavy-ion beam test results presented in [1] and performed at LBNL on two 0.13-µm Flash-Based FPGAs (ProASIC3 and IGLOO). The obtained results confirmed the previously obtained radiation test results in [1] concerning the maximum SET-PW detected but raised new questions of worst case designs for SET-PW broadening due to the FPGA design's implementation in terms of its LCs' configuration or utilized routing structures. Additional test cases varying LC-configuration from inverters to buffers were tested and the results provided explanations of these findings at the device level. The data showed that the variation of the SET-PW is related to the basic mechanism of signal propagation in the P and N transistors.

This work showed also that SET-FI tests based on simulation should be performed prior to any radiation test experiments that utilize long LCI-strings for SET characterization so to maintain the SET-PW. Each SET-PW should be checked at the output of each pair of LCIs. Otherwise the SET-PW will be random as was observed in the case of the AGL test design using random routing compared to the deterministic routing where each LCI is placed very close to the next LCI, with minimum routing in between. Furthermore, FI tests and careful timing simulations were proven be very helpful for the evaluation of SET mitigation solutions based on its filtering to locate the worst case of SET propagation in the FPGA.

This paper shows clearly that SET propagation in all new highly-scaled technologies such as in the non-volatile circuits (ASIC, Flash-based FPGAs, etc.) or in the volatile circuits (SRAM-Based FPGAs, etc.), should be carefully studied. Finally, by being a non-volatile reprogrammable ASIC, the Flash-based FPGA constitutes a good vehicle for the test of these state-of-the-art fault-tolerant techniques. It should be reminded that all testing was done on commercial parts and that flight parts are to be marketed in 2009.

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