RT54SX72SU Heavy Ion Beam Test Report

August 6, 2004

J.J. Wang
(650) 318-4576
jih-jong.wang@actel.com

SUMMARY

RT54SX72SU from UMC foundry is heavy-ion-beam tested for single event effects (SEE) at Brookhaven National Lab. The test team is a joint force of NASA/Goddard and Actel; NASA provides the testing design, and Actel prepares the devices. The major results include:

- The triple-module-redundant (TMR) hardened register cell shows high tolerance to single event upset (SEU). The SEU rate for the benchmark environment, GEO at solar minimum, meets the target (< 10^{-10} upsets/bit-day) with a comfortable margin. Also, no clock upset or any single event functional interrupt (SEFI) are observed.
- The measured SEUs are most likely due to single event transient (SET) induced upsets because the measured SEUs at a low clock frequency (0.5 MHz) are much less than SEUs at a high clock frequency (10 MHz). For contrast, the SEU rate at GEO MIN for 0.5 MHz clock is below 2.2×10^{-14} upsets per bit-day and the SEU rate for 10 MHz clock is 3.9×10^{-12} upsets per bit-day.
- Single event latch-up (SEL) is not detected in any run; the maximum LET (linear energy transfer) used in this report is 104 MeV•cm^2/mg.
- Single event dielectric rupture (SEDR) is observed in two out of three samples; it occurs when power supply is at 10% over-voltage and for ions with high LET, between 37.5 and 59.7 MeV•cm^2/mg. For power supply at 10% under-voltage, the SEDR cannot be detected for LET up to 59.7 MeV•cm^2/mg.

I. TEST OBJECTIVES

The general objective is to investigate the single event effects (SEE) of the RT54SX72SU device. For the hardened register cell (a flip-flop) in this device, the single event upset (SEU) cross-section as a function of LET needs to be acquired to predict the SEU rate in space environments. The device susceptibility of single event latch-up (SEL) and single event dielectric rupture (SEDR) are also measured.

II. DEVICE UNDER TEST

Table 1 lists the information about devices under test (DUT).

Table 1. DUT Information

Device	RT54SX72SU
Package	PQ256
Foundry	UMC
Technology	0.22 µm CMOS
Die Size	7.67 mm x 14.2 mm
Die Lot Number	D0Y311
Quantity Tested	3
Serial Number	LAN7001, LAN7002, LAN7003
IO Configuration	3.3V PCI
Design	TMRSXS

II. TEST METHODS

This test generally follows the guidelines in two SEE testing standards: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

A. *Heavy Ion Beam Source*

The testing uses the heavy ion beam of Tandem Van de Graaff SEU facility located at Brookhaven National Laboratory. Table 2 shows irradiation details for each run.

B. *Test Logic Design*

The logic design, called TMRSXS, has four 100-bit (flip-flops) shift registers: SOFTA, SOFT, HARDA and HARD, which are clocked by a common clock. Each bit in SOFTA is a D flip-flop constructed by a register cell. A buffer separates each bit. Because this buffer has only one fan-out, it permits the fastest type of connection, called a Direct-Connect. DOC is the output of SOFTA. SOFT is identical to SOFTA except that there are no buffers between the bits, so there are no Direct-Connects. DOS is the output of SOFT.

Each bit in HARDA is triple module redundant (TMR) hardened at the user-level. Note that the user-level TMR is different from the hard-wired TMR, which is transparently designed in each register cell. Each user-level TMR bit consists of three flip-flops and two multiplexes and an inverter. The first multiplex functions as a majority voter. The second multiplex and the inverter function as a disagreement detector. The outputs of all disagreement detectors in the register are logically inputting to an OR gate. To detect SET, an extra buffer and inverter are added to the "clear" and "preset" pins of each user-level TMR bit. Any ion strike on either the invert or the buffer will potentially upset the three flip-flops simultaneously. DOVH is the output of HARDA, and the output of the OR gate connected to all the disagreement detectors is 0_ERR. HARD is similar to HARDA except that there is no additional SET detecting buffer or inverter in each user-level TMR bit. DOH is the output of HARD, and the output of the OR gate connected to disagreement detectors is 1_ERR.

C. *Experimental Setup*

A PC is used as the command-control console to automate the testing. GUI software commands the communications between an I/O-counter board residing in the PC and the DUT board. The I/O-counter board can

send and receive signals to and from the DUT for error counting and parameters monitoring. There is also a control chip on the DUT board for data processing. RS422 interfaces are used for inter-board communication to achieve good signal integrity for long cables.

Figure 1 shows a conceptual block diagram illustrating the SEU-error counting mechanism. A data pattern generated by a data-generator module in the I/O-counter passes through the DUT shift register (SR) and compares with the same data pattern passed through a control path. Since the irradiation only occurs on the DUT chip, SEUs will produce pulses at the output of the comparator. These pulses are received by the I/O-counter and counted as SEU errors. Notice that outputs 0_ERR and 1_ERR don't need the comparator to generate SEU errors, and these two outputs directly feed into counters on the I/O-counter board. TMRSXS design uses six counters for DUT outputs DOC, DOS, DOH, DOVH, 0_ERR and 1_ERR.

Monitoring both the power supply currents I_{CCI} and I_{CCA} and the device functionality is the method to detect the SEL and SEDR. SEL causes losing functionality and latching I_{CC} to a high state, usually of few hundred milliamps; if the device doesn't stay at latch-up state long enough to cause permanent damage, recycling power can recover the device to the normal state. In a test run of total fluence of 1 x 10^7 Ions/cm^2, SEDR usually only ruptures few antifuses, and subsequently causes I_{CCA} permanently jumping few milliamps for each antifuse rupture; the device functionality is usually not disturbed.

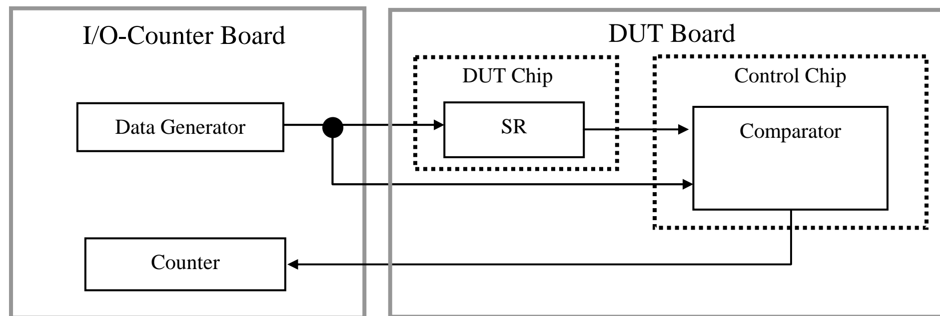

Figure 1 Block diagram showing the mechanism for SEU-error counting

III. TEST RESULTS AND DISCUSSIONS

A. *Test Data*

Table 2 shows the test data; key remarks and results are:

1. All runs are conducted at room temperature.
2. 10% de-rating of the nominal power supply, i.e. V_{CCI}/V_{CCA} = 4.5/2.25 V, is used for the worst-case scenario SEU measurement; 10% over-rating the nominal power supply, i.e. V_{CCI}/V_{CCA} = 5.5/2.75 V, is used for the worst-case scenario SEL and SEDR detections.
3. Figure 2 shows the importance of the board orientation; it also shows the relative orientation of the board and the hard-wired TMR flip-flop, which has three sub-flip-flops, ff1, ff2 and ff3. Only when two or more of the sub-flip-flops suffer upsets simultaneously due to an ion strike, the TMR flip-flop can have an upset. Thus the orientation of 0°-roll with a tilt gives the TMR flip-flop more susceptible to SEU than does the orientation of ±90°-roll with the same tilt. However, the data in Table 2 shows that the SEU-errors are relatively independent of the roll angles. This insensitivity to the board orientation can be explained by the wide separation of the sub-flip-flops. Three dimensional mixed mode simulation demonstrated that even at ±90°-roll and 60°-tilt orientation, a single heavy ion with LET of 100 MeV•cm^2/mg cannot upset the TMR flip-flop

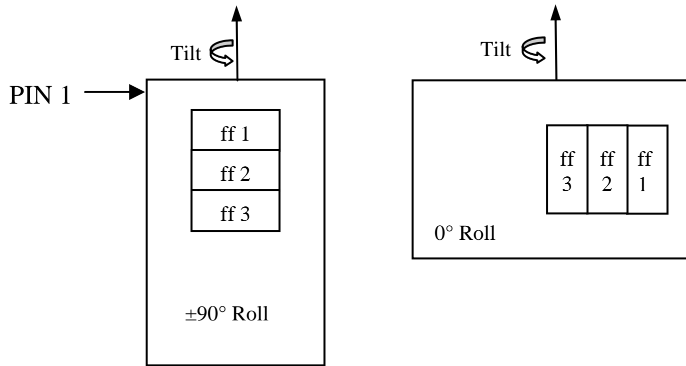

Figure 2 Relative orientations of the hard-wired TMR flip-flop and the DUT board.

4. DOVH and DOH show no SEU errors even for 10 MHz clock while DOS and DOC show noise level SEU errors for 0.5 MHz clock and observable SEU errors for 10 MHz. This indicates the SET detecting buffers and inverters in DOVH are not susceptible to ion strikes even with the high LET used in this test, and also that the SEU-errors in DOS and DOC are due to the SET inside the hard-wired TMR flip-flop.
5. There are very few SEU errors in 1_ERR and 0_ERR, even for 10 MHz clock.
6. Clock upset or SEFI (single event functional interrupt) is not observed.
7. SEL is not detected in any run.
8. SEDRs are observed in two of the three DUTs biased at the worst-case scenario. No SEDR occurs for any DUT biased at V_{CCI}/V_{CCA} = 4.5/2.25 V. High angle tilt is worse than zero tilt; DUT7001 shows SEDR at 55° tilt but not at 0° tilt. The reason is that the antifuse dielectric is not uniformly parallel to the surface; the antifuse dielectric is sloped to the surface at the two sides. When an SEDR occurs, the tilted beam probably strikes one side of the antifuse dielectric so that the beam is near perpendicular to the side surface. Nevertheless, the device after several SEDR functions as normal. Each SEDR is accompanied by an permanent ICCA increase of few milliamps.

Table 2 Test Data

BNL Run	DUT	Bias (V) V_{CCI}/V_{CCA}	Ion	LET MeV-cm²/mg	Tilt Deg	Roll Deg	Flux Ions/cm²/sec	Fluence Ions/cm²	Upsets						Data Pattern	Clock Freq	Comments
									1_Err	DOC	DOVH	DOS	DOH	0_Err			
851	LAN7001	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	Zero	10M	
852	LAN7001	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	1	0	1	0	0	CB	10M	
853	LAN7001	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	1	0	2	0	0	CB	10M	
854	LAN7001	4.5/2.25	Br-81	43.3	30	0	1.00E+05	1.00E+07	0	1	0	2	0	0	CB	10M	
855	LAN7001	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	2	1	0	4	0	1	CB	10M	
856	LAN7001	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	1	0	2	0	0	CB	10M	
857	LAN7001	4.5/2.25	Br-81	43.3	30	-90	1.00E+05	1.00E+07	0	0	0	3	0	0	CB	10M	
858	LAN7001	4.5/2.25	Br-81	43.3	30	-90	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
859	LAN7001	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	0.5M	
860	LAN7001	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
861	LAN7001	4.5/2.25	Br-81	43.3	30	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
862	LAN7001	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
863	LAN7002	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	0	2	0	4	0	1	CB	10M	
864	LAN7002	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	0	0	0	2	0	0	CB	0.5M	
865	LAN7002	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	10M	
866	LAN7002	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	0	0	1	0	0	CB	0.5M	
867	LAN7002	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	3	0	2	0	0	CB	10M	
868	LAN7002	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
869	LAN7003	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	3	0	4	0	1	CB	10M	
870	LAN7003	4.5/2.25	Br-81	53	45	-90	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
871	LAN7003	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	0	0	0	2	0	3	CB	10M	
872	LAN7003	4.5/2.25	Br-81	53	45	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
873	LAN7003	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	0	0	1	0	0	CB	10M	
874	LAN7003	4.5/2.25	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
875	LAN7003	4.5/2.25	I-127	59.7	0	0	1.00E+05	1.00E+07	0	2	0	2	0	2	CB	10M	
876	LAN7003	4.5/2.25	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
877	LAN7003	4.5/2.25	I-127	104	55	0	1.00E+05	1.00E+07	0	1	0	0	0	2	CB	10M	
878	LAN7003	4.5/2.25	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
879	LAN7003	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	1	0	0	CB	10M	SEDR
880	LAN7003	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	1	0	1	0	0	CB	10M	SEDR
881	LAN7002	4.5/2.25	I-127	59.7	0	0	1.00E+05	1.00E+07	0	1	0	5	0	2	CB	10M	
882	LAN7002	4.5/2.25	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
883	LAN7002	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
884	LAN7002	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
885	LAN7002	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	10M	
886	LAN7002	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	3	0	1	0	0	CB	10M	
887	LAN7001	4.5/2.25	I-127	59.7	0	0	1.00E+05	1.00E+07	2	1	0	2	0	1	CB	10M	
888	LAN7001	5.0/2.50	I-127	59.7	0	0	1.00E+05	1.00E+07	0	3	0	0	0	0	CB	10M	
889	LAN7001	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	10M	
890	LAN7001	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	3	0	0	CB	10M	SEDR
891	LAN7001	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	SEDR
892	LAN7001	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	0.5M	
893	LAN7001	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	SEDR
894	LAN7001	5.5/2.75	I-127	104	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	SEDR
895	LAN7001	5.5/2.75	I-127	59.7	0	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
896	LAN7001	5.5/2.75	Br-81	65.4	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	0.5M	
897	LAN7001	5.5/2.75	Br-81	65.4	55	0	1.00E+05	1.00E+07	0	0	0	0	0	0	CB	10M	
898	LAN7001	5.5/2.75	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	10M	
899	LAN7003	5.5/2.75	Br-81	65.4	55	0	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	10M	
900	LAN7003	5.5/2.75	Br-81	37.5	0	0	1.00E+05	1.00E+07	0	1	0	0	0	0	CB	10M	

B. Single Event Upset

Figure 3 shows the cross-section per flip-flop with respect to LET. In this Figure, the data are derived from the DOS and DOC data in Table 2 that use the checkerboard pattern and the worst-case bias scenario, i.e. V_{CCI}/V_{CCA} = 4.5/2.25 V. As shown by the legend, the points are experimental data and curved lines are Weibull fits; each data point represents the average of the three DUTs. Clearly, the cross-section, or SEU-error, is strongly dependent on the clock frequency. SEU-errors for 10 MHz clock is about an order of magnitude higher than SEU-errors for 0.5 MHz. In fact, 0.5MHz data are practically in the noise level since a single error in each run can be just a noise due to accelerator operation. SpaceRad 4.5 simulator performs the SEU prediction by applying Weibull parameters to GEO solar-minimum environment with 100-mil Al shielding; the SEU rate is 3.93×10^{-12} upsets per bit-day for 10 MHz, and 2.2×10^{-14} upsets per bit-day for 0.5 MHz.

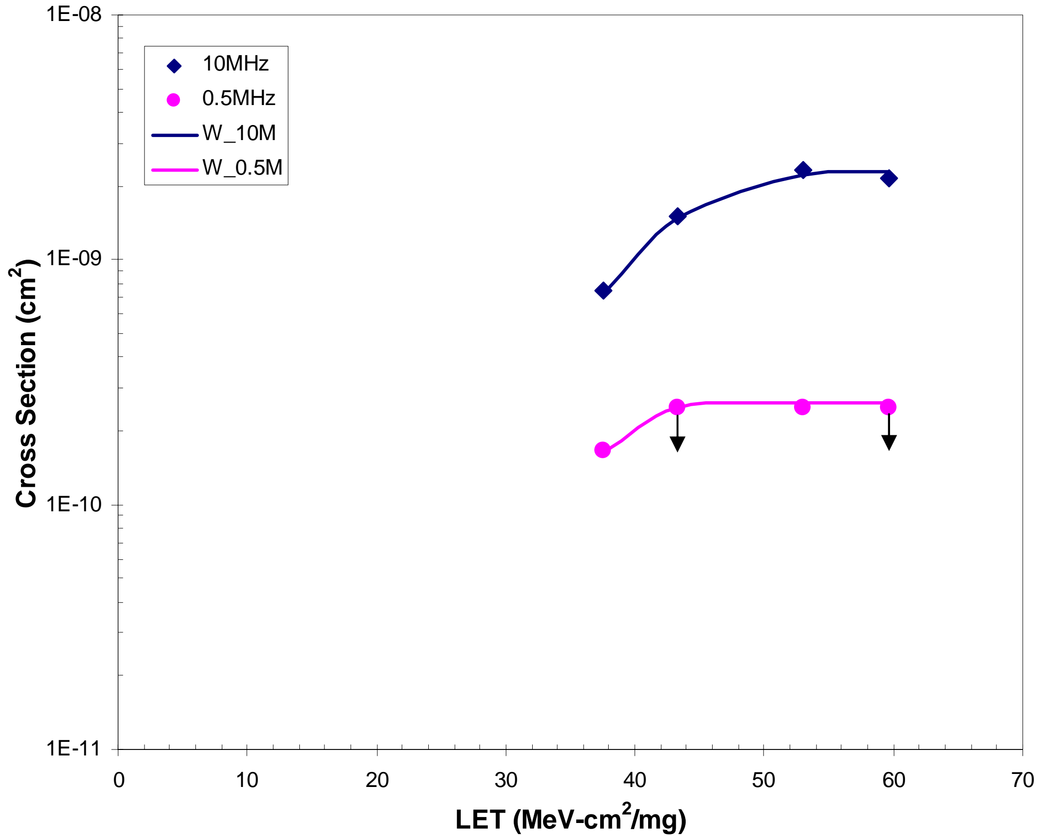

Figure 3 Cross section per register cell for 0.5MHz and 10MHz clock frequency. The points are average experimental data of three DUTs, and the curved lines are Weibull fits.