



RTSX72SU SEE Report–Analysis of NASA/Goddard High Speed SET/SEU Data

July 11, 2006

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Acknowledgements

The data in this report are collected by NASA/Goddard radiation group with some Actel engineering supports. Special thanks to the major contributors, Melanie Berg, Hak Kim, and Ray Ladbury.

I. SINGLE EVENT EFFECTS TESTING

A. Device Under Test

The devices-under-test (DUT) is the RTSX72SU device, a 0.22- μm antifuse FPGA manufactured by the UMC foundry. The lot number is D1JW01; this lot is manufactured using the revision-B mask-set.

B. Heavy Ion Beam Source

The heavy-ion-beam tests were performed at TAMU. Ion irradiations used effective LET of 20.2, 28.5, 40.4, 52.7 and 74.5 MeV $\cdot\text{cm}^2/\text{mg}$. For each run the effective fluence is $1 \times 10^7 \text{ cm}^{-2}$.

C. Test Logic Design and Data Pattern

The DUT design consists of six (6) identically designed shift registers called SR0 to SR5; each has 335 stages of D-flip-flops. Each D flip-flop is constructed from an R-cell. A global clock is shared by all the registers.

During testing, a checkerboard pattern clocked at 2, 50, or 100 MHz is running in the shift register under test.; the other five (5) registers are running a zero pattern.

D. Test Method and Procedure

The heavy-ion-irradiation-induced errors in the shift register under test are processed, counted and displayed. These raw data are processed and displayed as the typical cross-section versus effective LET plots in next section. Consult NASA/Goddard for the details of methodology and procedures.

II. RESULTS AND ANALYSES

A. Data and Weibull Fit

Fig. 1 to 5 displays the typical cross-section versus LET plot for SR0, SR1, SR2, SR3 and SR5 respectively; no data are obtained for SR4 due to hardware issues in that data-collection channel. Each plot has three (3) sets of data obtained at 2, 50 and 100 MHz respectively; each set of data is fitted by a Weibull function plotted as a continuous curve.

B. SEU Rate Prediction

CREME96 is used to perform the SEU rate prediction. The environment parameters are: GEO orbit, Solar Min, and 100-mil Al shielding. Two depths of the RPP are used; one is that $Z = 0.25 \mu\text{m}$ and Funnel = $0.5 \mu\text{m}$, and the other is that $Z = 1 \mu\text{m}$ and no funneling. The result of upsets per bit-day for each shift register running at a particular frequency is listed in the following tables.

Table 1 Predicted SEU rate using $Z = 0.25 \mu\text{m}$ and Funnel = $0.5 \mu\text{m}$

	2 MHz	50 MHz	100 MHz
SR0	6.17×10^{-12} upsets/bit/day	4.24×10^{-10} upsets/bit/day	1.18×10^{-9} upsets/bit/day
SR1	2.88×10^{-11} upsets/bit/day	7.18×10^{-10} upsets/bit/day	9.83×10^{-10} upsets/bit/day
SR2	3.62×10^{-11} upsets/bit/day	3.17×10^{-10} upsets/bit/day	1.22×10^{-9} upsets/bit/day
SR3	1.25×10^{-11} upsets/bit/day	4.58×10^{-10} upsets/bit/day	1.07×10^{-9} upsets/bit/day
SR5	1.25×10^{-11} upsets/bit/day	2.65×10^{-10} upsets/bit/day	1.18×10^{-9} upsets/bit/day

Table 2 Predicted SEU rate using $Z = 1 \mu\text{m}$ and Funnel = $0 \mu\text{m}$

	2 MHz	50 MHz	100 MHz
SR0	1.87×10^{-13} upsets/bit/day	4.36×10^{-10} upsets/bit/day	1.92×10^{-9} upsets/bit/day
SR1	2.70×10^{-13} upsets/bit/day	1.38×10^{-9} upsets/bit/day	2.41×10^{-9} upsets/bit/day
SR2	4.55×10^{-12} upsets/bit/day	2.86×10^{-10} upsets/bit/day	3.22×10^{-9} upsets/bit/day
SR3	5.83×10^{-13} upsets/bit/day	5.03×10^{-10} upsets/bit/day	2.64×10^{-9} upsets/bit/day
SR5	5.83×10^{-13} upsets/bit/day	2.35×10^{-10} upsets/bit/day	1.92×10^{-9} upsets/bit/day

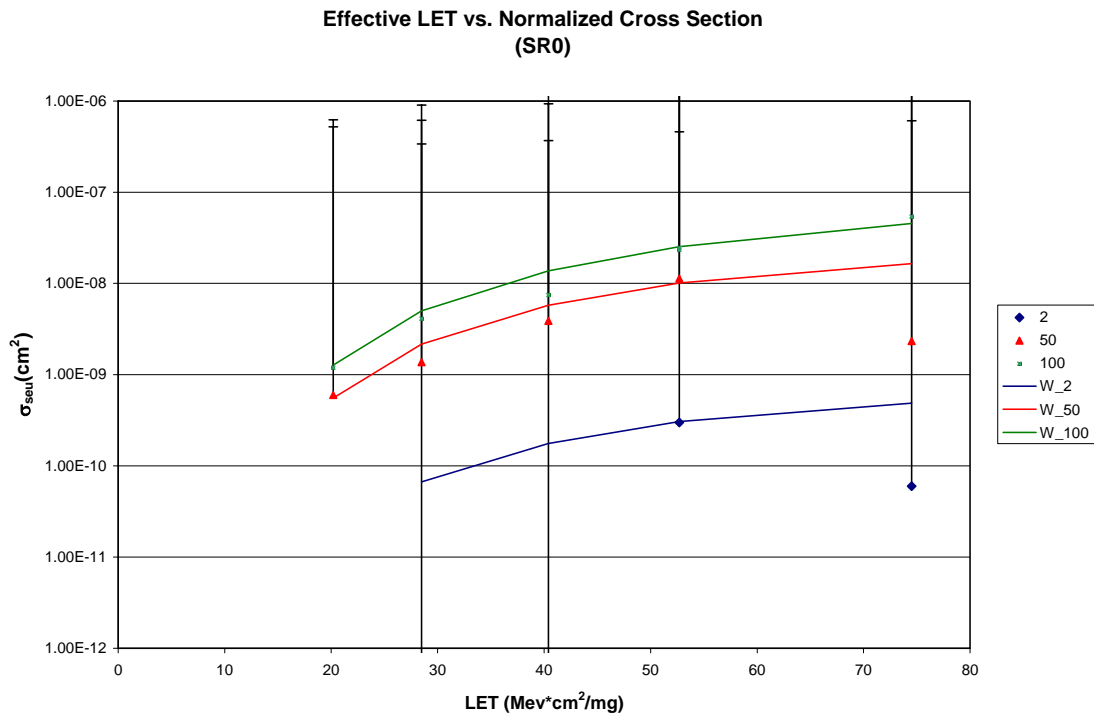


Fig. 1 Plot showing SEU cross section (σ_{SEU}) of SR0 versus effective LET for running a checkerboard pattern at 2, 50, and 100 MHz. Data points with error bars and Weibull-fitting curves are displayed.

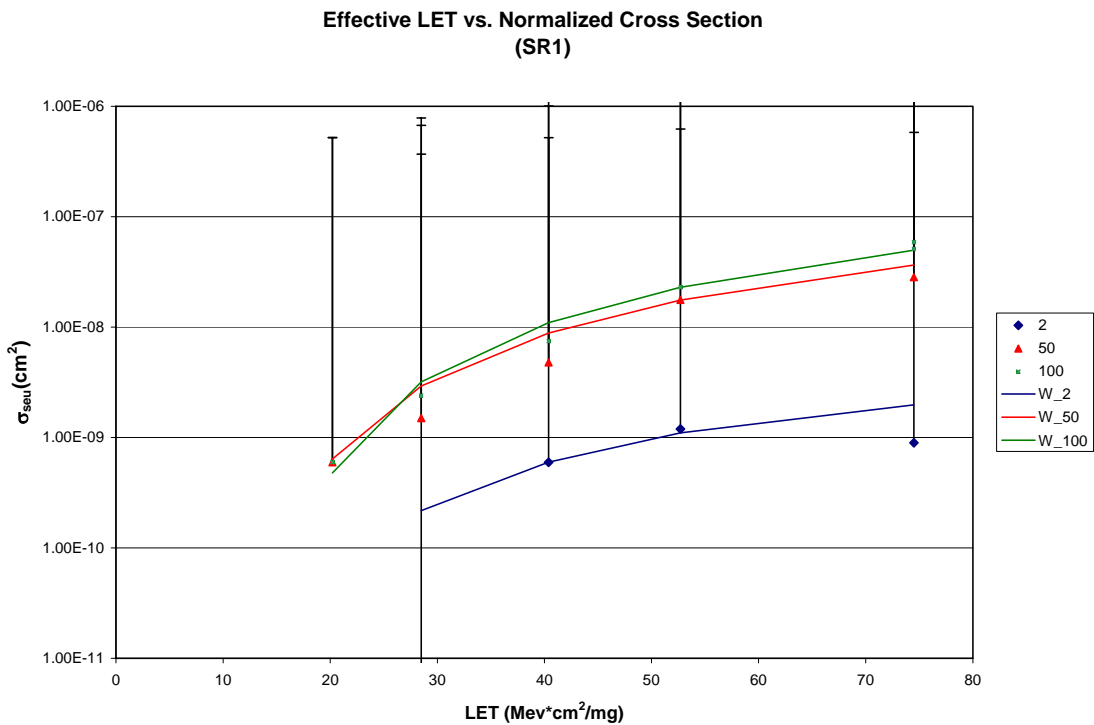


Fig. 2 Plot showing SEU cross section (σ_{SEU}) of SR1 versus effective LET for running a checkerboard pattern at 2, 50, and 100 MHz. Data points with error bars and Weibull-fitting curves are displayed.

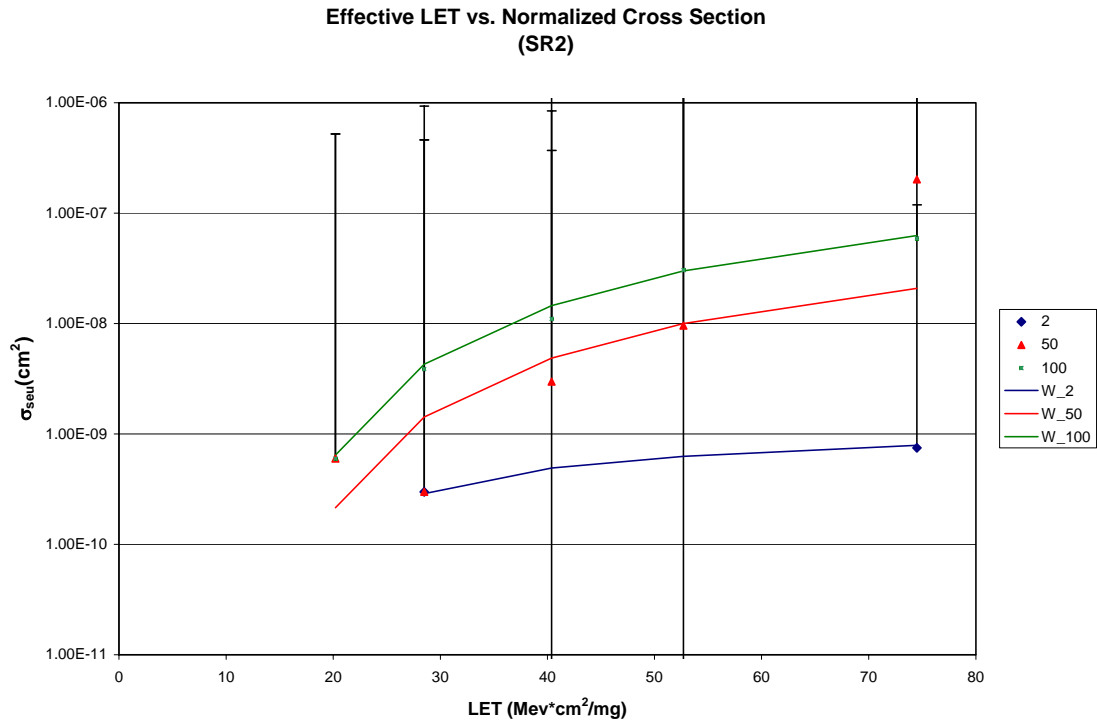


Fig. 3 Plot showing SEU cross section (σ_{SEU}) of SR2 versus effective LET for running a checkerboard pattern at 2, 50, and 100 MHz. Data points with error bars and Weibull-fitting curves are displayed.

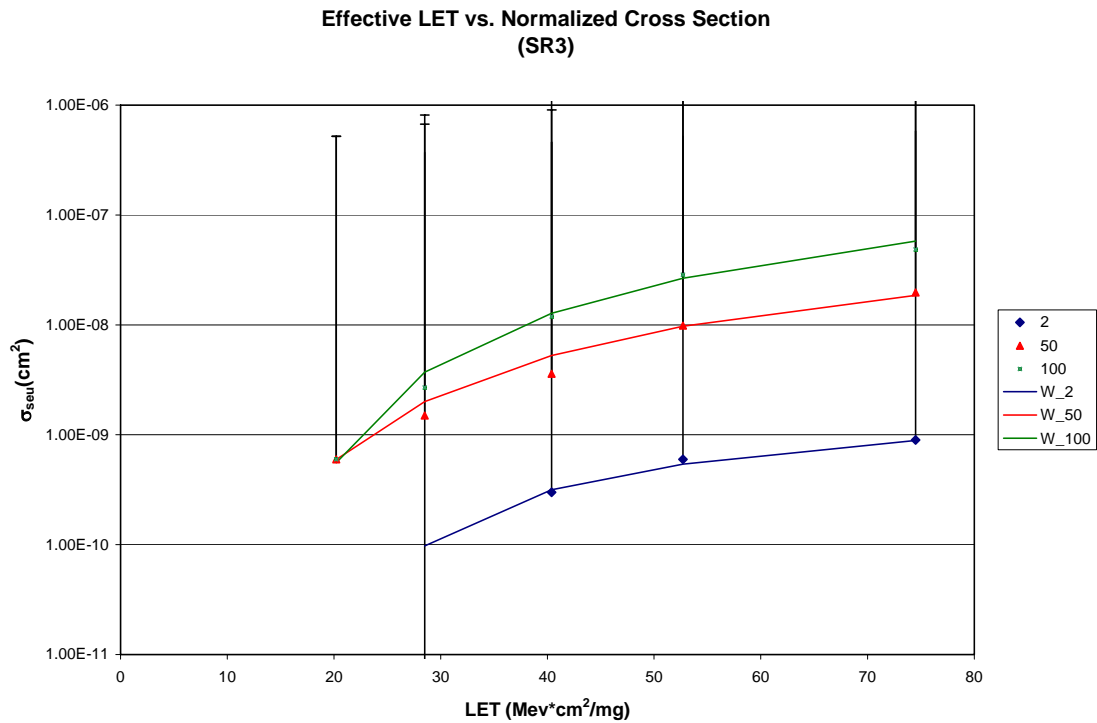


Fig. 4 Plot showing SEU cross section (σ_{SEU}) of SR3 versus effective LET for running a checkerboard pattern at 2, 50, and 100 MHz. Data points with error bars and Weibull-fitting curves are displayed.

Effective LET vs. Normalized Cross Section
(SR5)

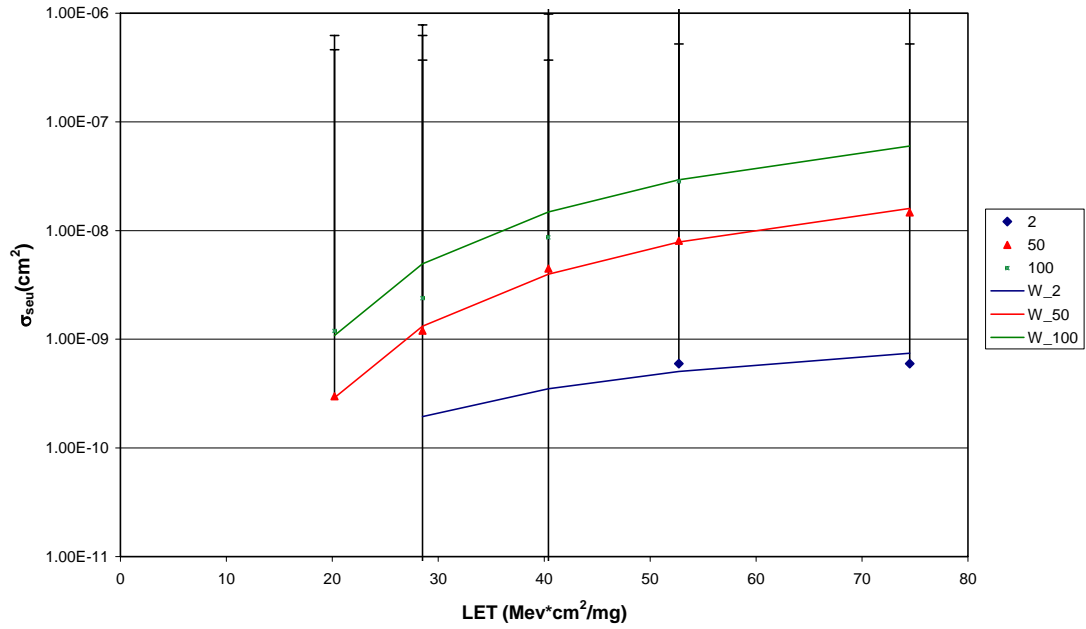


Fig. 5 Plot showing SEU cross section (σ_{SEU}) of SR5 versus effective LET for running a checkerboard pattern at 2, 50, and 100 MHz. Data points with error bars and Weibull-fitting curves are displayed.