TR0011
Test Report
Radiation-Tolerant ProASIC3 Single-Event Latch-Up

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

There are no changes to the technical content in revision 1.0 of this document.

1.2 Revision 0.0

Revision 0.0 was the first publication of this document.

2 Radiation-Tolerant ProASIC3 Single-Event Latch-Up

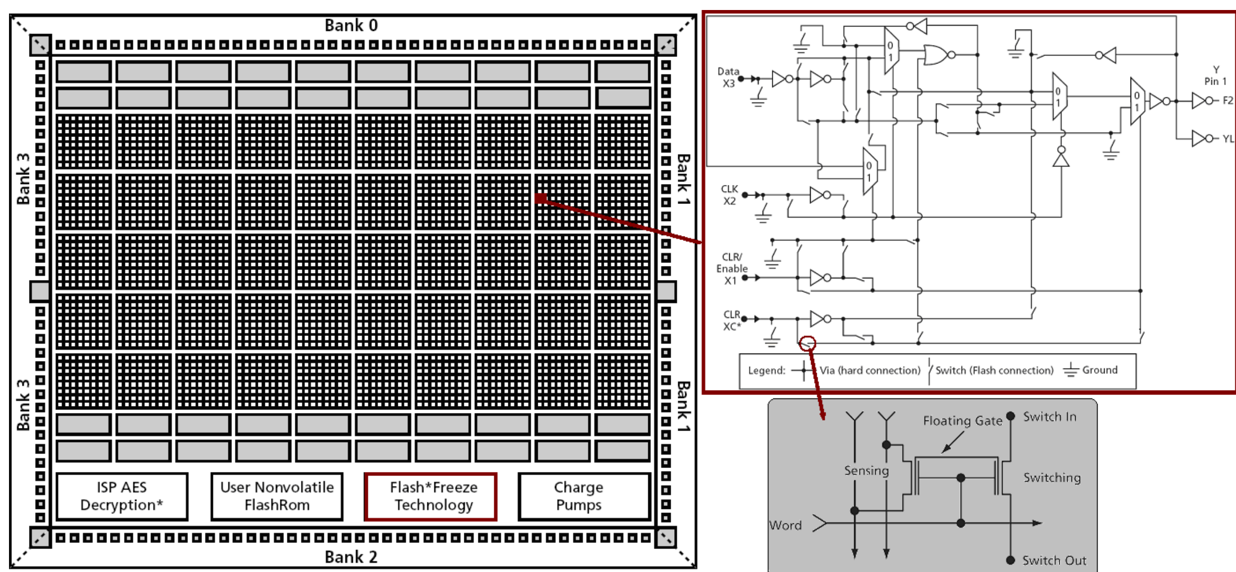
This report documents the SEL characterization, at room temperature and 125 °C, of the 0.13-µm RT ProASIC®3 product family. The SEL testing is performed by recording the currents of the FPGA core (VCCA = 1.5 V) and the inputs/outputs (VCCI = 2.5 V and 3.3 V) during all of the radiation test experiments. Radiation tests for the selected product were performed at Texas A&M University (TAMU). **The derived beam test results show sensitivities to SEL with an effective threshold LET of 68 MeV•cm²/mg at TAMU.** The calculated SEL error-rates in LEO orbits are extremely low (1.93E-12 SEL/FPGA/Day for A3PE600 and 2.71E-10 SEL/FPGA/Day for A3PE3000L). The devices under test (DUT) include A3EP600 and A3PE3000L devices; they are 0.13-µm Flash FPGAs manufactured by the UMC foundry.

2.1 Radiation Test Setup

2.1.1 Device-Under-Test

The RT ProASIC3 product family has up to 3 million system gates, 504 Kbits of true dual-port SRAM, 620 single-ended I/Os, and 300 differential I/O pairs. They also include 1 Kbit of on-chip, programmable, nonvolatile FlashROM (FROM) memory storage as well as up to 6 integrated phase-locked loops (PLL). The FPGA core consists of logic tiles, called VersaTiles, and routing structures. Each logic tile is a combination of CMOS logic and flash switches and can be configured as a three-input logic function or as a D-flip-flop with an optional enable, or as a latch by programming the appropriate flash switch interconnections. The logic tiles are connected with each other through routing structures and FG switches. These flash switches are distributed throughout the device to provide reconfigurable programming to connect signal lines to the appropriate logic-tile inputs and outputs, as shown in the following figure. The flash FPGAs are reprogrammable through the JTAG port and contain programming control circuits composed of charge pumps, sense amplifiers, digital-to-analog converters (DAC), CMOS logic, high-voltage (HV) NMOS transistors, and FG cells to store the factory parameters.

Figure 1 • **ProASIC3 FPGA Core, Versatile (logic tile), and Flash-Based Switch**



Each logic tile is a combination of CMOS logic and flash switches.

For beam test experiments, two devices from the ProASIC3 product series were selected: the A3PE600 and the A3PE3000L, manufactured at the UMC wafer fab. Each selected part was mounted on the PQ208 package. Note that the RT ProASIC3 devices use identical silicon as the tested ProASIC3 parts.

The following table lists the features of the two selected parts.

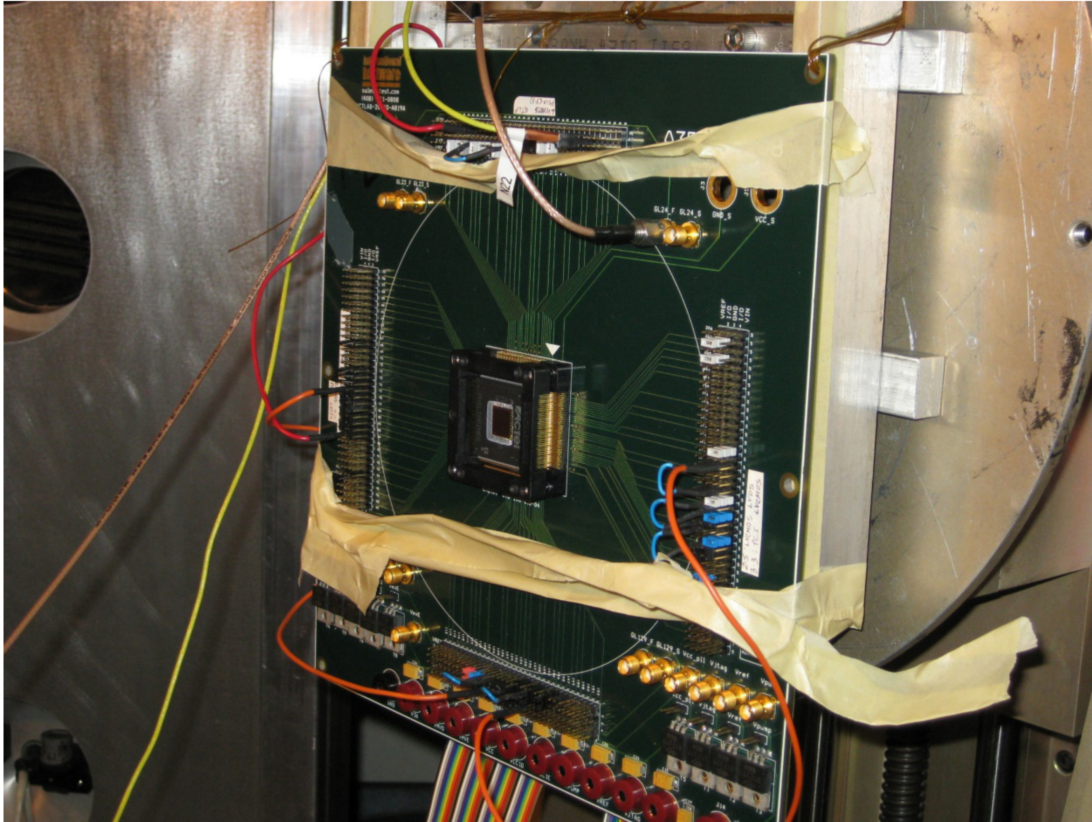
Table 1 • **Features of the Selected DUTs**

Part	A3PE600	A3PE3000L
System Gates	600K	3M
D-Flip-Flops	13,824	75,264
RAM Kbits	108	504
FROM	1K	1K
Secure (AES) ISP	Yes	Yes
Integrated PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Single-Ended I/O	270	620
Differential I/O Pairs	135	310
Package	PQ208	PQ208

2.2 Experimental Test Setup

For SEL characterization of the RT ProASIC3 FPGAs at high temperature, we have used the readily available board for product bench measurements. This board includes the DUT where most of its I/O pads are routed to test pins, as shown in Figure 2, page 4. The advantage of this board is its simplicity and the fact that it allows easy monitoring and control of the DUT voltage and current supplies. The monitoring and control of the DUT FPGA power supplies in-beam was performed by two HP power supplies, each driven by an individual GPIB bus. The GPIB cables are connected to a PC that monitors the current and allows detection of any abnormal increase or decrease in the DUT voltage or current and an automated power-cycle upon the occurrence of a latch-up. The following figure shows the voltage supplies that were monitored by the HP power supplies (FPGA core (VCCA), I/O banks (VCCI), charge pumps (VPP), JTAG (VJTAG), and PLL (VPLL)).

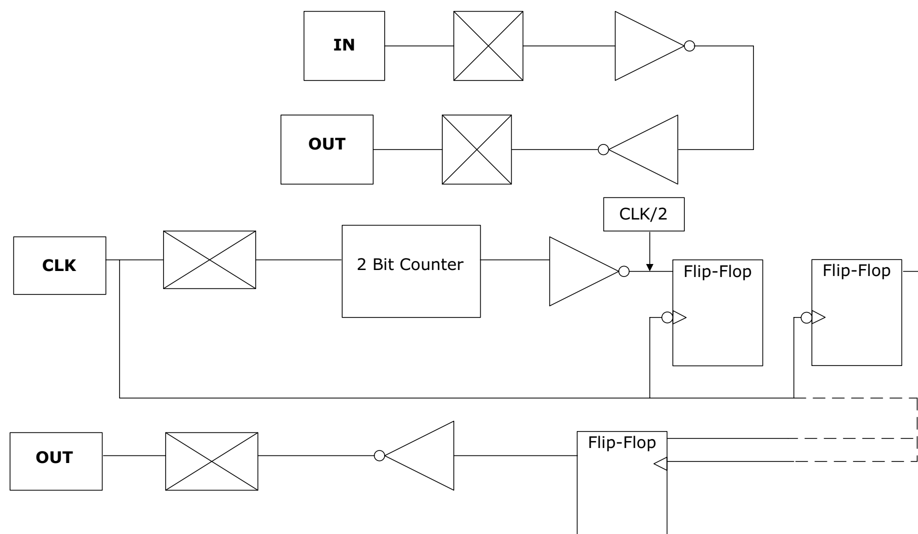
Figure 2 • **RT ProASIC3 SEL Bench Board**



2.3 Test Design

Two test designs have been tested on the ProASIC3E parts. They are identical in the number of used I/Os and core usage but different in the configuration of the I/O banks. Indeed, the first test design is for 3.3 V bias (+10%) on the I/Os and the second one is for 2.5 V bias (+10%) on the I/Os. The selected I/O configurations of both DUTs are shown in Table 2, page 5 and Table 3, page 6. Each of these DUT test design implements 32 separate shift registers, each using a total of 50 tiles configured as D-Flip-Flops and 48 short I/O channels of an input routed immediately to a nearby output, as shown in the following figure. In total, the DUT design is using one global clock signal, 1,571 tiles configured as DFF, 48 inputs, 48 outputs, and 32 outputs configured with registers. The entire design is using 1,571 logic tiles out of the 13,824 (75,264) available in the A3PE600 (A3PE3000L).

Figure 3 • **Block Diagram of the DUT Logic Test Design**



2.3.1 For VCCI = 3.3 V

Table 2 • **Features of I/O Bank Configurations (A3PE600 and A3PE3000L); LV33 = LVCMOS33**

I/O Standards	I/O Bank	Hot-Swap	Schmidt Trigger	Input Programmable Delay	Skew	Slew	Out Load	Out Drive	Resistor Pull	I/O Register
IN (10 LV33) OUT (11 LV33)	0	Yes	Yes	Yes	Yes	Low/ High	Yes	Yes	Yes	Yes
IN (5 PCI) OUT (9 PCI)	1	No	Yes	Yes	No	High	Yes	Yes	Yes	Yes
IN (4 GTLP33) OUT (8 SSTL3II)	2	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (6 PCIX) OUT (10 PCIX)	3	No	Yes	Yes	Yes	Low/ High	Yes	Yes	Yes	Yes
IN (5 LVTTL) OUT (9 LVTTL)	4	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (8 PCI) OUT (12 PCI)	5	No	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (4 GTLP33) OUT (8 SSTL3II)	6	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (6 PCIX) OUT (10 PCIX)	7	No	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes

2.3.2 For VCCI = 2.5 V

Table 3 • **Features I/O Bank Configurations (A3PE600 and A3PE3000L); LV25 = LVCMOS25, LV25_5 = LVCMOS25_5**

I/O Standards	I/O Bank	Hot-Swap	Schmidt Trigger	Input Programmable Delay	Skew	Slew	Out Load	Out Drive	Resistor Pull	I/O Register
IN (10 LV25) OUT (11 LV25)	0	Yes	Yes	Yes	Yes	Low/ High	Yes	Yes	Yes	Yes
IN (6 LV25_5) OUT (6 LV25_5)	1	No	Yes	Yes	No	High	Yes	Yes	Yes	Yes
IN (4 GTLP25) OUT (8 SSTL2II)	2	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (6 LV25_5) OUT (10 LV25_5)	3	No	Yes	Yes	Yes	Low/ High	Yes	Yes	Yes	Yes
IN (5 LV25) OUT (9 LV25)	4	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (8 LV25_5) OUT (12 LV25_5)	5	No	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (4 GTLP25) OUT (8 SSTL2II)	6	Yes	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes
IN (6 LV25_5) OUT (10 LV25_5)	7	No	Yes	Yes	Yes	High	Yes	Yes	Yes	Yes

2.4 Heavy-Ion Beam Test Results

2.4.1 Heavy Ion Beam Source

The ProASIC3E parts have been tested at TAMU. Irradiations used ions with an energy of 15 MeV/amu and effective LETs from 87.2 to 100.3 MeV•cm^2/mg. The features of the used gold (Au) heavy ions are given in the following table. The effective fluence for most of the runs ranges between 5 × 10^6 cm^{-2} and 1 × 10^7 cm^{-2}. Forty-five runs have been performed for the ProASIC3E parts (A3PE3000L and A3PE600) at 20 MHz and at room and high temperatures (125°C). The A3PE3000L has been exercised at two core voltages (1.2 V and 1.5 V), while two bias conditions have been tested for the VCCI (3.3 V and 2.5 V) to exercise both configurations of I/O banks in a test design.

Table 4 • **Features of the Heavy Ion Beams at TAMU**

Facility	Heavy Ions	Energy (MeV/Nucleon)	Angles	Range in Si (µm)	Effective LET (MeV•cm^2/mg)	DUT Location
TAMU	Gold (Au) 29.8	15	0/30	105.2	87.2 / 100.3	In-air

2.4.2 Test Results

The radiation test experiments performed showed SEL on the I/O banks and the FPGA core (ICCA) as well as the charge pumps current (I(VPP)) of both of the A3PE600 and A3PE3000L. Each increase of the charge pumps current in the FPGA core current was observed simultaneously with the ICCI.

The following table lists the details of the heavy ion beam test results for the A3PE600.

Table 5 • **Details of the Heavy Ion Test Results for the A3PE600**

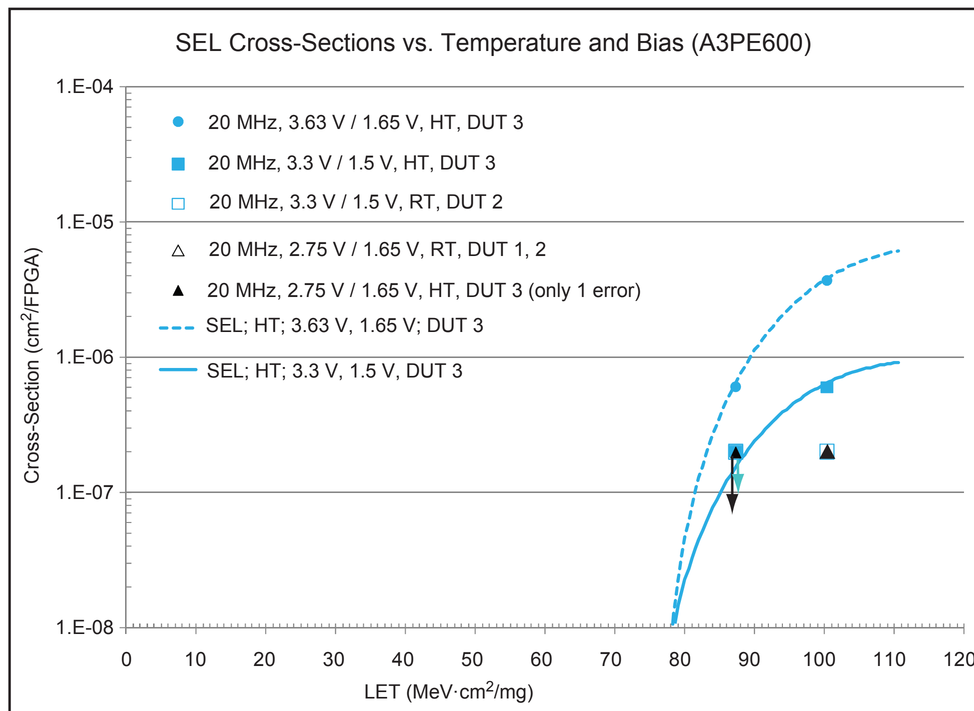
Run	DUT	SEL (VCCI)	SEL (V_{PP})	LET (MeV·cm^2/mg)	Fluence (ions/cm2)	Cross-Section (cm^2/FPGA)	Total Dose (Radium)	Flux (ions/(cm^2·s))	Test Conditions
103	2	3	0	100.3	5.00E+06	6.00E-07	8.03E+03	4.05E+04	20 MHz 3.63 V / 1.65 V Room Temp.
104	2	1	0	100.3	5.01E+06	2.00E-07	1.61E+04	4.45E+04	20 MHz 3.3 V / 1.5 V Room Temp.
105	2	0	0	100.3	4.99E+06	2.00E-07	2.41E+04	4.41E+04	20 MHz 2.75 V / 1.65 V Room Temp.
106	2	10	0	87.2	5.01E+06	2.00E-06	3.11E+04	4.62E+04	20 MHz 3.63 V / 1.65 V Room Temp.
107	2	0	0	87.2	4.98E+06	2.01E-07	3.81E+04	4.53E+04	20 MHz 3.3 V / 1.5 V Room Temp.
108	2	0	0	87.2	5.02E+06	1.99E-07	4.51E+04	4.52E+04	20 MHz 3.3 V / 1.5 V Room Temp.
109	3	2	0	100.3	7.46E+05	2.68E-06	1.20E+03	4.65E+04	20 MHz, 3.63 V / 1.65 V High Temp.
110	3	19	2	100.3	4.98E+06	3.81E-06	9.21E+03	4.63E+04	20 MHz 3.63 V / 1.65 V High Temp.
111	3	3	1	100.3	5.01E+06	5.99E-07	1.73E+04	4.45E+04	20 MHz 3.3 V / 1.5 V High Temp.
112	3	1	0	100.3	5.01E+06	2.00E-07	2.53E+04	4.32E+04	20 MHz 2.75 V / 1.65 V, High Temp.
113	3	0	0	100.3	5.01E+06	2.00E-07	3.34E+04	4.49E+04	20 MHz 2.75 V / 1.65 V High Temp.
114	3	0	0	87.2	5.01E+06	2.00E-07	4.04E+04	4.62E+04	20 MHz 2.75 V / 1.65 V High Temp.
115	3	3	1	87.2	4.99E+06	6.01E-07	4.73E+04	3.83E+04	20 MHz 3.63 V / 1.65 V, High Temp.

Table 5 • **Details of the Heavy Ion Test Results for the A3PE600 *(continued)***

Run	DUT	SEL (VCCI)	SEL (V_{PP})	LET (MeV·cm²/ mg)	Fluence (ions/cm2)	Cross-Section (cm²/FPGA)	Total Dose (Radium)	Flux (ions/(cm²·s))	Test Conditions
116	3	0	2	87.2	5.00E+06	2.00E-07	5.43E+04	4.48E+04	20 MHz 3.3 V / 1.5 V, High Temp.

The following figure shows the obtained SEL cross-sections on the I/O banks, when running the test design described above at 20 MHz versus bias and temperature.

Figure 4 • **SEL Cross-Section of the A3PE600 vs. Bias and Temperature**



The Weibull parameters used to draw the SEL cross-sections in Figure 4, page 8 are listed in the following table.

Table 6 • **Weibull Parameters of RT3PE600L**

Particles	Onset	S	W	Limiting Cross-Section
SEL-HT-3.3 V / 1.5 V	75.5	2.8	27	1E-06
SEL-HT-3.63 V / 1.5 V	73	2.8	27	1E-06

As expected, the SEL cross-sections have increased with the VCCI bias conditions (for 3.3 V and 3.63 V). At 2.75 V for VCCI, only one SEL was observed at high temperature (125°C) at an LET of 100.3 MeV.cm²/mg, but none at room temperature. As very little statistics of latch-ups on VPP were observed, its cross-section was not added to Figure 4, page 8, but note that the charge pumps can be unbiased during the RT ProASIC3 normal operation, which can eliminate all risks of SEL on the VPP. The VPP is needed only during the FPGA programming (a few minutes if the part will be reprogrammed in space), which makes its cross-section even much lower. If an SEL occurs on the VPP during programming mode, the part should be reprogrammed and power cycled. This cross-section will be extremely low in space.

The RT3PE3000L shows almost the same test result as the RT3PE600L. The details of the beam test results are listed in the following table.

Table 7 • **Details of the Heavy Ion Test Results for the A3PE3000L**

Run	DUT	SEL VCCI	SEL V_{PP}	SEL V_{CCA}	LET (MeV.cm^2/mg)	Fluence (ions/cm^2)	SEL VPP	SEL V_{CCA}	Cross-Section cm^2/FPGA	Total Dose (Radium)	Flux (ions/(cm^2.s))	Test Conditions
61	1	123	4	0	100.3	5.38E+06	7.43E-07		2.29E-05	8.65E+03	2.35E+04	20 MHz 3.6 V/1.65V RTD 67°C, DUT 1
62	1	125	5	0	100.3	5.01E+06			2.50E-05	1.56E+04	2.20E+04	20 MHz 3.3V/1.5V Temp = 60° C
63	1	4	1	0	87.2	5.00E+06	2.00E-07		8.01E-07	2.26E+04	2.15E+04	20 MHz 3.3V/1.5V Room Temp.
64	1	4	0	0	87.2	5.01E+06			7.99E-07	2.96E+04	2.09E+04	20 MHz 3.3 V / 1.5 V Room Temp.
65	1	15	0	0	87.2	5.00E+06			3.00E-06	3.66E+04	2.03E+04	20 MHz 3.3 V / 1.5 V Room Temp.
66	1	8	0	0	87.2	5.00E+06			1.60E-06	4.36E+04	2.02E+04	20 MHz 3.6 V / 1.65 V Room Temp.
67	2	82	1	0	100.3	5.01E+06			1.64E-05	8.05E+03	1.94E+04	20 MHz 3.3 V / 1.2 V Room Temp.
68	2	75	1	0	100.3	5.00E+06	2.00E-07		1.50E-05	1.61E+04	1.82E+04	20 MHz 3.3 V / 1.2 V Room Temp.
69	2	64	7	1	100.3	3.09E+06	2.27E-06	3.24E-07	2.07E-05	2.68E+04	1.78E+04	20 MHz 3.63 V / 1.32 V Room Temp.

Table 7 • Details of the Heavy Ion Test Results for the A3PE3000L *(continued)*

Run	DUT	SEL VCCI	SEL V_{PP}	SEL V_{CCA}	LET (MeV.cm^2/mg)	Fluence (ions/cm^2)	SEL VPP	SEL V_{CCA}	Cross-Section cm^2/FPGA	Total Dose (Radium)	Flux (ions/(cm^2.s))	Test Conditions
70	2	17	2	0	87.2	3.21E+06			5.30E-06	3.38E+04	1.71E+04	20 MHz 3.63 V / 1.32 V, Room Temp.
71	2	41	0	0	87.2	5.00E+06			8.20E-06	4.08E+04	1.72E+04	20 MHz 3.5 V / 1.2 V Room Temp.
72	2	15	1	0	87.2	1.54E+06	3.08E-07		9.74E-06	4.51E+04	1.72E+04	20 MHz 3.63 V / 1.32 V Room Temp.
73	3				100.3	8.37E+05			1.19E-06	1.35E+03	1.75E+04	Cover was on
74	3	51	3	0	100.3	2.49E+06	1.20E-06		2.05E-05	5.35E+03	1.69E+04	20 MHz 3.5 V / 1.2 V, High Temp.
75	3	3	0	0	86.9	2.49E+06			1.20E-06	9.36E+03	1.71E+04	20 MHz 3.5 V / 1.2 V High Temp.
76	3	31	0	0	86.9	2.50E+06			1.24E-05	1.34E+04	1.86E+04	20 MHz 3.3 V / 1.2 V High Temp.
77	4	1	0	0	86.9	1.01E+06			9.91E-07	1.62E+03	1.64E+04	20 MHz 3.3 V / 1.2 V High Temp.
78	4	8	0	0	86.9	2.50E+06			3.21E-06	5.63E+03	1.63E+04	20 MHz 3.3 V / 1.2 V High Temp.
79	4	0	0	0	100.3	5.00E+06			2.00E-07	1.37E+04	1.38E+04	20 MHz 2.5 V / 1.2 V Room Temp.
80	4	1	0	0	100.3	1.20E+05			8.35E-06	1.39E+04	1.47E+04	20 MHz 3.3 V / 1.2 V Room Temp.

Table 7 • Details of the Heavy Ion Test Results for the A3PE3000L _(continued)_

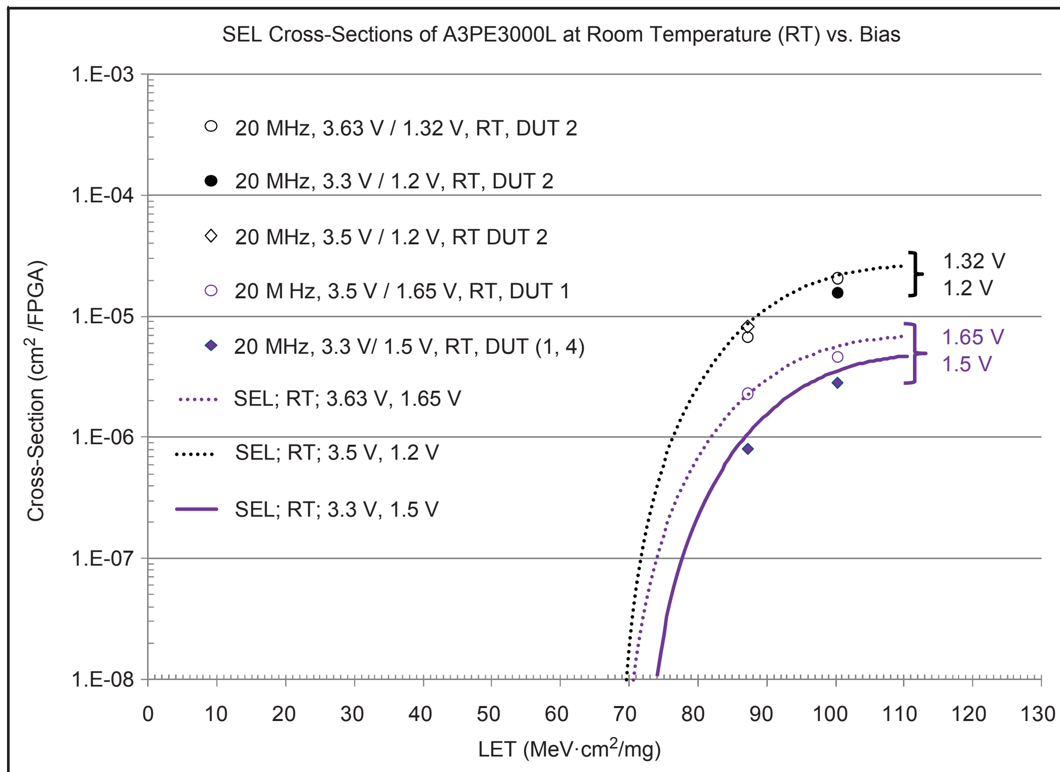
Run	DUT	SEL VCCI	SEL V_{PP}	SEL V_{CCA}	LET (MeV.cm^2/mg)	Fluence (ions/cm^2)	SEL VPP	SEL V_{CCA}	Cross-Section cm^2/FPGA	Total Dose (Radium)	Flux (ions/(cm^2.s))	Test Conditions
81	4	0	0	0	100.3	5.00E+06			2.00E-07	2.19E+04	1.40E+04	20 MHz 2.5 V / 1.2 V Room Temp.
82	4	0	0	0	100.3	1.00E+07			1.00E-07	3.80E+04	1.59E+04	20 MHz 2.5 V / 1.5 V Room Temp.
83	4	0	0	0	100.3	9.99E+06			1.00E-07	5.40E+04	4.07E+04	20 MHz 2.75 V / 1.65 V Room Temp.
84	4	0	0	0	100.3	1.00E+07			9.99E-08	7.01E+04	3.60E+04	20 MHz 2.75 V / 1.32 V Room Temp.
85	4	14	0	0	100.3	5.00E+06			2.80E-06	7.82E+04	3.79E+04	20 MHz 3.3 V / 1.5 V Room Temp.
86	5				100.3	3.28E+04			3.05E-05	5.28E+01	2.68E+04	Initialization problem
87	5	47	1	0	100.3	5.00E+06			9.39E-06	8.09E+03	4.11E+04	20 MHz 3.63 V / 1.65 V High Temp.
88	5	0	0	0	100.3	5.00E+06			2.00E-07	1.61E+04	3.98E+04	20 MHz 2.75 V / 1.65 V High Temp.
89	5	0	0	0	100.3	5.00E+06			2.00E-07	2.42E+04	3.85E+04	20 MHz 2.75 V / 1.32 V High Temp.
90	5	2	0	0	100.3	5.00E+06			4.00E-07	3.22E+04	3.64E+04	20 MHz 3.3 V / 1.5 V Room Temp.

Table 7 • **Details of the Heavy Ion Test Results for the A3PE3000L *(continued)***

Run	DUT	SEL VCCI	SEL V_{PP}	SEL V_{CCA}	LET (MeV.cm²/mg)	Fluence (ions/cm²)	SEL VPP	SEL V_{CCA}	Cross-Section cm²/FPGA	Total Dose (Radium)	Flux (ions/(cm².s))	Test Conditions
91	5	23	0	0	100.3	5.01E+06			4.59E-06	4.03E+04	3.43E+04	20 MHz 3.6 V / 1.65 V Room Temp.
92	5	31	2	0	100.3	5.00E+06			6.21E-06	4.83E+04	4.78E+04	20 MHz 3.63 V / 1.65 V High Temp.
93	5	41	1	0	100.3	5.00E+06	1.14E-07		8.21E-06	5.63E+04	4.11E+04	20 MHz 3.63 V / 1.65 V High Temp.
94	5				87.2	2.40E+05			4.16E-06	5.66E+04	3.83E+04	Initialization problem
95	5	1	0	0	87.2	5.00E+06			2.00E-07	6.36E+04	4.23E+04	20 MHz 3.63 V / 1.65 V High Temp.

The following figure shows the SEL cross-sections of A3PE3000L based on the beam test results given in Table 7, page 9.

Figure 5 • **SEL Cross-Section of the A3PE3000L vs. Bias at Room Temperature**



As shown in Figure 5, page 12, at both tested core voltages (1.2 V and 1.5 V) and for 3.3 V I/O standards, the SEL cross-sections vary with the bias on the I/O banks (3.3 V, 3.63 V (3.3 V +10%)). At both core voltages, the data shows that the SEL cross-sections increase with the VCCI bias. However, the core voltage bias at 1.2 V shows a higher SEL cross-section than at 1.5 V. Figure 6, page 13 shows that the SEL cross-sections increase with temperature at LET 100.3 MeV.cm^2/mg but decrease at LET 87.2 MeV.cm^2/mg. More data is needed to confirm this observation, which may be simply due to the lack of statistics or due to part-to-part variation. Furthermore, as shown in Figure 7, page 14, at both core voltages (1.2 V and 1.5 V), **for both** VCCI **biases (2.5 V and 2.75 V (2.5 V + 10%)), no SEL was observed on the RT3PE3000L until an LET of 100.3 MeV.cm^2/mg**.

Again, the statistics on the SEL in VPP and VCCA are very low and appeared always simultaneously with the latch-up on the VCCI.

Figure 6 • **SEL Cross-Section of the A3PE3000L vs. Bias and Temperature**

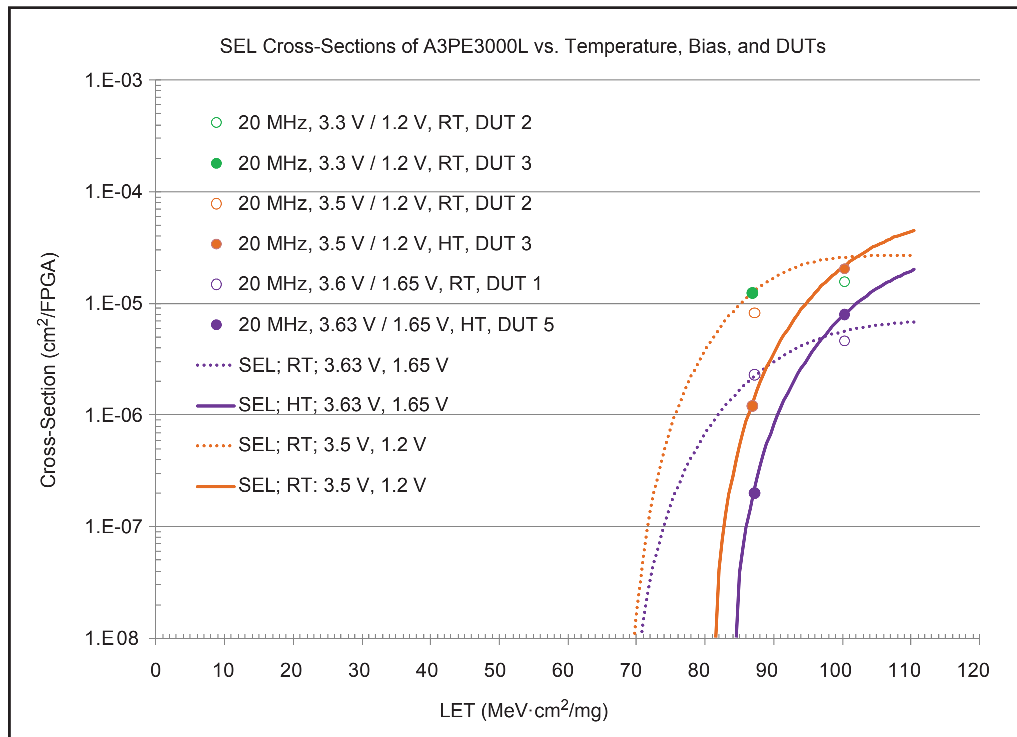
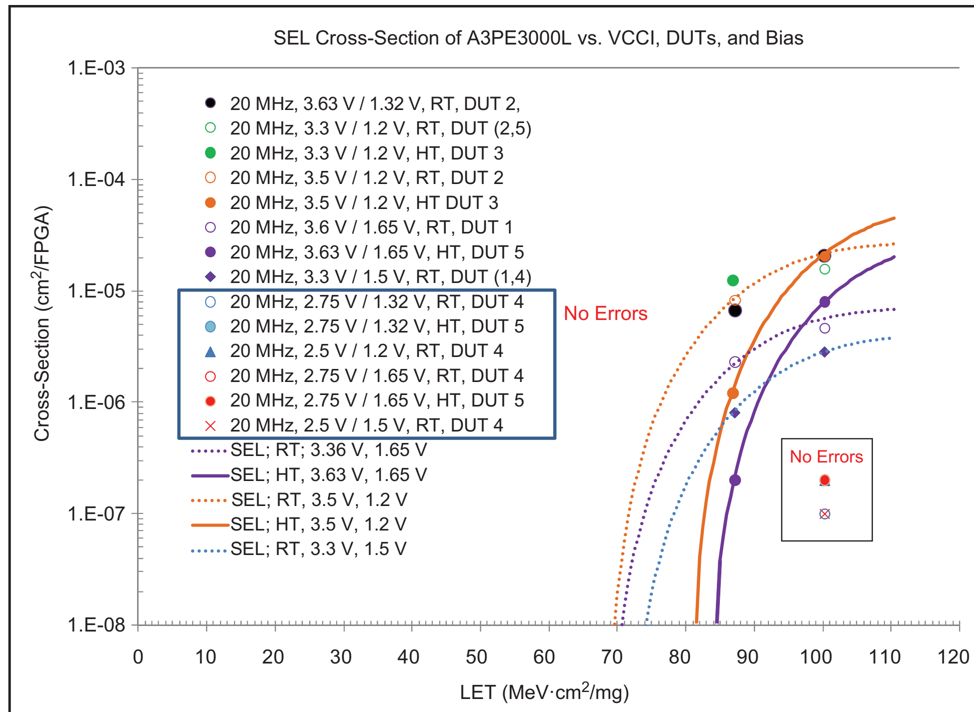


Figure 7 • **SEL Cross-Section of the A3PE3000L vs. VCCI, Bias, and Temperature**



The Weibull parameters are listed in the following table and these parameters are used in generating the SEL cross-sections of Figure 5, page 12, Figure 6, page 13, and Figure 7, page 14.

Table 8 • **Weibull Parameters of RT3PE3000L**

Particles	Onset	S	W	Limiting Cross-Section
SEL-RT-3.3 V / 1.5 V	71	2.8	27	4E-6
SEL-HT-3.5 V / 1.2 V	80	2.8	27	6E-5
SEL-RT-3.5 V / 1.2 V	68	3.1	25	2.5E-5
SEL-HT-3.63 V / 1.65 V	82.5	2.8	27	3E-5
SEL-RT-3.63 V /1.65 V	68	2.8	27	7E-6

To estimate the risks for SEL in a low earth orbit (LEO) space application, we have calculated the expected SEL error rate at an LEO orbit with an apogee and a perigee of 1,000 Km and an inclination of 41 degrees. The selected parameters for this orbit (APMAX or APMIN) as well as the calculated orbital error-rates are shown in the following table. The calculated error-rates are extremely low and demonstrate an expected good survivability of the RT ProASIC3 device in LEO orbits.

Table 9 • **LEO Orbital Error Rates for SEL in the RT3PE600L and the RT3PE3000L**

Particles	Orbit	SEL (A3PE600) SEL/FPGA/Day	SEL (A3PE600) SEL/FPGA/ 10^9 Yrs.	SEL (A3PE3000L) SEL/FPGA/Day	SEL (A3PE3000L) SEL/FPGA/ 10^7 Yrs.
Protons	APMAX/APMIN				
Heavy Ions	APMIN = APMAX – Solar Min.	1.93E-12	0.713	2.71E-10	1