RT0001 Reliability Report
Microsemi FPGA and SoC Products

Contents

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 17.0

The following is a summary of the changes in revision 17.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology - Updated with information from Table 28, Table 50, Table 54, Table 110, Table 114 & Table 123 (created)
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family - Updated with information from Table 28, Table 50, Table 54
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010) - Added note 13
- Updated Table 26, Unbiased Humidity - Updated with information from PA-215 (Wafer lot # 2MPP470711)
- Updated Table 27, Temperature Cycle - Updated with information from PA-215 (Wafer lot # 2MPP470711)
- Updated Table 28, High Temperature Operating Life (HTOL) - Updated with information from lot # HRW0300
- Updated Table 50, CMOS High Temperature Operating Life (HTOL) - Updated with information from lot # DCHTJ1
- Updated Table 54, High Temperature Operating Life (HTOL) - Updated with information from lot # RCGR5
- Updated Table 67, Temperature Cycle (T_C), –55 °C to +125 °C - Updated with information from AEC-PA-003 (Wafer lot # ZA815072) & from PA-204 (Lot # QMSRG)
- Updated Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH - Updated with information from AEC-PA-003 (Wafer lot # ZA815072) & from PA-204 (Lot # QMSRG)
- Updated Table 69, High Temperature Storage (HTS), 150 °C - Updated with information from AEC-PA-003 (Wafer lot # ZA815072)
- Updated Table 75, Temperature Cycle (T_C), –55 °C to +125 °C - Updated with information from PA-215 (Wafer lot # ZA736018)
- Updated Table 77, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH - Updated with information from PA-215 (Wafer lot # ZA736018)
- Updated Table 84, Temperature Humidity Bias (THB), 85 °C / 85% RH - Updated with information from PA-215 (Wafer lot # ZA822043)
- Added Table 85, Temperature Cycle (TC), –55 °C to +125 °C - Created with information from PA-215 (Wafer lot # ZA822043)
- Updated Table 90, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles - Updated with information from PA-215 (Wafer lot # QP352)
- Updated Table 91, Temperature Cycle (TC), –55 °C to +125 °C - Updated with information from PA-215 (Wafer lot # QP352) & from PA-206 (Lot # QMM3P)
- Updated Table 92, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH - Updated with information from PA-206 (Lot # QMM3P)
- Updated Table 97, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles - Updated with information from PA-215 (Wafer lot # QPJF3)
- Updated Table 98, Temperature Cycle (TC), –55 °C to +125 °C - Updated with information from PA-215 (Wafer lot # QPJF3)
- Updated Table 114, Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE - Updated with information from Pipeclean lots, FP205, FP206, FP207 & ORT (Refer to TRB on 08/21/19)
- Updated Table 116, Low Temperature Operating Life - Updated with information from PA-214 (Wafer lot # K37KK) & PA-216 (Wafer lot # K594901)
- Updated Table 117, Temperature Cycle (TC), −55 °C to +125 °C - Updated with information from PA-214 (Wafer lot # K37KK) & PA-216 (Wafer lot # K594901)

- Updated Table 118, Biased Humidity Accelerated Stress Test (HAST), 110 °C/85% RH - Updated with information from PA-214 (Wafer lot # K37KK) & PA-216 (Wafer lot # K594901)
- Added Table 123, Nonvolatile Memory Low-Temperature Retention and Read Disturb (LTDR) - Added this table.

1.2 Revision 16.0

The following is a summary of the changes in revision 16.0 of this document.

- Added Equivalent Device Hours
- Updated Table 1, Reliability Summary: FIT Rate by Device Technology
  - 0.45 µm CMOS FPGA
  - 0.25 µm UMC CMOS FPGA
  - 0.15 µm UMC CMOS FPGA
  - 0.13 µm UMC Flash CMOS FPGA
  - 65 nm UMC Flash CMOS FPGA
  - 28 nm UMC SONOS Flash FPGA
  - Added 0.6 µm XFAB Data
  - Added 0.8 µm XFAB data
  - Added 1.0 µm XFAB data
- Added Table 2, List of MSA Products
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family
  - 0.45 µm CMOS FPGA(MX)
  - 0.25 µm UMC CMOS FPGA (RTSX-SU)
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm UMC Flash CMOS FPGA (ProASIC3-A3P/RT3PEL)
  - 65 nm UMC Flash CMOS FPGA (RTG4)
  - 28 nm UMC SONOS Flash FPGA (PolarFire)
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010)
  - Added G5 (PolarFire) ESD Performance data
  - Added LX77XX ESD Performance
  - Added AA6XX ESD data
- Updated Table 28, High Temperature Operating Life (HTOL)
- Updated Table 45, Retention 225 °C Unbiased 100% Erased
- Updated Table 46, CMOS Reliability–High Temperature Operating Life (HTOL)
- Updated Table 49, Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs
- Updated Table 60, High Temperature Operating Life (HTOL)
- Updated Table 67, Temperature Cycle (T_C), –55 °C to +125 °C
- Updated Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
- Updated Table 91, Temperature Cycle (TC), –55 °C to +125 °C
- Updated Table 92, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
- Updated Table 93, High Temperature Storage (HTS), 150 °C
- Updated Table 97, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles
- Updated Table 99, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
- Updated Table 111, High Temperature Operating Life (HTOL)
- Updated Table 112, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM
- Updated Table 113, High Temperature Data Retention (PCHTDR+HTR) for Non-Volatile Memory: After NVCE
- Added Table 115, High Temperature Operating Life (HTOL) through Table 127, Temperature Cycles (TC)

1.3 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Updated the file name as recommended.
- Removed the term SoC throughout the document as required.

1.4 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology for
  - 1.0 µm CMOS FPGA
  - 0.8 µm CMOS FPGA
  - 0.45 µm CMOS FPGA
  - 0.25 µm UMC CMOS FPGA
  - 0.22 µm UMC CMOS FPGA
  - 0.22 µm UMC Flash CMOS FPGA
  - 0.15 µm UMC CMOS FPGA
  - 0.13 µm Infineon Flash CMOS FPGA
  - 0.13 µm UMC Flash CMOS FPGA
  - 65nm UMC Flash CMOS FPGA
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family for
  - 1.0 µm CMOS FPGA, and ACT2
  - 0.8 µm CMOS FPGA (ACT3)
  - 0.45 µm CMOS FPGA(MX)
  - 0.25 µm UMC CMOS FPGA (RTSX-SU)
  - 0.22 µm UMC CMOS FPGA (SX-A/eX)
  - 0.22 µm UMC Flash CMOS FPGA (ProASICPLUS)
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm Infineon Flash CMOS FPGA (SmartFusion-A2F)
  - 0.13 µm UMC Flash CMOS FPGA (ProASIC3-A3P/RT3PEL)
  - 65nm UMC Flash CMOS FPGA (RTG4)
- Added RTG4 ESD performance details in Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010)
- Updated SXA for CQ84 packages in Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010).
- Updated Table 5, Summary of ESD Performance for AEC-Q100 Qualified Product Families (AEC-Q100-002) for SmartFusion2/IGLOO2 families.
- Updated Table 7, High Temperature Operating Life (HTOL) for A1280A.
- Updated Table 14, 0.8 µm FPGA High Temperature Operating Life (HTOL) for
  - 14100A PG257 FP6341801 1621 80 1000
  - 1425A CQ132 UCJT05 1220 80 1000
- Updated Table 28, High Temperature Operating Life (HTOL) for
  - A42MX04 PG84 HRW0300 1513 45 168
  - A42MX09 PG132 HRRC100 1513 8 72
  - A42MX09 PG132 HRRC100 1513 80 1000
  - A42MX16 PG176 HR5TP00 1451 9 168
- Updated Table 46, CMOS Reliability–High Temperature Operating Life (HTOL) for
  - RTSX32SU CQFP84 D1N8F1 1106 8 1000
  - RTSX32SI CQFP208 D1N8F1 1126 8 2000
  - RTSX32SU CQFP208 D1RH41 1323 100 168
  - RTSX32SU CQFP208 D1RH41 1423 8 1000
  - RTSX72SU CQFP208 D1WW91 1221 24 1000
  - RTSX72SU CQFP256 D1WWA1 1321 100 168
  - RTSX72SU CQFP208 D20BR1 1330 100 168
  - RTSX72SU CQFP208 D1SLL1 1334 8 1000
  - RTSX72SU CQFP208 D1SLL1 1334 8 1000
  - RTSX72SU CQFP208 D6LRQ1 1628 23 1000
- Updated Table 49, Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs for
  - V5.22.8 16,000
  - V5.22.10 8,000
  - V5.22.11 23,000
- Updated Table 50, CMOS High Temperature Operating Life (HTOL) for A54SX72A details.
- Updated Table 54, High Temperature Operating Life (HTOL) for APA1000 details.
- Updated Table 60, High Temperature Operating Life (HTOL) for

- RTAX4000S CG1272 D3KYP1 1251 1 0 2000 125 2000
- RTAX4000S CQ352 D3LG61 1249 8 168 125 168
- RTAX4000S CQ352 D3LG61 1324 24 2000 125 2000
- RTAX2000S CQ352 D55A31 1138 15 168 125 168
- RTAX2000S CQ352b D55A31 1138 15 854 125 854
- RTAX2000S CGS624 D56J31 1225 24 2000 125 2000
- RTAX2000S CQ352 D5A7S1 1213 8 1000 125 1000
- RTAX1000S CQ352 D5G811 1250 27 2005 125 2005
- RTAX2000D CQ352 D5G821 1546 24 2000 125 2000
- RTAX20002 CG1152 D5HK31 1307 23 2000 125 2000
- RTAX2000S CGS624 D5S2W1 1220 14 168 125 168
- RTAX4000D CQ352 D64NH1 1251 7 2024 125 2024
- RTAX250S CQ352 D59RQ1 MIXED 100 168 125 168
- RTAX2000S CQ256 D63WR 1214 24 168 125 168
- RTAX2000S CQ256 D63WR 1214 15 168 125 168
- RTAX2000S CQ256 D66PC1 1235 24 2007 125 2007
- RTAX2000S CQ352 D6CTJ1 1248 14 168 125 168
- RTAX2000S CG1152 D6G7Q1 1506 8 1000 125 1000
- RTAX2000S CQ352 D6G7Q1 1445 8 1000 125 1000
- RTAX250S CQ352 D8KNM1 1526 100 168 125 168
- RTAX250S CQ352 D8KNM1 1526 80 1000 125 1000
- RTAX2000S CQ352 D68N41 1238 14 168 125 168
- RTAX1000S CQ352 D6AS91 1314 24 168 125 168
- RTAX4000S CQ352 D6CM91 1317 8 168 125 168
- RTAX2000S CGS624 D6CN11 1405 8 2000 125 2000
- RTAX2000S CQ352 D6CN21 1304 14 168 125 168
- RTAX2000S CQ352 D6CN21 1345 24 2002 125 2002
- RTAX1000S CQ352 D6CSS1 1249 24 168 125 168
- RTAX1000S CQ352 D6CSS1 1448 24 2000 125C 2000
- RTAX1000S CQ352 D6CST1 1313 24 168 125 168
- RTAX2000S CQ256 D6CTH1 1338 23 2000 125 2000
- RTAX2000S CQ352 D6G7P1 1434 8 2000 125 2000
- RTAX2000S CQ352 D6G7P1 1434 8 1000 125 1000
- RTAX2000S CG1152 D6G7Q1 1351 14 171 125 171
- RTAX2000S CQ352 D6M7F1 1304 14 168 125 168
- RTAX4000D CQ352 D6NR61 1312 8 180 125 180
- RTAX2000S CQ352 D6W3Q1 1316 14 168 125 168
- RTAX2000S CQ352 D71CM1 1343 14 168 125 168
- RTAX2000S CQ256 D71CM1 1350 79 1010 125 1010
- RTAX2000S CQ352 D72TK1 1343 14 168 125 168
- RTAX2000S CQ256 D75K91 1348 14 168 125 168
- RTAX2000S CQ352 D77J81 1405 14 168 125 168
- RTAX2000S CQ352 D79G91 1410 14 168 125 168
- RTAX4000S CQ352 D7FLT1 1418 8 168 125 168
- RTAX4000D CQ352 D7P6Q1 1419 8 168 125 168
- RTAX4000D CQ352 D82W41 1614 8 160 125 160
- RTAX4000D CQ352 D82W41 1614 8 24 125 24
- RTAX250S CQ208 D8KNM1 1534 24 2000 125 2000
- RTAX2000D CQ352 D8QLF1 1546 14 168 125 168
- RTAX4000S CQ352 D8TW11 1614 8 168 125 168
- RTAX4000S CG1272 D8TW11 1624 24 1002 125 1002

- Updated Table 64, Unit-hours of Life Test Data for reliability summary silicon sculptor programming software details.
  - V5.22.4 203,322 50,688
  - V5.22.5 16,000 1,344
  - V5.22.8 32,000
  - V5.22.9 16,800 48,000 4,032
  - V5.22.10 128,000 2,352
  - V5.22.11 4,872 25,392 48,000 1,472

- Updated Table 82, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles for SmartFusion FCG484 package details.
  - A2F200 FGG484 ZA027289 1216 76 168 133 168 0 12768
- Updated Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles for reliability report for different product families.
  - RT3PE3000L CG896 QKN6Y 1406 60 1000 125 1000 0 0 0 60000
  - RT3PE3000L CQ256 QMLPK 1625 80 1000 125 1000 0 0 0 80000
- Replaced 0.065 µm with 0.65 nm through out the report.
- Added 65 nm UMC Flash FPGA Reliability Summary, page 90.
- Added Table 111, High Temperature Operating Life (HTOL)
  - RT4G150 CG1657 KRMLM 1625 24 1000 125C 1000
  - RT4G150 CG1657 KPAQS 1606 18 2000 125C 2000
  - RT4G150 CG1657 KRAFJ 1615 18 2000 125C 2000
  - RT4G150 CG1657 KRAQF 1616 18 2000 125C 2000
- Added Table 112, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM
  - RT4G150 LG1657 KNLGG 1550
  - RT4G150 LG1657 KNPNP 1604
  - RT4G150 LG1657 KRAFJ 1615
  - RT4G150 LG1657 KRAQF 1616
- Added Table 113, High Temperature Data Retention (PCHTDR+HTR) for Non-Volatile Memory: After NVCE
  - RT4G1501 LG1657 KNLGG 1550
  - RT4G1501 LG1657 KRAFJ 1615
  - RT4G1501 LG1657 KRAQF 1616
  - RT4G1502 Wafer KRSLW NA
  - RT4G1502 Wafer KRMLM NA
  - RT4G1502 LG12724 KRKTL 1623
- Added Table 114, Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE
  - RT4G1501 LG1657 KNLGG 1550
  - RT4G1501 LG1657 KRAFJ 1615
  - RT4G1501 LG1657 KRAQF 1616

1.5 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology (SAR 74739). FIT rates for the following device technology have been updated
  - 0.065 um UMC Flash CMOS FPGA
  - 0.13 um Infineon Flash CMOS FPGA (ProASIC3- A3P)
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family (SAR 74739)
  - Added Note 3 for IGLOO2 on Accelerated Programming Qualification.
- Updated 0.13 µm Infineon Flash FPGA Reliability Summary (ProASIC3 – A3P), page 66 (SAR 74739)
- Updated Table 66, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles (SAR 74739)
  - Added A3P250-VQG, W/L ZA418036, 231 pcs, 500cycles@ -65°C to +150°C
- Updated Table 67, Temperature Cycle (T_C), –55 °C to +125 °C (SAR 74739)
  - Added A3P250-VQG, W/L ZA418036, 231 pcs, 500cycles@ -65°C to +150°C
- Updated Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH (SAR 74739)
  - Added A3P250-VQG100,W/L ZA418036, 231pcs, 96hrs UHAST at 130°C and 85% RH
  - Added A3P250-VQG100,W/L ZA418036, 231pcs, 96hrs Biased HAST at 130°C and 85% RH
  - Added A3P1000-FGG256, W/L ZA424029, 45pcs, 264rs UHAST at 130°C and 85% RH
- Updated Table 69, High Temperature Storage (HTS), 150 °C (SAR 74739)
  - Added A3P250-VQG100,W/L ZA418036, 77pcs, 1000hrs at 150°C
- Updated Table 102, Low Temperature Operating Life (LTOL) (SAR 74739)
  - Added A3P250-VQG100,W/L ZA418036

- Updated 65 nm UMC Flash FPGA Reliability Summary (SmartFusion2—M2S (S,T,TS), IGLOO2–M2GL (S,T,TS) Product Families), page 84 Product Families, FIT changed from 6.05 to 3.22 (SAR 74739)
- Updated Table 101, High Temperature Operating Life (HTOL) (SAR 74739)
  - Added M2S150-FCG1152, W/L SAYLT/SCCTJ, 136pcs, 4000hrs @ 133.2°C
- Updated Table 103, Temperature Cycle (TC), –55 °C to +125 °C (SAR 74739)
  - Added M2S150-FCG1152, W/L SCCTJ, 225pcs, 700cycles @ -55°C to +125°C
  - Added M2S010-TQ/TQG144, W/L SGQJF, 225pcs, 500cycles @ -65°C to +150°C
  - Added M2S090-FCS325, W/L SCTAY,225pcs,700cycles @ -55°C to +125°C
  - Added M2S090-FCS325, W/L SFAKR,225pcs,1000cycles @ -55°C to +125°C
  - Added M2S150-FCSG536,W/L SHNNJ, 225pcs, 700cycles @ -55°C to +125°C
  - Added M2S090-FG676,W/L SHTGQ, 225pcs, 1000cycles @ -55°C to +125°C
  - Added M2S090-FGG676,W/L SCMSP, 25pcs, 1000cycles @ -55°C to +125°C
  - Added M2S050-VF400, W/L SN9Y144, 25pcs, 1000cycles @ -55°C to +125°C
  - Added M2S050-FGG896, W/L SK1P8,SG3N704,SH5Y8, 225pcs, 1000cycles @ -55°C to +125°C
- Updated Table 104, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH (SAR 74739)
  - Added M2S150-FCG1152, W/L SCCTJ, 225pcs, 264hrs at 110°C and 85% RH
  - Added M2S010-TQ/TQG144, W/L SGQJF, 225pcs,264hrs at 130°C and 85% RH
  - Added M2S090-FCS325, W/L SCTAY, 225pcs, 264hrs at 110°C and 85% RH
  - Added M2S090-FCS325, W/L SFAKR, 225pcs, 264hrs at 110°C and 85% RH
  - Added M2S150-FCSG536, W/L SHNNJ, 225pcs, 264hrs at 110°C and 85% RH
  - Added M2S090-FG676,W/L SHTGQ 225pcs, 264hrs at 110°C and 85% RH
  - Extended M2S090-FG676,W/L SHTGQ, 225pcs, to 528hrs at 110°C and 85% RH
  - Added M2S090-FGG676,W/L SCMSP, 25pcs, 264hrs at 110°C and 85% RH
  - Added M2S050-VF400,W/L SN9Y144, 25pcs, 264hrs at 110°C and 85% RH
  - Added M2S050-FGG896, W/L SK1P8,SG3N704,SH5Y8, 225pcs, 264hrs at 110°C and 85% RH
- Updated Table 105, High Temperature Storage (HTS), 150 °C (SAR 74739)
  - Added M2S150-FCG1152, W/L SCCTJ, 81pcs, 4000hrs @ 150°C
  - Added M2S150-FCG1152, W/L SCCTJ, 235pcs,1000hrs @ 150°C
  - Added M2S010-TQ/TQG144, W/L SGQJF, 225pcs, 1000hrs @ 150°C
  - Added M2S090-FCS325, W/L SCTAY, 225pcs, 1000hrs @ 150°C
  - Added M2S090-FCS325, W/L SFAKR, 225pcs, 1000hrs @ 150°C
  - Added M2S150-FCSG536, W/L SHNNJ, 225pcs, 1000hrs @ 150°C
  - Added M2S090-FG676, W/L SHTGQ, 225pcs, 1000hrs @ 150°C
  - Added M2S090-FGG676, W/L SCMSP, 25pcs, 1000hrs @ 150°C
  - Added M2S050-VF400,W/L SN9Y144,25pcs, 1000hrs @ 150°C
  - Added M2S050-FGG896, W/L SK1P8,SG3N704,SH5Y8, 225pcs,1000hrs @ 150°C
- Updated Table 106, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM (SAR 74739)
  - Added M2S010-WL SLASS, 106pcs, 500cycles
- Updated Table 107, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): eNVM (SAR 74739)
  - Added M2S010-WL SLASS, 45pcs, 1000 cycles
- Updated Table 108, High Temperature Data Retention (HTDR) for Non-Volatile Memory: After NVCE (SAR 74739)
  - Added M2S150-FCG1152, W/L SCCTJ,80pcs, 3000hrs
- Updated Table 109, Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE (SAR 74739)
  - Added M2S150-FCG1152, W/L SCCTJ,80pcs, 4000hrs

1.6 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology. FIT rates for the following device technology have been updated:
  - 0.45 µm CSM CMOS FPGA

- 0.45 µm UMC CMOS FPGA
- 0.25 µm UMC CMOS FPGA
- 0.22 µm UMC CMOS FPGA
- 0.22 µm UMC Flash CMOS FPGA
- 0.15 µm UMC CMOS FPGA
- 0.13 µm IFX Flash CMOS FPGA
- 0.13 µm UMC Flash CMOS FPGA
- 0.065 µm UMC Flash CMOS FPGA

- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family.
  - 0.45 µm CSM CMOS FPGA (A42MX)
  - 0.45 µm CSM CMOS FPGA (A42MX)
  - 0.25 µm UMC CMOS FPGA (RTSX-SU)
  - 0.22 µm UMC CMOS FPGA (SX-A)
  - 0.22 µm UMC Flash CMOS FPGA (APA)
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm IFX Flash CMOS FPGA (A3P & A2F)
  - 0.13 µm UMC Flash CMOS FPGA (A3P/RT3PEL & AGL)
  - 0.065 µm UMC Flash CMOS FPGA (M2S/M2GL)
  - Added footnote 2 “IGLOO2 – M2GL family of devices is covered under 0.065um SmartFusion2 – M2S FPGA family by similarity”.
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010)
  - Added SmartFusion2 and IGLOO2 device family members
  - Updated footnote 9
- Updated 0.45um CSM FPGA Reliability Summary, FIT changed from 19.62 to 18.05. Table 24, High Temperature Operating Life (HTOL)
  - Added: A42MX36-CQ208, W/L HPY9H00, 80pcs, 2000hrs @ 125°C
- Updated 0.45um UMC FPGA Reliability Summary, FIT changed from 35.79 to 24.06. Table 28, High Temperature Operating Life (HTOL)
  - Added: A42MX24-PQ208,W/L HPY9H00, 80pcs, 2000hrs @ 125°C
- Updated 0.25µm UMC FPGA Reliability Summary, FIT changed from 1.18 to 1.17. Table 46, CMOS Reliability–High Temperature Operating Life (HTOL)
  - Added RTSX72SU-CQ256, W/L D6AA61, 80pcs, 1000hrs @ 125°C
  - Corrected WL# from D1N8F1 to D1N8A1 for RTSX72SU, DC 0641, 15units, 1000hrs @ 125°C
  - Added Reliability Summary for Silicon Sculptor Programming Software
- Updated 0.22um UMC FPGA Reliability Summary, FIT changed from 1.78 to 1.76. Table 50, CMOS High Temperature Operating Life (HTOL)
  - Added: A54SX72A-CQ208, W/L D77SP1, 80pcs, 1000hrs @ 125°C
- Updated 0.22um UMC Flash FPGA Reliability Summary, FIT changed from 13.28 to 10.77. Table 54, High Temperature Operating Life (HTOL)
  - Added APA300-CQ208, W/L MK91G, 24pcs, 2000hrs @ 125°C
  - Added APA1000-CQ208, W/L MWJ9W, 78pcs, 1000hrs @ 125°C
  - Added APA300-CQ208, W/L R21A5, 80pcs, 1000hrs @ 125°C
- Updated 0.15 µm UMC FPGA Reliability Summary, FIT changed from 7.04 to 6.82. Table 60, High Temperature Operating Life (HTOL)
  - Added RTAX2000S-CQ256, W/L D71CM1, 79pcs, 1000hrs @ 125°C
  - Added RTAX2000SL-CQ256, W/L D6CTH1, 23pcs, 2000hrs @ 125°C
  - Added RTAX2000S-CQ352, W/L D6CN21, 24pcs, 2000hrs @ 125°C
  - Added RTAX4000DL-CQ352, W/L D64NH1, 7pcs, 2000hrs @ 125°C
  - Added Reliability Summary for Silicon Sculptor Programming Software
- Updated 0.13 µm Infineon Flash FPGA Reliability Summary (ProASIC3 – A3P), FIT changed from 4.18 to 4.01.
- Updated Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles
  - Added A3P1000-BGAG484, W/L ZA252062, 77pcs, 1000hrs @ 134°C
- Updated Table 67, Temperature Cycle (T_C), –55 °C to +125 °C
  - Added A3P1000-PQG208, W/L ZA31005102, 47pcs, 500cycles at -65°C to +150°C (Condition C)
  - Added A3P250-QNG132, W/L ZA249133, 47pcs, 500cycles at -65°C to +150°C (Condition C)
- Updated Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
  - Added A3P1000-PQG208, W/L ZA31005102, 47pcs, 96hrs UHAST at 130°C and 85% RH

- Added A3P250-QNG132, W/L ZA249133, 47pcs, 96hrs UHAST at 130°C and 85% RH
- Updated Table 69, High Temperature Storage (HTS), 150 °C
  - Added A3P1000-PQG208, W/L ZA31005102, 45pcs, 1000hrs at 150°C
  - Added A3P250-QNG132, W/L ZA249133, 47pcs, 1000hrs at 150°C
- Updated 0.13 µm Infineon Flash FPGA Reliability Summary (SmartFusion – A2F), FIT changed from 11.70 to 10.51.
- Updated Table 82, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles
  - Added A2F200-FGG484, W/L ZA027289, 76pcs, 1000hrs @ 133°C
- Updated Table 83, High Temperature Storage (HTS), 150 °C
  - Added A2F200-FGG484, W/L ZA027289, 47pcs, 1000hrs @ 150°C
- Updated Table 84, Temperature Humidity Bias (THB), 85 °C / 85% RH
  - Added A2F200-FGG484, W/L ZA027289, 53pcs, 1008hrs @ 85°C / 85% RH
- Updated 0.13 µm UMC Flash FPGA Reliability Summary (IGLOO – AGL/AGLE; IGLOO PLUS – AGLP; IGLOO nano – AGLN), FIT changed from 7.22 to 6.78.
- Updated Table 89, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles
  - Added AGL1000-FGG484, W/L QL1Y6, 75pcs, 1000hrs @ 132°C
- Updated Table 91, Temperature Cycle (TC), –55 °C to +125 °C
  - Added AGLP030-VQG128, W/L QJY60, 47pcs, 500cycles @ -65°C to +150°C (Condition C)
- Updated Table 92, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
  - Added AGLP030-VQG128, W/L QJY60, 47pcs, 96hrs at 130°C and 85% RH
- Updated Table 93, High Temperature Storage (HTS), 150 °C
  - Added AGL1000-FGG484, W/L QL1Y6, 47pcs, 1000hrs @ 150°C
- Updated 0.13 µm UMC Flash FPGA Reliability Summary (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3EL – A3PL, A3PEL;ProASIC3 nano – A3PN, RT ProASIC3 – RT3P), FIT changed from 15.54 to 14.15
- Updated Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles
  - Added RT3PE3000L-CGA484, W/L QKN6Y, 80pcs, 1000hrs @ 125°C
  - Added RT3PE3000L-CGA484, W/L QJA2G, 78pcs, 1000hrs @ 125°C
  - Added RT3PE3000L-LGA896, W/L QJA2G, 6pcs, 1000hrs @ 125°C
- Updated Table 98, Temperature Cycle (TC), –55 °C to +125 °C
  - Added A3P600-FGG256, W/L QL7H0, 45pcs, 700cycles @ -55°C to +125°C
  - Added A3PN250-VQG100, W/L QL5CL, 45pcs, 500cycles @ -65°C to +150°C (Condition C)
- Updated Table 99, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
  - Added A3PN250-VQG100, W/L QL5CL, 45pcs, 1000hrs @ 85°C / 85% RH
- Updated Table 100, High Temperature Storage (HTS), 150 °C
  - Added A3P600-FGG256, W/L QL7H0, 45pcs, 1000hrs @ 150°C
  - Added A3PN250-VQG100, W/L QL5CL, 45pcs, 1000hrs @ 150°C
- Updated 0.065 µm UMC Flash FPGA Reliability Summary (SmartFusion2 – M2S (S,T,TS), IGLOO2 – M2GL (S,T,TS) Product Families, FIT changed from 24.51 to 6.05
- Updated Table 101, High Temperature Operating Life (HTOL)
  - Added M2S050-FG896, W/L SQ4L9, 80pcs, 6000hrs @ 138.6°C
  - Added M2S050-FG896, W/L SQ4L9, 19pcs, 2000hrs @ 146.8°C
  - Added M2S150-FCG1152, W/L SAYLT/SCCTJ, 136pcs, 2000hrs @ 133.2°C
- Updated Table 102, Low Temperature Operating Life (LTOL)
  - Added M2S050-FG896, W/L SQ4L9, 34pcs, 1000hrs @ -51°C
  - Added M2S150-FCG1152, W/L SCCTJ, 37pcs, 1000hrs @ -50°C
- Updated Table 103, Temperature Cycle (TC), –55 °C to +125 °C
  - Added M2S150-FCG1152, W/L SCCTJ, 81pcs, 700cycles @ -55°C to +125°C
- Updated Table 104, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH
  - Added M2S150-FCG1152, W/L SCCTJ, 80pcs, 264hrs at 110°C and 85% RH
- Updated Table 105, High Temperature Storage (HTS), 150 °C
  - Added M2S150-FCG1152, W/L SCCTJ, 81pcs, 1000hrs @ 150°C
- Updated Table 106, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM
  - For M2S050-FG896, W/L SA1A8/SK1P8/SK1P9 corrected total units from 231 to 360
  - Added M2S050-FG896, W/L SQ4L9, 94pcs, 550cycles
  - Added M2S150-FCG1152, W/L SAYLT, 319pcs, 550cycles
  - Added footnotes to clarify NVCE test temperatures
- Updated Table 107, Endurance/Non-Volatile Memory Cycling Endurance (NVCE): eNVM
  - For M2S050-FG896, W/L SA1A8/SK1P8/SK1P9 corrected total units from 231 to 360

- Added M2S050-FG896, W/L SQ4L9, 94pcs, 10,000cycles
- Added footnotes to clarify NVCE test temperatures

- Updated Table 108, High Temperature Data Retention (HTDR) for Non-Volatile Memory: After NVCE
  - Updated M2S050-CQ208, W/L SA1A8/SK1P8/SK1P9, 132pcs, from 1000hrs to 3000hrs @ 250°C (additional hrs completed), knowledge based testing
  - Added M2S050-FG896, W/L SQ4L9, 47pcs, 10hrs @ 125°C (per JEDEC 47)
  - Added M2S150-FCG1152, W/L SAYLT, 80pcs, 10hrs @ 125°C (per JEDEC 47)
  - Added M2S150-CQ208, W/L SAYLT, 80pcs, 2000hrs @ 250°C, knowledge based testing
  - Added footnotes to clarify NVCE cycles and test temperatures
- Updated Table 109, Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE
  - Updated M2S050-CQ208, W/L SA1A8/SK1P8/SK1P9, 135pcs, from 1000hrs to 3000hrs @ 25°C (additional hrs completed)
  - Added M2S050-FG896, W/L SQ4L9, 47pcs, 1000hrs @ 25°C
  - Added M2S150-FCG1152, W/L SAYLT, 80pcs, 2000hrs @ 25°C
  - Corrected footnote 2 from 1K to 10K eNVM cycles
  - Added footnote 3
- Updated Table 110, High Temperature Storage Life (HTSL), 150 °C: After NVCE
  - Updated M2S050-FG896, W/L SA1A8/SK1P8/SK1P9, 90pcs, from 1000hrs to 3000hrs @ 150°C (additional hrs completed)
  - Added M2S150-FCG1152, W/L SAYLT, 79pcs, 3000hrs @ 150°C
  - Added footnote 3
- General update, footnote added for all Flash retention 250°C testing to clarify units assembled in CQFP packages are not commercially available (i.e., the engineering package is for reliability testing only)
- General correction: Package type corrected from FPGA to FBGA

1.7 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology. Added FIT rate for 0.065 µm UMC Flash CMOS FPGA device technology.
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family. Added FIT rate for 0.065 µm UMC Flash CMOS FPGA (SmartFusion2 - M2S) device technology.
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010). Added SmartFusion2 ESD performance data and footnote 9.
- Added reliability data for 0.065 µm UMC Flash CMOS FPGA (SmartFusion2 - M2S) device technology Table 101, High Temperature Operating Life (HTOL) to Table 110, High Temperature Storage Life (HTSL), 150 °C: After NVCE.

1.8 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology. FIT rates for the following device technology have been updated:
  - 1.0 µm CMOS FPGA
  - 0.45 µm CSM CMOS FPGA
  - 0.45 µm UMC CMOS FPGA
  - 0.22 µm UMC CMOS FPGA
  - 0.22 µm UMC Flash CMOS FPGA
  - 0.15 µm UMC CMOS FPGA
  - 0.13 µm UMC Flash CMOS FPGA
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family. FIT rates for following device technology have been updated:
  - 1.0 µm CMOS FPGA (ACT1)
  - 0.45 µm CSM CMOS FPGA (A42MX)
  - 0.45 µm CSM CMOS FPGA (A42MX)
  - 0.22 µm UMC CMOS FPGA (SX-A)

- 0.22 µm UMC Flash CMOS FPGA (APA)
- 0.15 µm UMC CMOS FPGA (RTAX-S)
- 0.13 µm UMC Flash CMOS FPGA (ProASIC3 – A3P/RT3PEL)

- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010): Added footnote 4 to A3P125: “Passed 2000V HBM on all pins except VCC_PLL, which meets 500V."
- Updated 1.0 µm FPGA reliability data, FIT changed from 5.68 to 5.62. Table 7, High Temperature Operating Life (HTOL)
- Added: A1020B-CQ84B, W/L FP6502401, 79pcs, 615hrs @ 125°C.
- Updated 0.45 µm CSM FPGA reliability data, FIT changed from 22.30 to 19.62. Table 24, High Temperature Operating Life (HTOL)
  - Added: A42MX36-CQ256, W/L 2ACH323581, 80pcs, 1000 hrs @ 125°C.
  - Added: A42MX36-CQ256, W/L 2ACG311291, 79pcs1000 hrs @ 125°C.
- Updated 0.45 µm UMC FPGA reliability data, FIT changed from 69.06 to 35.79. Table 28, High Temperature Operating Life (HTOL)
  - Added: A42MX24-PQ208, W/L HMGN000, 79pcs, 2000hrs @ 125°C.
  - Corrected units hours for A40MX04-PL84, W/L HKJAH00 from 9,000 to 90,000
  - Corrected unit hours for A42MX24-PQ208, W/L HLF8Q0G from 8,000 to 80,000
  - Updated total unit hours accordingly
- Table 31, High Temperature Storage (HTS), 150 °C
  - Corrected units hours for A40MX04-PL84, W/L HKJAH00 from 8,000 to 80,000
  - Corrected unit hours for A42MX24-PQ208, W/L HKJNS00 from 8,000 to 80,000
  - Updated total unit hours accordingly to 160,000
- Updated 0.25 µm UMC FPGA reliability data. Table 46, CMOS Reliability–High Temperature Operating Life (HTOL)
  - Corrected product name from RTSX32SU to RTSX72SU for, W/L D1N8A1, DC 0831, 12pcs, 1000hrs @ 125°C
  - Corrected product name from RTSX32SU to RTSX72SU and DC from 0831 to 0939 for W/L D1SG01, 100pcs, 168hrs @ 125°C
- Updated 0.22 µm UMC FPGA reliability data, FIT changed from 1.83 to 1.78. Table 49, Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs
  - Added: A54SX32A-CQ208, W/L D5GTW1, DC 1125, 80pcs, 1000hrs @ 125°C
  - Added: A54SX72A-PQ208, W/L D54RJ1, DC 1036, 100pcs, 168hrs @ 125°C
- Updated 0.22 µm UMC Flash FPGA reliability data, FIT changed from 15.85 to 13.28. Table 54, High Temperature Operating Life (HTOL)
  - Added: APA1000-CQ352, W/L MR91L, DC 1025, 24pcs, 2000hrs @ 125°C
  - Added: APA300-PQ208, W/L MTG7J02, DC 1045, 77pcs, 168hrs @ 125°C
  - Added: APA600-CQ208, W/L R00KY, DC 1226, 80pcs, 1000hrs @ 125°C
- Updated 0.15 µm UMC FPGA reliability data, FIT changed from 7.25 to 7.04. Table 60, High Temperature Operating Life (HTOL)
  - Added: RTAX2000S-CQ352, W/L D55A21, DC 1049, 7pcs, 1000hrs @ 125°C
  - Added: RTAX2000SL-CQ256, W/L D55A31, DC 1052, 22pcs, 2000hrs @ 125°C
  - Added: RTAX2000S-CQ352, W/L D54C81, DC 1106, 8pcs, 1000hrs @ 125°C
  - Added: RTAX2000S-CQ352, W/L D63WS1, DC 1225, 80pcs, 1000hrs @ 125°C
  - Added: RTAX4000SL-CQ352, W/L D41891, DC 1110, 24pcs, 1000hrs @ 125°C
- Updated 0.13 µm UMC Flash FPGA reliability data, FIT changed from 8.14 to 7.87
- (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3/EL – A3PL, AEPEL; ProASIC3 nano – A3PN, RT ProASIC3 – RT3P). Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles
  - Added: RT3PE3000L-CG896, W/L QJA2G, DC 1205, 47pcs, 2307hrs @ 125°C
  - Corrected number of units tested from 82pcs to 81pcs for RT3PE3000L-CG896, W/L QHR8G, DC 0925

1.9 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology: FIT Rate by Device Technology. FIT rates for the following device technology have been updated:
  - 1.0 µm CMOS FPGA
  - 0.25 µm UMC CMOS FPGA

- 0.22 µm UMC Flash CMOS FPGA
- 0.15 µm UMC CMOS FPGA
- 0.13 µm Infineon Flash CMOS FPGA
- 0.13 µm UMC Flash CMOS FPGA

- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family: FIT Rate by Device Technology and Product Family. FIT rates for following device technology have been updated:
  - 1.0 µm CMOS FPGA (ACT 2)
  - 0.25 µm UMC CMOS FPGA (RTSX-SU)
  - 0.22 µm UMC Flash CMOS FPGA (SX-A)
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm Infineon Flash CMOS FPGA (SmartFusion – A2F)
  - 0.13 µm UMC Flash CMOS FPGA (IGLOO - AGL)
  - 0.13 µm UMC Flash CMOS FPGA (ProASIC3 – A3P/RT3PEL)
- Updated 1.0 µm FPGA reliability data, FIT changed from 5.57 to 5.68. Table 7, High Temperature Operating Life (HTOL): Fit increased slightly as four duplicate entries were removed and added one new.
  - Removed: A1280A-CQ172, W/L U1H363, 58pcs, 615hrs at 125°C, A1280A-CQ172, W/L U1H83, 45pcs, 1671hrs at 125°C, A1280A-PGA176, W/L U1H511, 77pcs, 615hrs at 125°C, and A1280A-CQ172, W/L U1H439, 18pcs, 1000 hrs at 125°C.
  - Added: A1280A-CQFP172, W/L FP5986501, 80pcs, 1000 hrs at 125°C.
- Updated 0.45 µm UMC FPGA Reliability Summary Table 28, High Temperature Operating Life (HTOL) to Table 31, High Temperature Storage (HTS), 150 °C. Corrected the W/L numbers and date codes for all line items.
- Updated 0.25 µm FPGA reliability data, FIT improved from 1.25 to 1.18.
- Table 46, CMOS Reliability–High Temperature Operating Life (HTOL), added three new line items:
  - RTSX72SU-CQ256, W/L D303Y1,80 pcs, 6000 hrs at 125°C
  - RTSX72SU-CQ208, W/L D1SG11, 24 pcs, 2000 hrs at 125°C
  - RTSX32SU-CQ84, W/L D1RH51, 24 pcs, 2000 hrs at 125°C
- Updated 0.22 µm FPGA reliability data, FIT changed from 1.834 to 1.831. Table 49, Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs, added one new line item:
  - A54SX72A-CQ208, W/L D4TW61, 80 pcs, 1000 hrs at 125°C
- Correction to Table 49, Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs for total devices tested:
  - In revision 8, total devices was incorrectly reported as 4770 (typo); should have been 4470 (Total Device Hrs and corresponding FIT were reported correctly).
  - For Revision 9, total device tested = 4470 + 80 = 4550.
- Updated 0.15 µm FPGA reliability data, FIT changed from 7.58 to 7.25. Table 60, High Temperature Operating Life (HTOL), added six new line items:
  - RTAX2000S-CQFP352, W/L D517P1, 79 pcs, 1500 hrs at 125 °C
  - RTAX2000S-CQFP352, W/L D4CYF1, 80 pcs, 1000 hrs at 125 °C
  - RTAX2000S-CQFP352, W/L D4CYF1, 8 pcs, 2000 hrs at 125 °C
  - RTAX4000S-CQFP352, W/L D3T0N1, 44 pcs, 1000 hrs at 125 °C
  - RTAX4000S-CGA1152, W/L D404N1, 6 pcs, 1000 hrs at 125°C
  - RTAX4000D-CQFP352, W/L D4LJQ1, 47 pcs, 1000 hrs at 125°C
- Table 63, Temperature Cycle:
  - Added new line RTAX4000D-CQFP352, W/L D4LJQ1, 15 pcs, 100 cycles at –65°C to 150°C.
  - Removed reference to note as all TC line items tested from –65°C to 150°C.
- Updated 0.13 µm Infineon Flash FPGA (ProASIC3 – A3P) reliability data: Table 67, Temperature Cycle (T_C), –55 °C to +125 °C: Added new line
  - A3P250-VQFP100, W/L ZA840056, 47 pcs, 500 cycles at –65°C to +150°C
- Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH: Added new line
  - A3P250-VQFP100, W/L ZA840056, 47pcs, 100 hrs of UHAST at 130 °C, 85% RH
- Updated 0.13 µm Infineon Flash FPGA (Fusion – AFS) reliability data: Table 75, Temperature Cycle (T_C), –55 °C to +125 °C: Added new line
  - AFS600-FPGAG4881, W/L ZA932055, 47 pcs, 1000 cycles at –55°C to +125°C
- Updated 0.13 µm Infineon Flash FPGA (SmartFusion – A2F) reliability data, FIT improved from 30.11to 11.7. Table 82, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Updated additional HTOL hrs and a new line for A2F500:

- Updated A2F200-FGG484, W/L ZA917060/ZA91706101/ZA94100501, 247 pcs to 2000 hrs
- Updated A2F200-FGG484, W/L ZA925010, 82 pcs to 1000 hrs
- Added A2F500-FGG484, W/L ZA0140281, 82 pcs, 1000 hrs at 136°C

- Updated 0.13 µm UMC Flash FPGA Reliability Data (IGLOO – AGL/AGLE; IGLOO PLUS – AGLP; IGLOO nano - AGLN). Table 89, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Added HTOL data, FIT improved from 7.70 to 7.22
  - Added AGL600-FGG256, W/L QHSYQ, 79 pcs, 1000 hrs at 130°C
- Updated 0.13 µm UMC Flash FPGA reliability data (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3/EL – A3PL, AEPEL; ProASIC3 nano – A3PN, RT ProASIC3 – RT3P). Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Reformatted entire table to show data correctly.
- Updated units and Tj for line item below, FIT improved from 17.86 to 16.60. RT3PE3000L-CGA896, W/L QHR8G, 82 pcs, 1000 hrs at 142°C
  - Updated Tj to 142°C from 125°C (Ta)
  - Updated units from 79 to 82
- Table 98, Temperature Cycle (TC), –55 °C to +125 °C: Added new line:
  - RT3PE3000L-CGA8962, W/L QHR8G, 15 pcs, 100 cycles at –65°C to +150°C
- Table 100, High Temperature Storage (HTS), 150 °C: Added new line:
  - ·A3PE3000-FPGAG484, W/L QHR8G, 72 pcs, 3000 hrs at 150°C

1.10 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology. FIT rates for the following device technology have been updated:
  - 1.0 µm CMOS FPGA
  - 0.8 µm CMOS FPGA
  - 0.45 µm CSM CMOS FPGA
  - 0.45 µm UMC CMOS FPGA – Added
  - 0.25 µm UMC CMOS FPGA
  - 0.22 µm UMC Flash CMOS FPGA
  - 0.15 µm UMC CMOS FPGA
  - 0.13 µm Infineon Flash CMOS FPGA
  - 0.13 µm UMC Flash CMOS FPGA
- Added footnote for MTBF versus MTTF under Table 1, Reliability Summary: FIT Rate by Device Technology.
- For 0.8 µm CMOS FPGA, Table 1, Reliability Summary: FIT Rate by Device Technology had a typo of 1 failure (Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family and Table 14, 0.8 µm FPGA High Temperature Operating Life (HTOL) were correct).
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family. FIT rates for following device technology have been updated:
  - 1.0 µm CMOS FPGA, ACT1 & ACT2
  - 0.8 µm CMOS FPGA (ACT3)
  - 0.45 µm CSM CMOS FPGA
  - 0.45 µm UMC CMOS FPGA – Added
  - 0.25 µm UMC CMOS FPGA (RTSX-SU)
  - 0.22 µm UMC Flash CMOS FPGA (ProASICPLUS)
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm Infineon Flash CMOS FPGA (ProASIC3 – A3P)
  - 0.13 µm Infineon Flash CMOS FPGA (Fusion – AFS)
  - 0.13 µm Infineon Flash CMOS FPGA (SmartFusion – A2F)
  - 0.13 µm UMC Flash CMOS FPGA (IGLOO - AGL)
  - 0.13 µm UMC Flash CMOS FPGA (ProASIC3 – A3P/RT3PEL)
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010).
- Updated 1.0 µm FPGA reliability data, FIT improved from 6.49 to 5.57.
- Table 7, High Temperature Operating Life (HTOL): Added HTOL data and footnote 3. Removed duplicate entry for A1280A-CQ172B, W/L U1H486, 1000 hrs at 125°C.
- Updated 0.8 µm FPGA reliability data, Table 14, 0.8 µm FPGA High Temperature Operating Life (HTOL). Added HTOL data; FIT improved from 5.46 to 4.47.

- Updated 0.45 µm CSM FPGA reliability data, Table 24, High Temperature Operating Life (HTOL). Added HTOL data; FIT improved from 26.8 to 22.3.
- Updated 0.45 µm UMC FPGA Reliability Data to ORT Report: Added the following tables:
  - Table 28, High Temperature Operating Life (HTOL)
  - Table 29, Biased Humidity Accelerated Stress Test (HAST), 110°C / 85% RH
  - Table 30, Temperature Cycle (TC), –55°C to +125°C
  - Table 31, High Temperature Storage (HTS), 150 °C
- Updated 0.25 µm UMC FPGA reliability data, Table 46, CMOS Reliability–High Temperature Operating Life (HTOL): Added HTOL data, FIT improved from 1.26 to 1.25.
- Updated 0.22 µm UMC FPGA reliability data, Table 54, High Temperature Operating Life (HTOL): Added HTOL data, FIT improved from 18.59 to 15.85.
- Updated 0.15 µm FPGA reliability data, FIT improved from 10.47 to 7.58.
  - Table 60, High Temperature Operating Life (HTOL): Added RTAX-S HTOL data.
  - Table 61, Low Temperature Operating Life (LTOL): Added RTAX-S LTOL data.
- Updated 0.13 µm Infineon Flash FPGA (ProASIC3 – A3P) reliability data, Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles: Added ProASIC3 HTOL data. FIT improved from 4.40 to 4.18.
- Updated 0.13 µm Infineon Flash FPGA (Fusion – AFS) reliability data, Table 73, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Added AFS HTOL data, FIT improved from 6.61 to 6.51.
- Added 0.13 µm Infineon Flash FPGA (SmartFusion – A2F) reliability data. Added the following tables:
  - Table 82, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles
  - Table 83, High Temperature Storage (HTS), 150 °C
  - Table 86, Endurance (eNVM)
  - Table 87, Retention (eNVM) after 1100 Program/Erase Cycles
  - Table 88, Low Temperature Retention and Read Disturb (eNVM) at 25 °C after 1100 Program/Erase Cycles, 25 °C
- Updated 0.13 µm UMC Flash FPGA Reliability Data (IGLOO – AGL/AGLE; IGLOO PLUS – AGLP; IGLOO nano - AGLN)
  - Table 89, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Added HTOL data, FIT improved from 10.94 to 7.70
  - Table 91, Temperature Cycle (TC), –55 °C to +125 °C: Added TC Data
  - Table 93, High Temperature Storage (HTS), 150 °C: Added HTS Data
  - Table 94, Endurance 550 Program/Erase Cycles: Added Endurance Data
  - Table 95, Retention at 250 °C after 550 Program/Erase Cycles: Added Retention Data
- Updated 0.13 µm UMC Flash FPGA reliability data (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3/EL – A3PL, AEPEL; ProASIC3 nano – A3PN)
  - Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: Added HTOL Data, one failure reported at 3000 hrs of HTOL operation at Tj 135.24C, which is equivalent to 44 years of operation at 55C. Footnote added
  - Table 100, High Temperature Storage (HTS), 150 °C: Added HTS Data

1.11 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology: FIT Rate by Device Technology: FIT rates for following Device Technology have been updated:
  - 0.45 µm CMOS FPGA
  - 0.15 µm UMC CMOS FPGA
  - 0.13 µm Infineon Flash CMOS FPGA
  - 0.13 µm UMC Flash CMOS FPGA
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family: FIT Rate by Device Technology and Product Family: FIT rates for following Device Technology have been updated:
  - 0.45 µm CMOS FPGA
  - 0.15 µm UMC CMOS FPGA (RTAX-S)
  - 0.13 µm Infineon Flash CMOS FPGA (ProASIC3 – A3P)
  - 0.13 µm Infineon Flash CMOS FPGA (Fusion - AFS)

- 0.13 µm UMC Flash CMOS FPGA (IGLOO – AGL)
- 0.13 µm UMC Flash CMOS FPGA (ProASIC3 – A3P)

- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010):
  - Updated ESD data for A3P, AFS, A3PL, and AGL
  - Added ESD data for AGLP and RTAX4000S
- Added Table 5, Summary of ESD Performance for AEC-Q100 Qualified Product Families (AEC-Q100-002)
- Updated 0.45 µm (MX) FPGA Reliability Data, Table 24, High Temperature Operating Life (HTOL), Table 26, Unbiased Humidity, and Table 27, Temperature Cycle.
  - Updated HTOL Table 23, High Temperature Operating Life (HTOL): A42MX36-CQ208, 1/77units failed at 168 hrs, total 1000 hrs @ 125°C
  - Updated Un biased HAST Table 25, Biased Humidity (HAST): A42MX24-PQG208, 47 units, 100 hrs
  - Updated TC Table 26, Unbiased Humidity: A42MX24-PQG208, 47 units, 1000 cycles
- UpdatedAntifuse FIT Rate Calculator, page 49.
  - Updated Antifuse FIT from 23 to 17
  - Updated the version of calculator
- Updated 0.22 µm (SXA) UMC FPGA Reliability Data Table 52, Biased Humidity (HAST) and Table 53, Temperature Cycle.
  - Updated Un biased HAST Table 46, CMOS Reliability–High Temperature Operating Life (HTOL): A54SX72A-PQG208, 47 units, 100 hrs
  - Updated TC Table 47, CMOS Reliability Low Temperature Operating Life (LTOL): A54SX72A-PQG208, 46 units, 1000 cycles
- Updated 0.22 µm Flash (APA) FPGA Reliability Data in Table 59, Temperature Cycle.
  - Updated TC Table 53, Temperature Cycle: APA1000-PQG208, 46 units, 1000 cycles
- Updated 0.15 µm UMC CMOS FPGA (RTAX-S) Reliability Data, Table 60, High Temperature Operating Life (HTOL).
  - Updated and added additional 1494138 Unit Hrs of RTAX-S data, 1 SRAM failure at 1000 hrs
- Updated 0.13 µm Infineon Flash FPGA (ProASIC3 – A3P) Reliability Data, Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles, Table 67, Temperature Cycle (T_C), –55 °C to +125 °C, Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH, and Table 70, Temperature Humidity Bias (THB), 85 °C / 85% RH:
  - Updated HTOL Table 58, Retention 225 °C Unbiased 100% Erased: A3P1000-FGG484, 231 units, 1000 hrs @ 134°C (total 2008 hrs)
  - Updated TC Table 60, High Temperature Operating Life (HTOL): A3PE1500-PQG208, 48 units, 1000 cycles
  - Updated Biased HAST Table 61, Low Temperature Operating Life (LTOL): A3PE1500-PQG208, 47units, 100 hrs
  - Updated THB Table 63, Temperature Cycle: A3P1000- PQG208, 22units, 2000 hrs, A3P1000- PQG208, 22units, 2000 hrs, A3P1000- FGG256, 22units, 2000 hrs, and A3P250- FGG256, 22units, 2000 hrs
- Updated 0.13 µm Infineon Flash FPGA Reliability Summary (Fusion – AFS), page 72, Table 73, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles through Table 81, Retention (eNVM) at 250 °C after 1000 Program/Erase Cycles.
  - Updated HTOL Table 66, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles: AFS1500-FGG256/FG256, 110 units, 1000 hrs @ 135°C, AFS600-FG256, 68 units, additional 2200 hrs @ 141°C (total 3200 hrs)
  - Updated LTOL Table 67, Temperature Cycle (T_C), –55 °C to +125 °C: AFS1500-FGG256, 68 units, 1000 hrs @ –55°C
  - Updated TC Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH: AFS1500-FGG256, 48 units, 1000 cycles
  - Updated HTS Table 69, High Temperature Storage (HTS), 150 °C: AFS1500-FGG256, 50 units, 1000 cycles
  - Updated HAST Table 70, Temperature Humidity Bias (THB), 85 °C / 85% RH: AFS1500-FGG256, 69 units, 264 hrs
  - Updated Endurance NVM Table 71, Endurance (Room Temperature): AFS1500-FGG256/FG256, 77 units, 550 cycles
  - Updated Retention Table 73, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: AFS1500-CQ208, 77 units, 168 hrs

- Updated 0.13 µm UMC Flash FPGA Reliability Summary (IGLOO—AGL/AGLE; IGLOO PLUS–AGLP; IGLOO nano–AGLN), page 78, Table 89, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles, Table 90, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles, Table 91, Temperature Cycle (TC), –55 °C to +125 °C, and Table 93, High Temperature Storage (HTS), 150 °C.
  - Updated HTOL Table 75, Temperature Cycle (T_C), –55 °C to +125 °C: AGLE3000-FGG484, 45 units, 1000 hrs @ 130°C, AGL1000-FGG484, 129 units, 1000 hrs @ 132°C, and AGLP125-VQ100, 129 units, 1000 hrs @ 128°C
  - Updated LTOL Table 76, High Temperature Storage (HTS), 150 °C: Corrected typo for total number of units
  - Updated TC Table 77, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH: AGL600-FG256, 80 units, 1000 cycles, and AGLP125-VQ100, 129 units, 1000 cycles
  - Updated HTS Table 79, Endurance (eNVM) at Room Temperature: AGLP125-VQ100, 129 units, 1000 cycles
- Added to 0.13 µm UMC Flash FPGA Reliability Summary (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3EL – A3PL, A3PEL; ProASIC3 nano – A3PN, RT ProASIC3 – RT3P), page 82, Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles: High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles:
  - A3PE3000-FGG484, 129 units, additional 1000 hrs @ 135°C (total 2000 hrs)

1.12 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 1, Reliability Summary: FIT Rate by Device Technology: FIT rates for following Device Technology have been updated/added:
  - Updated 0.13 µm Infineon Flash CMOS FPGA
  - Added 0.13 µm UMC Flash CMOS FPGA
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family: FIT rates for following Device Technology have been updated/added:
  - Updated 0.13 µm Infineon Flash CMOS FPGA (ProASIC3 – A3P)
  - Added 0.13 µm Infineon Flash CMOS FPGA (Fusion – AFS)
  - Added 0.13 µm UMC Flash CMOS FPGA (IGLOO – AGL)
  - Added 0.13 µm UMC Flash CMOS FPGA (ProASIC3 – A3P)
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010): ESD Performance
  - Format ESD data reported for eX, SX-A, RTSX-S and RTSX-SU
  - Updated ESD data for A3P
  - Added ESD data for AFS and AGL
- Updated entire0.13 µm Infineon Flash FPGA Reliability Summary (ProASIC3 – A3P), page 66, Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles to Table 72, Retention at 250 °C After 550 Program/Erase Cycles:
- Formatted all table headers added more information (test conditions, etc.)
- Updated Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles:
  - A3P125- FGG144, 82 units, 1000 hrs @ 130°C
  - A3P1000-FGG484, 231 units, 1008 hrs @ 134°C
  - A3P1000-FGG484, 2427 units, 48 hrs @ 134°C
  - A3PE1500-FGG484, 77 units, 1000 hrs @ 134°C
- Updated Table 66, Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles: A3PE1500-FGG484, 77 units, 1000 hrs @ –55°C
- Updated Table 67, Temperature Cycle (T_C), –55 °C to +125 °C, –55°C to +125°C:
  - A3P1000-FGG484, 231 units, 1000 cycles
  - A3PE1500-FGG484, 77 units, 1000 cycles
- Updated Table 68, Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH:
  - A3P1000-FGG484, 231 units, 96 hrs
  - A3PE1500-FGG484, 77 units, 264 hrs
- Added new data and tables for Table 69, High Temperature Storage (HTS), 150 °C and Table 70, Temperature Humidity Bias (THB), 85 °C / 85% RH.
- Updated Table 71, Endurance (Room Temperature):
  - A3P1000-FGG484, 231 units, 550 cycles

    - A3PE1500-FGG484, 77 units, 550 cycles
- Updated Table 72, Retention at 250 °C After 550 Program/Erase Cycles:
    - A3P1000-CQ208, 231 units, 1008 hrs @ 150°C
    - A3P1000-CQ208, 149 units, 3000 hrs @ 250°C
    - A3PE1500-CQ208, 77 units, 1000hrs @ 250°C
- Added the 0.13 µm Infineon Flash FPGA Reliability Summary (Fusion – AFS), page 72, Table 73, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles to Table 81, Retention (eNVM) at 250 °C after 1000 Program/Erase Cycles.
- Added the 0.13 µm UMC Flash FPGA Reliability Summary (IGLOO—AGL/AGLE; IGLOO PLUS–AGLP; IGLOO nano–AGLN), page 78; IGLOO, Table 89, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles, to Table 95, Retention at 250 °C after 550 Program/Erase Cycles.
- Added the 0.13 µm UMC Flash FPGA Reliability Summary (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3EL – A3PL, A3PEL; ProASIC3 nano – A3PN, RT ProASIC3 – RT3P), page 82; Table 96, High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles, to Table 100, High Temperature Storage (HTS), 150 °C.

1.13 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- ORT Report updates are not done quarterly, usually updated twice a year or by request from Actel Technical Review Board (TRB). Labels referencing quarter/year are being replaced with a revision number. This version of the ORT report is Rev 4.
- Updated Table 1, Reliability Summary: FIT Rate by Device Technology: FIT rates for following Device Technology have been updated
    - 0.25 µm UMC CMOS FPGA
    - 0.22 µm UMC Flash CMOS FPGA
    - 0.15 µm UMC CMOS FPGA
    - 0.13 µm Infineon Flash CMOS FPGA
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family: FIT rates for following Device Technology have been updated
    - 0.25 µm UMC CMOS FPGA (RTSX-SU)
    - 0.22 µm UMC Flash CMOS FPGA (ProASICPLUS)
    - 0.15 µm UMC CMOS FPGA (Axcelerator)
    - 0.15 µm UMC CMOS FPGA (RTAX-S)
    - 0.13 µm Infineon Flash CMOS FPGA (ProASIC3)
- Updated Table 46, CMOS Reliability–High Temperature Operating Life (HTOL): 0.25 µm UMC RTSX-SU HTOL data
    - Updated test time (added 250 hrs) for RTSX32SU, CQFP208, W/L D1JW21 and D1AYJ1, DC 0519 and 0502: 150 units, Test Time = 750, Unit Hrs = 112500
    - Added new data: RTSX32SU, CQFP208, W/L D1JW21 and D1AYJ1, DC 0519 and 0502, 150 units, Test Time = 750, Unit Hrs = 112500
    - Updated the TOTAL Units for 0.25 µm FPGA to 4744 and Total Test Time Hours = 9299758
- Updated Table 47, CMOS Reliability Low Temperature Operating Life (LTOL): 0.25 µm UMC RTSX-SU LTOL data
    - Updated test time (added 500 hrs) for RTSX32SU, CQFP208, W/L D1JW21 and D1AYJ1, DC 0519 and 0502: 150 units, Test Time = 1000, Unit Hrs = 150000
    - Added new data: RTSX32SU, CQFP208, W/L D1JW21 and D1AYJ1, DC 0519 and 0502, 150 units, Test Time = 500, Unit Hrs = 75000
    - Updated the TOTAL Units for 0.25 µm FPGA to 1376 and TOTAL Test Time Hours to 1767244
- Updated Figure 52, page 54: 0.22 µm UMC SX-A Biased Humidity (HAST) data
    - Added new data: A54SX32A, PBGA329, W/L D26E61, DC 0610, 45 units, Test Time = 528, Unit Hrs = 23760
    - Updated the TOTAL Units for 0.22 µm FPGA to 195 and TOTAL Test Time Hours to 38760
- Updated Table 53, Temperature Cycle: 0.22 µm UMC SX-A Temperature Cycle data
    - Added new data: A54SX32A, PBGA329, W/L D26E61, DC 0610, 22units, Test Cycles = 1000, Unit Cycles = 22000
    - Updated the TOTAL Units for 0.22 µm FPGA to 577 and Total Test Cycles to 539000
    - Removed the generic (-65°C - +150°C) row and added footnotes for (-65°C - +150°C) and (-55°C - +125°C) for each line in the table

- Updated Table 54, High Temperature Operating Life (HTOL): 0.22 µm UMC Flash APA HTOL data
  - Updated test time (added 500hrs) for APA1000, CQFP352, W/L MK3KA, DC 0517, 132 units, Test Time = 1115 Unit Hrs = 147180
  - Updated the Total Test Time Hours = 631548
- Updated Table 57, Retention 225 °C Unbiased 100% Programmed and Table 58, Retention 225 °C Unbiased 100% Erased: 0.22 µm UMC Flash APA Retention Programmed and Erased
  - The W/L numbers for APA1000, CGA391, 73 units was incorrectly stated as ZA026941, corrected to MAE49, MC147, MC148.
- Updated Table 60, High Temperature Operating Life (HTOL): 0.15 µm UMC Axcelerator and RTAX-S HTOL data
  - Updated test time (added 1000 hrs@132°C) for RTAX1000S, , W/L D1GAH1, DC 0444, 120 units, Test Time @ 132°C = 6000, Unit Hrs @ 125°C = 1024560
  - Updated test time (added 832 hrs @132°C) for RTAX1000S, , W/L D1KH51, 37 units, Test Time @ 132°C = 1000, Unit Hrs @125°C = 52651
  - Updated test time (added 832 hrs @ 132°C) for RTAX1000S, CQFP352, W/L D1KH51, 8units, Test Time @ 132°C = 1000, Unit Hrs @125°C = 11384
  - Added new data: AX2000, FPGA896, W/L D2A5A1, DC 0620, 77 units, Test Time = 1000 @ 125°C, Unit Hrs @ 125°C = 77000
  - Added new data: RTAX1000S, , W/L D1KH51, 24 units, Test Time @ 132°C = 168, Unit Hrs @125°C = 5736
  - Added new data: RTAX2000S, CQFP352, W/L D1NSG1, 14 units, Test Time @ 132°C = 168, Unit Hrs @ 125°C = 3346
  - Added new data: RTAX250S, CQFP208, W/L D1H381, 6 units, Test Time @ 125°C = 1000, Unit Hrs @ 125°C = 6000
  - Added new data: RTAX2000S, CQFP352, W/L D1KHN1, 78 units, Test Time @ 125°C = 1000, Unit Hrs @125°C = 78000
  - Added new data: RTAX1000S, CQFP352, W/L D1NR91, 24 units, Test Time @ 132°C = 168, Unit Hrs @ 125°C = 5736
  - Added new data: RTAX2000S, CQFP352, W/L D1KHN1, 14 units, Test Time @ 132°C = 168, Unit Hrs @ 125°C = 3346
  - Added new data: RTAX2000S, CQFP352, W/L D21PH1, 6 units, Test Time @ 125°C = 168, Units Hrs @ 125°C = 1008
  - Updated the TOTAL Units for 0.15 µm FPGA to 1397 and Total Test Cycles = 2310665
- Updated Table 61, Low Temperature Operating Life (LTOL): 0.15 µm UMC Axcelerator and RTAX-S LTOL data
  - Added new data: RTAX2000S, CQFP352, W/L D1KHN1, 78 units, Test Time = 168, Unit Hrs = 13104
  - Updated the TOTAL Units for 0.15 µm FPGA = 992 and Total Test Time Hours = 481604
  - Updated the TOTAL Units for 0.13 µm FPGA = 633 and Total Test Time Hours = 1531494
- Updated Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles: 0.13 µm IFX A3P HTOL data
  - Changed the table format to report TJ and Test Time during HTOL testing and Test Time at TJ 125°C
  - Added new data: A3P060, FPGA256, W/L ZA612052, DC 0626, 129 units, Test Time @ 133°C = 1000, Unit Hrs @ 125°C = 192855
  - Added new data: A3P250, FPGA256, W/L ZA628252.05, DC 0628, 77 units, Test Time @ 133°C = 1000, Unit Hrs @ 125°C = 115115
  - Added new data: A3P400, FPGA256, ZA614042, DC 0637, 77units, Test Time @ 133°C = 1000, Unit Hrs @ 125°C = 115115
- Updated Table 71, Endurance (Room Temperature) and Table 72, Retention at 250 °C After 550 Program/Erase Cycles: Removed text “Room Temperature” as these are run at 250°C

1.14 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Added tables Table 65, High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles through Table 72, Retention at 250 °C After 550 Program/Erase Cycles for 0.13 µm IFX CMOS FPGA (ProASIC3).

- Updated Table 57, Retention 225 °C Unbiased 100% Programmed and Table 61, Low Temperature Operating Life (LTOL).
  - Added AX2000-FPGA896, W/L D16T91, DC0431 to Table 60, High Temperature Operating Life (HTOL).
  - Added RTAX-S Data to Table 60, High Temperature Operating Life (HTOL) and Table 61, Low Temperature Operating Life (LTOL).
- Updated Table 54, High Temperature Operating Life (HTOL).
  - Added APA1000-CQ256, W/L MK3K1, DC 0517, 132 units, Test Time = 615, Unit Hrs = 81180.
- Updated Table 46, CMOS Reliability–High Temperature Operating Life (HTOL), 0.25 µm UMC RTSX-SU HTOL data.
  - Updated RTSX72SU, CQFP208, W/L D1AYH1 and D1KT11, DC 0519 and 0445—73 units, Test Time = 31,237, Unit Hrs = 2280268; 5 units, Test Time = 20,824, Unit Hrs = 104122
  - Added RTSX32SU, CQFP208, W/L D1JW21 and D1AYJ1, DC 0519 and 0502: 150units, Test Time = 500, Unit Hrs = 75000.
  - Added RTSX72SU, CQFP256, W/L D1N2W1, 77units, Test Time = 1000, Unit Hrs = 7000.
- Updated Table 47, CMOS Reliability Low Temperature Operating Life (LTOL), 0.25 µm UMC RTSX-SU LTOL data.
  - Added RTSX32SU, CQFP208, W/L D1JW21and D1AYJ1, DC 0519 and 0502: 150 units, Test Time = 500, Units Hrs = 75000.
  - Updated RTSX32SU, CQFP208, W/L D122H1 and D1JW21, DC 0434 and 0442—152 units, Test Time = 5000, Unit Hrs = 760000; 2 units, Test Time = 4000, Unit Hrs = 8000
  - Updated RTSX32SU, CQFP208, W/L D1AYH1 and D1KT11, DC 0445 and 0519:
  - 75 units, Test Time = 6000, Unit Hrs = 450000.
- Updated Table 4, Summary of ESD Performance for All Product Families (TM 3015/JS001-2010) ESD Performance for RTAX-S and ProASIC3.
- Updated Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family.
  - Updated 0.25 µm UMC CMOS FPGA (RTSX-SU) data
  - Updated 0.15 µm UMC CMOS FPGA (Axcelerator) data
  - Added 0.15 µm UMC CMOS FPGA (RTAX) data
  - Added 0.13 µm IFX CMOS FPGA (ProASIC3) data
- Updated Table 1, Reliability Summary: FIT Rate by Device Technology.
  - Updated 0.25 µm UMC CMOS FPGA data
  - Updated 0.15 µm UMC CMOS FPGA data
  - Added 0.13 µm IFX CMOS FPGA data

1.15 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Note relating to UMC 0.25 µm RTSX-SU antifuse FIT rates added to Table 1, Reliability Summary: FIT Rate by Device Technology.
- XL and DX devices in 0.8 µm CMOS FPGA were removed from Table 3, Reliability Summary: FIT Rate by Device Technology and Product Family and Table 15, 85°C/85%Temperature Humidity Bias.
- Removed “Table 9. Thermal Shock." Table had header only; no data.
- Revised entire section 0.25 µm UMC FPGA Reliability Summary, page 46 and added new data from UMC 0.25 µm RTSX-SU antifuse reliability testing.
- Revised entire section 0.22 µm UMC FPGA Reliability Summary, page 51 and added new data from UMC 0.22 µm A54SX72A antifuse reliability testing.
- Started including the Date Codes for the packages used in the reliability studies.
- New ORT data has been added, 0.22 µm Flash FPGA (Table 52, Biased Humidity (HAST)).
- 0.22/0.25 µm CMOS FPGA results have been updated with new test results.

1.16 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- Product 1010A was removed from 1.0 µm FPGA, ACT1 Family.
- All the earlier devices manufactured by TI were removed from 1.0 µm FPGA, ACT1, and ACT2 Families.
- Industry standard nomenclature was used for the package names.

- All the FIT rates were checked and corrected as necessary
- The Group E Inspection—Generic Data (Radiation Hardness), page 25 section has been added.
- ESD performance data has been removed.

2 Overview

2.1 Accelerated Reliability Testing

The failure rate of semiconductor devices is inherently small. For this reason, Microsemi uses accelerated testing to assess reliability of its FPGA and SoC devices. Over-stresses are used to produce the same failure mechanisms that would be seen under normal conditions but in a much shorter period of time. Acceleration factors are used by Microsemi to estimate failure rates based on the results of accelerated testing. The objective of this testing is to identify the failure mechanisms and eliminate them as a cause of failure during the useful life of Microsemi's FPGA and SoC products.

Die selection is determined by both the largest die size and/or the currently available die. Microsemi will, whenever possible, test the largest die in a given family. Package selection for the testing is determined by test board availability and will not always include the largest package available. The primary use of this report is to include the reliability data of the silicon devices.

2.1.1 Standard FIT Rate and MTTF Assumptions

All of the Failure in Time (FIT) rates and Mean Time to Failure (MTTF) numbers reported here use a base set of assumptions. FIT rate is calculated using JESD85 (Methods for Calculating Failure Rates in Units of FITs) standard. The failure rate is calculated using -square distribution at 60% confidence interval from the small number of failures and limited sample size of the population tested. The -squared value is calculated from the inverse -squared distribution using the desired probability level and degrees of freedom. The failure rate is then calculated from the -square value:

$$\text{Failure Rate} = \frac{\chi^2 10^9}{2(\text{A.F.} \times \text{Device Hours})}$$

EQ 1

Where ?2 = -Squared value at 60% confidence level and (2f + 2) degrees of freedom, where f is the number of failures, Device Hours = (No. of Devices) × (No. of Hours)

Equivalent Device Hours= D × H × A.F.

The Acceleration Factor (A.F.) is calculated using the Arrhenius relationship.

Acceleration Factor = Exp {(E_a/k) × (1/Tuse – 1/Tstess)}

EQ 2

Where:

E_a = Activation Energy (eV), assumed 0.7 eV

k = Boltzmann's constant (8.617 × 10–5 eV/K)

Tstress = Temperature at accelerated conditions in degrees Kelvin (K = 125 °C + 273.16)

Tuse = Temperature at normal use conditions in degrees Kelvin (K = 55 °C + 273.16)

A.F. = Acceleration Factor

Assuming that the actual usage voltage is within the rated specification, acceleration coefficients are calculated for temperature stress. Sample sizes, total devices tested, device hours, and failures can be found in the data tables for each product family. The Arrhenius Life-Temperature relationship is widely used to model product life as a function of temperature. This relationship is used to express both a single failure mechanism's sensitivity to temperature and the product thermal acceleration factor.

2.1.2 Table Footnotes

Notes at the end of each table correspond to the numbers indicated by the superscript in the product column of that table. Failures indicated in parentheses represent false failures due to ESD or EOS.

3 Reliability Summary

3.1 Reliability Summaries

Table 1 • **Reliability Summary: FIT Rate by Device Technology**

Device Technology	Number of CMOS Failures	Equivalent Device Hours	TJ (°C)	EA, eV	Confidence	FIT	MTTF
1.0 µm CMOS FPGA	1	3.66E+08	55	0.7	60%	5.53	1.81E+08
1.0 µm CMOS FPGA (RH1020)	0	3.97E+07	55	0.7	60%	23.05	4.34E+07
0.8 µm CMOS FPGA (RH1280)	1	9.16E+07	55	0.7	60%	22.04	4.54E+07
0.8 µm CMOS FPGA	0	2.17E+08	55	0.7	60%	4.21	2.37E+08
0.6 µm CMOS FPGA	0	1.82E+08	55	0.7	60%	5.04	1.99E+08
0.6 µm RT54SX CMOS FPGA	0	2.29E+07	55	0.7	60%	39.88	2.51E+07
0.45 µm CSM CMOS FPGA	1	1.09E+08	55	0.7	60%	18.05	5.41E+07
0.45 µm UMC CMOS FPGA	0	5.15E+07	55	0.7	60%	17.78	5.62E+07
0.35 µm CMOS FPGA	0	6.31E+07	55	0.7	60%	14.51	6.89E+07
0.25 µm MEC CMOS FPGA	2	7.51E+07	55	0.7	60%	41.40	2.42E+07
0.25 µm Infineon Flash CMOS FPGA	0	3.62E+07	55	0.7	60%	25.30	3.95E+07
0.25 µm UMC CMOS FPGA	0	7.96E+08	55	0.7	60%	1.15	8.70E+08
0.22 µm UMC CMOS FPGA	0	5.31E+08	55	0.7	60%	1.72	5.81E+08
0.22 µm UMC Flash CMOS FPGA	0	1.01E+08	55	0.7	60%	9.10	1.10E+08
0.15 µm UMC CMOS FPGA	2	5.79E+08	55	0.7	60%	5.36	1.86E+08
0.13 µm Infineon Flash CMOS FPGA	0	4.57E+08	55	0.7	60%	2.00	4.99E+08
0.13 µm UMC Flash CMOS FPGA	1	2.89E+08	55	0.7	60%	7.00	1.43E+08
65 nm UMC Flash CMOS FPGA	0	3.38E+08	55	0.7	60%	2.71	3.69E+08
28 nm UMC SONOS Flash FPGA	4	2.26E+08	55	0.7	60%	23.13	4.32E+07
0.6 µm XFAB MSA	0	1.93E+06	55	0.7	60%	6.07	1.65E+08
0.8 µm XFAB MSA	0	5.93E+05	55	0.7	60%	19.79	5.05E+07
1.0 µm XFAB MSA	0	1.19E+08	55	0.7	60%	7.70	1.30E+08

Note: Refer to the 0.25 µm UMC FPGA Reliability Summary, page 46 for RTSX-SU antifuse FIT rate reliability data.

Note: Technically, mean time between failures (MTBF) should be used only in reference to repairable items, while MTTF should be used for non-repairable items. However, MTBF is commonly used for both repairable and non-repairable items, hence MTTF or MTBF = 1/FIT.

Note: MSA products comprise hi-rel, industrial and other products

Table 2 • **List of MSA Products**

Product Family	Product/Product Family
Industrial/Other	AA 51X, AA 53X, AA 54X, AA 55 X, AA 56X, AA 58X
	P XXX
Hi-rel	AAHS298, AA 7XX, AA 6XX
	LX 45XX, LX 77XX

Table 3 • **Reliability Summary: FIT Rate by Device Technology and Product Family**

Device Technology and Product Family	Number of CMOS Failures	Equivalent Device Hours	TJ (°C)	EA, eV	Confidence	FIT	MTTF
1.0 µm CMOS FPGA	1	3.66E+08	55	0.7	60%	5.53	1.81E+08
– *ACT1*	1	1.93E+08	55	0.7	60%	10.49	9.53E+07
– *ACT2*	0	1.73E+08	55	0.7	60%	5.29	1.89E+08
1.0 µm CMOS FPGA (RH1020)	0	3.97E+07	55	0.7	60%	23.06	4.34E+07
0.8 µm CMOS FPGA (RH1280)	1	9.16E+07	55	0.7	60%	22.04	4.54E+07
0.8 µm CMOS FPGA (ACT3)	0	2.17E+08	55	0.7	60%	4.21	2.37E+08
0.6 µm CMOS FPGA	0	1.82E+08	55	0.7	60%	5.04	1.99E+08
– *ACT3*	0	6.13E+07	55	0.7	60%	14.93	6.70E+07
– *XL*	0	7.73E+07	55	0.7	60%	11.83	8.45E+07
– *DX*	0	4.31E+07	55	0.7	60%	21.25	4.70E+07
0.6 µm RT54SX CMOS FPGA	0	2.29E+07	55	0.7	60%	39.88	2.51E+07
0.45 µm CSM CMOS FPGA (MX)	1	1.09E+08	55	0.7	60%	18.05	5.41E+07
0.45 µm UMC CMOS FPGA (MX)	0	5.14E+07	55	0.7	60%	17.81	5.61E+07
0.35 µm CMOS FPGA (SX)	0	6.31E+07	55	0.7	60%	14.51	6.89E+07
0.25 µm MEC CMOS FPGA	2	7.51E+07	55	0.7	60%	41.40	2.42E+07
– *SX-A*	0	3.15E+07	55	0.7	60%	29.08	3.44E+07
– *RTSX™-S*	2	4.37E+07	55	0.7	60%	71.23	1.40E+07
0.25 µm Infineon Flash CMOS FPGA (ProASIC®)	0	3.62E+07	55	0.7	60%	25.30	3.95E+07
0.25 µm UMC CMOS FPGA (RTSX-SU)	0	7.96E+08	55	0.7	60%	1.15	8.70E+08
0.22 µm UMC CMOS FPGA (SX-A/eX[1])	0	5.31.E+08	55	0.7	60%	1.72	5.81E+08
0.22 µm UMC Flash CMOS FPGA (ProASICPLUS®)	0	1.01E+08	55	0.7	60%	9.10	1.10E+08
0.15 µm UMC CMOS FPGA (Axcelerator)	0	2.67E+07	55	0.7	60%	34.23	2.92E+07
0.15 µm UMC CMOS FPGA (RTAX-S)	2	5.15E+08	55	0.7	60%	6.03	1.66E+08
0.13 µm Infineon Flash CMOS FPGA (ProASIC3 – A3P)	0	2.28E+08	55	0.7	60%	4.01	2.50E+08
0.13 µm Infineon Flash CMOS FPGA (Fusion – AFS)	0	1.41E+08	55	0.7	60%	6.51	1.54E+08

Table 3 • **Reliability Summary: FIT Rate by Device Technology and Product Family *(continued)***

Device Technology and Product Family	Number of CMOS Failures	Equivalent Device Hours	TJ (°C)	EA, eV	Confidence	FIT	MTTF
0.13 µm Infineon Flash CMOS FPGA (SmartFusion–A2F)	0	8.80E+07	55	07	60%	10.39	9.62+07
0.13 µm UMC Flash CMOS FPGA (IGLOO®–AGL)	0	1.37E+08	55	0.7	60%	6.78	1.48E+08
0.13 µm UMC Flash CMOS FPGA (ProASIC3–A3P/RT3PEL)	1	1.54E+08	55	0.7	60%	13.15	7.61E+07
65 nm UMC Flash CMOS FPGA (SmartFusion®2–M2S/IGLOO®2–M2GL[2, 3])	0	2.48E+08	55	0.7	60%	3.22	3.11E+08
65 nm UMC Flash CMOS FPGA (RTG4)	0	4.82E+07	55	0.7	60%	18.98	5.27E+07
28 nm UMC SONOS Flash FPGA (PolarFire)	4[4]	2.26E+08	55	0.7	60%	23.13	4.32E+07

1. The eX family of devices is covered under the 0.22 µm FPGA family by similarity (extension). Testing is conducted on the SX-A devices for the eX family. The smallest SX-A device (A54SX08A) is the largest die equivalent to the eX256.
2. The IGLOO®2-M2GL family of devices is covered under 65 nm; SmartFusion®2-M2S FPGA family by similarity (extension). M2GL and M2S are fabricated at UMC, using the same foundry process and mask set. M2GL has a reduced product feature set compared to the M2S product family.
3. For customer defined accelerated programming qualification, the maximum number of programming cycles allowed in SmartFusion2 or IGLOO2 is defined for the life of the product. Refer to the datasheet for specifications. Typical real-life programming usage varies from one-time programming, to a few programming cycles on the production lines, to periodic in-application updates, to multiple programming cycles per day during system development and integration in a lab environment. If accelerated programming qualification is required, Microsemi recommends a maximum of 6 back-to-back programming cycles with a minimum of 15 minutes between programming cycles, followed by a 24-hour wait before the next round of programming cycles.
4. Root cause is attributed to random metal particles and metal bridging. Improvement plans are in place.

3.2 ESD Performance

Table 4 • **Summary of ESD Performance for All Product Families (TM 3015/JS001-2010)**

Product Family	ESD (Volts) HBM	Family Members	Fab Technology
ACT1	2000	A1010B, A1020B	1.0 µm
ACT2	1000	A1225A, A1240A, A1280A, RT1280A	1.0 µm
RH1020	4100	RH1020, RT1020	1.0 µm
RH1280	1500	RH1280	0.8 µm
ACT3	2000	A1415A, A1425A, A1460A, A14100A, and RT Variants	0.8 µm
XL	1500	A1225XL, A1240XL, A1280XL	0.6 µm
DX	2000	A3265DX, A32100DX, A32140DX, A32200DX, A32300DX	0.6 µm
RT54SX	2000	RT54SX16, RT54SX32	0.6 µm
MX	2000[1]	A40MX02, A40MX04,A42MX09, A42MX16, A42MX24, A42MX36	0.45 µm
SX	2000	A54SX08, A54SX16, A54SX16P, A54SX32	0.35 µm
SX-A	2000[2]	A54SX16A, A54SX32A, A54SX72A	0.25 µm
RTSX-S	2000[2]	RT54SX32S, RT54SX72S	0.25 µm

Table 4 • **Summary of ESD Performance for All Product Families (TM 3015/JS001-2010)** ***(continued)***

Product Family	ESD (Volts) HBM	Family Members	Fab Technology
ProASIC	2000	A500K050, A500K130, A500K180, A500K270	0.25 µm
RTSX-SU	2000[2]	RT54SX32SU, RT54SX72SU	0.25 µm
SX-A	2000[2]	A54SX08A, A54SX16A, A54SX32A, A54SX72A	0.22 µm
eX	2000[2]	eX64, eX128, eX256	0.22 µm
ProASIC[PLUS]	2000	APA075, APA150, APA300, APA450, APA600, APA750, APA1000	0.22 µm
Axcelerator®	2000	AX125, AX250, AX500, AX1000, AX2000	0.15 µm
RTAX-S	2000	RTAX250S, RTAX1000S, RTAX2000S, RTAX4000S	0.15 µm
ProASIC3® ProASIC3®E[3]	2000	A3P015, A3P030, A3P060, A3P125[4], A3P250, A3P400, A3P600, A3P1000, A3PE600, A3PE1500, A3PE3000	0.13 µm
ProASIC®3L ProASIC®3/EL[3] RT3PEL	2000	A3P250L, A3P600L, A3P1000L, A3PE600L, A3PE3000L, RT3PE600L[5], RT3PE3000L[5]	0.13 µm
ProASIC®3 nano[6]	2000	A3PN010, A3PN015, A3PN020, A3PN030, A3PN060, A3PN125, A3PN250	0.13 µm
Fusion®[3]	2000	AFS090[7], AFS250[7], AFS600[8], AFS1500[8]	0.13 µm
SmartFusion®[3]	2000	A2F060, A2F200, A2F500	0.13 µm
IGLOO®/IGLOO®e[3]	2000	AGL015, AGL030, AGL060[4], AGL125[4], AGL250[4], AGL400[4], AGL600[4], AGL1000[4], AGLE600[4], AGLE3000[4]	0.13 µm
IGLOO® PLUS[3]	2000	AGLP030, AGLP060[4], AGLP125[4]	0.13 µm
IGLOO® nano[6]	2000	AGLN010, AGLN015, AGLN020, AGLN060, AGLN125, AGLN250, AGLN030Z, AGLN060Z, AGLN125Z, AGLN250Z	0.13 µm
SmartFusion[2] IGLOO2	2000	M2S005, M2S010, M2S025, M2S050[9], M2S090, M2S150 M2GL005, M2GL010, M2GL025, M2GL050[9], M2GL060, M2GL090, M2GL150	65 nm
RTG4[10]	2000	RT4G150	65 nm
G5 (PolarFire)[11, 12]	2000	MPF500T, MPF300T, MPF300XT, MPF200T, MPF100T	28 nm
AA6xx	250	AA6xx	0.8 µm
AA6xx	500	AA6xx	0.8 µm
AAHS298B	2000	AAHS298B	1.0 µm
LX7710	1500	LX7710	1.0 µm
LX7730[13]	1000	LX7730	0.6 µm/1.0 µm

1. MX (Foundry UMC) passed 2000 V HBM on all pins except power supply pins Vpp and VSV, which meet 1500 V.
2. Except for 4 GNDQ pins, all other pins pass ESD performance of 2000 V, HBM. Refer to the application note at AC233: Electro-Static Discharge for more details.
   On the 4 GNDQ pins: eX devices passed 50 V HBM.
   SX-A, RTSX-S, and RTSX-SU devices passed at 75 V HBM. However, SX-A devices that are packaged in CQ 84 packages passed HBM 2000 V, including the GNDQ pins.
3. ProASIC3, ProASIC3E, ProASIC3L, ProASIC3/EL, IGLOO, IGLOOe, IGLOO PLUS, and Fusion passed 200 V CDM.
4. Passed 2000 V HBM on all pins except VCC_PLL, which meets 500 V.
5. Passed 2000 V HBM on all pins except VCC_PLL / VCOMP_PLL, which meet 500 V.
6. ProASIC3 nano, IGLOO nano, and SmartFusion passed 500 V CDM.
7. Passed 2000 V HBM on all pins except VCC33A, which meets 500 V.

8. Passed 2000 V HBM on all pins except VCC33A and VCC33PMP, which meet 250 V.
9. Passed 2000 V HBM on all pins except for the SERDES internal PLL supply which meet 1000 V HBM. Passed 500 V CDM on all pins except for SERDES internal PLL supply which meet 250 V.
10. RTG4 passes JS-001-2014 2000 V HBM, with the exception of the VDDAIO pin which meets 250 V and passes MIL-STD-883B 250 V HBM which is limited by the VDDAIO supply pin.
11. MPF500T, MPF300T, MPF300XT, MPF 200T, and MPF 100T passed 2 kV [Class 2] with the exception of Tx/Rx, which passed 1 kV [Class 1C].
12. CDM note: Pass 500V [Class C2] (non Tx/Rx) and Pass 250V [Class C1] (Tx/Rx)
13. LX7730 passed 500 V (1 kV for logic IO and supplies).

Table 5 • **Summary of ESD Performance for AEC-Q100 Qualified Product Families (AEC-Q100-002)**

Product Family	ESD (volts) HBM	Family Members	Fab Technology
ProASIC3	1500	A3P060, A3P125, A3P250, and A3P1000	0.13 µm
SmartFusion2/ IGLOO2	2000	M2S005S, M2S010TS, M2S025TS, M2S060TS, M2S090TS, M2GL005S, M2GL010TS, M2GL025TS, M2GL060Ts, M2GL090TS	65 nm

3.3 Group E Inspection—Generic Data (Radiation Hardness)

Verification of radiation performance for each wafer lot is performed through in-line parameter monitoring in the QML RHA wafer production line. The following table lists the summarized radiation performance of RH FPGAs.

Table 6 • **Radiation Performance for RadHard Devices (Data Published on SMDs)**

Total Dose		RH1280	RH1020	Units
TID	Total Ionizing Radiation Dose	300	300	krads (Si)
SEP (Single Event Phenomena)				
SEL	Single Event Latch-Up	177	>84	LETth (MeV-cm2/mg)
SEU	Single Event Upset – Combinatorial	17	>8	LETth (MeV-cm2/mg)
	Single Event Upset – Sequential	4	–	LETth (MeV-cm2/mg)
SEDR	Single Event Dielectric Rupture	>60	>40	LETth (MeV-cm2/mg)

Note: Wafer Lot Acceptance (SEM)—RHCMOS4EF (ONO PBEOL) wafer process utilizes plugged vias, which eliminates the step coverage issue, so the SEM metalization inspection is not required.

3.4 1.0 µm FPGA Reliability Summary

Table 7 • **High Temperature Operating Life (HTOL)**

						Test Hours/Failures				
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
A1010B	PLCC68	U1G-01		79	1000	0	0	0		79000
A1010B	PLCC68	U1G-02		57	500	0	0			28500
A1010B	PQFP100	U9G01P		76	1000	0	0	0		76000
A1020B	CQFP84	UP121		24	1000	0	0	0		24000
A1020B	PGA84	U1P057/0014		97	2000	0	0	0	0	194000
A1020B	PGA84	JJ-13		30	1000	0	0	0		30000

Table 7 • **High Temperature Operating Life (HTOL)** ***(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
A1020B	PGA84	JJ-13		80	500	0	0			40000
A1020B	PLCC84	JJ-14		45	1000	0	0	0		45000
A1020B	PLCC84	JJ-15		45	1000	0	0	0		45000
A1020B	PLCC84	JJ-17		45	1000	0	0	0		45000
A1020B	PLCC84	JJ-16		80	1000	0	0	0		80000
A1020B	PLCC84	U1P-01		40	1000	0	0	0		40000
A1020B	PLCC84	U1P-02		40	1000	0	0	0		40000
A1020B	PLCC84	JJ-24		87	1000	0	0	0		87000
A1020B	PLCC84	EBFJ001		40	1000	0	0	0		40000
A1020B	PLCC84	EBFI004		40	1000	0	0	0		40000
A1020B	PLCC84	U1P209B		40	1000	0	0	0		40000
A1020B	PLCC84	U9P-004		47	1000	0	0	0		47000
A1020B	PLCC84	U9P046		100	1000	0	0	0		100000
A1020B	PLCC84	6085878		100	1000	0	0	0		100000
A1020B	PLCC84	U9P128		100	1000	0	0	0		100000
A1020B	PLCC84	UB9P034		98	2000	0	0	0	0	196000
A1020B	PQFP100	U1P41HM		80	1000	0	0	0		80000
A1020B	PQFP100	U1P05		129	1000	0	0	0		129000
A1020B[1]	PGA84	UB1P001		77	615	0	0	0		47355
A1020B[2]	PQFP100	U9P01, U9P021A		133	1000	0	1	0		133000
A1020B	VQFP80	U1P25		45	500	0	0			22500
A1020B	VQFP80	U1P83		43	1000	0	0	0		43000
A1020B	VQFP80	U1P25		39	1000	0	0	0		39000
A1020B1	PGA84	UB1P008		77	615	0	0	0		47355
A1020B	PGA84	FP4946901	0849	80	1000	0	0	(1)[3]		79000
A1020B1	CQFP84	U1RT01		80	1671	0	0	0		133680
A1020B	PGA84	FP2458201		77	1000	0	0	0		77000
A1020B	PGA84	UB1P012		77	1000	0	0	0		77000
A1020B	CQFP84	FP6502401	1047	79	615	0	0			48567
A1225A	PGA100	UJ-01		80	1000	0	0	0		80000
A1225A	PQFP100	MIX		32	1000	0	0	0		32000
A1225A	PQFP100	UJ-01		127	1000	0	0	0		127000
A1225A	PQFP100	U1J-02		80	1000	0	0	0		80000
A1240A	PGA132	TI3257		7	500	0	0			3500
A1240A	PGA132	UI-01		50	1000	0	0	0		50000
A1240A	PLCC84	UI-03		80	1000	0	0	0		80000

Table 7 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A1240A	PLCC84	E-04		30	2000	0	0	0	0	60000
A1240A	PQFP144	MIX		36	1000	0	0	0		36000
A1240A	PQFP144	E-02,03		100	1000	0	0	0		100000
A1240A	PQFP144	U1I-26		80	1000	0	0	0		80000
A1240A	PGA132	FP3879301		80	1000	0	0	0		80000
A1240A[1]	PGA132	FP16459		77	615	0	0			47355
A1280A[1]	CQFP172	UB1H001		77	615	0	0			47355
A1280A	CQFP172	U1H486		81	1000	0	0	0		81000
A1280A[1]	CQFP172	U1H442		81	615	0	0			49815
A1280A[1]	CQFP172	U1H363		58	615	0	0			35670
A1280A[1]	CQFP172	U1H83		45	1670	0	0	0		75150
A1280A[1]	PGA176	U1H511		77	615	0	0			47355
A1280A	PGA176	JH05		15	2000	0	0	0	0	30000
A1280A	PGA176	JH06		15	2000	0	0	0	0	30000
A1280A	PGA176	JH03(K)		25	2000	0	0	0	0	50000
A1280A	PGA176	JH03(SB)		25	2000	0	0	0	0	50000
A1280A	PGA176	UH-01		26	1000	0	0	0		26000
A1280A	PGA176	UH-02		26	1000	0	0	0		26000
A1280A	PGA176	UH-05		40	1000	0	0	0		40000
A1280A	PGA176	UH-10,14		75	1000	0	0	0		75000
A1280A	PGA176	U1H-35		132	168	0				22176
A1280A	PQFP160	UH-04		79	1000	0	0	0		79000
A1280A	PQFP160	ADC18X		130	1000	0	0	0		130000
A1280A	PQFP160	EBFJ002		30	168	0				5040
A1280A	PQFP160	EBFJ003		30	168	0				5040
A1280A	PQFP160	EBFJ004		20	168	0				3360
A1280A	PQFP160	U1H-01		27	2000	0	0	0	0	54000
A1280A	PQFP160	U1H-02		27	2000	0	0	0	0	54000
A1280A	PQFP160	U1H-18		80	1000	0	0	0		80000
A1280A[1]	CQFP172	UB1H029		77	615	0	0			47355
A1280A	CQFP172	U1H439		18	1000	0	0	0		18000
RT1280A[1]	CQFP172	U1H611		15	615	0	0			9225
RT1280A	CQFP172	U1H609S		10	1000	0	0	0		10000
RT1280A	CQFP172	FP21573		12	1000	0	0	0		12000
RT1280A	CQFP172	U1H611		12	1000	0	0	0		12000
RT1280A	CQFP172	FP5986501	1004	80	1000	0	0	0		80000

Table 7 • **High Temperature Operating Life (HTOL)** ***(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A1280A	CQQFP172	FP651601	1519	79	1000	0	0	0		79000
Total Units for 1.0 µm FPGA = 4789								**Total Test Time Hours = 4692353**		
Total Failures for 1.0 µm FPGA = 1										
ACT1										
Total Units for 1.0 µm FPGA = 2406								**Total Test Time Hours = 2472957**		
Total Failures for 1.0 µm ACT1 FPGA = 1										
ACT2										
Total Units for 1.0 µm FPGA = 2383								**Total Test Time Hours = 2219396**		
Total Failures for 1.0 µm ACT2 FPGA = 0										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
2. Functional failure was observed for the product A1020B, run U9P01, at 500 hours. No defects were observed after decapsulation.
3. Functional failure was observed during Group C for the product A1020B, run FP4946901, at 1000 hours. FA concluded ESD/EOS event caused by voltage spike. Group C passed per TRB approval. Observation only; not counted towards device FIT.

Table 8 • **85 °C/85% Temperature Humidity BIAS**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A1020B	PLCC84	JJ-14		27	1000	0	0	0		27000
A1020B	PLCC84	JJ-15		27	1000	0	0	0		27000
A1020B	PLCC84	JJ-17		27	1000	0	0	0		27000
Total Units for 1.0 µm FPGA = 81								**Total Test Time Hours = 81000**		
Total Failures for 1.0 µm FPGA = 0										

Table 9 • **Biased Humidity (HAST)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	50	100	200	250	Unit Hours
A1020B	PLCC84	EBFJ001		44	100	0	0			4400
A1020B	PLCC84	EBFI004		36	100	0	0			3600
A1020B	PLCC84	U9P01		29	100	0	0			2900
A1020B	PLCC84	U9P021A		50	100	0	0			5000
A1020B	PLCC84	U9P039		50	100	0	0			5000
A1020B	PLCC84	U9P046		50	100	0	0			5000
A1020B	PLCC84	6085878		50	100	0	0			5000
A1020B	PLCC84	103501		61	100	0	0			6100
Total Units for 1.0 µm FPGA = 370								**Total Test Time Hours = 37000**		
Total Failures for 1.0 µm FPGA = 0										

Table 10 • **Temperature Cycle**

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Cycles/Failures: Test Cycles	100	500	1000	2000	Cycles
					(0 °C to +125 °C)					
		Total Units for 1.0 µm FPGA =		0				Total Test Cycles =		0
					Total Failures for 1.0 µm FPGA = 0 (0°C to +125°C)					
					(–55 °C to +125 °C)					
A1020B	PLCC68	U9P186		30	1000	0	0	0		30000
A1020B	PQFP100	U9G042		25	1000	0	0	0		25000
		Total Units for 1.0 µm FPGA =		55				Total Test Cycles =		55000
					Total Failures for 1.0 µm FPGA = 0 (–55°C to +125°C)					
					(–65 °C to +150 °C)					
A1010B	PLCC68	U1G-01,02		40	1000	0	0	0		40000
A1020B	PLCC84	JJ14-17		81	1000	0	0	0		81000
A1020B	PLCC84	U1P-01,02		40	1000	0	0	0		40000
A1020B	PLCC84	EBFJ001		80	1000	0	0	0		80000
A1020B	PQFP100	U1P41HM		80	1000	0	0	0		80000
A1020B	PLCC84	EWAI003		80	1000	0	0	0		80000
A1020B	PLCC84	U1P-209B		15	1000	0	0	0		15000
A1020B	PQFP100	U1P05		80	1000	0	0	0		80000
A1020B	PLCC84	U9P021A		55	1000	0	0	0		55000
A1020B	PLCC84	U9P01		23	1000	0	0	0		23000
A1020B	PLCC84	U9P039		50	1000	0	0	0		50000
A1020B	PLCC84	U9P046		50	1000	0	0	0		50000
A1020B	PLCC84	6085878		50	1000	0	0	0		50000
A1020B	PLCC84	103501		62	1000	0	0	0		62000
		Total Units for 1.0 µm FPGA =		786				Total Test Cycles =		786000
					Total Failures for 1.0 µm FPGA = 0 (–65 °C to +150 °C)					

Table 11 • **Pressure Pot (Unbiased Autoclave)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	96	168	240	336	Unit Hours
A1010B	PLCC68	U1G-01		40	264	0	0	0		10560
A1020B	PLCC84	JJ14-17		81	264	0	0	0		21384
A1020B	PLCC84	U1P-01		40	264	0	0	0		10560
A1020B	PLCC84	U09039		50	264	0	0	0		13200
		Total Units for 1.0 µm FPGA =		211				Total Test Time Hours =		55704
					Total Failures for 1.0 µm FPGA = 0					

3.5 1.0 µm FPGA (RH) Reliability Summary

Table 12 • **1.0 µm FPGA (RH) High Temperature Operating Life (HTOL)[1]**

					Test Hours/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
RH1020	CQFP172	T8036		78	1000	0	0	0		78000
RH1020	CQFP172	T9064		40	1000	0	0	0		40000
RH1020[2]	CQFP172	T9085		15	615	0	0			9225
RH1020	CQFP172	T9089		8	1000	0	0	0		8000
RH1020	CQFP172	T2208		18	1000	0	0	0		18000
RH1020[3]	CQFP172	T2404		48	1000	0	0	0		48000
Total Units for 1.0 µm RH1020 FPGA =				**207**	**5615**			**Total Test Time Hours =**		**201225**
Total Failures for 1.0 µm RH1020 FPGA = 0										

1. Data from BAE.
2. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
3. One unit failed at –55 °C after completing 1000 hours, which was verified to be false failure due to tester noise.

3.6 0.8 µm FPGA (RH) Reliability Summary

Table 13 • **0.8 µm FPGA (RH) High Temperature Operating Life (HTOL)[1]**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
RH1280	CQFP172	FPGAQQC11	95507A.1	6	1000	0	0	0		6000
RH1280	CQFP172	FPGAQQC11	95507C.1	17	1000	0	0	0		17000
RH1280	CQFP172	FPGAQQC11	95506C.1, 2, 3	34	1000	0	0	0		34000
RH1280	CQFP172	FPGAQQC11	95506D.1	20	1000	0	0	0		20000
RH1280	CQFP172	T7013C		12	1000	0	0	0		12000
RH1280	CQFP172	T7013C	96580C.1	33	1000	0	0	0		33000
RH1280[2]	CQFP172	T7013C	96580E.1	32	1000	1	0	0		32000
RH1280	CQFP172	T9065	1990510 and 1990511	61	1000	0	0	0		61000
RH1280	CQFP172	T9066		10	1000	0	0	0		10000
RH1280	CQFP172	T9072		12	1000	0	0	0		12000
RH1280	CQFP172	T9088-		38	1000	0	0	0		38000
RH1280	CQFP172	T2208		59	1000	0	0	0		59000
Total Units for 1.0 µm RH1280 FPGA =				**334**	**12000**			**Total Test Time Hours =**		**334000**
Total Failures for 1.0 µm RH1280 FPGA = 1										

1. Data from BAE.
2. No defect found. Part destroyed in analysis.

3.7 0.8 µm FPGA Reliability Summary

Table 14 • **0.8 µm FPGA High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A14100A[1]	CQFP256	UBCLP01A		77	615	0	0	0		47355
A14100A[1]	CQFP256	UCL058		82	615	0	0	0		50430
A14100A[1, 2]	CQFP256	UCL072		78	615	(1)	0	0		47970
A14100A[3]	CQFP256	UCL049		15	1,000	0	0	(1)		15000
A14100A	CQFP256	UCL055		18	1,000	0	0	0		18000
A14100A[1]	CQFP256	UCL058		82	561	0				46002
A14100A	CQFP256	UCL073		10	1,000	0	0	0		10000
A14100A[1]	CQFP256	UCL082		10	1,670	0	0	0		16700
A14100A	PBGA313	25290820		45	1000	0	0	0		45000
A14100A	RQFP208	24239130		51	1000	0	0	0		51000
A14100A	RQFP208	UCLO1		25	1000	0	0	0		25000
A14100A	CQFP256	FP4947201		80	1000	0	0	0		80000
A14100A	CQFP256	FP2732701		12	1000	0	0	0		12000
A14100A	CQFP256	UBCL011		12	1000	0	0	0		12000
A14100A	CQFP256	UCL086		10	1000	0	0	0		10000
A14100A[1]	CQFP256	UBCL009		80	615	0	0			49200
A1425A[1]	PGA133	UCJ01/02E/03		130	615	0	0	0		79950
A1425A	PGA133	JK08,09,10		140	1000	0	0	0		140000
A1425A	PGA133	ACN32804, ACN30805, ACN33807		130	1000	0	0	0		130000
A1425A[1]	PGA133	UCJ01, 2, 3		130	615	0	0	0		79950
A1425A	PLCC84	JK08, 09, 10		135	1000	0	0	0		135000
A1425A	PQFP100	UCJ013		100	1000	0	0	0		100000
A1440A	VQFP100	51940		79	1000	0	0	0		79000
A1440A	VQFP100	JN05		79	1000	0	0	0		79000
A1460A[1]	PGA207	UCK056		80	561	0				44880
A1460A[1]	CPGA207	UCKT01		81	561	0				45441
A1460A[1]	PGA207	UCK005		77	615	0	0	0		47355
A1460A[1]	PGA207	UCK056		80	615	0	0			49200
A1460A[1]	PGA207	UCKT01		81	615	0	0			49815
A1460A	PGA207	JL-01		80	1000	0	0	0		80000
A1460A	PGA207	JL-06B		65	1000	0	0	0		65000

Table 14 • **0.8 µm FPGA High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A1460A	PGA207	PC435091, PC435092, PC435093		80	1000	0	0	0		80000
A1460A	PQFP208	20072420	0026	30	1000	0	0	0		30000
A1460A	PQFP208	20094560	0022	29	1000	0	0	0		29000
A1460A	PQFP208	20145270	0026	30	1000	0	0	0		30000
A1460A	PQFP208	29350050	9947	65	2000	0	0	0	0	130000
A1460A	PQFP208	UCK070	9946	22	2000	0	0	0	0	44000
A1460A	PQFP208	JL-01		80	1000	0	0	0		80000
A1460A	PQFP208	JL-03		62	1000	0	0	0		62000
A1460A	PGA207	FP4341401		80	1000	0	0	0		80000
A1460A	PGA207	FP12176		79	1000	0	0	0		79000
A1460A	PGA207	FP2157501		80	1000	0	0	0		80000
A1460A	PGA207	FP03898A		77	1000	0	0	0		77000
RT14100A	CQFP256	UCL055		18	1000	0	0	0		18000
RT14100A	CQFP256	UCL073	9949	15	1000	0	0	0		15000
RT14100A	CQFP256	UCL073	0019	10	1000	0	0	0		10000
RT14100A[1]	CQFP256	UCL72	9931 9925	77	561	0				43197
A14100A	PG257	FP6341801	1621	80	1000	0	0	0		80000
A1425A	CQ132	UCJT05	1220	80	1000	0	0	0		80000
Total Units for 0.8 µm FPGA = 3148					**Total Test Time Hours = 2627445**					
Total Failures for 0.8 µm FPGA = 0										
Total Units for 0.8 µm ACT3 FPGA = 3148					**Total Test Time Hours = 2627445**					
Total Failures for 0.8 µm ACT3 FPGA = 0										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
2. Product A14100A, run UCL072, at 168 hours, one unit failed gross-functional. FA shown contact spike caused by ESD/EOS, qualification passed by TRB approval.
3. Product A14100A, run UCL049, at 1000 hours, unit failed was proven by FA as EOS. No functional failures observed.

Table 15 • **85°C/85%Temperature Humidity Bias**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A14100A	PBGA313	25290820		45	1000	0	0	0		45000
Total Units for 0.8 µm FPGA = 45					**Total Test Time Hours = 45000**					
Total Failures for 0.8 µm FPGA = 0										

Table 16 • Biased Humidity (HAST)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	50	100	200	250	Unit Hours
A1425A	PLCC84	JK8,9,10		81	100	0	0			8100
A1425A	PQFP100	ACN32804, ACN30805, ACN33807		80	100	0	0			8000
A1425A	PQFP100	UCJ01,2,3		80	100	0	0			8000
A1440A	VQFP100	JN05		45	100	0	0			4500
A1440A	VQFP100	51940		45	100	0	0			4500
A1460A	PQFP208	JL04A		80	100	0	0			8000
A1460A	PQFP208	WB24279010		47	100	0	0			4700
A14100A	RQFP208	24239130		14	100	0	0			1400
Total Units for 0.8 µm FPGA = 472							**Total Test Time Hours = 47200**			
Total Failures for 0.8 µm FPGA = 0										

Table 17 • Temperature Cycle

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Cycles/Failures					
					Test Cycles	100	200	500	1000	Cycles
					(–65°C to +150°C)					
A14100A	PBGA313	25290820		78	500	0	0	0		39000
A14100A	RQC208	MIX		24	100	0				2400
A14100A	RQC209	MIX		24	100	0				2400
A14100A	RQFP208	24239130		14	500	0	0	0		7000
A14100A	RQFP208	UCLO1		31	500	0	0	0		15500
A14100A	RQFP208	2537198		19	100	0				1900
A1425A	PGA133	JK8,9,10		81	500	0	0	0		40500
A1425A	PLCC84	JK8,9,10		83	500	0	0	0		41500
A1425A	PQFP100	UCJ01,2,3		80	500	0	0	0		40000
A1425A	PQFP100	ACN32804, ACN30805, ACN33807		80	500	0	0	0		40000
A1440A	PQFP160	JN-02		80	500	0	0	0		40000
A1440A	VQFP100	JN-05		80	500	0	0	1		40000
A1440A	VQFP100	51940		45	500	0	0	0		22500
A1460A	PGA207	JL-01		80	500	0	0	0		40000
A1460A	PGA207	PC435091, PC435092, PC435093		80	500	0	0	0		40000
A1460A	PQFP208	JL-01		80	500	0	0	0		40000
A1460A	PQFP208	25364430		45	500	0	0	0		22500

Table 17 • **Temperature Cycle *(continued)***

					Number of Cycles/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	100	200	500	1000	Cycles
A1460A	PQFP208	2610001		80	500	0	0	0		40000
Total Units for 0.8 µm FPGA = 1084									**Total Test Cycles =**	**515200**
Total Failures for 0.8 µm FPGA = 1										

Table 18 • **Pressure Pot (Unbiased Autoclave)**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	48	96	168	336	Unit Hours
A14100A	PBGA313	25290820		45	96	0	0			4320
Total Units for 0.8 µm FPGA = 45									**Total Test Time Hours =**	**4320**
Total Failures for 0.8 µm FPGA = 0										

3.8 0.6 µm FPGA Reliability Summary

Table 19 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
A1225XL	PQFP100	ACP02187.1		26	1000	0	0	0		26000
A1225XL	PQFP100	ACQ10102		56	1000	0	0	0		56000
A1240XL	PLCC84	ACP57584.1		100	1000	0	0	0		100000
A1240XL	PQFP144	MIX		56	1000	0	0	0		56000
A1240XL	PQFP144	ACR50594.1		228	168	0				38304
A1240XL	PQFP144	ACR50594.1		143	168	0				24024
A1240XL	PQFP144	ACR50594.1		227	168	0				38136
A1240XL	PQFP144	ACP01117.1, ACN51939.1		52	1000	0	0	0		52000
A1280XL[1]	CQFP172	ACT10293.1		80	561	0	0			44880
A1280XL[1]	CQFP172	ACT10293.1		80	615	0	0			49200
A1280XL[1]	CQFP172	ACY953401		77	615	0	0			47355
A1280XL[1,2]	PGA176	ACU413553		77	615	(1)	0			47355
A1280XL[1]	PGA176	ACV715861		77	561	0	0			43197
A1280XL	PLCC84	MIX		100	1000	0	0	0		100000
A1280XL	PQFP160	ACR53214		129	168	0				21672
A1280XL	PQFP160	ACU458071/0008		86	2000	0	0	0	0	172000
A1280XL	PQFP160	ACP212072, ACP19329.1		76	1000	0	0	0		76000

Table 19 • **High Temperature Operating Life (HTOL)** ***(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A14100BP	RQFP208	26026670		27	1000	0	0	0		27000
A1415A	PQFP100	ACP17300		100	1000	0	0	0		100000
A1425A	PGA133	UCJ01,02,03		130	1670	0	0	0		217100
A1425A	PQFP100	ACP17300		101	2000	0	0	0	0	202000
A1425A	PQFP100	ACP122761		100	1000	0	0	0		100000
A1425A	PQFP100	ACP12285		88	1000	0	0	0		88000
A1460BP	PQFP208	25430540		52	1000	0	0	0		52000
A32100DX[1]	CQFP84	ACR50293.1		80	615	0	0			49200
A32140DX	PQFP208	ACP562551		28	2000	0	0	0	0	56000
A32140DX	PQFP208	G10854		26	1000	0	0	0		26000
A32140DX	PQFP160	ACP540231		26	1000	0	0	0		26000
A32140DX	PQFP160	25464510		26	1000	0	0	0		26000
A32140DX	PQFP208	ACP33277.1		75	1000	0	0	0		75000
A32140DX	PQFP208	ACP56255.1		52	1000	0	0	0		52000
A32200DX[1,3]	CQFP256	ACT16685.1		77	1000	(1)	0	0		77000
A32200DX	CQFP256	ACV648421		5	615	0	0			3075
A32200DX[1]	CQFP256	ACV648421		5	615	0	0			3075
A32200DX[1]	PQFP208	26207340		29	1000	0	0	0		29000
A32300DX	RQFP240	ACQ09069.1		26	2000	0	0	0	0	52000
A3265DX	PQFP160	ACP163684		78	1000	0	0	0		78000
Total Units for 0.6 µm FPGA = 2801					**Total Test Time Hours = 2330573**					
Total Failures for 0.6 µm FPGA = 0										
ACT3										
Total Units for ACT3 FPGA = 598					**Total Test Time Hours = 786100**					
Total Failures for ACT3 FPGA = 0										
XL										
Total Units for XL FPGA = 1670					**Total Test Time Hours = 992123**					
Total Failures for XL FPGA = 0										
DX										
Total Units for DX FPGA = 1207					**Total Test Time Hours = 552350**					
Total Failures for DX FPGA = 0										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
2. Product A1280XL, run 2ACU413553, at 160 hours; unit failed was verified to be ESD/EOS.
3. Product A32200DX, run ACT16685.1, at 160 hours, rejects are due to electrical over stress (EOS) or (ESD), which are induced by HP1 tester during the same time frame in which these devices are tested. Failure modes are not life-test induced; therefore, the qualification is still passed.

Table 20 • **Biased Humidity (HAST)**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	50	100	200	250	Unit Hours
A1225Xl	PQFP100	ACP02187.1		17	100	0	0			1700
A1240XL	PQFP144	ACP01117.1, ACN51939.1		31	100	0	0			3100
A1280XL	PQFP160	ACP19329.1 ACP212072		76	100	0	0			7600
A1280XL	PQFP160	ACP33235.1		76	100	0	0			7600
A1280XL	PQFP160	ACQ01769		40	100	0	0			4000
A1280XL	PQFP160	ACQ05561		39	100	0	0			3900
A3265DX	PQFP160	ACP163684		40	100	0	0			4000
A1415A	PQFP100	ACP17300		50	100	0	0			5000
A1425A	PQFP100	ACP122761		50	100	0	0			5000
A32140DX	PQFP160	ACP54023.1		26	100	0	0			2600
A32140DX	PQFP208	ACP33277.1, ACP55730.1, ACP54023.1		76	100	0	0			7600
A32200DX	PQFP208	26207340		26	100	0	0			2600
A14100BP	RQFP208	26330340		26	100	0	0			2600
A32200DX	PQFP208	ACQ03818.1		30	100	0	0			3000
A1280XL	PQFP160	26084380		58	100	0	0			5800
A32140DX	PQFP208	55558		25	100	0	0			2500
		Total Units for 0.6 µm FPGA =		**686**			**Total Test Time Hours =**			**68600**
				Total Failures for 0.6 µm FPGA = 0						

Table 21 • **Temperature Cycle**

					Number of Cycles/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	100	200	500	1000	Cycles
A1280XL	TQFP176	25026540		17	500	0	0	0		8500
A1280XL	PQFP160	25312500, 25312480		76	500	0	0	0		38000
A1280XL	PQFP160	25312500, 25312480		76	200	0	0			15200
A1280XL	PQFP160	25312500, 25312480		75	500	0	0	0		37500
A1280XL	PQFP160	25312500, 25312480		75	500	0	0	0		37500
A1280XL	PQFP160	25312500, 25312480		74	500	0	0	0		37000
A1280XL	PQFP160	25312500, 25312480		76	500	0	0	0		38000
A1280XL	PQFP160	25504560		36	500	0	0	0		18000
A1425A	PGA133	JK8,9,10		81	500	0	0	0		40500
A1425A	PLCC84	JK8,9,10		83	500	0	0	0		41500
A1425A	PQFP100	UCJ01,2,3		80	500	0	0	0		40000

Table 21 • **Temperature Cycle *(continued)***

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**100**	**200**	**500**	**1000**	**Cycles**
A1425A	PQFP100	ACN32804, ACN30805, ACN33807		80	500	0	0	0		40000
A1440A	PQFP160	JN-02		80	500	0	0	0		40000
A1440A	VQFP100	JN-05		80	500	0	0	1		40000
A1440A	VQFP100	51940		45	500	0	0	0		22500
A1460A	PQFP208	JL-01		80	500	0	0	0		40000
A1460A	PGA207	JL-01		80	500	0	0	0		40000
A1460A	PGA207	PC435091, PC435092, PC435093		80	500	0	0	0		40000
A1460A	PQFP208	25364430		45	500	0	0	0		22500
A1460A	PQFP208	2610001		80	500	0	0	0		40000
A14100A	RQFP208	24239130		14	500	0	0	0		7000
A14100A	RQFP208	UCLO1		31	500	0	0	0		15500
A14100A	RQFP208	2537198		19	100	0				1900
A14100A	PBGA313	25290820		78	500	0	0	0		39000
A14100A	RQFP208	MIX		24	100	0				2400
A14100A	RQFP208	MIX		24	100	0				2400
		Total Units for 0.6 µm FPGA = 1589							**Total Test Cycles = 744900**	
				Total Failures for 0.6 µm FPGA = 1						

Table 22 • **Pressure Pot (Unbiased Autoclave)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**48**	**96**	**168**	**336**	**Unit Hours**
A1280XL	TQFP176	25312480		45	168	0	0	0		7560
A14100A	PBGA313	25290820		45	96	0	0			4320
		Total Units for 0.6 µm FPGA = 90							**Total Test Time Hours = 11880**	
				Total Failures for 0.6 µm FPGA = 0						

3.9 0.6 µm RTSX FPGA Reliability Summary

Table 23 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
RT54SX16[1]	CQFP256	P05		77	615	0	0			47355
RT54SX16	CQFP256	P04	9931	46	2000	0	0	0	0	92000
RT54SX16	PQFP208	P02, P03, P04		81	1000	0	0	0		81000
RT54SX16	CQFP256	T6HP12		101	240	0				24240

Table 23 • **High Temperature Operating Life (HTOL) *(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
RT54SX32[1]	CQFP208	T6JP01A		76	615	0	0			46740
RT54SX32[1]	CQFP256	T6JP05A		5	615	0	0			3075
Total Units for 0.6 µm RTSX FPGA = 386								**Total Test Time Hours =**		**294410**
Total Failures for RTSX 0.6 µm FPGA = 0										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.

3.10 0.45 µm CSM FPGA Reliability Summary

Table 24 • **High Temperature Operating Life (HTOL)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
A40MX04	PLCC84	2ACR23038.3		30	2000	0	0	0	0	60000
A40MX04	PLCC84	2ACR23038.3		45	2000	0	0	0	0	90000
A40MX04	PLCC84	2ACT160021		77	2000	0	0	0	0	154000
A40MX04	PLCC84	2ACU040091	9919	77	2000	0	0	0	0	154000
A40MX04	PLCC84	2XZR24206.5		29	2000	0	0	0	0	58000
A42MX16	PLCC84	2ACU492561	0012	148	1000	0	0	0		148000
A42MX16	PQFP160	2XZR25104.1		26	2000	0	0	0	0	52000
A42MX24	PQFP160	2XYE254371	0920	77	1500	0	0	0		115500
A42MX24	PQFP160	2XYE254371	0920	80	1000	0	0	0		80000
A42MX36[1]	CQFP208	2ACZ310131		77	615	0	0	0		47355
A42MX36[1,2]	CQFP256	2ACT363611		77	615	(1)[2]	0			47355
A42MX36	PQFP208	2ACT10221		27	2000	0	0	0	0	54000
A42MX36[1]	CQFP208	2ACU523241	0019	45	615	0	0	0		27675
A42MX36	CQFP208	2ACC512631	0733	77	1000			1[3]		76000
A42MX36	CQFP256	2ACH323581	1212	80	1000	0	0	0		80000
A42MX36	CQFP256	2ACG311291	1116	79	1000	0	0	0		79000
A42MX36	CQFP208	2MPK091041	1330	80	1000	0	0	0		80000
Total Units for 0.45 µm FPGA = 1131								**Total Test Time Hours =**		**1402885**
Total Failures for 0.45 µm FPGA = 1										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
2. Product A42MX36, run 2ACT363611, at 168 hours, unit failed was verified to be ESD/EOS.
3. Product A42MX36, run 2ACC512631, 1 failure observed after 1000 hours. pull point (no intermediate pull points), counted towards device FIT (used Ea of 0.7 eV as FA inconclusive, root cause could not be established). Report available upon request.

Table 25 • Biased Humidity (HAST)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					Unit Hours
					Test Time	50	100	200	250	
A40MX04	PLCC84	2ACR23038.3		81	100	0	0			8100
A40MX04	PLCC84	2ACR23039.1		25	100	0	0			2500
A42MX09	PQFP160	2ACT110181		30	100	0	0			3000
A42MX16	PQFP160	2XZR25104.1		25	100	0	0			2500
A42MX36	BGA272	2ACT180141		76	100	0	0			7600
A42MX36	PQFP208	2ACT110221		27	50	0				1350
Total Units for 0.45 µm FPGA = 264								**Total Test Time Hours = 25050**		
Total Failures for 0.45 µm FPGA = 0										

Table 26 • Unbiased Humidity

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					Unit Hours
					Test Time	50	100	200	250	
A42MX09	PQFP160	2ACT052662	9817	30	100	0	0			3000
A42MX24	PQFPG208[1, 2]	2ACD420191	0806	47	100	0	0			4700
A42MX36	BGG272[2]	2MPP470711	1836	76	264					20064
Total Units for 0.45 µm FPGA = 153								**Total Test Time Hours = 27764**		
Total Failures for 0.45 µm FPGA = 0										

1. G indicates lead-free.
2. Unbiased HAST (JESD22 A118), 130 °C and RH = 85%.

Table 27 • Temperature Cycle

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Cycles/Failures					Cycles
					Test Cycles	200	500	1000	2000	
(–65 °C to +150 °C)										
A40MX04	PLCC84	2XZR24206.5		26	1000	0	0	0		26000
A40MX04	PLCC84	2ACR23038.3		26	1000	0	0	0		26000
A42MX09	PQFP160	2ACT210121		30	1000	0	0	0		30000
A42MX16	PQFP160	2XZR25104.1		26	1000	0	0	0		26000
A42MX36	PQFP208	2ACT110221		27	1000	0	0	0		27000
A42MX24	PQFPG208[1]	2ACD420191	0806	47	1000	0	0	0		47000
A42MX36	BGG272[1, 2]	2MPP470711	1836	76	700	0	0			53200
Total Units for 0.45 µm FPGA = 258									**Total Test Cycles = 235200**	
Total Failures for 0.45 µm FPGA = 0										

1. G indicates lead-free.

3.11 0.45 µm UMC FPGA Reliability Summary

Table 28 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A40MX04	PLCC84	HKJAH00	0736	90	1000	0	0	0		90000
A42MX24	PQFP208	HLF8Q0G	0941	80	1000	0	0	0		80000
A42MX24	PQFP208	HMGN000	1111	79	2000	0	0	0	0	158000
A42MX24	PQFP208	HPY9H00	1309	80	2000	0	0	0	0	160000
A42MX04	PG84	HRW0300	1513	45	168	0				7560
A42MX09	PG132	HRRC100	1513	8	72					576
A42MX09	PG132	HRRC100	1513	80	1000	0	0	0		80000
A42MX16	PG176	HR5TP00	1451	9	168	0				1512
A42MX36	CQ208	2MPN120391	1644	80	1000	0	0	0		80000
A42MX36	CQ208	2ACH323581	1247	8	168	0				1344
A40MX04	CQ84	HRW0300	1513	8	160	0				1280
Total Units for 0.45 µm FPGA = 567								**Total Test Time Hours = 660272**		
Total Failures for 0.45 µm FPGA = 0										

Table 29 • **Biased Humidity Accelerated Stress Test (HAST), 110°C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A40MX04	PLCC84	HKJAH00	0736	82	100	0	0			820
A42MX24	PQFP208	HKJNS00	0734	50	100	0	0			500
Total Units for 0.45 µm FPGA = 132								**Total Test Time Hours = 1320**		
Total Failures for 0.45 µm FPGA = 0										

Table 30 • **Temperature Cycle (TC), –55°C to +125°C**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**1000**	**2000**	**Cycles**
A40MX04	PLCC84	HKJAH00	0736	85	1000	0	0	0		85000
A42MX24	PQFP208	HKJNS00	0734	80	1000	0	0	0		80000
Total Units for 0.45 µm FPGA = 165									**Total Test Cycles = 165000**	
Total Failures for 0.45 µm FPGA = 0										

Table 31 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**2000**	**Unit Hours**
A40MX04	PLCC84	HKJAH00	0736	80	1000	0	0	0		80000
A42MX24	PQFP208	HKJNS00	0734	80	1000	0	0	0		80000
Total Units for 0.45 µm FPGA = 160								**Total Test Time Hours = 160000**		
Total Failures for 0.45 µm FPGA = 0										

3.12 0.35 µm FPGA Reliability Summary

Table 32 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A54SX16[1,2]	CQFP208	2ACW210771		105	615	(2)	0	0		
A54SX16	PQFP208	2ACT110031		74	2000	0	0	0	0	148000
A54SX16	PQFP208	2XZR402521		38	1000	0	0	0		38000
A54SX16	PQFP208	2ACU420072		99	1000	0	0	0		99000
A54SX16	PQFP208	2ACT100081		81	2000	0	0	0	0	162000
A54SX16P	PQFP208	2ACT141821		45	1000	0	0	0		45000
A54SX32[1]	CQFP208	2ACU390881		45	615	0	0			27675
A54SX32[1]	CQFP208	2ACT500021		45	615	0	0			27675
A54SX32	PQFP208	2ACV103721		88	1000	0	0	0		88000
A54SX32	PQFP208	2XZT091468		43	2000	0	0	0	0	86000
A54SX32	PQFP208	2ACT330111, 2ACT330101, 2HCU462006		88	1000	0	0	0		88000
Total Units for 0.35 µm FPGA = 751								**Total Test Time Hours = 809350**		
Total Failures for 0.35 µm FPGA = 0										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.
2. Product A54SX16, run 2ACW21O771; the group C lot was started with 77 units and two devices failed during functional test. The failure analysis with the two failure devices was started to narrow down the failure location and find the root cause of failure. Bench setup testing was done to reproduce the failure seen on the tester. Unfortunately, the two devices in FA, plus one more reference unit from the same lot, were misplaced in the lab and got lost during the Microsemi SoC Products Group (formerly Actel) facility move from Sunnyvale to Mountain View. The devices may have been scrapped by mistake as reject parts. Therefore, the failure analysis could not be continued. An additional 29 units from the same inspection lot were submitted for full group C process and all passed. As a result, this group C qualification was passed with 105(2) result based on the LTPD(5) criteria. Actel TRB approved this group C result, and agreed this was a one-time accident due to the facility move, which should not recur with the currently established handling procedure for FA devices.

Table 33 • **Low Temperature Operating Life (LTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A54SX32	PQFP208	2ACT330111, 2ACT330101, 2HCU462006		88	1000	0	0	0		88000
Total Units for 0.35 µm FPGA = 88								**Total Test Time Hours = 88000**		
Total Failures for 0.35 µm FPGA = 0										

Table 34 • **Biased Humidity (HAST)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A54SX32	BGA329	2ACU211641	9941 9942 9943	81	100	0	0			8100
A54SX16	PQFP208	2ACU241341 2ACU420072 2ACU222448	9947 0002 0004	84	100	0	0			8400
A54SX32	BGA329	2ACU410201	0013 0014 0015	76	100	0	0			7600
Total Units for 0.35 µm FPGA = 241								**Total Test Time Hours = 24100**		
Total Failures for 0.35 µm FPGA = 0										

Table 35 • **Unbiased Humidity (HAST)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A54SX16	PQFP208	2ACU241341 2ACU420072 2ACU222448	9947 0002 0004	84	100	0	0			8400
Total Units for 0.35 µm FPGA = 84								**Total Test Time Hours = 8400**		
Total Failures for 0.35 µm FPGA = 0										

Table 36 • **Temperature Cycle**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**1000**	**2000**	**Cycles**
				(–65 °C to +150 °C)						
A54SX16	PQFP208	2ACU241341	9947	93	1000	0	0	0		93000
		2ACU420072	0002							
		2ACU222448	0004							
A54SX32	BGA329	2ACU410201	0013	76	1000	0	0	0		76000

Table 36 • **Temperature Cycle *(continued)***

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**1000**	**2000**	**Cycles**
		2ACU410201	0014							
		2ACU410201	0015							
A54SX32	PQFP208	2HCU462006	0010	76	1000	0	0	0		76000
		2HCU410216	0017							
		2HCV022691	0017							
Total Units for 0.35 µm FPGA = 245								**Total Test Cycles = 245000**		
Total Failures for 0.35 µm FPGA = 0										

3.13 0.25 µm MEC FPGA Reliability Summary

Table 37 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A54SX32A	PQFP208	T25J002		80	1000	0	0	0		80000
A54SX32A	PQFP208	T25JP03		88	1000	0	0	0		88000
A54SX32A	PQFP208	T25J002, P05, 04		50	500	0	0			25000
A54SX72A[1, 2]	CQFP208	T25K065		77	615	(1)	0			47355
A54SX72A	PQFP208	T25K001		88	1000	0	0	0		88000
A54SX72A	PQFP208	T25K065		77	615	0	0			47355
A54SX72A	PQFP208	T25KP04		28	1000	0	0	0		28000
RT45SX32S	CQFP208	T25JSP03		8	2000	0	0	0	0	16000
RT54SX32S	CQFP208	T25JS001		8	4000	0	0	0	0	32000
RT54SX32S	CQFP208	T25JS001		25	1000	0	0	0		25000
RT54SX32S	CQFP208	T25JSP03		24	1000	0	0	0		24000
RT54SX32S[1]	CQFP208	T25JSP03		52	615	0	0			31980
RT54SX32S	CQFP208	T25JS004		22	2000	0	0	0	0	44000
RT54SX32S	CQFP208	BP1037101		100	1000	0	0	0		100000
RT54SX32S	CQFP208	T25JS004		20	1000	0	0	0		20000
RT54SX32S[1]	CQFP256	T25JSP03		76	615	0	0			46740
RT54SX32S[3]	CQFP208	BP0083301, T25JS004, T25JS001(KM1)		150	1000	0	1	1(2)		149250
RT54SX72S	CQFP208	T25KS005		22	1000	0	0	0		22000
RT54SX72S[1, 2]	CQFP256	T25KS005		80	615	0	(1)			49200
Total Units for 0.25 µm MEC FPGA = 1075								**Total Test Time Hours = 963880**		
Total Failures for 0.25 µm MEC FPGA = 2										

1. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.

2. Product A54SX72A, run T25K065, and product RT54SX72S, run T25KS005; the failures determined were EOS.
3. K-antifuse failed at 250 hours, F-antifuse failure at 1000 hours, and 2 ESD failures at 1000 hours.

Table 38 • **Low Temperature Operating Life (LTOL)**

					Test Hours/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A54SX32A	PQFP208	T25J002, P05, P04		80	1000	0	0	0		80000
A54SX32A	PQFP208	T25JP03		88	1000	0	0	0		88000
A54SX32A	PQFP208	T25J002, P05, P04		50	500	0	0			25000
RT54SX32S[1]	CQFP208	BP0083301, T25JS004, T25JS001(KM1)		149	250	0	1			37250
A54SX72A	PQFP208	T25K001		88	1000	0	0	0		88000
A54SX72A	PQFP208	T25KP04		28	1000	0	0	0		28000
Total Units for 0.25 µm MEC FPGA = 483								**Total Test Time Hours =**		**346250**
Total Failures for 0.25 µm MEC FPGA = 1										

1. One K-antifuse failed at 250 hours.

Table 39 • **Biased Humidity (HAST)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A54SX32A	PQFP208	T25J002, P05, P04		80	100	0	0			8000
A54SX72A	PQFP208	T25KP04		28	100	0	0			2800
Total Units for 0.25 µm MEC FPGA = 108							**Total Test Time Hours =**			**10800**
Total Failures for 0.25 µm MEC FPGA = 0										

Table 40 • **Temperature Cycle**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**1000**	**2000**	**Cycles**
				(-65 °C to +150 °C)						
A54SX32A	PQFP208	T25J002, P05, P04		80	1000	0	0	0		80000
A54SX72A	PQFP208	T25KP04		28	1000	0	0	0		28000
Total Units for 0.25 µm MEC FPGA = 108								**Total Test Cycles =**		**108000**
Total Failures for 0.25 µm MEC FPGA = 0										

3.14 0.25 µm Flash FPGA Reliability Summary

Table 41 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A500K130	BGA272	ZA026941 ZA035953 ZA034979	0039, 0040	76	1000	0	0	0		76000
A500K130	BGA272	ZA051811		80	1000	0	0	0		80000
A500K270	BGA456	ZA027920		28	1000	0	0	0		28000
A500K130	BGA272	ZA051811		120	1000	0	0	0		120000
A500K130	BGA272	ZA051811		80	1000	0	0	0		80000
A500K130	BGA272	ZA049887		80	1000	0	0	0		80000
Total Units for 0.25 µm Flash FPGA = 464								**Total Test Time Hours = 464000**		
Total Failures for 0.25 µm Flash FPGA = 0										

Table 42 • **Low Temperature Operating Life (LTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A500K130	BGA272	ZA026941 ZA035953 ZA034979	0039, 0040	76	1000	0	0	0		76000
Total Units for 0.25 µm Flash FPGA = 76								**Total Test Time Hours = 76000**		
Total Failures for 0.25 µm Flash FPGA = 0										

Table 43 • **Endurance**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**1000**	**Cycles**
					Room Temperature					
A500K130	CGA272	ZA026941		15	50	0				750
Total Units for 0.25 µm Flash FPGA = 15								**Total Number of Cycles = 750**		
Total Failures for 0.25 µm Flash FPGA = 0										

Table 44 • **Retention 225°C Unbiased 100% Programmed**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A500K130	CGA272	ZA026941		9	1000	0	0	0		9000
Total Units for 0.25 µm Flash FPGA = 9								**Total Test Time Hours = 9000**		
Total Failures for 0.25 µm Flash FPGA = 0										

Table 45 • **Retention 225 °C Unbiased 100% Erased**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
A500K130	CGA272	ZA026941		8	1000	0	0	0		8000
Total Units for 0.25 µm Flash FPGA = 8								Total Test Time Hours =		8000
Total Failures for 0.25 µm Flash FPGA = 0										

3.15 0.25 µm UMC FPGA Reliability Summary

Table 46 • **CMOS Reliability–High Temperature Operating Life (HTOL)**

					Test Hours/Failures						
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	6000	Unit Hours
RTSX32SU[1]	CQFP208	D122H1	0434	149	4,781	0	0	0	0		712402
RTSX32SU[1]	CQFP208	D122H1	0434	1	1,912	0	0	0			1912
RTSX32SU[1]	CQFP208	D122H1	0434	150	4,781	0	0	0	0	0	717182
RTSX32SU[1]	CQFP208	D122H1, D1JW21	0434, 0442	2	10,412	0	0	0	0	0	20824
RTSX32SU[1]	CQFP208	D122H1, D1JW21	0434, 0442	148	31,237	0	0	0	0	0	4623009
RTSX72SU[1]	CQFP208	D1AYH1, D1KT11	0519, 0445	1	15,618	0	0	0	0	0	15618
RTSX72SU[1]	CQFP208	D1AYH1, D1KT11	0519, 0445	73	31,237	0	0	0	0	0	2280268
RTSX72SU[1]	CQFP208	D1AYH1, D1KT11	0519, 0445	5	20,824	0	0	0	0	0	104122
RTSX32SU[1]	CQFP208	D110A1		68	0.91						62
RTSX72SU[1]	CQFP208	D0YMJ1		32	0.91						29
RTSX32SU[1]	CQFP208	D122H1		100	0.91						91
RTSX72SU[1]	CQFP256	DIJW01		35	54						1886
RTSX32SU[1]	CQFP256	D1HLK1		100	54						5389
RTSX32SU[1]	CQFP208	D110A1		100	4.2						420
RTSX32SU[1]	CQFP208	D110A1		100	162						16168
RTSX32SU[1]	CQFP208	D110A1		98	1.83						179
RTSX32SU[1]	CQFP208	D110A1		100	1.83						183
RTSX72SU[1]	CQFP208	D0YMJ1		68	0.91						62
RTSX72SU[1]	CQFP208	D0Y311		100	0.9						91
RTSX32SU[1]	CQFP256	D122H1	0441	100	54						5389
RTSX32SU[1]	CQFP208	D19S61	0450	100	54						5389
RTSX72SU[1]	CQFP208	D1AYH1		100	0.91						91
RTSX32SU[1]	CQFP208	D1AYJ1	0450	100	54						5389
RTSX32SU[1]	CQFP208	D1AYJ1	0502	100	54						5389

Table 46 • **CMOS Reliability–High Temperature Operating Life (HTOL)** ***(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures						
					Test Time	168	500	1000	2000	6000	Unit Hours
RTSX72SU[1]	CQFP208	D1HLH4	0504	100	54						5389
RTSX72SU[1]	CQFP208	D1HLJ1	0446	100	54						5389
RTSX32SU[1]	CQFP256	D1HLK1	0507	100	54						5389
RTSX72SU[1]	CQFP208	D1JW01	0501	100	54						5389
RTSX32SU[1]	CQFP208	D1JW21	0451	100	54						5389
RTSX32SU[1]	CQFP208	D1JW21	0452	100	54						5389
RTSX32SU[1]	CQFP208	D1JW21	0511	100	54						5389
RTSX32SU[1]	CQFP208	D1JW21	0512	100	54						5389
RTSX32SU[1]	CQFP208	D1JW21	0523	100	54						5389
RTSX32SU[1]	CQFP256	D1JW21	0518	100	54						5389
RTSX72SU[1]	CQFP208	D1KT11	0515	100	54	(1)[2]					5389
RTSX72SU[1]	CQFP208	D1MM81	0519	100	54						5389
RTSX72SU[1]	CQFP256	D1MM91	0513	100	54						5389
RTSX72SU[1]	CQFP256	D1N2W1	0520	100	54						5389
RTSX72SU[1]	CQFP256	D1N8A1	0517	100	54						5389
RTSX32SU[1]	CQFP256	D1N8F1	0518	100	54						5389
RTSX72SU[1]	CQFP256	D1P8T1	0522	100	54						5389
RTSX32SU[1]	CQFP256	D1P8W.1	0531	100	54						5389
RTSX32SU[1]	CQFP208	D1AYJ1	0450	80	321	0					25664
RTSX72SU[1]	CQFP208	D1HLJ1		79	321	0					25343
RTSX72SU[1]	CQFP208	D0Y311	0410	133	1,000	(1)[2]	0	0			133000
RTSX72SU[1]	CQFP208	D0Y311	0410	8	168	0					1344
RTSX32SU[1]	CQFP208	D19S61	0436	80	615	(1)[2]	0				49181
RTSX32SU[1]	CQFP208	D110A1		135	168	0					22680
RTSX32SU[1]	CQFP256	D122H1		100	1000	0	0	0			100000
RTSX32SU[1]	CQFP208	D1AYJ1	0504	22	1000	0	0	0			22000
RTSX32SU[1]	CQFP208	D1JW21, D1AYJ1	0519, 0502	150	750	0	0				112500
RTSX72SU[1]	CQFP256	D1N2W1		77	1000	0	0	0			77000
RTSX32SU[1]	CQFP208	D1JW21, D1AYJ1	0519, 0502	150	750	0	0				112500
RTSX72SU[1]	CQFP208	D1MM81	0534	15	1000	0	0	0			15000
RTSX72SU[1]	CQFP256	D1JW01	0501	20	1000	0	0	0			20000
RTSX72SU[1]	CQFP208	D1N8A1	0641	15	1000	0	0	0			15000
RTSX72SU[1]	CQFP256	D1N8A1	0831	12	1000	0	0	0			12000
RTSX72SU[1]	CQFP256	D1SG01	0939	100	168	0					16800
RTSX32SU[1]	CQFP208	D1P8W1	0842	14	2000	0	0	0	0		28000

Table 46 • CMOS Reliability–High Temperature Operating Life (HTOL) (continued)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures						
					Test Time	168	500	1000	2000	6000	Unit Hours
RTSX72SU	CQFP256	D303Y1	0720	80	6000	0	0	0	0	0	480000
RTSX72SU	CQFP208	D1SG11	0947	24	2000	0	0	0	0		48000
RTSX72SU	CQFP84	D1RH51	1007	24	2000	0	0	0	0		48000
RTSX72SU	CQFP256	D6AA61	1351	80	1000	0	0	0			8000
RTSX32SU	CQFP84	D1N8F1	1106	8	1000	0	0	0			8000
RTSX32SU	CQFP84	D1N8F1	1106	8	1000	0	0	0			8000
RTSX32SU	CQFP84	D1N8F1	1126	8	2000	0	0	0	0		16000
RTSX32SU	CQFP208	D1RH41	1323	100	168	0					16800
RTSX32SU	CQFP208	D1RH41	1423	8	1000	0	0	0			8000
RTSX72SU	CQFP208	D1WW91	1221	24	2000	0	0	0	0		48000
RTSX72SU	CQFP256	D1WWA1	1321	100	168	0					16800
RTSX72SU	CQFP208	D20BR1	1330	100	168	0					16800
RTSX72SU	CQFP208	D1SLL1	1334	8	2000	0	0	0	0		16000
RTSX72SU	CQFP208	D6LRQ1	1628	23	1000	0	0	0			23000
RTSX32SU	CQ84	D1RH51	1524	8	1000	0	0	0			8000
RTSX72SU	CQ208	D6LRQ1	1628	23	1000	0	0	0			23000
RTSX72SU	CQ208	D1RCS1	1701	8	2000	0	0	0	0		16000
Total Units for 0.25 µm FPGA = 5554										**Total Test Time Hours = 10214958**	
Total Failures for 0.25 µm FPGA = 0											

1. As part of antifuse reliability testing, HTOL tests were performed on RT54SX32-SU and RT54SX72-SU (UMC 0.25 mm) at varying temperatures and voltages. HTOL data from these tests has been summarized above for CMOS FIT calculation based on the following assumptions.
   - Voltage Acceleration:
     - Tests where VCCA > VCCA (max) (3.0 V) have been ignored.
     - Tests where VCCA = 2.5 V to 3.0 V, voltage acceleration factor for these tests was assumed to be 1.
   - Temperature Acceleration:
     - Stress Temperature = Junction Temperature (i.e., Tstress = TJ).
     - The burn-in hours have been normalized to a TJ of 125 °C (i.e., 106 units at TJ 145 °C burn-in time 168 hours is equivalent to 106 units at TJ 125 °C burn-in time 446.105 hours).
2. ESD failures are represented in parentheses.

Table 47 • CMOS Reliability Low Temperature Operating Life (LTOL)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures							
					Test Time	168	500	1000	2000	3000	6000	Unit Hours
RTSX32SU[1]	CQFP208	D122H1	0434	149	500	0	0					74500
RTSX32SU[1]	CQFP208	D122H1	0434	150	500	0	0					75000
RTSX72SU[1]	CQFP208	D1AYH1, D1KT11	0445, 0519	75	6000	0	0	0	0	0	0	450000
RTSX32SU[1]	CQFP208	D122H1, D1JW21	0434, 0442	152	5000	0	0	0	0	0		760000

Table 47 • **CMOS Reliability Low Temperature Operating Life (LTOL) *(continued)***

						Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**3000**	**6000**	**Unit Hours**
RTSX32SU[1]	CQFP208	D122H1, D1JW21	0434, 0442	2	4000	0	0	0	0	0		8000
RTSX72SU[1]	CQFP256	D0Y311	0410	134	500	0	0					67000
RTSX72SU[1]	CQFP256	D0Y311	0410	8	168	0						1344
RTSX32SU[1]	CQFP256	D19S61	0436	6	1000	0	0	0				6000
RTSX72SU[1]	CQFP208	D0YMJ1		100	500	0	0					50000
RTSX72SU[1]	CQFP208	D0Y311		100	168	0						16800
RTSX72SU[1]	CQFP208	D1AYH1		100	168	0						16800
RTSX32SU[1]	CQFP208	D122H1		100	168	0						16800
RTSX32SU[1]	CQFP208	D1JW21, D1AYJ1	0519, 0502	150	1000	0	0	0				150000
RTSX32SU[1]	CQFP208	D1JW21, D1AYJ1	0519, 0502	150	500	0	0					75000
Total Units for 0.25 µm FPGA = 1376											**Total Test Time Hours =**	**1767244**
Total Failures for 0.25 µm FPGA = 0												

1. LTOL data from antifuse reliability testing performed on RT54SX32-SU and RT54SX72-SU (UMC 0.25 mm).

Table 48 • **Temperature Cycle**

				Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Number of Units**	**Test Cycles**	**200**	**500**	**1000**	**2000**	**Cycles**
			(–65 °C to +150 °C)						
RTSX32SU	CQFP208	D110A1	68	100					6800
RTSX72SU	CQFP208	D0YMJ1	68	100					6800
RTSX32SU	CQFP208	D110A11	135	100					13500
Total Units for 0.22 µm FPGA = 271							**Total Test Cycles =**		**27100**
Total Failures for 0.25 µm FPGA = 0									

3.16 Antifuse Reliability Overview

Failure rates described in this section refer only to the antifuse portion for UMC 0.25 µm RTSX32-SU and RTSX72-SU Microsemi's FPGA products programmed using the standard programming algorithm.

In the ideal case, all the testing would have been performed on these devices alone. However, because of their high cost and lower availability, additional lifetests have been performed on the commercial device type A54SX72A (UMC 0.22 µm). Antifuse failures have been observed in both the military (RTSX32-SU and RTSX72-SU) devices as well as in the commercial (A54SX72A) devices.

3.16.1 Antifuse FIT Rate Calculator

A failure rate calculator in the form of an excel spreadsheet has been developed by The Aerospace Corporation. The statistical procedure used in the calculator to analyze the lifetest data is called the Maximum Likelihood Method (MLE). The model assumed for antifuse failures is a Weibull cumulative

failure distribution as a function of time t (in hours) for n antifuses (EQ 3). The scale factor is given by α (hours) and the shape factor is given by β (dimensionless).

$$F(t) = 1 - \exp\left[(-n)\left(\frac{t}{\alpha}\right)^{\beta}\right]$$

EQ 3

The MLE shape factor was found to be less than one for the antifuses, describing a decreasing failure rate situation. A cumulative failure time model for the antifuse types where failures have been detected is therefore given by

- n1 and α 1 for the number and scale factor respectively for the failing antifuses in military FPGA
- n2 and α 2 for the number and scale factor respectively for the failing antifuse in commercial FPGA
- where as the same shape factor β has been assumed for both military and commercial categories.

The maximum likelihood method was programmed in S-Plus (*http://www.insightful.com*) to determine the coefficients α 1, α 2, and β for both military and commercial FPGAs in one pass. A simultaneous estimate of all three parameters was made with all available data.

The calculator allows the user to describe a particular FPGA design, along with mission parameters, and computes an averaged failure rate for the mission.

Average antifuse FIT for UMC 0.25 µm RTSX-SU FPGA products at a 60% confidence bound is a FIT of 17.

- FIT calculator version used 2.12 (UMC Standard Algorithm FIT Rate Calculator Data v2.12.xls, updated May 2008)
- Total of 1 failure observed for medium timing perceptibility
- Parts are programmed with standard programming algorithm
- Standard Aerospace Industry Design used: Microsemi has provided design characteristics of 42 different Aerospace Industry FPGA programming designs. To provide a guideline, an average or standard design has been obtained by simply taking the average of the antifuses of the various types and using in the FIT rate calculator.
- Screen hours 500
- 10 years of mission life

3.17 Reliability Summary – Silicon Sculptor Programming Software

The following table shows the number of unit-hours of life test data accumulated on radiation-tolerant FPGAs programmed with specific revisions of Silicon Sculptor programming software. Life tests are performed for several reasons: as part of device qualification (1,000 hours or 6,000 hours), as customer-specific life tests (1,000 hours or 2,000 hours), as part of Group C life test (1,000 hours or 2,000 hours), or as part of our standard Enhanced Lot Acceptance (ELA) testing which is performed on samples from every single wafer lot of RT FPGAs (168 hours). Microsemi's official position is that customers are recommended to use the latest version of software. However, customers who are unable

to upgrade to use the latest version of the software may find the life test data useful to determine how much reliability data is accumulated on each version of the programming software.

Table 49 • **Unit-hours of Life Test Data Accumulated on Radiation-Tolerant FPGAs**

Silicon Sculptor S/W Version	RTSX32SU	RTSX72SU	Total per Version
V4.78.1		16,800	16,800
V4.80.0		33,600	33,600
V5.2.0	16,800	64,800	81,600
V5.4.1		16,800	16,800
V5.6.0	48,000		48,000
V5.8.1	16,800		16,800
V5.18.1		2,856	2,856
V5.22.0		64,800	64,800
V5.22.2	8,000		8,000
V5.22.3	8,000		8,000
V5.22.4	16,800	164,000	180,800
V5.22.8		16,000	16,000
V5.22.10	8,000		8,000
V5.22.11		46,000	46,000
V5.22.13	8,000	16,000	24,000
Grand Total	**130,400**	**441,656**	**572,056**

3.18 0.22 µm UMC FPGA Reliability Summary

Table 50 • **CMOS High Temperature Operating Life (HTOL)**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
A54SX08A	PQFP208	DC183 0012		50	1000	0	0	0		50000
A54SX08A	PQFP208	D1X181		90	1000	0	0	0		90000
A54SX08A	PQFP208	D1X191		84	1000	0	0	0		84000
A54SX08A	PQFP208	D7K052 W 2		90	1000	0	0	0		90000
A54SX32A	PQFP208	D7682 14.15 0028		100	1000	0	0	0		100000
A54SX32A and A54SX08A	PQFP208	D7682.14 (HS), D7766.12 (HS), D7682.15 (FS), D7766.19 (FS), DC183(HS)		150	3340	0	0	0	0	501000
A54SX32A	CQFP208	D5GTW1	1125	80	1000	0	0	0		80000
A54SX72A	PQFP208	D03TC1		101	2000	0	0	0	0	202000
A54SX72A	PQFP208	D4F117		38	168	0				6384
A54SX72A	PQFP208	DCT03.1		22	168	0				3696

Table 50 • **CMOS High Temperature Operating Life (HTOL)** ***(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
A54SX72A	FC484[1]	D55011		26	168	0				4368
A54SX72A	PQFP208	D09A21		77	516	0	0			39732
A54SX72A	PQFP208	D09A21		19	168	0				3192
A54SX72A	PQFP208	D03TC1(74), D0KA91 (26)		100	168	0				16800
A54SX72A	PQFP208	DOKA91		100	168	0				16800
A54SX72A	PQFP208	DOKA91		100	168	0				16800
A54SX72A	PQFP208	DCT03.1		90	168	0				15120
A54SX72A	PQFP208	DCT03.1		69	120					8280
A54SX72A and A54SX08A	PQFP208	D2E131, D2E151, D1X171		76	1000	0	0	0		76000
A54SX72A	PQFP208	DC0143		38	516	0	0			19608
A54SX72A	CQFP256	D0F1J1.1		96	615	0				59040
A54SX72A	CQFP256	D0F1J1.1		23	615	0				14145
A54SX72A[2]	PQFP208	D1RCP1		106	446	0				47287
A54SX72A[2]	PQFP208	D1RCP1		108	1328	0	0	0		143391
A54SX72A[2]	PQFP208	D1JTT1		108	2439	0	0	0	0	263361
A54SX72A[2]	PQFP208	D14S71		1	813	0	0			813
A54SX72A[2]	PQFP208	D14S71		131	2439	0	0	0	0	319447
A54SX72A[2]	PQFP208	D1RCP1		200	813	0	0			162568
A54SX72A[2]	PQFP208	D1JTT1		1	446	0				446
A54SX72A[2]	PQFP208	D1JTT1		1	2159	0	0	0	0	2159
A54SX72A[2]	PQFP208	D1JTT1		97	2655	0	0	0	0	257573
A54SX72A[2]	PQFP208	D0H0N1		100	0.65					65
A54SX72A[2]	PQFP208	D03TC1		94	0.66					62
A54SX72A[2]	PQFP208	D09YJ1		100	2.05					205
A54SX72A[2]	PQFP208	D09YJ1		98	1.98					194
A54SX72A[2]	PQFP208	D09YJ1		139	1.97					274
A54SX72A[2]	PQFP208	D092A16		107	6.11					654
A54SX72A[2]	PQFP208	D146W1		104	42.8					4448
A54SX72A[2]	PQFP208	D0KA91		90	6.11					550
A54SX72A[2]	PQFP208	D1JTT1		99	446	0				44165
A54SX72A[2]	PQFP208	D1AYG3		91	446	0				40596
A54SX72A[2]	PQFP208	D1JTT1		1	2092	0	0	0	0	2092
A54SX72A[2]	PQFP208	D1JTT1		100	2655	0	0	0	0	265539
A54SX72A[2]	PQFP208	D1JTT1		102	7966	0	0	0	0	812548
A54SX72A[2]	PQFP208	D1JTT1		108	2655	0	0	0	0	286782

Table 50 • **CMOS High Temperature Operating Life (HTOL) *(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A54SX72A[2]	PQFP208	D03TC1		101	2105	0	0	0	0	212602
A54SX72A[2]	PQFP208	D1JTT1		1	1774	0	0	0		1774
A54SX72A[2]	PQFP208	D1JTT1		203	2655	0	0	0	0	539044
A54SX72A[2]	PQFP208	D1AYG3		108	1328	0	0	0		143391
A54SX72A[2]	PQFP208	D1AYG3		108	1328	0	0	0		143391
A54SX72A[2]	PQFP208	D1AYG3		1	430	0				430
A54SX72A[2]	PQFP208	D1AYG3		107	1328	0	0	0		142063
A54SX72A[2]	PQFP208	D1RCP1		108	5311	0	0	0	0	573564
A54SX72A[2]	PQFP208	D1RCP1		108	5311	0	0	0	0	573564
A54SX72A	CQFP208	D4TW61	1018	80	1000	0	0	0		80000
A54SX72A	PQFP208	D54RJ1	1036	100	168	0				16800
A54SX72A	CQFP208	D77SP1	1334	80	1000	0	0	0		80000
A54SX72A	CQFP208	D8KN57	1527	80	1000	0	0	0		80000
A54SX72A	CQFP256	D9PFP1	1644	79	1000	0	0	0		79000
A54SX72A	CQFP256	D8KN57	1634	8	168	0				1344
A54SX72A	CQFP208	DCHTJ1	1903	80	1000	0	0	0		80000
		Total Units for 0.22 µm FPGA =		**4977**		**Total Test Time Hours =**				**6819151**
		Total Failures for 0.22 µm FPGA = 0								

1. Engineering package.
2. As part of antifuse reliability testing, HTOL tests were performed on A54SX72A (UMC 0.22 µm) at varying temperatures and voltages. HTOL data from these tests has been summarized above for CMOS FIT calculation based on the following assumptions.

   Voltage Acceleration:

   Tests where $V_{CCA} > V_{CCA(max)}$ (3.0 V) have been ignored

   Tests where V_{CCA} = 2.5 V to 3.0 V, voltage acceleration factor for these tests was assumed to be 1.

   Temperature Acceleration:

   Stress Temperature = Junction Temperature (i.e., $T_{stress} = T_J$).

   The burn-in hours have been normalized to a TJ of 125 °C (i.e., 106 units at T_J 145 °C burn-in time 168 hours is equivalent to 106 units at T_J 125°C burn-in time, 446.105 hours).

Table 51 • **Low Temperature Operating Life (LTOL)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A54SX08A	PQFP208	DC183	0012	50	1000	0	0	0		50000
A54SX32A	PQFP208	D7682 14.15	0028	100	1000	0	0	0		100000
A54SX72A	PQFP208	DC0143		38	168	0				6384
A54SX72A and A54SX08A	PQFP208	D2E13, D2E151, D1X171		76	1000	0	0	0		76000
A54SX72A	PQFP208	D4F117		38	168	0				6384

Table 51 • Low Temperature Operating Life (LTOL) (continued)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	168	500	1000	2000	Unit Hours
A54SX72A	PQFP208	DCT03.1		22	168	0				3696
A54SX72A[1]	PQFP208	D03TC1		101	2000	0	0	0	0	202000
A54SX72A[1]	PQFP208	D1JTT1		108	1000	0	0	0		108000
A54SX72A	PQFP208	D0KA91		85	168	0				14280
A54SX72A	FC484[2]	D55011		26	168	0				4368
A54SX32A and A54SX08A	PQFP208	DC183(HS)		150	1000	0	0	0		150000
		Total Units for 0.22 µm FPGA =		**794**				**Total Test Time Hours =**		**721112**
		Total Failures for 0.22 µm FPGA = 0								

1. LTOL data from antifuse reliability testing on A54SX72A (UMC 0.22 µm).
2. Engineering package.

Table 52 • Biased Humidity (HAST)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures: Test Time	50	100	200	500	Unit Hours
A54SX08A	PQFP208	DC183	0012	50	100	0	0			5000
A54SX32A	PQFP208	D7682 14.15	0028	100	100	0	0			10000
A54SX72A	PQFPG208[1, 2]	D20CW1	0828	47	100	0	0			4700
		Total Units for 0.22 µm FPGA =		**197**			**Total Test Time Hours =**			**19700**
		Total Failures for 0.22 µm FPGA = 0								

1. G indicates lead-free.
2. Unbiased HAST (JESD22 A118), 130 °C and RH = 85%.

Table 53 • Temperature Cycle

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Cycles/Failures: Test Cycles	200	500	1000	2000	Cycles
				(–65 °C to +150 °C)						
A54SX08A	PQFP208	DC183	0012	50	1000	0	0	0		50000
A54SX32A	PQFP208	D7682 14.15	0028	100	1000	0	0	0		100000
A54SX72A	PQFP208	DC0143		38	500	0	0			19000
A54SX72A + 08A	PQFP208	D2E131,D2E151, D1X171		76	1000	0	0	0		76000
A54SX72A	PQFP208	D4F117		38	500	0	0			19000
A54SX72A	FC484[1]	D55011		26	1000	0	0	0		26000

Table 53 • **Temperature Cycle *(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Cycles/Failures					
					Test Cycles	200	500	1000	2000	Cycles
A54SX32A + 08A	PQFP208	D7682.14 (HS), D7766.12(HS) D7682.15 (FS), D7766.19(FS) DC183(HS)		150	1000	0	0	0		150000
A54SX32A	TQFP176	BP34640-1 and D1JA1	0515, 0516, 0517	77	1000	0	0	0		77000
A54SX32A	PBGA329	D26E61	0610	22	1000	0	0	0		22000
A54SX72A	PQFPG208[2]	D20CW1	0828	46	1000	0	0	0		46000
Total Units for 0.22 µm FPGA = 601								**Total Test Cycles = 563000**		
Total Failures for 0.22 µm FPGA = 0										

1. Engineering package.
2. G indicates lead-free.

3.19 0.22 µm UMC Flash FPGA Reliability Summary

Table 54 • **High Temperature Operating Life (HTOL)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
APA1000	PBGA456	M279F, M279C		43	1000	0	0	0		43000
APA750	PBGA456	M1T74, M3AA6		86	1000	0	0	0		86000
APA750	PBGA456	MFJ2W, MFJ2S, MFJ2T		77	1000	0	0	0		77000
APA750	PBGA456	MFRGH, MFPQ8		18	1000	0	0	0		18000
APA750	PBGA456	MFR6H, MFPQ8		18	1000	0	0	0		18000
APA750	PBGA456	MFJ2W, MFJ2T, MFJ2S		77	1000	0	0	0		77000
APA750[1]	PBGA456	M3AA4	0336	84	2000	(1)	0	(1)	0	167668
APA1000	CQFP352	MK3KA	0517	132	1115	0	0	0		147180
APA600	CQFP352	MR5T2		80	1000	0	0	0		80000
APA600[2]	CQFP208	MNRML		47	615	0	0			28905
APA1000	CQFP352	MR91L	1025	24	2000	0	0	0	0	48000
APA300	CQFP208	MK91G	1036	24	2000	0	0	0	0	48000
APA300	PQFP208	MTG7J02	1045	77	168	0				12936
APA1000	CQFP208	MWJ9W	1144	78	1000	0	0	0		78000
APA600	CQFP208	R00KY	1226	80	1000	0	0	0		80000
APA300	CQFP208	R21A5	1346	80	1000	0	0	0		80000
APA1000	CQFP208	R569Y	1608	80	1000	0	0	0		80000

Table 54 • High Temperature Operating Life (HTOL) (continued)

APA600	CQFP208	RCGR5	1821	80	1000	0	0	0	80000
APA600	CQFP208	RCGR5	1821	80	500	0	0		40000
Total Units for 0.22 µm Flash FPGA = 1265								**Total Test Time Hours = 1289689**	
Total Failures for 0.22 µm Flash FPGA = 0									

1. One device failed at 168 hours and it was confirmed due to ESD. The second one failed at 1500 hours and this failure resulted from testing a feature that has been removed from silicon. The test programs have subsequently been updated.
2. Tested at 150 °C. Equivalent hours corresponding to 125 °C were used to calculate the FIT rates.

Table 55 • Low Temperature Operating Life (LTOL)

					Test Hours/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
APA1000	PBGA456	M297F, M279C		26	1000	0	0	0		26000
APA750	PBGA456	M1T74, M3AA6		51	1000	0	0	0		51000
Total Units for 0.22 µm Flash FPGA = 77								**Total Test Time Hours = 77000**		
Total Failures for 0.22 µm Flash FPGA = 0										

Table 56 • Endurance

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**1000**	**Cycles**
Room Temperature										
APA1000	CGA391	M297F, M279C		30	500	0	0	0		15000
APA750	CGA391	MFJ2W, MFJ2S, MFJ2T		30	500	0	0	0		15000
Total Units for 0.22 µm Flash FPGA = 60								**Total Test Cycles = 30000**		
Total Failures for 0.22 µm Flash FPGA = 0										

Table 57 • Retention 225 °C Unbiased 100% Programmed

					Test Hours/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**72**	**500**	**1000**	**3000**	**Unit Hours**
APA1000	CGA391	MAE49, MC147, MC148		73	3000	0	0	0	0	219000
APA750	CGA391	MFJ2W, MFJ2S, MFJ2T		12	1000	0	0	0		12000
Total Units for 0.22 µm Flash FPGA = 85								**Total Test Time Hours = 231000**		
Total Failures for 0.22 µm Flash FPGA = 0										

Table 58 • Retention 225 °C Unbiased 100% Erased

						Test Hours/Failures				
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	72	500	1000	3000	Unit Hours
APA1000	CGA391	MAE49, MC147, MC148		73	3000	0	0	0	0	219000
APA750	CGA391	MFJ2W, MFJ2S, MFJ2T		73	1000	0	0	0		73000
Total Units for 0.22 µm Flash FPGA = 146								Total Test Time Hours =		292000
Total Failures for 0.22 µm Flash FPGA = 0										

Table 59 • Temperature Cycle

					Number of Cycles/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	200	500	1000	2000	Cycles
APA750	PBGA456[1]	M3AA4		16	1000	0	0	0		16000
APA1000	PQFPG208[2, 3]	MQRRS	0839	46	1000	0	0	0		46000
Total Units for 0.22 µm Flash FPGA = 62								Total Test Cycles =		62000
Total Failures for 0.22 µm Flash FPGA = 0										

1. Condition B, –55 °C to +125 °C.
2. G indicates lead-free.
3. Condition C, –65 °C to +150 °C.

3.20 0.15 µm UMC FPGA Reliability Summary

Table 60 • High Temperature Operating Life (HTOL)

					Test Hours/Failures							
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Time at T_J 125 °C	168	500	1000	2000	6000	Unit Hours
AX1000	PQFP208	DO3121, DO3131, DO4CA1		129	1000	125	1000	0	0	0			129000
AX1000	PQFP208	D097H1, DO97J1		77	1000	125	1000	0	0	0			77000
AX2000	FBGA896	D0HGC1, DOH3M6		38	1000	125	1000	0	0	0			38000
AX2000	FBGA896	D16T91	0431	22	1000	125	1000	0	0	0			22000
AX2000	FBGA896	D2A5A1	0620	77	1000	125	1000	0	0	0			77000
RTAX1000S[1]	CQFP352	D1GAH1	0444, 0507	98	1000	132	1423	0	(4)[2]	0			133762
RTAX2000S[1]	CQFP352	D1L9R1	0506	87	1000	132	1423	0	(2)[2]	0			120955
RTAX1000S[1]	CGA624	D1GAH1	0444	150	1000	132	1423	(1)[3]	(5)[3]	0			204912
RTAX1000S[1]	CGA624	D1GAH1	0444	28	1000	132	1423	0	1[4]	0			38421

Table 60 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
RTAX1000S[1]	CGA624	D1GAH1	0444	120	6000	132	8538	0	0	0	0	0	1024560
RTAX2000S[1]	CGA1152	D1PPY1		6	1000	132	1423	0	0	0			8538
RTAX2000S[1]	CQFP352	D1N9H1		6	1000	132	1423	0	0	0			8538
RTAX2000S[1]	CQFP352	D1GAG1		14	168	132	239	0					3346
RTAX2000S[1]	CQFP352	D1N9H1		14	168	132	239	0					3346
RTAX2000S[1]	CQFP352	D21PH1		14	168	132	239	0					3346
RTAX1000S[1]	CGA624	D1KH51		37	1000	132	1423	0	0	0			52651
RTAX1000S[1]	CQFP352	D1KH51		8	1000	132	1423	0	0	0			11384
RTAX2000S[1]	CQFP352	D1R0G1		14	168	132	239	0					3346
RTAX2000S[1]	CQFP352	D1L9R1		14	168	132	239	0					3346
RTAX2000S[1]	CQFP352	D1PPY1		14	168	132	239	0					3346
RTAX250S[1]	CQFP352	D1H381		100	168	132	239	0					23900
RTAX1000S[1]	CGA624	D1PQ01		150	1000	132	1423	0	0	0			213450
RTAX2000S[1]	CQFP352	D1N9H1		14	168	132	239	0					3346
RTAX1000S[1]	CGA624	D1KH51		24	168	132	239	0					5736
RTAX2000S[1]	CQFP352	D1NSG1		14	168	132	239	0					3346
RTAX250S[1]	CQFP208	D1H381		6	1000	125	1000	0	0	0			6000
RTAX2000S[1]	CQFP352	D1KHN1		78	1000	125	1000	0	0	0			78000
RTAX1000S[1]	CQFP352	D1NR91		24	168	132	239	0					5736
RTAX2000S[1]	CQFP352	D1KHN1		14	168	132	239	0					3346
RTAX2000S[1]	CQFP352	D21PH1		6	1000	125	1000	0	0	0			6000
RTAX4000S[1]	LGA1272	D30141	0730	75	6000	142	13844	0	0	0	0	0	1038310
RTAX4000S[1]	LGA1272	D30141	0730	1	3000	142	6922	0	0	0	0		6922
RTAX4000S[1,5]	LGA1272	D30141	0730	1	2000	142	4614	0	0	0	0		4614
RTAX2000	CQFP352	D1L9R1		6	2000	125	2000	0	0	0	0		12000
RTAX250S	CQFP352	D1M6K1		100	168	125	168	0					16800
RTAX2000S	CQFP352	D2S8K1		79	1000	125	1000	0	0	0			79000
RTAX2000S	CGA624	D2S8M1		14	168	125	168	0					2352
RTAX2000S	CGA624	D2T2A1		24	1000	125	1000	0	0	0			24000
RTAX2000S	CQFP352	D21PH1		8	2000	125	2000	0	0	0	0		16000
RTAX2000S	CGA624	D1N9H1		6	2000	125	2000	0	0	0	0		12000
RTAX2000S	CGA624	D1N9H1		2	1000	125	1000	0	0	1[6]			2000
RTAX2000S	CGA624	D2T2A1		8	2000	125	2000	0	0	0	0		16000
RTAX2000S	CGA624	D2S8N5		14	168	125	168	0					2352
RTAX2000S	CGA624	D2T2C1		14	168	125	168	0					2352

Table 60 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
RTAX2000S	CQFP352	D2T2C1		11	2000	125	2000	0	0	0	0		22000
RTAX2000S	CQFP352	D2WG61		11	2000	125	2000	0	0	0	0		22000
RTAX2000S	CGA624	D2S8N5		8	1000	125	1000	0	0	0			8000
RTAX4000S[1]	LGA1272	D31CA1	0735	24	2000	131	2708	0	0	0	0		64992
RTAX2000S	CGA624	D2WG61		14	168	125	168	0					2352
RTAX2000S	CGA624	D334Y1		14	168	125	168	0					2352
RTAX4000S	LGA1272	D31CA1		15	2000	125	2000	0	0	0	0		30000
RTAX2000S	CQFP352	D334Y1		8	2000	125	2000	0	0	0	0		16000
RTAX1000S	CQFP352	D1NR91		8	1000	125	1000	0	0	0			8000
RTAX1000S	CQFP352	D1NR91		11	2000	125	2000	0	0	0	0		22000
RTAX2000S	CGA624	D32R41		24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CQFP352	D3CA81		14	168	125	168	0					2352
RTAX2000S	CQFP352	D3HY41		14	168	125	168	0					2352
RTAX4000S	CQFP352	D31CF1		8	168	125	168	0					1344
RTAX4000S	LGA1272	D30121		8	168	125	168	0					1344
RTAX2000S	CGA624	D3HY31		14	168	125	168	0					2352
RTAX250S[1]	CQFP208	D1H381 D1M6K1		82	3000	132	4269	0	0	0	0		350062
RTAX250S[1]	CQFP208	D1H381		8	1000	131	1354	0	0	0			10833
RTAX250S[1]	CQFP352	D1H381		8	1000	131	1354	0	0	0			10833
RTAX250S[1]	CQFP352	D1H381		7	1000	131	1354	0	0	0			9479
RTAX250S[1]	CQFP352	D1H381		1	500	131	677	0	0				677
RTAX1000S[1]	CGA624	D1PQ01		150	1000	132	1423	0	0	0			213452
RTAX1000S[1]	CQFP352	D1NR91		25	2000	134	3141	0	0	0	0		78521
RTAX1000S[1]	CQFP352	D2S8P8		24	168	134	264	0					6332
RTAX1000S[1]	CQFP352	D1NR91		8	1000	134	1570	0	0	0			12563
RTAX2000S[1]	CGA624	D2S8N5 D2S8M1		82	3000	134	4711	0	0	0	0		386323
RTAX2000S[1]	CQFP352	D3T0N1		80	1000	137	1817	0	0	0			145389
RTAX2000S[1]	CGA624	D2T2C1		8	1000	137	1817	0	0	0			14539
RTAX2000S[1]	CQFP352	D3CA81		8	1000	137	1817	0	0	0			14539
RTAX2000S[1]	CQFP352	D3HY41		8	1000	137	1817	0	0	0			14539
RTAX2000S[1]	CQFP352	D3WJA1		14	168	137	305	0					4274
RTAX2000S[1]	CAFP352	D404N1		14	168	137	305	0					4274
RTAX2000S[1]	CGA624	D2T2A1		8	1000	137	1817	0	0	0			14539

Table 60 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
RTAX2000S[1]	CQFP352	D3CA81		8	2000	137	3635	0	0	0	0		29078
RTAX2000S[1]	CQFP352	D3WJA1		8	1000	137	1817	0	0	0			14539
RTAX1000S[1]	CGA624	D1PQ01		2	168	137	305	0					611
RTAX1000S[1]	CGA624	D1PQ01		22	2000	137	3635	0	0	0	0		79964
RTAX1000S[1]	CQFP352	D1PQ01		8	1000	137	1817	0	0	0			14539
RTAX2000S[1]	CGA624	D3WJA1		8	1000	131	1354	0	0	0			10833
RTAX2000S[1]	CGA624	D477A1		14	168	137	305	0					4274
RTAX2000S[1]	CQFP352	D45C11		14	168	137	305	0					4274
RTAX2000S	CQFP352	D517P1	1034	79	1500	125	1500	0	0	0			118500
RTAX2000S	CQFP352	D4CYF1	1004	80	1000	125	1000	0	0	0			8000
RTAX2000S	CQFP352	D404N1	0938	8	2000	125	2000	0	0	0	0		16000
RTAX2000S	CQFP352	D55A21	1049	7	1000	125	1000	0	0	0			7000
RTAX2000SL	CQFP256	D55A31	1052	22	2000	125	2000	0	0	0	0		44000
RTAX2000S	CQFP352	D54C81	1106	8	1000	125	1000	0	0	0			8000
RTAX2000S	CQFP352	D63WS1	1225	80	1000	125	1000	0	0	0			80000
RTAX4000S	CQFP352	D3T0N1	0818	44	1000	125	1000	0	0	0			44000
RTAX4000S	CGA1152	D404N1	0825	6	1000	125	1000	0	0	0			6000
RTAX4000D	CQFP352	D4LJQ1	1003	47	1000	125	1000	0	0	0			47000
RTAX4000SL	CQFP352	D41891	1110	24	1000	125	1000	0	0	0			24000
RTAX2000S	CQFP256	D71CM1	1350	79	1000	125	1000	0	0	0			79000
RTAX2000SL	CQFP256	D6CTH1	1338	23	2000	125	2000	0	0	0	0		46000
RTAX2000S	CQFP352	D6CN21	1345	24	2000	125	2000	0	0	0	0		48000
RTAX4000DL	CQFP352	D64NH1	1251	7	2000	125	2000	0	0	0	0		14000
RTAX4000S	CG1272	D3KYP1	1251	10	2000	125	2000	0	0	0	0		20000
RTAX4000S	CQ352	D3LG61	1249	8	168	125	168	0					1344
RTAX4000S	CQ352	D3LG61	1324	24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CQ352	D55A31	1138	15	168	125	168	0					2520
RTAX2000S	CQ352	D55A31	1138	15	854	125	854	0	0				12810
RTAX2000S	CGS624	D56J31	1225	24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CQ352	D5A7S1	1213	8	1000	125	1000	0	0	0			8000
RTAX1000S	CQ352	D5G811	1250	27	2005	125	2005	0	0	0	0		54135
RTAX2000D	CQ352	D5G821	1546	24	2000	125	2000	0	0	0	0		48000
RTAX20002	CG1152	D5HK31	1307	23	2000	125	2000	0	0	0	0		46000
RTAX2000S	CGS624	D5S2W1	1220	14	168	125	168	0					2352
RTAX4000D	CQ352	D64NH1	1251	7	2024	125	2024	0	0	0	0		14168

Table 60 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
RTAX250S	CQ352	D59RQ1	MIXED	100	168	125	168	0					16800
RTAX2000S	CQ256	D63WR	1214	24	168	125	168	0					4032
RTAX2000S	CQ256	D63WR	1214	15	168	125	168	0					2520
RTAX2000S	CQ256	D66PC1	1235	24	2007	125	2007	0	0	0	0		48168
RTAX2000S	CQ352	D6CTJ1	1248	14	168	125	168	0					2352
RTAX2000S	CG1152	D6G7Q1	1506	8	1000	125	1000	0	0	0			8000
RTAX2000S	CQ352	D6G7Q1	1445	8	1000	125	1000	0	0	0			8000
RTAX250S	CQ352	D8KNM1	1526	100	168	125	168	0					16800
RTAX250S	CQ352	D8KNM1	1526	80	1000	125	1000	0	0	0			80000
RTAX2000S	CQ352	D68N41	1238	14	168	125	168	0					2352
RTAX1000S	CQ352	D6AS91	1314	24	168	125	168	0					4032
RTAX4000S	CQ352	D6CM91	1317	8	168	125	168	0					1344
RTAX2000S	CGS624	D6CN11	1405	8	2000	125	2000	0	0	0	0		16000
RTAX2000S	CQ352	D6CN21	1304	14	168	125	168	0					2352
RTAX2000S	CQ352	D6CN21	1345	24	2002	125	2002	0	0	0	0		48048
RTAX1000S	CQ352	D6CSS1	1249	24	168	125	168	0					4032
RTAX1000S	CQ352	D6CSS1	1448	24	2000	125	2000	0	0	0	0		48000
RTAX1000S	CQ352	D6CST1	1313	24	168	125	168	0					4032
RTAX2000S	CQ256	D6CTH1	1338	23	2000	125	2000	0	0	0	0		46000
RTAX2000S	CQ352	D6G7P1	1434	8	2000	125	2000	0	0	0	0		16000
RTAX2000S	CQ352	D6G7P1	1434	8	1000	125	1000	0	0	0			8000
RTAX2000S	CG1152	D6G7Q1	1351	14	171	125	171	0					2394
RTAX2000S	CQ352	D6M7F1	1304	14	168	125	168	0					2352
RTAX4000D	CQ352	D6NR61	1312	8	180	125	180	0					1440
RTAX2000S	CQ352	D6W3Q1	1316	14	168	125	168	0					2352
RTAX2000S	CQ352	D71CM1	1343	14	168	125	168	0					2352
RTAX2000S	CQ256	D71CM1	1350	79	1010	125	1010	0	0	0			79790
RTAX2000S	CQ352	D72TK1	1343	14	168	125	168	0					2352
RTAX2000S	CQ256	D75K91	1348	14	168	125	168	0					2352
RTAX2000S	CQ352	D77J81	1405	14	168	125	168	0					2352
RTAX2000S	CQ352	D79G91	1410	14	168	125	168	0					2352
RTAX4000S	CQ352	D7FLT1	1418	8	168	125	168	0					1344
RTAX4000D	CQ352	D7P6Q1	1419	8	168	125	168	0					1344
RTAX4000D	CQ352	D82W41	1614	8	160	125	160	0					1280
RTAX4000D	CQ352	D82W41	1614	8	24	125	24						192

Table 60 • **High Temperature Operating Life (HTOL)** ***(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
RTAX250S	CQ208	D8KNM1	1534	24	2000	125	2000	0	0	0	0		48000
RTAX2000D	CQ352	D8QLF1	1546	14	168	125	168	0					2352
RTAX4000S	CQ352	D8TW11	1614	8	168	125	168	0					1344
RTAX4000S	CG1272	D8TW11	1624	24	1002	125	1002	0	0	0			24048
RTAX4000SL	CQ352	DA28R1	1708	8	168	125	168	0					1344
RTAX4000S	CQ352	DAC0F1	1741	8	168	125	168	0					1344
RTAX2000S	CQ352	D9WYQ1	1716	14	168	125	168	0					2352
RTAX2000S	CQ352	D9WYQ1	1716	80	1000	125	1000	0	0	0			80000
RTAX2000S	CGS624	D77J81	1650	24	2000	125	2000	0	0	0	0		48000
RTAX4000S	CG1272	D8TW11	1624	23	1000	125	1000	0	0	0			23000
RTAX4000S	CQ352	DC2WR1	1743	8	168	125	168	0					1344
RTAX4000S	CQ352	DC78W1	1746	8	168	125	168	0					1344
RTAX2000S	CQ352	DAHWT1	1744	14	168	125	168	0					2352
RTAX2000S	CQ352	DC78T1	1750	14	168	125	168	0					2352
RTAX2000S	CQ352	DC9RF1	1805	14	168	125	168	0					2352
RTAX2000D	CQ352	D8QLF1	1745	24	1000	125	1000	0	0	0			24000
RTAX2000S	CQ256	DAHWT1	1737	24	2000	125	2000	0	0	0	0		48000
RTAX1000S	CGS624	D6CST1	1820	24	2000	125	2000	0	0	0	0		48000
RTAX4000D	CQ352	D75KA1	1350	8	168	125	168	0					1344
RTAX4000D	CQ352	D75KA1	MIXED	9	168	125	168	0					1512
RTAX250S	CQ208	D8KNM1	1806	8	500	125	500	0	0				4000
RTAX2000D	CQ352	D8QLF1	1745	24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CGS624	D9WYQ1	1811	24	2000	125	2000	0	0	0	0		48000
RTAX4000S	CG1272	DA28R1	1822	24	2009	125	2009	0	0	0	0		48216
RTAX4000S	CG1272	DAC0F1	1807	24	2000	125	2000	0	0		0		48000
RTAX2000S	CGS624	DC78T1	1814	24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CQ352	DC9RF1	1815	8	500	125	500	0	0				4000
RTAX2000S	CQ352	DC9RF1	1815	8	500	125	500	0	0				4000
RTAX2000S	CQ352	DCPHF1	1816	14	168	125	168	0					2352
RTAX2000S	CGS624	DCPHF1	1831	24	2000	125	2000	0	0	0	0		48000
RTAX4000S	CQ352	DCPHG1	1833	8	168	125	168	0					1344
RTAX4000S	CQ352	DCRNK1	1834	8	168	125	168	0					1344
RTAX4000S	CQ352	DCSGS1	1825	8	168	125	168	0					1344
RTAX2000S	CQ352	DCWA41	1829	14	168	125	168	0					2352
RTAX2000S	CG1152	DCWA41	1845	24	2000	125	2000	0	0	0	0		48000

Table 60 • High Temperature Operating Life (HTOL) (continued)

					Test Hours/Failures								
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Time at T_J 125 °C	168	500	1000	2000	6000	Unit Hours
RTAX2000S	CQ352	DCWA51	1824	14	168	125	168	0					2352
RTAX2000S	CGS624	DCWA51	1838	24	2000	125	2000	0	0	0	0		48000
RTAX2000S	CQ352	DF1W81	1834	14	168	125	168	0					2352
RTAX2000S	CQ352	DF7W41	1842	14	168	125	168	0					2352
RTAX2000S	CQ352	DCYKA1	1842	14	168	125	168	0					2352
RTAX2000S	CQ352	DF7W31	1845	14	168	125	168	0					2352
RTAX2000S	CQ352	DF7W91	1849	14	168	125	168	0					2352
RTAX2000S	CQ352	DFAWC1	1923	14	168	125	168	0					2352
Total Units for 0.15 µm FPGA = 4858												**Total Test Time Hours = 7428820**	
Total Failures for 0.15 µm FPGA = 2													

1. HTOL data summarized above for CMOS FIT calculation based on the following assumptions.
   Voltage Acceleration:
   VCCA = 1.6 V, voltage acceleration factor for these tests has been assumed to be 1.
   Temperature Acceleration:
   Stress Temperature = Junction Temperature (i.e., Tstress = TJ).
   The burn-in hours have been normalized to a TJ of 125 °C (i.e., 100 units at TJ 132 °C burn-in time 1000 hours is equivalent to 100 units at TJ 125 °C burn-in time 1423.015 hours)
2. ESD represented in parentheses – ESD failures due to high ESD levels on test loadboard sockets. Failure analysis was completed and to improve the ESD environment during the testing and programming flow, Microsemi's CQFP test socket vendor manufactured socket lids with an ESD fatriendly polymer material that reduces the ESD charge to about 15 V. Microsemi has replaced all CQFP socket lids in our test and programming facility with these "ESD-Friendly" lids. Microsemi issued PCN0512 for ESD-Friendly Lid Replacement for CQFP Programming Modules.
3. Continuity failures caused by contention problems with the burn-in driver and the device. Failure analysis was completed and contention was fixed on the burn-in board adaptor.
4. CMOS failure happened at 500 hours. Failure analysis concluded the root cause as incomplete oxide etch during fabrication process.
5. Unit passed 2000 hours (4614 hours at 125 °C) but failed post 3000 hours (6922 hours at 125 °C). Failure not counted towards device FIT, as FA concluded it was due to the F/G leak test procedure. Test procedure has been updated and FA report is available upon request.
6. One unit failed SRAM at 1000 hours.

Table 61 • Low Temperature Operating Life (LTOL)

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
AX1000	PQFP208	DO3121, DO3131, DO4CA1		129	1000	0	0	0		129000
AX1000	PQFP208	D097H1, D097J1		77	1000	0	0	0		77000
AX2000	FBGA896	D0HGC1, D0H3M6		38	1000	0	0	0		38000
RTAX1000S	CQFP352	D1GAH1	0444, 0507	78	1000	0	(1)[1]	0		77000
RTAX1000S	CGA624	D1GAH1		144	250	0				36000

Table 61 • **Low Temperature Operating Life (LTOL) *(continued)***

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
RTAX1000S	CGA624	D1GAH1		150	250	(2)[2]				37000
RTAX1000S	CGA624	D1PQ01		148	250	0				37000
RTAX1000S	CGA624	D1PQ01		150	250	0				37500
RTAX2000S	CQFP352	D1KHN1		78	168	0				13104
RTAX250S	CQFP208	D1H381 D1M6K1		82	3000	0	0	0	0	246000
RTAX4000S	LGA1272	D31CA1		24	1000	0	0	0		24000
RTAX2000S	CGA624	D2S8N5 D2S8M1		82	3000	0	0	0	0	246000
Total Units for 0.15 µm FPGA = 1180								**Total Test Time Hours = 997604**		
Total Failures for 0.15 µm FPGA = 0										

1. ESD represented in parentheses – ESD failures due to high ESD levels on test loadboard sockets. Failure analysis was completed and to improve the ESD environment during the testing and programming flow, Microsemi's CQFP test socket vendor manufactured socket lids with an ESD friendly polymer material that reduces the ESD charge to about 15V. Microsemi has replaced all CQFP socket lids in our test and programming facility with these "ESD-Friendly" lids. Microsemi issued PCN0512 for ESD-Friendly Lid Replacement for CQFP Programming Modules.
2. Continuity failures caused by contention problems with the burn-in driver and the device. Failure analysis was completed and contention was fixed on the burn-in board adaptor.

Table 62 • **Biased Humidity**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
AX1000	PQFP208	DO3121, DO3131, DO4CA1		129	100	0	0			12900
AX2000	FBGA896	D0HGC1, D0H3M6		38	100	0	0			3800
Total Units for 0.15 µm FPGA = 167							**Total Test Time Hours = 16700**			
Total Failures for 0.15 µm FPGA = 0										

Table 63 • **Temperature Cycle**

					Number of Test Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**100**	**200**	**500**	**1000**	**Cycles**
				(–65 °C to +150 °C)						
AX1000	PQFP208	DO3121, DO3131, DO4CA1		129	500	0	0	0		64500
AX1000	PQFP208	D097H1, D097J1		77	500	0	0	0		38500

Table 63 • **Temperature Cycle *(continued)***

AX2000	FBGA896	D0HGC1, D0H3M6		22	500	0	0	0		11000
RTAX4000S	LGA1272	D30141		15	1000	0	0	0	0	15000
RTAX4000D	CQFP352	D4LJQ1	1003	15	100	0				150
Total Units for 0.15 µm FPGA = 258								**Total Test Cycles = 129150**		
Total Failures for 0.15 µm FPGA = 0										

3.21 Reliability Summary – Silicon Sculptor Programming Software

The following tables list the number of unit-hours of life test data accumulated on Radiation-Tolerant FPGAs programmed with specific revisions of Silicon Sculptor programming software. Life tests are performed for several reasons: as part of device qualification (1,000 hours or 6,000 hours), as customer-specific life tests (1,000 hours or 2,000 hours), as part of Group C life test (1,000 hours or 2,000 hours), or as part of our standard Enhanced Lot Acceptance (ELA) testing which is performed on samples from every single wafer lot of RT FPGAs (168 hours). Microsemi's official position is that customers are recommended to use the latest version of software. However, customers who are unable to upgrade to use the latest version of the software may find the life test data useful to determine how much reliability data is accumulated on each version of the programming software.

Table 64 • **Unit-hours of Life Test Data**

Silicon Sculptor S/W Version	RTAX250S	RTAX1000S	RTAX2000S	RTAX4000S	RTAX2000D	RTAX4000D	Total per Version
V3.89	24,800						24,800
V3.93	6,000						6,000
V4.64.0	16,800						16,800
V4.68.1			33,704	528,000			561,704
V4.70.0			2,352				2,352
V4.70.1	5,000	10,000	57,856	2,520			75,376
V4.74			2,352	1,344			3,696
V4.76.0				2,520			2,520
V4.78.0			80,000				80,000
V4.78.1			8,000				8,000
V4.80.0	32,000	74,064	20,704				126,768
V5.2.0	48,000	4,032	116,056				168,088
V5.4.1		6,048		44,000			50,048
V5.6.0	48,000		15,056	6,000		282,799	351,855
V5.8.1		11,368	81,352				92,720
V5.10.1			14,000				14,000
V5.12.0	8,000	4,032	10,352				22,384
V5.12.1	16,800	4,032	64,704				85,536
V5.14.1		12,032	114,352	51,344	2,352		180,080
V5.18.0		4,032	89,408			1,680	95,120
V5.22.0			264,464			1,344	265,808

Table 64 • **Unit-hours of Life Test Data *(continued)***

Silicon Sculptor S/W Version	RTAX250S	RTAX1000S	RTAX2000S	RTAX4000S	RTAX2000D	RTAX4000D	Total per Version
V5.22.1	8,000		4,704				12,704
V5.22.2		93,032	86,112	1,344		14,504	194,992
V5.22.3		8,064	96,872	30,000		1,440	136,376
V5.22.4			203,322	50,688			254,010
V5.22.5			16,000			1,344	17,344
V5.22.8			32,000				32,000
V5.22.9	16,800	48,000	4,032				68,832
V5.22.10	128,000				2,352		130,352
V5.22.11			4,872	48,392	48,000	1,472	102,736
V5.22.13			183,056	5,376	24,000		212,432
V5.22.14	8,000	48,000	271,520	100,248	48,000	2,856	478,624
Grand Total	**366,200**	**326,736**	**1,877,202**	**871,776**	**124,704**	**307,439**	**3,397,785**

3.22 0.13 µm Infineon Flash FPGA Reliability Summary (ProASIC3 – A3P)

Table 65 • **High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles**

					Test Hours/Failures							
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Time at T_J 125°C	168	500	1000	2000	Unit Hours
A3P060	FBGA256	ZA612052	0626	129	1000	133	1495	0	0	0		192855
A3P060	FBGA144	ZA835014	0838	77	1000	137	1817	0	0	0		139937
A3P125	FBGAG144[1]	ZA614041	0646	82	1000	130	1288	0	0	0		105616
A3P250	FBGA256	ZA519154	0527	15	168	133	251	0				3765
A3P250[2]	FBGA256	ZA519154, ZA519154.01, ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	3000	133	4485	0	0	0	0	578565
A3P250	FBGA256	ZA628252.05	0628	77	1000	133	1495	0	0	0		115115
A3P400	FBGA256	ZA614042	0637	77	1000	133	1495	0	0	0		115115
A3P1000[2]	FBGAG484[1]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	129	2000	134	3141	0	0	0	0	405189
A3P1000	FBGAG484[1]	ZA63718002	0640	77	1000	134	1570	0	0	0		120890

Table 65 • **High Temperature Operating Life (HTOL) After 550 Program/Erase Cycles *(continued)***

					Test Hours/Failures							
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A3P1000	FBGAG484[1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	2008	134	3153	0	0	0		728343
A3P1000	FBGAG484[1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	2427	48	134	75					182025
A3PE1500	FBGAG484[1]	ZA707790	0715, 0716, 0717	77	1000	134	1570	0	0	0		120890
A3P1000	FBGAG484	ZA252062	1312	77	1000	134	1570	0	0	0		120890
Total Units for 0.13 µm FPGA = 3604											**Total Test Time Hours = 2929195**	
Total Failures for 0.13 µm FPGA = 0												

1. G indicates lead-free.
2. Initial 1000 hours HTOL completed per qualification requirement, HTOL was continued up to:
   3000 hours for A3P250, all units passed.
   2000 hours for A3P1000, all units passed.

Table 66 • **Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A3P250	FBGA256	ZA519154	0527	15	168	0				2520
A3P250[1]	FBGA256	ZA519154, ZA519154.01, ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	2000	0	0	0	0	258000
A3P1000	FBGAG484[2]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	129	1000	0	0	0		129000
A3PE1500	FBGAG484[2]	ZA707790	0715, 0716, 0717	77	1000	0	0	0	0	77000
A3P250	VQG100[2, 3]	ZA418036	1430, 1431, 1432	231	500	0	0			115500
Total Units for 0.13 µm FPGA = 581									**Total Test Time Hours = 582020**	
Total Failures for 0.13 µm FPGA = 0										

1. Initial 1000 hours LTOL completed per qualification requirement, LTOL was continued up to 2000 hours, all units passed.

2. G indicates lead-free.
3. VQ100 package release by extension.

Table 67 • **Temperature Cycle (T_C), –55 °C to +125 °C**

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Test Cycles/Failures					
					Test Cycles	200	500	1000	2000	Cycles
A3P250	FBGA256	ZA519154, ZA519154.01, ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	1000	0	0	0		129000
A3P1000	FBGAG484[1]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	77	1000	0	0	0		77000
A3P1000	FBGAG484[2,1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	1000	0	0	0		231000
A3PE1500	FBGAG484[1]	ZA707790	0715, 0716, 0717	77	1000	0	0	0		77000
A3PE1500	PQFPG208[1,3]	ZA732709	0811	48	1000	0	0	0		48000
A3P250	VQFP100[3]	ZA840056	1010	47	500	0	0			23500
A3P1000	PQFPG208[1,3]	ZA31005102	1314	47	500	0	0			23500
A3P250	QNG132[1,3]	ZA249133	1320	47	500	0	0			23500
A3P250	VQG100[1,3]	ZA418036	1430, 1431, 1432	231	1000	0	0	0		231000
A3PE3000	FGG896	QMSRG	1607	50	1000	0	0	0		50000
A3PE1500	FBGAG484[1,4]	ZA623005	1703	47	1000	0	0	0		47000
A3P1000	FBGAG484[1,4]	ZA717024	1727	75	1000	0	0	0		75000
A3P1000	FGG256[5]	ZA815072	1825	80	1000			0		80000
			1826	80	1000			0		80000
			1827	80	1000			0		80000
		Total Units for 0.13 µm FPGA =		**1346**					**Total Test Cycles =**	**1275500**
			Total Failures for 0.13 µm FPGA = 0							

1. G indicates lead-free.
2. Automotive (AEC Q-100) Grade 1 –50 °C to +150 °C.
3. Condition C, –65 °C to +150 °C (AECQ-100) Grade.
4. Condition B (JESD22 A104), -55 °C to 125 °C
5. Condition H (JESD22 A104), -55 °C to 150 °C or Grade 1 (AEC-Q100)

Table 68 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A3P250	FBGA256	ZA519154	0527	22	264	0	0	0	0	5808
A3P250	FBGA256	ZA519154, ZA519154.01, ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	264	0	0	0	0	34056
A3P1000	FBGAG484	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	77	264	0	0	0	0	34056
A3P1000	FBGAG484[1,2]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	96	0				22176
A3PE1500	FBGAG484[2]	ZA707790	0715, 0716, 0717	77	264	0	0	0	0	20328
A3PE1500	PQFPG208[2,3]	ZA732709	0811	47	100	0	0			4700
A3P250	VQFP100[3]	ZA840056	1010	47	100	0	0			4700
A3P1000	PQFPG208[2,3]	ZA31005102	1314	47	96	0				4512
A3P250	QNG132[2,3]	ZA249133	1320	47	96	0				4512
A3P250	VQG100[1,2,3]	ZA418036	1430, 1431, 1432	231	96	0				22176
A3P250	VQG100[1,2]	ZA418036	1430, 1431, 1432	231	96	0				22176
A3P1000	FGG256[2,3]	ZA424029	1433	45	264	0	0	0	0	11880
A3PE3000	FGG896	QMSRG	1607	50	264	0	0	0	0	13200
A3PE1500	FGG484[2,4,5]	ZA623005	1703	47	264	0	0	0	0	12408
A3P1000	FGG484[2,4,5]	ZA717024	1727	75	264	0	0	0	0	19800
A3P1000	FGG256[4]	ZA815072	1825	80	264	0	0	0	0	21120
			1826	80	264	0	0	0	0	21120
			1827	80	264	0	0	0	0	21120
A3P1000	FGG256[6]	ZA815072	1825	80	264	0	0	0	0	21120
			1826	80	264	0	0	0	0	21120
			1827	80	264	0	0	0	0	21120
Total Units for 0.13 µm FPGA = 1883							**Total Test Time Hours = 363208**			
Total Failures for 0.13 µm FPGA = 0										

1. Automotive (AEC-Q100) 130 °C and RH = 85%.
2. G indicates lead-free.
3. Unbiased HAST (JESD22 A118), 130 °C and RH = 85%.
4. Unbiased HAST (JESD22 A118), 110 °C and RH = 85%.
5. AuPCC wire.
6. Biased HAST (JESD22 A118), 110 ºC and RH = 85%

Table 69 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**2000**	**Unit Hours**
A3P250	FBGA256	ZA519154, ZA519154.01, ZA523569, and ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	1000	0	0	0		129000
A3P1000	FBGAG484[1]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	77	1000	0	0	0		77000
A3P1000	FBGAG484[1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	1000	0	0	0		231000
A3PE1500	FBGAG484[1]	ZA707790	0715, 0716, 0717	77	1000	0	0	0		77000
A3P1000	PQFPG208[1]	ZA31005102	1314	45	1000	0	0	0		45000
A3P250	QNG132[1]	ZA249133	1320	47	1000	0	0	0		47000
A3P250	VQG100[1,2]	ZA418036	1430, 1431, 1432	77	1000	0	0	0		77000
A3P1000	FGG256[1]	ZA815072	1825	47	1000	0	0	0		47000
			1826	47	1000	0	0	0		47000
			1827	47	1000	0	0	0		47000
Total Units for 0.13 µm FPGA = 824									**Total Test Cycles = 824000**	
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. Automotive (AEC-Q100).

Table 70 • **Temperature Humidity Bias (THB), 85 °C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**2000**	**Unit Hours**
A3P1000	FBGAG484[1]	ZA641734	0647	77	2000	0	0	0	0	154000

Table 70 • Temperature Humidity Bias (THB), 85 °C / 85% RH (continued)

A3P1000	PQFPG208[1]	ZA648504	0712	22	2000	0	0	0	0	44000
A3P1000	PQFPG208[1]	ZA719018	0743	22	2000	0	0	0	0	44000
A3P1000	FBGAG256[1]	ZA627018	0634	22	2000	0	0	0	0	44000
A3P250	FBGAG256[1]	ZA644020	0711	22	2000	0	0	0	0	44000
	Total Units for 0.13 µm Flash FPGA = 165							**Total Test Time Hours = 330000**		
	Total Failures for 0.13 µm Flash FPGA = 0									

1. G indicates lead-free.

Table 71 • Endurance (Room Temperature)

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**3000**	**Cycles**
A3P250	FBGA256	ZA519154	0527	5	3000	0	0	0	0	150000
A3P250	FBGA256	ZA519154, ZA519154.01 ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	550	0	0	0		70950
A3P1000	FBGAG484[1]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	77	550	0	0	0		42350
A3P1000	FBGAG484[1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	550	0	0	0		127050
A3PE1500	FBGAG484[1]	ZA707790	0715, 0716, 0717	77	550	0	0	0		42350
	Total Units for 0.13 µm Flash FPGA = 519							**Total Test Cycles = 432700**		
	Total Failures for 0.13 µm Flash FPGA = 0									

1. G indicates lead-free.

Table 72 • Retention at 250 °C After 550 Program/Erase Cycles

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**72**	**500**	**1000**	**3000**	**Unit Hours**
A3P250	CQFP208[1]	ZA519154	0527	45	168	0				7560

Table 72 • Retention at 250 °C After 550 Program/Erase Cycles (continued)

A3P250	CQFP208[1]	ZA519154, ZA519154.01, ZA523569, ZA523569.01	0532, 0533, 0534, 0536, 0537, 0538, 0541, 0543	129	1000	0	0	0		129000
A3P1000	CQFP208[1]	ZA546185, ZA538175.02, ZA548138	0604, 0602, 0608, 0609	77	500	0	0			38500
A3P1000	CQFP208[1]	ZA63718002 ZA63717902 ZA64173402 ZA70708902	0640 0642 0645 0707	231	1008[2]	0	0	0		232848
A3P1000	CQFP208[1]	ZA64173402, ZA648504, ZA649017	0650 0717 0705	149	3000	0	1[3]	0	0	447000
A3PE1500	CQFP208[1]	ZA707790	0715, 0716, 0717	77	1000	0	0	0		77000
Total Units for 0.13 µm Flash FPGA = 559								**Total Test Time Hours =**		**446408**
Total Failures for 0.13 µm Flash FPGA = 1										

1. Not commercially available (i.e., the engineering package is for reliability testing only).
2. Retention at 150 °C per Automotive AEC-Q100.
3. Single-bit random failure on erase side at 168 hours; physical analysis shows poly1 defect.

3.23 0.13 µm Infineon Flash FPGA Reliability Summary (Fusion – AFS)

Table 73 • High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles

								Test Hours/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**168**	**500**	**1000**	**2000**	**Unit Hours**
AFS1500	FBGA256	ZA915053	0919	77	168	141	370	0				28467
AFS1500	FBGA256, FBGAG256[1]	ZA748708 ZA74902101	0806 0810	110	2000	144	5068	0	(1)[2]	0	0	557579
AFS600	FBGA256	ZA652744, ZA652745, ZA701716	0702 0709 0712	129	1000	141	2200	0	0	0	0	283903
AFS600	FBGA256	ZA705109	0718	87	168	141	369	0				32163
AFS600	FBGA256	ZA729021	0741	68	3200	141	7042	0	0	0	0	478894
AFS600	FBGA256	ZA729021	0741	70	1000	141	2200	0	0	0	0	154056

Table 73 • High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles *(continued)*

					Test Hours/Failures							
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Time at T_J 125°C	168	500	1000	2000	Unit Hours
AFS250	FBGA256, FBGAG256[1]	ZA702009, ZA702008, ZA704181	0733	163	1000	135	1649	0	0	0		268819
Total Units for 0.13 µm FPGA = 704											**Total Test Time Hours =**	**1803883**
Total Failures for 0.13 µm FPGA = 0												

1. G indicates lead-free.
2. 1 unit failed after 500 hours of HTOL, continuity failure observed on PTBASE pin at ATE test (resistive short). Burning power supply monitoring logs during HTOL do not show increase in current. Probable root cause suspected as ESD (handling after 500 hr. pull point for electrical testing), hence not counted towards device FIT.

Table 74 • Low Temperature Operating Life (LTOL) at –55 °C After 550 Program/Erase Cycles

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	168	500	1000	2000	Unit Hours
AFS1500	FBGA256, FBGAG256[1]	ZA748708 ZA74902101	0806 0810	68	1000	0	0	0		68000
AFS600	FBGA256	ZA652744, ZA652745, ZA701716	0702 0709 0712	129	1000	0	0	0		129000
AFS250	FBGA256, FBGAG256[1]	ZA702009, ZA702008, ZA704181	0733	48	1000	0	0	0		48000
Total Units for 0.13 µm FPGA = 245									**Total Test Time Hours =**	**245000**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 75 • Temperature Cycle (T_C), –55 °C to +125 °C

					Number of Test Cycles/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	200	500	1000	2000	Cycles
AFS1500	FBGAG256[1]	ZA748708 ZA74902101	0806 0810	48	1000	0	0	0		48000
AFS600	FBGA256	ZA617031, ZA619115, ZA617032	0623 0631 0629	129	1000	0	0	0		129000
AFS600	FBGA484[1]	ZA932055	1008	47	1000	0	0	0		47000
AFS1500	FGG256[1]	ZA736018	1832	47	700	0	0			32900
Total Units for 0.13 µm FPGA = 271									**Total Test Cycles =**	**256900**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 76 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**2000**	**Unit Hours**
AFS1500	FBGAG256[1]	ZA748708 ZA74902101	0806 0810	50	1000	0	0	0		50000
AFS250	QNG180[1]	ZA702009, ZA702008, ZA704181	0723	45	1000	0	0	0		45000
Total Units for 0.13 µm FPGA = 95								**Total Test Cycles =**		**95000**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 77 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
AFS1500	FBGAG256[1]	ZA748708 ZA74902101	0806 0810	69	264	0	0	0	0	18216
AFS600	FBGA256	ZA729021	0741	45	264	0	0	0	0	11880
AFS250	FBGA256, FBGAG256[1]	ZA702009, ZA702008, ZA704181	0733	75	264	0	0	0	0	19800
AFS1500	FGG256[1,2]	ZA736018	1832	47	264	0	0	0	0	12408
Total Units for 0.13 µm FPGA = 236								**Total Test Time Hours =**		**62304**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. Unbiased HAST (100 °C / 85% RH)

Table 78 • **Endurance (FPGA NVM) at Room Temperature**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**1000**	**Cycles**
Room Temperature										
AFS1500	FBGA256 FBGAG256[1]	ZA748708 ZA74902101	0806 0810	77	550	0	0	0		42350
AFS600	FBGA256	ZA617031, ZA619115, ZA617032	0623 0631 0629	129	550	0	0	0		70950
Total Units for 0.13 µm Flash FPGA = 206								**Total Test Cycles =**		**113300**
Total Failures for 0.13 µm Flash FPGA = 0										

1. G indicates lead-free.

Table 79 • **Endurance (eNVM) at Room Temperature**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**1000**	**Cycles**
				Room Temperature						
AFS600	FBGA256	ZA617031, ZA619115, ZA617032	0623 0631 0629	129	1000	0	0	0	0	129000
Total Units for 0.13 µm Flash FPGA = 129									**Total Test Cycles =**	**129000**
Total Failures for 0.13 µm Flash FPGA = 0										

Table 80 • **Retention (FPGA NVM) at 250 °C after 550 Program/Erase Cycles**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**72**	**500**	**1000**	**2000**	**Unit Hours**
AFS1500	CQFP208[1]	ZA748708 ZA74902101	0806 0810	77	2000	0	0	0	0	154000
AFS600	CQFP208[1]	ZA617031, ZA619115, ZA617032	0623 0631 0629	129	500	0	0			64500
Total Units for 0.13 µm Flash FPGA = 206								**Total Test Time Hours =**		**218500**
Total Failures for 0.13 µm Flash FPGA = 0										

1. Not commercially available (i.e., the engineering package is for reliability testing only).

Table 81 • **Retention (eNVM) at 250 °C after 1000 Program/Erase Cycles**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number Units**	**Test Time**	**72**	**500**	**1000**	**3000**	**Unit Hours**
AFS600	CQFP208[1]	ZA617031, ZA619115, ZA617032	0623 0631 0629	129	500	0	0			64500
Total Units for 0.13 µm Flash FPGA = 129								**Total Test Time Hours =**		**64500**
Total Failures for 0.13 µm Flash FPGA = 0										

1. Not commercially available (i.e., the engineering package is for reliability testing only).

3.24 0.13 µm Infineon Flash FPGA Reliability Summary (SmartFusion – A2F)

Table 82 • **High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles**

					Test Hours/Failures							
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**TJ (°C)**	**Test Time at Tj 125 °C**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A2F200	FBGAG484[1]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	247	2000	133	2990	0	0	0	0	738571
A2F200	FBGAG484[1]	ZA925010	1004	82	1000	133	1495	0	0	0		122597
A2F500	FBGAG484[1]	ZA01402801	1018	82	1000	136	1731	0	0	0		141977
A2F200	FBGA484	ZA027289	1216	76	1000	133	1495	0	0	0		113626
A2F200	FGG484	ZA027289	1216	76	168	133	168	0				12768
Total Units for 0.13µm FPGA = 563										**Total Test Time Hours = 1129539**		
Total Failures for 0.13 µm FPGA = 0												

1. G indicates lead-free.

Table 83 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**2000**	**Unit Hours**
A2F200	FBGAG484[1]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	90	1000	0	0	0		90000
A2F200	FBGA484	ZA027289	1216	47	1000	0	0	0		47000
Total Units for 0.13 µm FPGA = 137								**Total Test Cycles = 137000**		
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 84 • **Temperature Humidity Bias (THB), 85 °C / 85% RH**

					Test Hours/Failures				
Product	**Packages**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A2F200	FBGA484	ZA027289	1216	53	1008	0	0	0		53424
A2F500	CSG288[1,2]	ZA822043	1834	47	264	0				12408
Total Units for 0.13 µm FPGA = 100								**Total Test Time Hours = 63832**		
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. Unbiased HAST (100 ºC, 85% RH).

Table 85 • **Temperature Cycle (TC), –55 °C to +125 °C**

						Test Hours/Failures				
Product	Packages	Wafer Lot	Date Code	Number of Units	Test Cycles	200	500	1000	2000	Cycles
A2F500	CSG288[1]	ZA822043	1834	47	700	0				32900
Total Units for 0.13 µm FPGA = 47								**Total Test Cycles = 32900**		
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 86 • **Endurance (eNVM)**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	100	500	1000	Cycles
A2F200[1]	FBGAG484[2]	ZA917060 ZA91706101 ZA9410050	0923 0943 0947	201	1100	0	0	0	221100
A2F200[1]	CQFP208[3]	ZA917060 ZA91706101 ZA9410050	0923 0943 0947	117	1100	0	0	0	128700
A2F200[4]	FBGAG484[2]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	128	1100	0	0	0	140800
Total Units for 0.13 µm FPGA = 446								**Total Test Cycles = 490600**	
Total Failures for 0.13 µm FPGA = 0									

1. Room temperature, 25 °C.
2. G indicates lead-free.
3. Not commercially available (i.e., the engineering package is for reliability testing only).
4. Temperature +55 °C ≤ T_J ≤ 85 °C.

Table 87 • **Retention (eNVM) after 1100 Program/Erase Cycles**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	10	500	1000	Unit Hours
A2F200[1]	CQFP208[2]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	117	1000	250	0	0	0	117000
A2F200[3]	FBGAG484[4]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	128	10	125	0			1280
Total Units for 0.13 µm Flash FPGA = 245									**Total Test Time Hours = 118280**	
Total Failures for 0.13 µm Flash FPGA = 0										

1. HTDR after 1100 program/erase cycles at 25 °C.
2. Not commercially available (i.e., the engineering package is for reliability testing only).
3. HTDR per JEDEC after 1100 program/erase cycles at +55 °C ≤Tj ≤ 85 °C.
4. G indicates lead-free.

Table 88 • **Low Temperature Retention and Read Disturb (eNVM) at 25 °C after 1100 Program/Erase Cycles, 25 °C**

					Test Hours/Failures					
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	10	50	100	500	Unit Hours
A2F200	FBGAG484[1]	ZA917060 ZA91706101 ZA94100501	0923 0943 0947	120	500	0	0	0	0	60000
Total Units for 0.13 µm Flash FPGA = 120								Total Test Time Hours = 60000		
Total Failures for 0.13 µm Flash FPGA = 0										

1. G indicates lead-free.

3.25 0.13 µm UMC Flash FPGA Reliability Summary (IGLOO—AGL/AGLE; IGLOO PLUS–AGLP; IGLOO nano–AGLN)

Table 89 • **High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles**

					Test Hours/Failures								
Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Time at T_J 125°C	168	500	1000	2000	4000	Unit Hours
AGLE3000	FBGAG484[1]	QHC25 QHC3T	0809 0813	45	1000	130	1288	0	0	(3)[2]			57968
AGL1000	FBGAG484[1]	QHF28	0816	129	1000	132	1423	0	0	0			183569
AGL600	FBGAG256[1]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	4000	130	5152	(1)[3]	0	0		0	664608
AGLN250	VQFPG100[1]	QHT2W	0915	129	2000	128	2330	0	0	0	0		300563
AGLP125	VQFP100	QHJFP	0823	129	2000	128	2330	0	0	0			300563
AGL030	VQFP100	QH6MQ	0745	77	168	130	216	0					16632
AGL600	FBGAG256[1]	QHSYQ	0925	79	1000	130	1288	0	0	0			101767
AGL1000	FBGAG484	QL1Y6	1250	75	1000	132	1423	0	0	0			106726
Total Units for 0.13 µm FPGA = 792										Total Test Time Hours = 1732396			
Total Failures for 0.13 µm FPGA = 0													

1. G indicates lead-free.
2. 3/48 failed IIH and IIL post 1000 hours HTOL. All three failures confirmed to be due to V_{CCI} overshoots on the ATE tester during qualification read points, not counted towards device FIT. Implemented new VIH/L test vectors to eliminate the V_{CCI} overshoots and updated Test Program release procedures to include over/undershoot verification prior to release.
3. 1 unit failed HTOL post 168 hours due to bond wire shorting. Failure will be screened by post assembly electrical test, hence not counted towards device FIT. No other failures were observed until 5152 hours.
   Microsemi implemented I/O-to-I/O short test, 100% screening for production.
   STATS enhanced the wire loop height control of the affected wires and optimized mold parameter settings.

Table 90 • **Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles**

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours/Failures					
					Test Time	168	500	1000	2000	Unit Hours
AGL600	FBGAG256[1]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	1000	0	0	0		129000
AGL030	VQFP100	QH6MQ	0745	77	168	0				12936
Total Units for 0.13 µm FPGA = 206								**Total Test Time Hours = 141936**		
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 91 • **Temperature Cycle (TC), –55 °C to +125 °C**

Product	Package	Wafer Lot	Date Code	Number of Units	Number of Test Cycles/Failures					
					Test Cycles	200	500	1000	2000	Cycles
AGL600	FBGAG256[1]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	1000	0	0	(1)[2]		129000
AGL600	FBGA256	QHCFR	0820	80	1000	0	0	0		80000
AGL030	VQFP100	QH62A	0739, 0741, 0743	77	1000	0	0	0		77000
AGLN020	QNG68[1]	QHSKK	0909 0910	77	1000	0	0	0		77000
AGL060	CSG121[1]	QHR76	0928	45	1000	0	0	0		45000
AGLP125	VQFP100	QHJFP	0823	129	1000	0	0	0		129000
AGLP030	VQFPG128[1,3]	QJY60	1345	47	500	0	0			23500
AGLP125	CSG289[1]	QMM3P	1612, 1613	78	1000	0	0	0		78000
AGL400	CSG196[1,4]	QNRT9	1727, 1728	81	1000	0	0	0		81000
AGL1000	CSG289[1]	QP352	1834	47	700	0	0			32900
Total Units for 0.13 µm FPGA = 790									**Total Test Cycles = 752400**	
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. 1 unit failed after 1000 hours TC due to bond wire shorting. Failure will be screened by post assembly electrical test.
   Microsemi implemented I/O-to-I/O short test, 100% screening for production.
   STATS enhanced the wire loop height control of the affected wires and optimized mold parameter settings.
3. Condition C, –65 °C to +150 °C.
4. CSG196 package using Au flashed Palladium Coated Cu (AuPCC)

Table 92 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
AGL600	FBGAG256[1]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	264	0	0	0	0	34056
AGLN250	VQFPG100[1]	QHT2W	0915	77	264	0	0	0	0	20328
AGL060[2]	CSG121[1]	QHR76	0928	45	264	0	0	0	0	11880
AGLP030	VQFPG128[1,2]	QJY60	1345	47	96	0				4512
AGL1000	CSG281[1,2]	QLMWN	1417	45	264				0	11880
AGLP125	CSG289[1,2]	QMM3P	1612 1613	78	264	0	0	0	0	20592
AGL400	CSG196[1,3,4]	QNRT9	1727 1728	81	264	0	0	0	0	21384
AGL1000	CSG281[1,5]	QP352	1834	47	264	0	0	0	0	12408
		Total Units for 0.13 µm FPGA =		**549**			**Total Test Time Hours =**			**137040**
				Total Failures for 0.13 µm FPGA = 0						

1. G indicates lead-free.
2. Unbiased HAST (JESD22 A118), 130 °C and RH = 85%.
3. Unbiased HAST (JESD22 A118), 130 °C and RH = 85%.
4. CSG196 package using Au flashed Palladium Coated Cu (AuPCC).
5. Unbiased HAST (JESD22 A118), 100 °C and RH = 85%.

Table 93 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**200**	**500**	**1000**	**3000**	**Unit Hours**
AGL1000	PQFP208	QHR6N	0850	99	3000	0	0	0	0	297000
AGL600	FBGAG256[1]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	1000	0	0	0		129000
AGLN250	VQFPG100[1]	QHT2W	0915	77	1000	0	0	0		77000
AGLN250	VQFPG100[1]	QHT2W	0915	77	3000	0	0	0	0	231000
AGLP125	VQFP100	QHJFP	0823	129	1000	0	0	0		129000
AGL030	VQFP100	QH62A	0739, 0741, 0743	77	1000	0	0	0		77000
AGLN020	QNG68[1]	QHSKK	0909 0910	77	1000	0	0	0		77000
AGLP030	VQFPG128[1]	QJY60	1345	47	1000	0	0	0		47000

Table 93 • High Temperature Storage (HTS), 150 °C (continued)

AGLP125	CSG289	QMM3P	1612, 1613	78	1000	0	0	0	78000
AGL400	CSG196[1,2]	QNRT9	1727 1728	80	1000	0	0	0	80000
Total Units for 0.13 µm FPGA = 870								**Total Test Cycles = 1222000**	
Total Failures for 0.13 µm FPGA = 0									

1. G indicates lead-free.
2. CSG196 package using Au flashed Palladium Coated Cu (AuPCC).

Table 94 • Endurance 550 Program/Erase Cycles

					Number of Cycles/Failures				
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**1000**	**Cycles**
AGL1000[1]	PQFP208	QHR6N	0850	99	550	0	0	0		54450
AGL600[1]	FBGAG256[2]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	550	0	0	0		70950
AGLN250[1]	VQFPG100[2]	QHT2W	0915	77	550	0	0	0		42350
Total Units for 0.13 µm Flash FPGA = 305								**Total Test Cycles = 167750**	
Total Failures for 0.13 µm Flash FPGA = 0									

1. Room temperature, 25 °C.
2. G indicates lead-free.

Table 95 • Retention at 250 °C after 550 Program/Erase Cycles

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**72**	**500**	**1000**	**3000**	**Unit Hours**
AGL1000[1]	CQFP208[2]	QHRYQ	0910	80	3000	0	0	0	0	240000
AGL600[1]	CQFP208[2]	QH4GT1, QH4GW, QH4H01	0728, 0730, 0722, 0727, 0726, 0732	129	1000	0	0	0		129000
AGLN250[1]	CQFP208[2]	QHT2W	0915	77	3000	0	0	0	0	231000
Total Units for 0.13 µm Flash FPGA = 286								**Total Test Time Hours = 600000**		
Total Failures for 0.13 µm Flash FPGA = 0										

1. Program/erase cycles at room temperature, 25.°C.
2. Not commercially available (i.e., the engineering package is for reliability testing only).

3.26 0.13 µm UMC Flash FPGA Reliability Summary (ProASIC3, ProASIC3E – A3P, A3PE; ProASIC3L, ProASIC3EL – A3PL, A3PEL; ProASIC3 nano – A3PN, RT ProASIC3 – RT3P)

Table 96 • **High Temperature Operating Life (HTOL) after 550 Program/Erase Cycles**

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125 °C**	**168**	**500**	**1000**	**2000**	**3000**	**Unit Hours**
A3P600	FBGAG256[1]	QH4H0	0728	81	1000	130	1288	0	0	0			104343
A3PE3000	FBGAG484[1]	QHC9T	0806	1	2000	135	3298	0	0	0	0	1[2]	3298
			0808 0809	128	6000	135	9895	0	0	0	0	0	1266552
RT3PE3000L	CGA896	QHR8G	0925	81	1000	142	2307	0	0	0	0		186896
RT3PE3000L	CGA896	QJA2G	1205	47	1000	142	2307	0	0	0	0		108446
RT3PE3000L	CGA484	QKN6Y	1341	80	1000	125	1000	0	0	0			80000
RT3PE3000L	CGA484	QJA2G	1031	78	1000	125	1000	0	0	0			78000
RT3PE3000L	LGA896	QJA2G	1123	6	1000	125	1000	0	0	0			6000
RT3PE3000L	CG896	QKN6Y	1406	60	1000	125	1000	0	0	0			60000
RT3PE3000L	CQ256	QMLPK	1625	80	1000	125	1000	0	0	0			80000
Total Units for 0.13 µm FPGA = 642												**Total Test Time Hours =**	**1973535**
Total Failures for 0.13 µm FPGA = 1													

1. G indicates lead-free.
2. One CMOS failure was observed at 3000 hours, Tj 135.24°C (equivalent to 44 years of operation at 55°C); failure counted toward device FIT (used Ea of 0.7 eV as FA inconclusive; root cause could not be established). 128 units from this lot (QHC9T) continued to 6000 hours without failures.

Table 97 • **Low Temperature Operating Life (LTOL) at –55 °C after 550 Program/Erase Cycles**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**500**	**1000**	**2000**	**Unit Hours**
A3P600	FBGAG256[1]	QH4H0	0728	82	1000	0	0	0		82000
Total Units for 0.13 µm FPGA = 82									**Total Test Time Hours =**	**82000**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

Table 98 • **Temperature Cycle (TC), –55 °C to +125 °C**

					Number of Test Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**100**	**200**	**500**	**1000**	**Cycles**
A3PE3000	FBGAG484[1]	QHC9T	0806, 0808, 0809	77	1000	0	0	0	0	77000
A3P600	FBGAG256[1]	QL7H0	1323	45	700	0	0	0		31500
A3PN250	VQFPG100[1,2]	QL5CL	1309	45	500	0	0	0		22500
A3PE3000	FGG484[3]	QMYP4	1642, 1643, 1644	81	1000	0	0	0	0	81000
A3PE3000	FGG324[1,3]	QPJF3	1832	72	700	0	0	0		50400
Total Units for 0.13 µm FPGA = 320									**Total Test Cycles =**	**262400**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. Condition C, –65 °C to +150 °C.
3. Condition B, –55 °C to +125 °C

Table 99 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**250**	**Unit Hours**
A3PE3000	FBGAG484[1]	QHC9T	0806, 0808, 0809	77	264	0	0	0	0	20328
A3PE3000	FBGAG484[1]	QHR8G	0921	77	3000	0	0	0	0	231000
A3PN250	VQFPG100[1,2]	QL5CL	1309	45	1000	0	0	0	0	45000
A3PE3000	FGG484	QMYP4	1642, 1643, 1645	81	264	0	0	0	0	21384
A3PE3000	FGG324[1,3]	QPJF3	1832	72	264	0	0	0	0	19008
Total Units for 0.13 µm FPGA = 352									**Total Test Cycles =**	**336720**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.
2. Temperature Humidity Bias (THB), 85 °C / 85% RH.
3. Unbiased HAST (U-HAST) 100 °C / 85% RH

Table 100 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**500**	**1000**	**2000**	**3000**	**Unit Hours**
A3PE3000	FBGAG484[1]	QHC9T	0806, 0808, 0809	77	2000	0	0	0		154000
A3P600	FBGAG256[1]	QL7H0	1323	45	1000	0	0			45000
A3PN250	VQFPG100[1]	QL5CL	1309	45	1000	0	0			45000
A3PE3000	FGG484	QMYP4	1642, 1643, 1645	81	1000	0	0			81000
Total Units for 0.13 µm FPGA = 248									**Total Test Cycles =**	**325000**
Total Failures for 0.13 µm FPGA = 0										

1. G indicates lead-free.

3.27 65 nm UMC Flash FPGA Reliability Summary (SmartFusion2—M2S (S,T,TS), IGLOO2–M2GL (S,T,TS) Product Families)

Table 101 • **High Temperature Operating Life (HTOL)**

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**48**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
M2S050	FBGAG896[1]	SH5Y8 SK1P8 SK1P7	1303 1252 1304	244	1000	138.6	1963		0	0	0			478940
M2S050	FBGAG896[1]	SQ4L9	1318	80	6000	138.6	11777		0	0	0	0	0	942177
M2S050	FBGAG896[1]	SQ4L9	1318	19	2000	146.8	5772		0	0	0	0		109673
M2S150	FCG1152[1]	SAYLT SCCTJ	1406 1407 1408	136	6000	133.2	9059		0	0	0	0	0	1232067
M2S090	FGG676[1,2]	SCMSP SCTAY SCTCA	1409 1409 1414	246	1000	140	2099			0	0	0		516276

Table 101 • **High Temperature Operating Life (HTOL) *(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**48**	**168**	**500**	**1000**	**2000**	**6000**	**Unit Hours**
M2S090	FGG676[1,2]	SCMSP SCTAY SCTCA SFKSN SFPRP14 SGGAA20 SFKSN SFPRP14 SGGAA20	1409 1409 1414 1434 1436 1438 1439 1441 1443	3615	48	140.3	102	0						369576
Total Units for 65 nm FPGA = 4340													**Total Test Time Hours = 3648709**	
Total Failures for 65 nm FPGA = 0														

1. G indicates lead-free.
2. Automotive (AEC-Q100).

Table 102 • **Low Temperature Operating Life (LTOL)**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**168**	**500**	**1000**	**Unit Hours**
M2S050	FBGAG896[1]	SK1P7	1304	35	1000	-47	0	0	0	35000
M2S050	FBGAG896[1]	SQ4L9	1318	34	1000	-51	0	0	0	34000
M2S150	FCG1152[1]	SCCTJ	1406	37	1000	-50	0	0	0	37000
Total Units for 65 nm FPGA = 106									**Total Test Time Hours = 106000**	
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.

Table 103 • **Temperature Cycle (TC), –55 °C to +125 °C**

					Number of Test Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**700**	**1000**	**Cycles**
M2S050	FBGAG896[1]	SH5Y8 SK1P8 SK1P7	1303 1252 1304	84	1000	0	0	0	0	84000
M2S150	FCG1152[1]	SCCTJ	1406 1407 1408	81	700	0	0	0		56700
M2S090	FGG676[1,2]	SCMSP SCTAY SCTCA	1409 1409 1414	237	1000	0	0	0	0	237000
M2S010	FCG1152[1]	SCCTJ	1406 1407 1408	225	500	0	0			112500

Table 103 • **Temperature Cycle (TC), –55 °C to +125 °C *(continued)***

					Number of Test Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**200**	**500**	**700**	**1000**	**Cycles**
M2S150	FCG1152[1]	SCCTJ	1406 1407 1408	225	700	0	0	0		157500
M2S010	TQG144[1,3]	SGQJF	1439 1441 1414	225	500	0	0			112500
M2S090	FCS325	SCTAY	1421 1425 1426	225	700	0	0	0		157500
M2S090	FCS325	SFAKR	1421 1422 1423	225	1000	0	0	0	0	225000
M2S150	FCSG536[1]	SHNNJ	1510 1511 1512	225	700	0	0	0		157500
M2S090	FG676	SHTGO	1505 1506 1507	225	1000	0	0	0	0	225000
M2S090	FGG676[1]	SCMSP	1407	25	1000	0	0	0	0	25000
M2S050	VFG400[1]	SN9Y144	1325	25	1000	0	0	0	0	25000
M2S050	FGG896[1]	SK1P8 SG3N704 SH5Y8	1301 1303 1304	225	1000	0	0	0	0	225000
Total Units for 65 nm FPGA = 2252								**Total Test Cycles= 1800200**		
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.
2. Grade1, –55 °C to +150 °C.
3. Cond C, –65 °C to +150 °C.

Table 104 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH**

					Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**264**	**528**	**Unit Hours**
M2S050	FBGAG896[1]	SH5Y8 SK1P8 SK1P7	1303 1252 1304	84	264	0	0	0	0		22176
M2S150	FCG1152[1]	SCCTJ	1422 1423 1424	80	264	0	0	0	0		21120
M2S150	FCG1152[1]	SCCTJ	1406 1407 1408	225	264	0	0	0	0		59400

Table 104 • **Biased Humidity Accelerated Stress Test (HAST), 110 °C / 85% RH *(continued)***

					Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**50**	**100**	**200**	**264**	**528**	**Unit Hours**
M2S010	TQG144[1,2]	SGQJF	1439 1441 1441	225	264	0	0	0	0		59400
M2S090	FCS325	SCTAY	1421 1425 1426	225	264	0	0	0	0		59400
M2S090	FCS325	SFAKR	1421 1422 1423	225	264	0	0	0	0		59400
M2S150	FCSG536[1]	SHNNJ	1510 1511 1512	225	264	0	0	0	0		59400
M2S090	FG676[2]	SHTGO	1505 1506 1507	225	528	0	0	0	0	0	118800
M2S090	FGG676[1,2]	SCMSP	1407	25	264	0	0	0	0		6600
M2S050	VFG400[1]	SN9Y144	1325	25	264	0	0	0	0		6600
M2S050	FGG896[1]	SK1P8 SG3N704 SH5Y8	1301 1303 1304	225	264	0	0	0	0		59400
Total Units for 65 nm FPGA = 2265									**Total Test Time Hours= 659360**		
Total Failures for 65 nm FPGA = 0											

1. G indicates lead-free.
2. Unbiased HAST(JED22 A118), 130 °C and RH = 85%.

Table 105 • **High Temperature Storage (HTS), 150 °C**

					Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**500**	**1000**	**2000**	**3000**	**4000**	**Unit Hours**
M2S050	FBGAG896[1]	SH5Y8 SK1P8 SK1P7	1303 1252 1304	84	1000	0	0				84000
M2S150	FCG1152[1]	SCCTJ	1406 1407 1408	81	4000	0	0	0	0	0	81000
M2S090	FCG676[1]	SCMSP SCTAY SCTCA	1409 1409 1414	62	1000	0	0				62000
M2S150	FCG1152[1]	SCCTJ	1406 1407 1408	225	1000	0	0				225000

Table 105 • **High Temperature Storage (HTS), 150 °C *(continued)***

					Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**500**	**1000**	**2000**	**3000**	**4000**	**Unit Hours**
M2S010	TQG144[1]	SGQJF	1439 1441 1441	225	1000	0	0				225000
M2S090	FCS325	SCTAY	1421 1425 1426	225	1000	0	0				225000
M2S090	FCS325	SFAKR	1421 1422 1423	225	1000	0	0				225000
M2S150	FCSG536[1]	SHNNJ	1510 1511 1512	225	1000	0	0				225000
M2S090	FG676[1]	SHTGO	1505 1506 1507	225	1000	0	0				225000
M2S090	FGG676[1]	SCMSP	1407	25	1000	0	0				25000
M2S050	VFG400[1]	SN9Y144	1325	25	1000	0	0				25000
M2S050	FGG896[1]	SK1P8 SG3N704 SH5Y8	1301 1303 1304	225	1000	0	0				225000
Total Units for 65 nm FPGA = 1850									**Total Test Cycles =**		**2087000**
Total Failures for 65 nm FPGA = 0											

1. G indicates lead-free.

Table 106 • **Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**500**	**550**	**Cycles**
M2S050	FBGAG896[1,2]	SA1A8 SK1P8 SK1P9	1246 1301 1301	360	550	0	0	0	0	198000
M2S050	FBGAG896[1,3]	SQ4L9	1318	94	550	0	0	0	0	51700
M2S150	FCG1152[1,4]	SAYLT	1402	319	550	0	0	0	0	175450
M2S010	WL[5]	SLASS	NA	106	500	0	0	0		53000
Total Units for 65 nm FPGA = 879								**Total Test Cycles =**		**478150**
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.
2. NVCE performed at 25 °C (225 units) andand 75 °C (135 units).
3. NVCE performed at 25 °C (47 units) and 75 °C (47 units).
4. NVCE performed at 25 °C (239 units) and 78 °C (80 units).

5. Wafer Level.

Table 107 • **Endurance/Non-Volatile Memory Cycling Endurance (NVCE): eNVM**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**1000**	**3000**	**5000**	**10000**	**Cycles**
M2S050	FBGAG896[1,2]	SA1A8 SK1P8 SK1P9	1246 1301 1301	360	10000	0	0	0	0	3600000
M2S150	FBGAG896[1,3]	SQ4L9	1318	94	10000	0	0	0	0	940000
M2S010	WL[4]	SLASS	NA	45	10000	0	0	0	0	45000
Total Units for 65 nm FPGA =				**499**				**Total Test Cycles =**		**4990000**
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.
2. NVCE performed at 25 °C (225 units) and 75 °C (135 units).
3. NVCE performed at 25 °C (47 units) and 75 °C (47 units).
4. Wafer Level.

Table 108 • **High Temperature Data Retention (HTDR) for Non-Volatile Memory: After NVCE**

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**10**	**2000**	**3000**	**Unit Hours**
M2S050	FBGAG896[1,2]	SA1A8 SK1P8 SK1P9	1246 1301 1301	135	10	125	0			1350
M2S050	CQFP208[3,4]	SK1P9 SK1P8 SK1P7	1308	132	3000	250	0	0	0	396000
M2S050	FBGAG896[1,2]	SQ4L9	1318	47	10	125	0			470
M2S150	FCG1152[1,5]	SAYLT	1402	80	10	125	0			800
M2S150	CQFP208[6,4]	SAYLT	1411	80	3000	250	0	0	0	240000
Total Units for 65 nm FPGA =				**474**					**Total Test Time Hours =**	**638620**
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.
2. NVCE: 10 K eNVM cycles; 550 NVM cycles performed at 75 °C.
3. NVCE: 10 K eNVM cycles; 550 NVM cycles performed at 25 °C.
4. Not commercially available (i.e., the engineering package is for reliability testing only).
5. NVCE: 550 NVM cycles performed at 78 °C (M2S050 eNVM NVCE data is applicable to M2S150, eNVM size is the same).
6. NVCE: 550 NVM cycles performed at 25 °C (M2S050 eNVM NVCE data is applicable to M2S150, eNVM size is the same).

Table 109 • **Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE**

					Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**168**	**1000**	**2000**	**3000**	**4000**	**Unit Hours**
M2S050	FBGAG896[1, 2]	SA1A8 SK1P8 SK1P9	1246 1301 1301	135	3000	0	0	0	0		405000

Table 109 • Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE

M2S050	FBGAG896[1,2]	SQ4L9	1318	47	1000	0	0				47000
M2S150	FCG1152[1,3]	SAYLT	1402	80	4000	0	0	0	0	0	320000
Total Units for 65 nm FPGA = 262								**Total Test Time Hours=**			**772000**
Total Failures for 65 nm FPGA = 0											

1. G indicates lead-free.
2. NVCE: 10 K eNVM cycles; 550 NVM cycles performed at 25 °C.
3. NVCE: 550 NVM cycles performed at 25 °C (M2S050 eNVM NVCE data is applicable to M2S150, eNVM size is the same).

Table 110 • High Temperature Storage Life (HTSL), 150 °C: After NVCE

					Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**500**	**1000**	**2000**	**3000**	**Unit Hours**
M2S050	FBGAG896[1,2]	SA1A8 SK1P8 SK1P9	1246 1301 1301	135	3000	0	0	0	0	405000
M2S150	FCG1152[1,3]	SAYLT	1402	79	3000	0	0	0	0	237000
Total Units for 65 nm FPGA = 214								**Total Test Cycles =**		**642000**
Total Failures for 65 nm FPGA = 0										

1. G indicates lead-free.
2. NVCE: 10K eNVM cycles; 550 NVM cycles performed at 25 °C.
3. NVCE: 550 NVM cycles performed at 25 °C (M2S050 eNVM NVCE data is applicable to M2S150, eNVM size is the same).

3.28 65 nm UMC Flash FPGA Reliability Summary

3.28.1 RTG4 Product Family

Table 111 • High Temperature Operating Life (HTOL)

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**48**	**168**	**500**	**1000**	**2000**	**4000**	**Unit Hours**
RT4G150	CG1657	KRMLM	1625	24	1000	125	1000		0	0	0		0	24000
RT4G150	CG1657	KPAQS	1606	18	4000	125	4000		0	0	0	0	0	72000
RT4G150	CG1657	KRAFJ	1615	18	4000	125	4000		0	0	0	0	0	72000
RT4G150	CG1657	KRAQF	1616	18	4000	125	4000		0	0	0	0	0	72000
RT4G150	CG1657	KRAQF	1616	22	1000	125	1000	0	0	0	0			22000
RT4G150	CG1657	KRMLM	1625	24	1312	125	1312	0	0	0	0			31488
RT4G150	CG1657	KRKTL	1634	24	1000	125	1000	0	0	0	0			24000
RT4G150	CG1657	KWKSY	1640	48	4087	125	4087	0	0	0	0	0	0	196176
RT4G150	CG1657	KWJSL	1705	24	2000	125	2000	0	0	0	0	0		48000
RT4G150	CG1657	K418A	1739	24	2000	125	2000	0	0	0	0			24000
RT4G150	CG1657	K5363	1803	24	2000	125	2000	0	0	0	0	0		48000

Table 111 • **High Temperature Operating Life (HTOL) *(continued)***

					Test Hours/Failures								
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time at T_J 125°C**	**48**	**168**	**500**	**1000**	**2000**	**4000**	**Unit Hours**
RT4G150	CG1657	K6275	1905	24	1000	125	1000	0	0	0	0			24000
Total Units for 65 nm FPGA = 316													**Total Test Time Hours =**	**681664**
Total Failures for 65 nm FPGA = 0														

Table 112 • **Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM**

					Number of Cycles/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Cycles**	**50**	**100**	**200**	**220**	**Cycles**
RT4G150	LG1657	KNLGG	1550	57	470[1]	0	0	0	0	26790
		KNPNP	1604							
		KRAFJ	1615							
		KRAQF	1616							
RT4G140	LG1657	KTPGH	1630	50	220	0	0	0	0	11000
Total Units for 65 nm FPGA = 107									**Total Test Cycles =**	**37790**
Total Failures for 65 nm FPGA = 0										

1. NVCE performed at 80 °C. Total cycles exceed maximum customer cycles (i.e. 200 cycles) with guard band.

Table 113 • **High Temperature Data Retention (PCHTDR+HTR) for Non-Volatile Memory: After NVCE**

						Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**NVM Cycles**	**Test Time**	**T_J (°C)**	**168**	**500**	**1000**	**2000**	**Hours**
RT4G150[1]	LG1657	KNLGG	1550	27	470[1]	1000	150	0	0	0		27000
		KRAFJ	1615									
		KRAQF	1616									
RT4G150	LG1657	KTPGH	1630	25	220	2000	150	0	0	0	0	50000
RT4G150[2]	Wafer[3]	KRSLW	NA	27	530[2]	1000	250	0	0	0		27000
	Wafer[3]	KRMLM	NA									
	LG1272[4]	KRKTL	1623									
RT4G150	Wafer[3]	KWKSY KTPGH	1630	22	530	1000	250	0	0	0		22000
Total Units for 65 nm FPGA = 104										**Total Test Time Hours =**		**129000**
Total Failures for 65 nm FPGA = 0												

1. NVCE: 470 NVM cycles performed at T_J 80 °C. Total cycles exceed maximum customer cycles (i.e. 200 cycles) with guard band.
2. NVCE: 530 NVM cycles performed at T_J 80 °C. Total cycles exceed maximum customer cycles (i.e. 200 cycles) with guard band.
3. Wafer level testing.
4. LG1272 is not a commercially available package for RTG4.

Table 114 • **Low Temperature Retention and Read Disturb (LTDR) for Non-Volatile Memory: After NVCE**

							Test Hours/Failures					
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**168**	**1000**	**2000**	**3000**	**4000**	**Unit Hours**
RT4G150[1]	LG1657	KNLGG	1550	27	1000	25	0	0				27000
		KRAFJ	1615									
		KRAQF	1616									
RT4G150[1]	LG1657	KTPGH	1630	25	2000	25	0	0	0			50000
Total Units for 65 nm FPGA = 52											**Total Test Time Hours =**	**77000**
Total Failures for 65 nm FPGA = 0												

1. NVCE: 470 NVM cycles performed at T_J 80 °C. Total cycles exceed maximum customer cycles (i.e. 200 cycles) with guard band.

3.29 28 nm UMC Flash FPGA Reliability Summary (PolarFire)

Table 115 • **High Temperature Operating Life (HTOL)**

								Test Hours/Failures						
Product	**Package**	**Wafer Lot**	**Date Code**	**Number of Units**	**Test Time**	**T_J (°C)**	**Test Time T_J (125 °C)**	**48**	**168**	**500**	**1000**	**2000**	**4000**	**Unit Hours**
MPF300XT	FCG1152	K21T3	1748	87	4000	135	6596.8	0	0	0	0	0	0	573921.6
		K208H	1750	71	4000	135	6596.8	0	0	0	0	0	0	468372.8
		K0878	1751	80	4000	135	6596.8	0	0	0	0	0	0	527744
MPF300XT	FCG1152	K07G8	1746	16	2000	140	4197.2	0	0	0	0	0		67155.2
MPF300XT	FCG1152	K34KK	1809	16	2000	135	3298.4	0	0	0	0	0		52774.4
MPF300T	FCG1152	K5949	1817	133	1000	135	1649.2	0	1[1]	1[1]	1[1]			214396
MPF500T	FCG1152	K7978	1841	140	2000	135	1649.2	0	1[1,2]	0	0	0		458477.6
MPF300T	FCG1152	K691M65	1849	80	1000	135	1649.2	0	0	0	0			131936
MPF500T	FCG1152	K808N	1851	117	1000	135	1649.2		0	0	0			192956.4
MPF500T	FCG1152	K808N	1851	110	1000	135	1649.2		0	0	0			181412
MPF500T	FCG1152	K7978	1849	45	120	135	197.9	0						8905.5
MPF500T	FCG1152	K7978	1849	66	120	135	197.9	0						13061.4
MPF500T	FCG1152	K7978	1849	66	120	135	197.9	0						13061.4
Total Units for 28 nm FPGA = 1027													**Total Test Time Hours =**	**2904174.3**
Total Failures for 28 nm FPGA = 4														

1. Root cause is attributed to random metal particles and metal bridging. Improvement plans are in place.
2. Unit failed at 120 hrs read point.

Table 116 • Low Temperature Operating Life

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	T_J (°C)	Test Hours/Failures 168	500	1000	Unit Hours
MPF300XT	FCG1152	K0878	1751	34	1000	-50	0	0	0	34000
Total Units for 28 nm FPGA = 34									**Total Test Time Hours = 34000**	
Total Failures for 28 nm FPGA = 0										

Table 117 • Temperature Cycle (TC), −55 °C to +125 °C

Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	Test Cycles/Failures 200	500	700	1000	Cycles
MPF300XT		K18JF22	1747							
		K21T3	1748	78	700	0	0	0		54600
		K21T3	1750							
MPF300T	FCSG536	K37KK	1831							
			1832	75	700	0	0	0		52500
MPF300T	FCSG536	K594901	1835							
			1836	75	700	0	0	0		52500
			1837							
MPF500T	FCG1152	K71SR	1825							
			1827	78	700	0	0	0		54600
			1831							
Total Units for 28 nm FPGA = 306								**Total Test Cycles = 214200**		
Total Failures for 28 nm FPGA = 0										

Table 118 • Biased Humidity Accelerated Stress Test (HAST), 110 °C/85% RH

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 50	100	200	264	528	Unit Hours
MPF300XT	FCG1152	K18JF22	1747								
		K21T3	1748	78	264	0	0	0	0		20592
		K21T3	1750								
MPF300T	FCSG536[1]	K37KK	1831								
			1832	75	264	0	0	0	0		19800
			1833								
MPF300T	FCSG536[1]	K594901	1835								
			1836	75	264	0	0	0	0		19800
			1837								

Table 118 • Biased Humidity Accelerated Stress Test (HAST), 110 °C/85% RH *(continued)*

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 50	100	200	264	528	Unit Hours
MPF500T	FCG1152	K71SR	1825								
			1827	78	264	0	0	0	0		20592
			1831								
Total Units for 28 nm FPGA = 306									**Total Test Cycles =**		**80784**
Total Failures for 28 nm FPGA = 0											

1. Unbiased HAST (U-HAST).

Table 119 • High Temperature Storage (HTS), 150 °C

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 500	1000	2000	3000	4000	Unit Hours
MPF300XT	FCG1152	K18JF22	1747	78	1000	0	0				78000
		K21T3	1748								
		K21T3	1750								
MPF300T	FCSG536	K37KK	1831	75	1000	0	0				75000
			1832								
			1833								
MPF300T	FCSG536	K594901	1835	75	1000	0	0				75000
			1836								
			1837								
MPF500T	FCG1152	K71SR	1825	75	1000	0	0				78000
			1827								
			1831								
Total Units for 28 nm FPGA = 306										**Total Test Hours = 306000**	
Total Failures for 28 nm FPGA = 0											

Table 120 • Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA NVM

Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	Test Cycles/Failures 200	500	700	1000	Cycles
MPF300XT[1]	FCG1152	K18JF22	1747	80						
		K21T3	1750	80	500	0	0			120000
		K326T	1750	80						
MPF500T[1]	FCG1152	K71SR	Mixed	84	500	0	0			42000
MPF300T[1]	FCG1152	K691M65	1849	77	500	0	0			38500
Total Units for 28 nm FPGA = 401									**Total Test Cycles = 200500**	
Total Failures for 28 nm FPGA = 0										

1. NVCE performed at Tj > 85 °C

Table 121 • Endurance/Non-Volatile Memory Cycling Endurance (NVCE): FPGA sNVM

Product	Package	Wafer Lot	Date Code	Number of Units	Test Cycles	Test Cycles/Failures 1000	3000	5000	10000	Cycles
MPF300XT	FCG1152	K18JF22	1747	80						
		K21T3	1750	80	10000	0	0	0	0	2400000
		K326T	1750	80						
Total Units for 28 nm FPGA = 240									**Total Test Cycles =**	**2400000**
Total Failures for 28 nm FPGA = 0										

Table 122 • Memory Post Cycling High Temperature Data Retention (PCHTDR)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 500	1000	2000	3000	4000	Unit Hours
MPF300XT[1]	FCG1152	K18JF22	1747	41							
		K21T3	1750	41	1000	0	0				123000
		K326T	1750	41							
MPF500T[1]	FCG1152	K71SR	Mixed	42	1000	0	0				42000
MPF300T[1]	FCG1152	K691M65	1849	39	1000	0	0				39000
Total Units for 28 nm FPGA = 204										**Total Test Cycles =**	**204000**
Total Failures for 28 nm FPGA = 0											

1. Cycles as per NVCE at Tj >125 °C, Target Tj=150 °C.

Table 123 • Nonvolatile Memory Low-Temperature Retention and Read Disturb (LTDR)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 500	1000	2000	3000	4000	Unit Hours
MPF300XT[1]	FCG1152	K18JF22	1747	39							
		K21T3	1750	39	1000	0	0				117000
		K326T	1750	39							
MPF500T[1]	FCG1152	K71SR	Mixed	42	1000	0	0				42000
MPF300T[1]	FCG1152	K691M65	1849	38	1000	0	0				38000
Total Units for 28 nm FPGA = 197										**Total Test Cycles =**	**197000**
Total Failures for 28 nm FPGA = 0											

1. Cycles as per NVCE at Ta= 25 °C

Table 124 • High Temperature Operating Life (HTOL) on 1.0 µm Products

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 48	168	500	1000	2000	4000	Unit Hours
Mixed	Mixed	Mixed	Mixed	Mixed					0			1428000
LX7710MDWC-Q	CS20	E26846	1826	48	1000	125	1000	0	0			48000

Table 124 • **High Temperature Operating Life (HTOL) on 1.0 µm Products *(continued)***

Product	Package	Wafer Lot	Date Code	Number of Units	Test Time	Test Hours/Failures 48	168	500	1000	2000	4000	Unit Hours
LX7710MDWC-V	CS20	E26905	1826	48	1000	125	1000	0	0			48000
Total Units for 1.0 µm MSA =				**709**							**Total Test Time Hours =**	**1524000**
Total Failures for 1.0 µm MSA = 0												

3.30 Package Reliability—MSA Products

Table 125 • **Unbiased Highly Accelerated Stress Test (UHAST)**

Product	Package	Conditions	Hours	Units	Failures	Device Cycles
AA6XX	16-pin QSOP (RoHS)	130C/85RH	96	46	0	4416
			Total Units =	**46**	**Total Test Cycles =**	**4416**
			Total Failures = 0			

Table 126 • **Thermal Shock (TS)**

Product	Package	Conditions	Cycles	Units	Failures	Device Cycles
LX77XX	132 CQFP	55 °C to +125 °C	15	30	0	450
AAHS298	20-pin ceramic SOIC	55 °C to +125 °C	15	30	0	450
LX77XX	164 CQFP	55 °C to +125 °C	20	12	0	240
			Total Units =	**72**	**Total Test Cycles =**	**1140**
			Total Failures = 0			

Table 127 • **Temperature Cycles (TC)**

Product	Package	Conditions	Cycles	Units	Failures	Device Cycles
AA6XX	16 pin QSOP (RoHS)	JESD22-A104-B Condition C	500	45	0	22500
AAHS298	20-pin ceramic SOIC	Method 1010, condition C	100	45	0	4500
LX77XX	132 CQFP	-65 °C to +150 °C	100	30	0	3000
AA6XX	172 Ceramic CQFP	Method 1010, condition C	100	30	0	3000
			Total Units =	**150**	**Total Test Cycles =**	**33000**
			Total Failures = 0			

For more information, visit our website at www.microsemi.com.

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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