New Reprogrammable and Non-Volatile Radiation Tolerant FPGA: RTA3P

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Abstract—Heavy-ion and proton test results utilizing novel test methodologies of reprogrammable and non-volatile flash-based FPGAs are presented and discussed. The 5 programmable architectures in the A3P FPGA-family were tested: I/O structures, FPGA Core, PLL, FROM and SRAM. Furthermore, the circuitry used for the programming and the erase of the A3P product was exercised in proton beams. The data shows no major concern or disruption to all of the circuit features for fluences lower than 10^{11} of proton particles or TID higher than 15 Krad.[1] [2]

TABLE OF CONTENTS

1. INTRODUCTION

Reconfigurable Field Programmable Gate Arrays (FPGAs) present an attractive solution for high-level system integration in various aerospace and military applications. Flash-based FPGAs are non-volatile and provide remote in-system reprogramming to support future design iterations and field upgrades. The flash technology has the advantage of being a secure, low-power, single-chip solution. Unlike volatile memory-based FPGAs, it does not require additional non-volatile memory to load the device configuration data at system-power-up. This reduces cost, power, and initialization time and improves system reliability.

Furthermore, unlike volatile-memory-based FPGAs, the configuration floating gate (FG) switches of a non-volatile based FPGA cannot be upset, and therefore no change of functionality could result from radiation. Indeed, results obtained in extensive TID testing in X-Ray, to be published in future articles, showed that even at TID higher than the guaranteed TID limit of 20 Krad (around 70 Krad), the FG switches of the A3P FPGA core did not switch state, which means that the implemented test designs are still functional but at much lower frequencies. High current leakages were observed though at TID higher than 60 Krad.

For soft-error modes, the combinational logic is sensitive to Single Event Transients (SET) and the sequential logic is sensitive to both Single Event Upsets (SEU) and SET. The SEUs can be mitigated by Triple Module Redundancy (TMR), and SETs can be filtered at the inputs of the sequential elements [2-4]. Previous preliminary test results [1, 2] show that except its sensitivity to soft errors, it is relatively insensitive to other single event effects (SEE).

This paper presents a comprehensive characterization of SEE in a commercial Flash-based FPGA, the 0.13-µm ProASIC3 product family (A3P), by heavy-ion and proton beam irradiation. Previous work [5] shows some of this data in heavy ion beams. The current paper completes this SEE characterization with proton data and adds preliminary results showing the proton effects on the circuit's charge pumps used usually for the programming and the erase of the FPGA.

1

[1] 1-4244-1488-1/08/$25.00 ©2008 IEEE.
[2] IEEEAC paper #1317, Version 4, Updated October 26, 2007

The test will target mainly the SET and SEU characterization of the FPGA core. Other subsystems such as the I/O circuits, embedded memories and PLL (phase-locked loop) as well as the circuitry enabling the erase and the reprogramming of the FPGA will also be tested for SEE. Heavy-ion-beam tests were performed on several campaigns at two facilities, Lawrence Berkeley National Laboratories and Texas A&M University, while the proton experiments were performed at the cyclotron of the Crocker Nuclear Laboratory of the University of California in Davis (UC Davis). Heavy-ion (HI) beam experiments were performed with a wide HI cocktail (Neon, Argon, Cupper, Krypton and Xenon) at normal incidences and two additional tilt angles (30 and 45). No testing with rolling angles was performed or differentiation in the data between the data collected at normal incidence or tilt angles is provided in this paper. The test results are reported and discussed along with additional suggestions on mitigation methodologies suitable for the target device. The details of mitigation techniques can be found in a companion publication of NSREC 2007 [2]. Note that further detailed information about the TID limits and analytical data for the behavior of the charge pumps used for the programming and erase circuit under gamma rays will be presented separately in future publications.

2. Devices Under Test and Test Setup

The 0.13-µm ProASIC3 product family has up to 3 million system gates, 504 kbits of true dual-port SRAM, 616 single-ended I/O, and 300 differential I/O pairs. They also include 1 kbits of on-chip, programmable, nonvolatile Flash ROM (FROM) memory storage as well as up to 6 integrated phase locked loops (PLL). The FPGA core consists of a sea of logic tiles, called "VersaTiles", and routing structures. Each

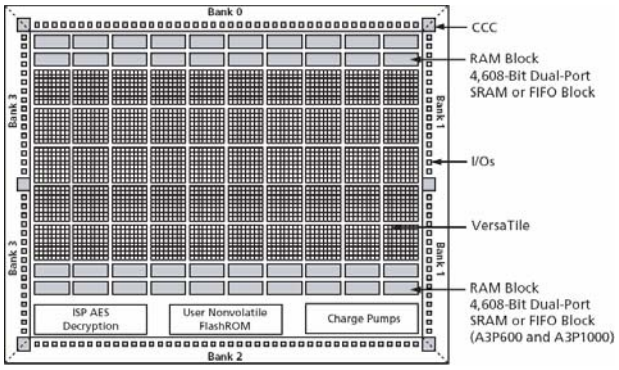

Figure 1 – ProASIC3 Flash FPGA Block Diagram Architecture

logic tile is a combination of CMOS logic and flash switches and can be configured as a three-input logic function or as a D-flip-flop with an optional enable, or as a latch by programming the appropriate flash switch interconnections. The logic tiles are connected with each other through routing structures and FG switches. These flash switches are distributed throughout the device to provide reconfigurable programming to connect signal lines to the appropriate logic-tile inputs and outputs [6].

DUT

For the beam test experiments, two devices from the ProASIC3 product family were selected: the A3P250 and the A3P1000. Each selected part is in a PQ208 package. Table 1 shows the features of the two selected parts. The test primarily targets the circuitry used for the DUT erase and programming depicted in the bottom of Fig. 1 as the block for "Charge Pumps" as well as the 5 configurable architectures in the A3P FPGA, as shown also in Fig. 1: 1) I/O structures, single-ended (SE) and low voltage differential signal (LVDS), 2) FPGA Core, 3) Clock Network and PLL, 4) FROM and 5) SRAM.

Table 1. Features of the Selected Parts

Part	A3P250	A3P1000
System Gates	250K	1M
D-Flip-Flops	6,144	24,576
RAM Kbits	36	144
Flash-ROM	1K	1K
Secure (AES) ISP	Yes	Yes
Integrated PLL	1	1
Global Signals	18	18
I/O Banks	4	4
Single-Ended I/O	151	154
Differential I/O Pairs	34	35

Experimental Test Setup

A new test setup was built for the A3P radiation testing. As shown in Fig. 2, it includes two boards: 1) a "master" board for the monitoring and control of the DUT operation in-beam and 2) a "slave" board for the communication between the host PC and the master board through two USB ports. The "master" board includes an A3P1000-FG484, called "master" FPGA, and a DUT (A3P-PQ208). IO "channels" of an input (SE or LVDS) routed immediately to a nearby output are also added between the "master" FPGA and the DUT.

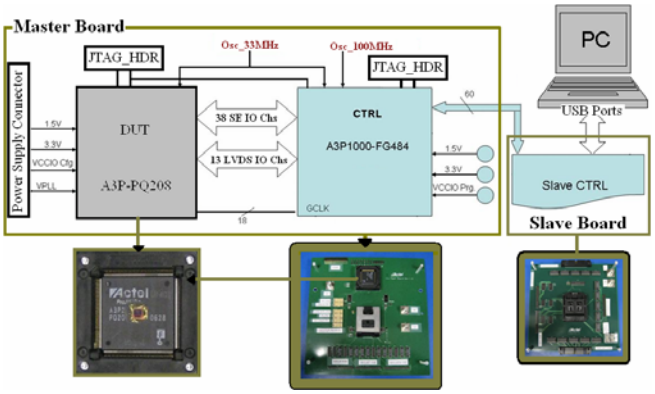

Figure 2 – Block diagram of the A3P Test Setup

There are 38 SE and 13 LVDS I/O channels on both FPGAs. This board architecture allows the implementation

of several separate designs on the same DUT to be tested simultaneously. The slave board includes an A3P1000-PQ208; it allows the data acquisition and data transfer to the host PC.

Software User Interface

For communication with the host PC, a new generic user interface was designed to communicate with the slave board. The communication protocol between the slave board and the host PC remains always the same for easy and fast implementation of any new SEE test experiment. Indeed, there are always a maximum of 64 display counters available to the designer, which names are adjustable according to the running experiments. These counters are usually used for display of number of SEE events among other indicators of the operation of the DUT design. In addition, this user interface allows the self-monitoring of the test system itself, by testing each board and FPGA individually as shown in the "Mode" knob on the top left of Figure 3. Among other features, it also allows the pattern selection to be accomplished by the "pattern" knob (all zeroes, all ones, checkerboard or inversion of checkerboard) exercised on the DUT inputs and the frequency at which the DUT design is running by using the "Frequency" knob.

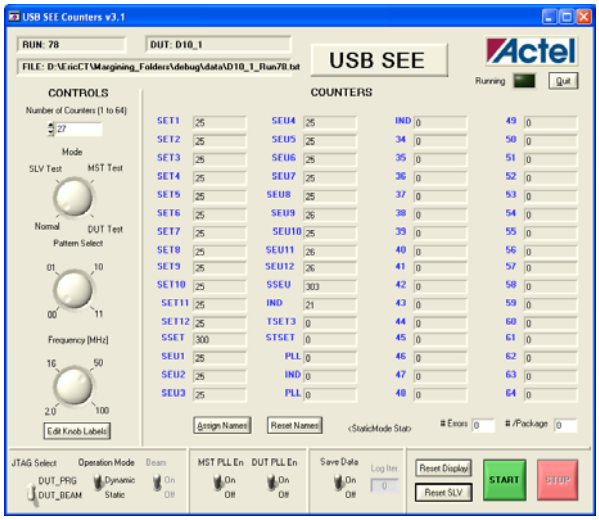

Figure 3 – SEE Software User Interface

3. Test Designs and Experimental Results

FPGA Core SEE Characterization (Flip-Flops)

The purpose of this testing is to determine the SEE cross-section of an A3P logic tile configured as a DFF. This should lead to the highest possible upset cross-section of a logic tile. The basic test design is a shift register (SR) using 86 logic tiles with each one of them configured as a DFF and one global clock signal but no reset signal. Note that if the SR design was using a reset line, this signal would be a global and using a global IO pad in the same way as any other global clock signal, whose cross-section will be given below.

On the other hand, since this is a 0.13-µm technology, the part might be sensitive to Multiple Bit Upset (MBU) [7], which in some cases cannot be mitigated effectively by TMR. For instance, if the MBU affects two TMR paths out of three, the output TMR result will be wrong. Therefore using TMR as a test methodology constitutes a good approach to detect some of the MBU or SEE on the FPGA's global signals. Note that the design should be using at least 99% of the FPGA resources and the three paths of a TMR circuit should be as close as possible to simulate the worst case of a TMR implementation. Hence in addition to the version (D1) having SR without mitigation, two versions of the TMR'd design have been implemented on the same DUT: 1) D2: TMR'd SR using one single global clock, where voters and IOs are also tripled and 2) D3: TMR'd SR where every I/O signal is tripled, including the global clock signal. All 3 DFF of a TMR'd DFF are always placed directly next to each other.

Test Design

Among the 37 SE channels, the non-mitigated test design D1 uses 28 SE channels of the DUT. Between each input/output of these 28 channels, a shift register (86 DFF) is inserted. In total, the D1 design uses 28 Input/Output and 2408 (86×28) DFF. D2 uses three copies of a TMR'd SR with no triplication of the clock signal, i.e. nine SE channels and one global clock, while D3 uses 4 copies of the TMR'd SR, i.e. 12 LVDS IO channels and 3 global clocks. D1 and D2 use 2 SE IO banks and D3 uses two LVDS IO Banks. The three versions of the design occupied 98% of the A3P250-PQ208. A detailed block diagram of these 3 design implementations, D1, D2 and D3, is given in Fig. 4. The testing was performed at the clock frequency of 2, 16 and 50 MHz.

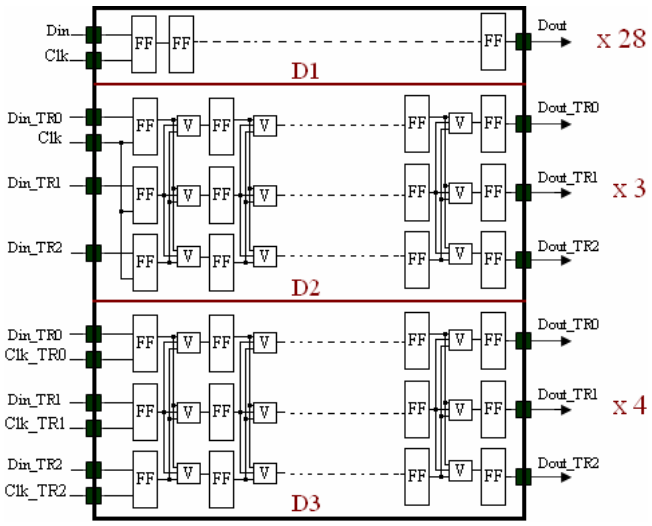

Figure 4 – Block Diagram of D1, D2 and D3 Test Designs

It should be mentioned that implementing the same design D1, D2 or D3 on several channels will help check the repeatability and the consistency of the tests for its non-dependency of different tested channels. Moreover, it allows checking for SEE on common global signals other than the user global clock and reset signals. For example, an SEE in global signals that link an IO bank can cause a simultaneous soft error in every channel using the same IO bank [2]. Indeed, a transient event was observed on all the channels belonging to a single IO bank with a cross-section of 2.37×10^{-6} cm^2 per IO-bank. The threshold LET of this event is around 7 MeV•mg/cm^2. This suggests that if a design is using all the tripled IOs in the same bank, its cross-section will be no less than 2.37×10^{-6} cm^2 per IO-bank.

Heavy Ion Beam Test Results

For the Design D1, the obtained results show three types of errors: 1) single error on one channel, 2) multiple errors on one single or few channels, and 3) single or multiple errors on all the IO channels associated to a common IO bank. All errors were transient and did not require any reconfiguration or power cycle of the FPGA. Type 1 is most likely due to an SEU in the DFF or to an SET in the clock signal associated to this DFF. Type 2 could be due to the clock signal or to another global signal besides the IOs since we didn't see all the IO channels disrupted at the same time. Type 3 is most likely due to the aforementioned event for the IO testing and observed in a single IO bank.

Fig. 5 shows the single DFF cross-sections at three different frequencies obtained from D1-test data. Note that for better visibility, WEIBULL curves in Fig. 5 (also in Fig. 6 and 7) have been drawn only for the 50MHz data. There is no dependency of cross sections on the frequency; this is expected for soft errors in the flip-flops when the static SEU rate dominates.

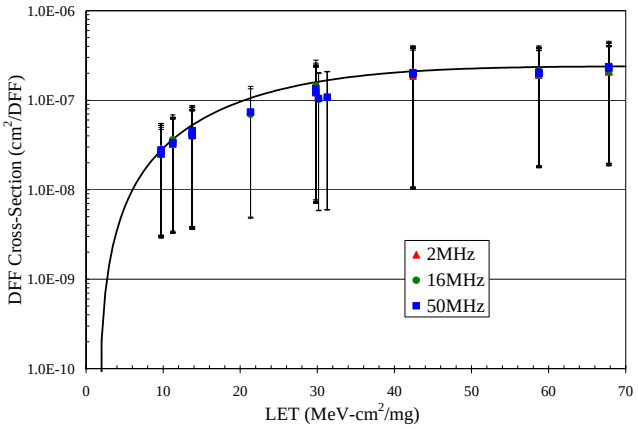

Figure 5 – A3P250-PQ208 DFF Cross-Section

Although not visible in Fig. 5, these data include global error cross-sections due to the IO bank or clock global signals; this subject will be discussed in detail in the following section. The global-error cross-sections are dependant on the clock frequency because they are due to the SET in the IO bank or clock global signals. It is well known that SET induced errors have a strong dependence on the clock frequency [8].

For the design D2, only errors type 2 and 3 have been observed, while for D3 only errors type 3 have been observed, which means that each SEE observed on the TMR'd design (D3) always affected an entire IO bank. To compare the SEE response of the three test designs and to validate the efficacy of the increase of mitigation level, TMR of the DFF and the triplication of the global clock signal, the SEE cross-sections were averaged on three channels for each design, since D2 was using only three channels. These cross-sections are given in Fig. 6. It is clear that increasing the frequency increases the D2 and D3 SEE cross-sections.

Fig. 6 shows a clear reduction in the SEE cross-sections from D1 to D2 and finally to D3 with the increase of the level of mitigation. In addition, the results show also that each observed error on the design D3, where all the resources have been TMR'd, always originates from an SET which affects an entire IO bank. The cross-section of the TMR'd design (4×10^{-6} cm^2 per design) in D3 is very close to twice the IO-bank-SET cross-section deduced from SET errors in designs D1 and D2. This is expected because D3 uses bank 1 and 3 for differential IOs while D1 or D2 only uses bank 2 for single-ended IOs. The IO-bank-SET is suspected to be due to SET occurring on the enable signal of a single IO bank. To accomplish complete SEE immunity, all the tripled IOs have to be separated on three different IO banks; this had been demonstrated already [2].

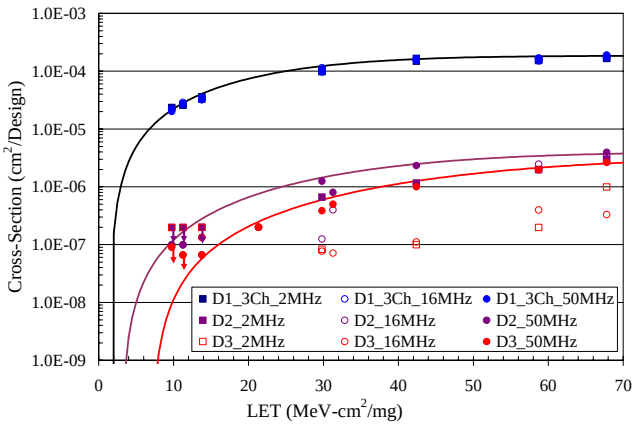

Figure 6 – D1, D2 and D3 SEE Cross-Sections at 2, 16 and 50 MHz

Furthermore, if we increase the number of usage of the FPGA core of D2 and D3, the SEE cross-sections should not increase because these cross-sections are dominated by SET on the global signals, i.e. Clock or IO bank enable signals. These cross-sections depend on the number of used

global clock signals (18 maximum), the used IO banks (4 maximum for the A3P and 8 for the A3PE) or the operation frequency. On the other hands, if the usage of resources of D1 should increase, its cross-section should increase linearly. Fig. 6 clearly indicates the increases of cross sections of D2 and D3 with frequency. Note that for design D1, the events where all the disrupted IO channels are not counted for this comparison. Fig. 7 shows the clock global cross-section; it is acquired simply by measuring the difference between designs D2 and D3.

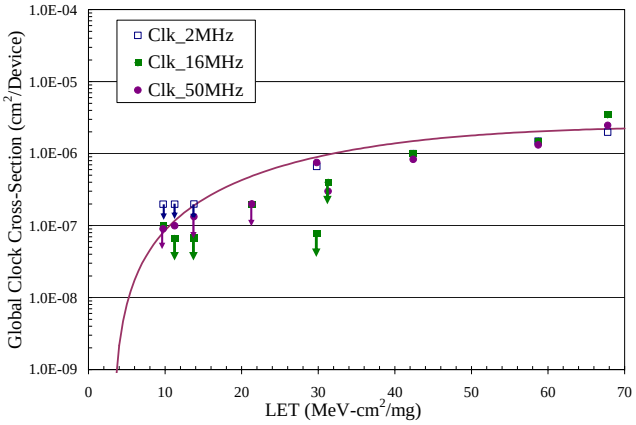

Figure 7 – A3P250-PQ208 Global Clock Cross-Section

Proton Beam Test Results

Beam test experiments showed very little SEE sensitivity at a proton energy of 63.5 MEV and when running the design at 50 MHz. Indeed, the DFF SEU cross-section was measured at 5.18×10^{-14} cm^2/DFF. Note also that at this energy and for a fluence of 6.49×10^{12} of proton particles, no SET in the configuration logic tiles, on the enable signal of the IO banks, on the IOs themselves or the global clock signal was observed. Because of such low SEU cross-section, the DFF design was not tested at lower energies, although it is advised to measure the threshold energy for the A3P DFF in future experiments.

PLL SEE Characterization

A PLL macro uses the CLKA input to drive its reference clock. It uses the GLA and optionally the GLB and GLC global outputs to drive the global networks (Fig. 8). A PLL macro can also drive the YB and YC regular core outputs, but if the GLB (or GLC) global output is used, the YB (or YC) output [6] cannot be reused. The purpose of this test design is the identification of all the PLL error modes due to beam irradiation.

Test Design

The test design uses a PLL whose output (GLA) clocks a triple DFF. Its input signal CLKA is using the 33MHz oscillator output and its GLA signal is running at 50 MHz. The three DFFs have three different inputs and three different outputs. The only common point between the three of them is the PLL output clock signal (DUTCLK). On the master FPGA, the three outputs of the DUT DFF are voted and their output is compared continuously with the DFF input provided from the master FPGA, which is clocked at 16 MHz. Any mismatch between the DFF voted value and the expected value (the input value), is counted as an error. The test design allows also the monitoring of the PLL LOCK signal. This signal should always be high indicating that the PLL is working properly; if it goes low then the PLL is unlocked and this will also be counted as an error. The purpose of this SEE characterization is the classification of the detected error types and the test of the efficiency of self-correction through the PLL POWERDOWN signals (Fig. 8) without having to power cycle the entire FPGA.

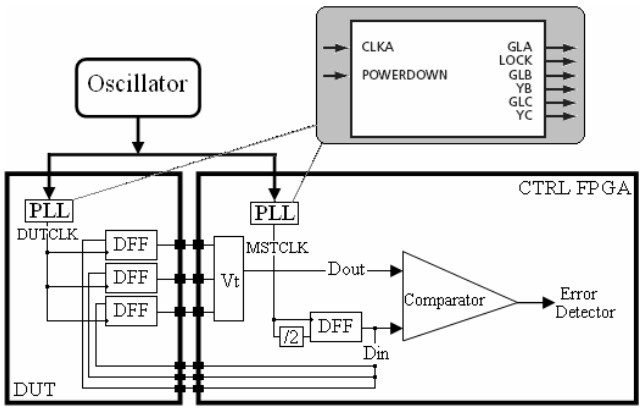

Figure 8 – Block Diagram of the PLL Test Design

The test design is implemented so six types of errors, called error-type 1 to error-type 6 summarized in Table 2, are expected. In the case of a mismatch between the Din and Dout signals of Fig. 8, the error would be counted as an error-type 1, which is similar to an SET event on the PLL clock signal if the error does not persist. However, if the error persists for longer than two clock cycles but less than 100 cycles, it will be counted instead as error-type 2. If the same error persists for longer than 100 clock cycles, it will be considered as error-type 3 and the master FPGA will then power cycle the PLL through the POWERDOWN signal and restart normal operation.

Table 2. PLL Error Modes in Beam

Error Type	Error Description
1	An SET has occurred on the DUTCLK signal.
2	A mismatch between Din and Dout that lasts less than 100 clock cycles.
3	A mismatch between Din and Dout that lasts longer than 100 clock cycles.
4	An SET has occurred on the LOCK signal.
5	The LOCK signal remains at '0' for less than 100 cycles and the PLL recovers by itself.
6	The LOCK signal remains at '0' for more than 100 cycles and the PLL can not recover by itself.

Simultaneously, the master FPGA is continuously checking for the status of the PLL LOCK signal. If this signal goes low, the master FPGA counts it as an SET on the LOCK signal (error type 4) and waits for 2 clock cycles. If the LOCK signal remains at '0' logic for less than 100 clock cycles and the PLL recovers by itself then the error is counted as a PLL lock case and considered instead an error-type 5. In the case where an error-type 5 would last longer than 100 cycles, it will be considered as an error-type 6 and the master FPGA would then power cycle the DUT PLL through the POWERDOWN signal. The block diagram of this test design is given in Fig. 8. Note that the actually implemented test design runs the DUT design at 50 MHz while the error checking on the master side is at 16 MHz.

Heavy-Ion Beam Test Results

The MSTCLK was exercised at two frequencies (2 and 16 MHz). In both cases, among the six expected types of errors, only two have been observed: errors from type 2 and 6. The latter was always combined with a difference between the Din and Dout signals lasting for more than 100 clock cycles. Only toggling the PLL POWERDOWN signal could restart the operation of the PLL in that case. As shown in Fig. 9, the test results show little variation between the cross-sections of error-type 6 obtained at both test frequencies (2 and 16 MHz). Error type 2 has been observed only at 16 MHz (frequency of the master FPGA). The LET_{th} for this type of errors is shown in Fig. 9 to be around 32 MeV-cm^2/mg. This value might seem high if the SET on the clock signal generated from the PLL occurred on the FG switches that links this signal to the tripled DFF. However, it might be expected if it is related to the internal PLL circuit. Only collecting more data could clarify this point. The saturation cross-section of the PLL in LOCK mode is 10^{-5} cm^2.

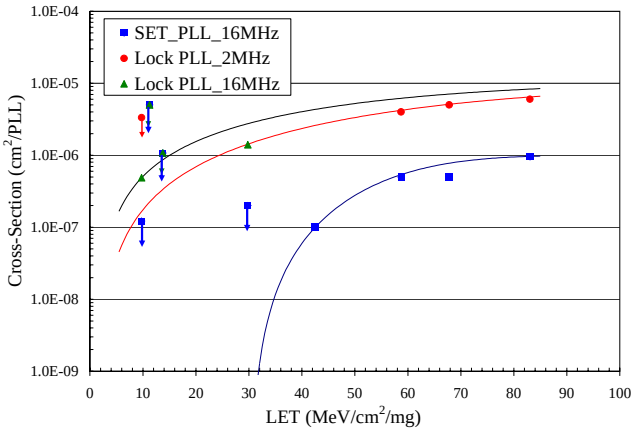

Figure 9 – A3P250-PQ208 PLL SEE Cross-Section

Proton Beam Test Results

No SEE was observed on the PLL during beam irradiation tests for a fluence of $9x10^{10}$ of proton particles having energy of 63.5 MEV, which was expected considering the low sensitivity of the FPGA core itself.

Flash ROM (FROM Memory) SEE Characterization

Test Design

ProASIC3 devices have 1 kbits of on-chip nonvolatile Flash memory that can be read from the FPGA core fabric. The Flash ROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the Flash ROM from the FPGA core. The flash ROM will be configured initially with a pattern that reflects the byte address and the master FPGA will be simply checking its content. The frequency of the FROM read was varied between 2 and 16 MHz to check the speed effects and quantify the number of SETs that had occurred during the beam testing. The FROM was read during and after irradiation. In beam, each FROM address was read 3 times successively to avoid counting SEE on the peripheral gates (7 DFF automatically connected to FROM address bus, 8 DFF connected at the data outputs, routing switches and active regions of the IO pads).

HI Beam Test Results

Fig. 10, shows the test results; there is no observable SEE sensitivity for LET < 83 MeV•cm^2/mg. This demonstrates the SEE hardness of the embedded FROM and opens its possibilities for space applications; for example it can be used as a boot memory for the embedded processors in the A3P FPGA.

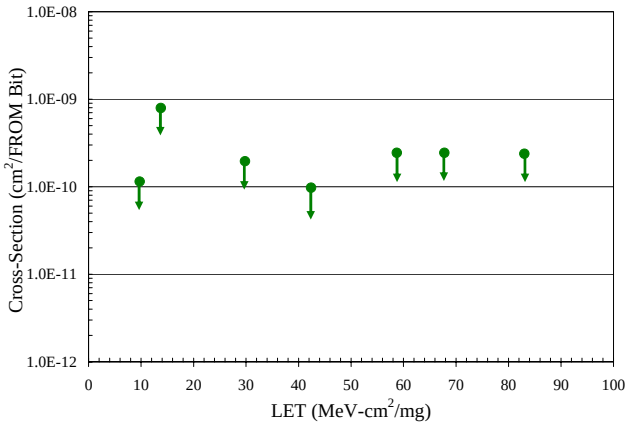

Figure 10 – FROM Bit SEU Cross-Section

Proton Beam Test Results

No SEE was observed on the FROM during beam irradiation tests for a fluence of $9x10^{10}$ of proton particles having an energy of 63.5 MEV. This was very much expected because of the already non-sensitivity to SEE in heavy-ion beams.

SRAM Memory SEE Characterization

The selected ProASIC3 devices (A3P250 and A3P1000) have embedded SRAM blocks along the north and south sides of the devices. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous

mode for both read and write operations. The read and write clocks are completely independent and each may operate at any desired frequency up to 350 MHz. To have better statistics, an A3P1000 was used as the DUT, which has 144 Kbits of SRAM bits, four times more than that in an A3P250.

Test Design

During beam-test experiments, the "master" FPGA initially writes a checkerboard pattern into the embedded SRAM and continuously checks its contents. When an upset is detected in the SRAM bits, the upset counter is incremented and the memory content is flipped back. Note that for ease of implementation, only one organization of SRAM was used: "RAM512x9". In the DUT design, all the logic used to interface with the SRAM, such as IOs, address decoder, read and write signals of the 32 SRAM blocks, are TMR'd and therefore mitigated to SEE. This means also that only SEE on the SRAM will be counted. This should avoid the overestimation of the SRAM SEE cross-section due to the SEE sensitivity of other programmable circuits used in the DUT test design. In this test, the maximum SRAM frequency is 16 MHz. The block diagram of the test design is given in Fig. 11.

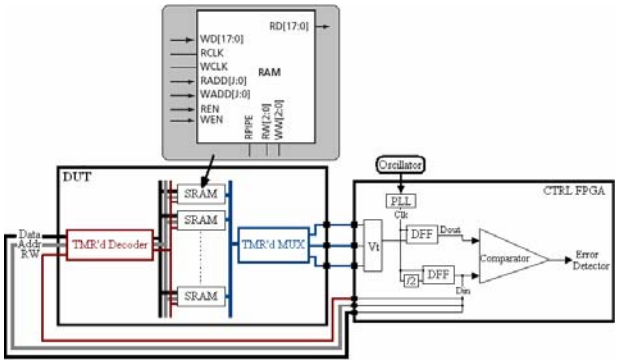

Figure 11 – Block Diagram of the SRAM Test Design

HI Beam Test Results

The test results show no SRAM SEE cross-section dependence on the frequency, indicating that most of the SET effects on the peripheral combinational logic are filtered out and only SEU on the SRAM blocks are counted. Also, no MBU were observed in the SRAM bits. Measured SEU cross-sections are given in Fig. 12. The saturation cross-section is approximately 4.22×10^{-8} cm^2/SRAM-bit.

The LET threshold is around 0.65 MeV-cm^2/mg, which considered very low. It should be mentioned also that additional testing should be done to find out about MBU in the SRAM blocks. Static tests should be used where the SRAM is read at the end of each run preferably irradiated at low fluxes to avoid hiding some of the bit-errors because of multiple hits. SEE mitigation solutions for the SRAM,

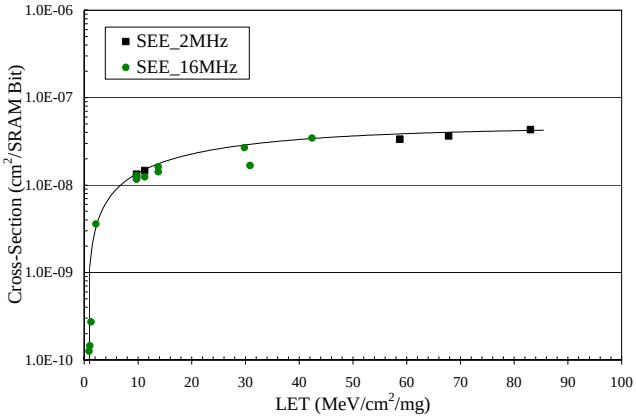

Figure 12 – HI SRAM Bit SEU Cross-Section

based mainly on EDAC approach such as the one employed for the SRAM of the RTAX FPGAs will be implemented and tested in the near future [9].

Proton Beam Test Results

In comparison with the other FPGA resources, the embedded SRAM blocks showed an SEU cross-section when running at 16 MHz in protons beams, for a cocktail of energies of 63.5, 30, 19.5 and 16.5 MEV. The obtained results are shown in Fig. 13. Additional tests shall be performed to establish the threshold proton energy to induce upsets in the SRAM bits.

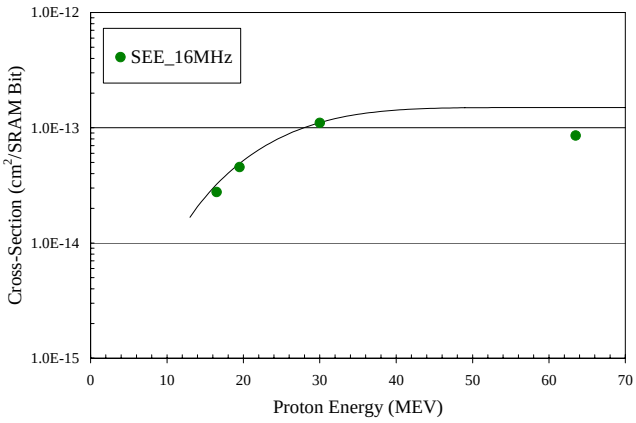

Figure 13 – Proton SRAM Bit SEU Cross-Section

4. PRELIMINARY STUDIES OF TID EFFECTS ON SEE SENSITIVITIES

Proton Characterization of the Programming and Erase Circuitry

One major advantage of the flash-based FPGAs compared to the previous generation of ACTEL FPGAs, based on the Antifuse technology, is the re-programmability feature. However, during erase and reprogramming of the part, high voltages are applied (±17.5 V) and one might think that there is a risk of permanent damage on the FG cells or other overhead circuitry if an ion hit during that mode. Therefore, radiation test experiments during the erase and the programming of this part are required to measure the SEE sensitivity of this specific part of the FPGA (charge pumps) and the overall consequences from an ion hit.

Ten A3P250-PQ208 circuits have been exercised in proton beams during the erase, reprogramming and verification of the programmed FG cells. The shift register design using 98% of the FPGA logic tiles (A3P250-PQ208) was used as a reference design. For each beam run, consecutive erase, reprogramming and verify cycles are launched and the functionality of the design is always checked at the end of each run. At least four full cycles of erase, program and verify cycle are executed during each beam run; each cycle requires 41 seconds. Each run exposes a new DUT to a dose of 13.4 Krad due to proton beam exposition and uses a fluence of 10^{11} of proton particles. Table 3 summarizes the obtained results.

Table 3.
Programming and Erase Error Modes in Proton Beams

Behavior Type	Error Description	Number of DUTs
1	All 4 programming and erase cycles have passed successfully	9
2	One erase/program cycle among 4 failed and the next one passed	1
3	Failure of the 5th cycle of erase / programming because of total exposure to TID (13.4 Krad) requiring annealing	2

Three types of behavior have been observed during the proton irradiation testing, as summarized in Table 3. Type 1 is showing the case where four erase, programming and verifying cycles have been performed without any failure including the design's operation. Type 2 shows the one case where only one verifying failure has been observed (second cycle), which could be due to the programming of false information in the FG cells (ON state instead of OFF state and vice versa). This type of errors was easily mitigated by running a second cycle of erase, reprogramming and verifying of the FG cells allowing the DUT to recover normal operation. This type of error has a cross-section of 10^{-12} cm^2/FPGA. Type 3 is the one where a fifth cycle was started and did fail because we reached a dose of 13.4 Krad, which is considered high for the normal operation of the charge pump circuit, according to TID tests in gamma rays at DMEA and shown in previous work [1] and considering the high dose rate exercised in this case (58 rad/s).

During all these runs, there was no permanent damage on the circuit and all errors that have been observed during these test cycles disappeared after annealing. Indeed, the two parts that have failed programming on the 5th time recovered functionality after annealing of the DUT at room temperatures for many days.

Although these preliminary results are encouraging and since the annealing effects on the floating gates are still under study, it is well-advised to avoid erasing and reprogramming the DUT in or off-beam after its exposure to a dose higher than 15 Krad. This statement is valid only if the applied dose rate from heavy ions, protons or gamma is around 50 rad/s as required by the JEDEC test standards and demonstrated in Ref. 1. In the case of the actual protons testing, the dose rate was around 58 rad/s, which might explain the observation of some failures on the 5th cycle of erase and programming at 13.4 Krad. Also the cross-section of writing wrong information (10^{-12} cm^2/FPGA) could be fundamentally due to the very little SEE sensitivity to protons of the A3P FPGA. Heavy ion data is hence required to confirm that no catastrophic failures could result from programming and erasing in beam since the FPGA's SEE sensitivities under HI irradiation are much higher relative to the proton sensitivity.

Testing Beyond the TID Limit

Most of the collected data for the measurements of the SEE cross-sections in this paper has been obtained for Total Ionizing Dose (TID) less than 25 Krad. Previous work [1] showed the TID performance of this device to be 15 Krad for the programming and erase circuitry and 25 Krad for the FPGA core itself (the FG cells). For the latter, the TID performance was mainly obtained when a degradation of 10% in the propagation delay of the logic tiles configured as a chain of buffers is attained, but no permanent damage on the FPGA was noted.

The purpose of this new specific test is to check the designs' functionality and their SEE performance for TID higher than 25 Krad as well as the maximum TID to which the design is still functional. The SRAM test design was selected for this study, since it uses various resources of the FPGA: 8.24 % of the FPGA logic tiles (configured as combinational or sequential logic), 100 % of the embedded SRAM memories, the embedded PLL and FROM and 44 % of the IOs. This design was also selected because of the SRAM high SEE sensitivity compared to the other FPGA resources, which could help monitoring the functionality and the SEE cross-sections if they do increase.

The DUT was exposed to beam for 5 consecutive runs where each of them has a fluence of $4x10^{10}$ of 16.5 MEV proton particles. This corresponds approximately to a TID of 15 Krad per run, and therefore to a total of 75 Krad for the five runs. During all these runs, the DUT design was functional and the error cross-section per run was consistent without any noticeable increase in the SEE sensitivities as shown in Table 4. It should also be noted that for all of the five runs, the detection of errors stops with the end of the beam time. This confirms that the FG cells are still functional upon a TID of 75 Krad. However, upon the start of the 6th run, the design stopped functioning. This could be due to a high charge loss in the FG cells. After four months of annealing in room temperature, the design did recover functionality but not the reprogramming capability. Time is needed to check if more annealing time will allow the recovering of the full operation of the charge pumps needed for the programming. These features are under study and will be described in future publications dedicated for the study of the TID limitation of the ProASIC3 parts.

Table 4. TID Effects from Proton Irradiation (Energy = 16.5 MEV) on the SEE Cross-Sections of an SRAM-Bit

Run	Accumulated TID [Krad]	SRAM Bit SEE Cross-Section [MeV-cm^2/mg]	Fluence [16.5 MEV Proton-Particles]
1	15	$2.48x\ 10^{-14}$	$4x10^{10}$
2	30	$2.29x\ 10^{-14}$	$4x10^{10}$
3	45	$2.51x\ 10^{-14}$	$4x10^{10}$
4	60	$2.80x\ 10^{-14}$	$4x10^{10}$
5	75	$2.71x\ 10^{-14}$	$4x10^{10}$
6	90	Design lost functionality right in the beginning of the run but recovered after annealing in room temperature	$4x10^{10}$

It should also be stated that an accurate estimation of the TID effects on the SEE cross-sections requires a better measurement of the accumulated dose. Indeed, until today, only gamma rays could provide an accurate measurement of the exposed dose and therefore it would be advised to expose the part to a certain dose in gamma rays and then measure the SEE cross-sections, within 2 hours or few days if transported in dry ice to avoid annealing effects. X-Ray and gamma testing are in process to locate the maximum TID to which a given design is still functional. These results shall be available in future publications.

In addition, it should be mentioned also that among the 60 parts, tested in all the HI experiments, 59 of them have recovered the DUT programming and erasing capabilities after many months of annealing in room temperature and did never lost functionalities in or off-beam. The TID for the 59 parts varied between 5 and 40 Krad. The only DUT that did not recover yet the programming capability was exposed to a TID of 41.5 Krad. Knowing that we could erase this part led us to assume that we might need more time to be able to reprogram it again. On the other side, all of the 24 parts that have been tested in protons could be erased but seven of them could not be reprogrammed. Time is needed to make sure that the seven remaining parts will recover this feature.

The main conclusion from these test experiments is that most of the tested parts did recover the programming and erase features after annealing in room temperature for many months. None of them lost functionality for dose that approximate 40 Krad even at the highest LET (83 MeV-cm^2/mg) or 63.5 MeV in protons. It is clear though that the recovering of the erase functionality is much quicker than the recovering of the programming capability.

This is certainly not a quantitative study but rather qualitative to make sure that there is no permanent damage from HI or protons on the part due to TID. Additional testing is hence mandatory to calculate accurately the annealing effects on the FG cells [10] and the circuitry used for the erase and the reprogramming of the FPGA.

5. CONCLUSION

A full SEE characterization at high-frequencies (up to 50 MHz) has been performed on the A3P flash-based FPGA family. The obtained results are presented and showed some SEE sensitivity in most of the programmable architectural features of the FPGA; the exception is the embedded FROM, which is very radiation hard. The previously observed transient event on each IO bank used for SE or LVDS IOs at high frequencies has been tested again with very different designs. If mitigation solutions of TMR and SET filtering are adopted for the logic and clock in A3P FPGA, the only remaining cross-section would be due to this type of event. On the other hand, if a complete SEE immunity is required at high frequencies (50 MHz and above), triplication of IOs is mandatory in addition to their separation on 3 different IO banks. Finally, as expected for a non-volatile FPGA, no observed error-event required a reconfiguration of the Flash-based FPGA nor were there any destructive SEE events even during the erase, the programming and the verifying of the FPGA.

The test methodologies and results presented in this paper will be the foundation of further research, both for the design of a radiation tolerant Flash-based FPGA and for providing mitigation solutions for use of the A3P product family in aerospace electronics. Once the RT-product derived from the commercial part (A3P) is released, orbital error rates will be calculated and published in future work.

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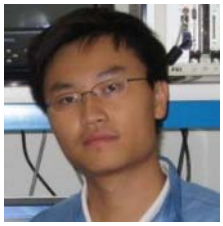
BIOGRAPHY

Sana Rezgui *received the B.E. (1996) from ENIT in Tunisia and the M.E. (1997) in electrical engineering from UPS in Toulouse, France and the Ph.D. (2001) in Microelectronics from INPG in France. She was a visiting researcher at JPL/NASA (2001) for transfer of technologies on I.C. testing and their error rate prediction in radiation environments. She was employed by NEE ANN Polytechnic of Singapore as a lecturer and consultant for IC testing (2002). She joined the Aerospace and Defense Group (2003) in Xilinx, Inc. and led the SEE test consortium for their FPGAs. Since 2006, she works as a principal engineer in the Technology and Development Group of Actel Corporation. She has published or co-published over 20 technical papers, in the field of radiation effects and hardening.*

J.J. Wang *received a Ph. D. degree in Material Science and Engineering from Case Western Reserve University in 1989. He worked as a Physicist at ARACOR, a research and development firm specializing in radiation applications, in Sunnyvale California for 6 years, doing material analysis and electrical characterization, acting as the principal investigator for various government funded projects, and writing proposals and winning several SBIR awards from DARPA, DOE and NSF. The research subjects include radiation effects on semiconductors, radiation detectors, and SOI electrical and material characterizations. Since 1995, he worked in Actel, had been involved in all the radiation related projects and products, including RH1020, RH1280, RH SX, RT1020, RT1280, RT1460, RT14100, RT54SX16, RT54SX32, RT54SX32S, RT54SX72S, RTAXS, and RTRIO. He managed the RH ONO process in BAE Manassas foundry, conducted TID and SEE testing, designed and developed, in collaboration with NASA Goddard sometimes, the enhancement methodologies for total dose and/or SEE tolerance in all RT products. Dr. Wang presented and published more than 30 times on the subject of radiation effects on semiconductor microelectronics in various conferences and journals.*



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Brian Cronquist *graduated cum laude (Chemistry Medal) in Chemistry from Santa Clara University in 1979. He worked at Synertek Corporation for 6 years developing ultra thin thermal oxide and precleaning technology, plasma etching and database scaling techniques and process simulation & integration. After a short 1 year stint at AMI developing and transferring logic and mixed signal processes, he joined the startup team of Sierra Semiconductor (now SierraPMC). He constructed and ran the diffusion/oxidation/LPCVD, ion implant and process integration areas of the Sierra wafer fab. In 1988 he helped start the Sierra partnered startup in Singapore, Chartered Semiconductor Manufacturing. He constructed, developed and managed the Diffusion/Oxidation/Cleans/APCVD & Integration process module engineering, maintenance and operations groups. He formed and directed the process/device development and program management customer engineering groups. He returned to the USA to Actel Corporation, where he currently is Sr. Director of Technology Development, managing new process/materials/device and radiation effects development and wafer foundry relationships for the anti-fuse and Flash products. He has published or co-published over 45 technical papers, many in the field of radiation effects and hardening.*

John McCollum *worked 2 years at Faichild R&D on bipolar switching performance, specifically platinum doped life time control and the development of Ion Implantation. He worked 15 years at Intel developing Intel's first bipolar PROM, Ion Implantation, the world's first 16K DRAM, as well as 64K and 256K DRAMs. Mr. McCollum developed Intel's first dual layer metal CMOS technology for the 386 microprocessor. He co-founded Actel and worked the last 20 years on process, antifuse and flash cell development, and FPGA Architecture at Actel. He holds over 50 patents, covering Process Technology, Antifuse and NVM technology, FPGA Architecture, Analog Processing and Radiation Hardening. He has presented numerous papers at IEDM, MAPLD, CSME, SPWG, and the FPGA Symposium. He is currently a Fellow in the Technology Development Department.*