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Synplify® Pro for Actel Edition Release Notes

Version D-2009.12A, January 2010

Release Note Topics

About this Release

This D-2009.12A release includes software improvements for the Synplify® Pro Actel Edition product. See *New Actel Feature Support* on page 2 and *New Features and Enhancements* on page 3 for the cumulation of features and enhancements included in the release.

New Actel Feature Support

This section contains a summary of the new Actel-specific features and enhancements for version D-2009.12A. Topics include:

New Actel Device Support

The synthesis tool supports the following new SmartFusion Actel device parts and packages:

Technology	Part	Package	Speed Grade
SmartFusion	A2F200M3F	FBGA256 FBGA484	Std
	A2F500M3G		Std

Note: SmartFusion adds support for the MSS_CCC macro.

SmartFusion supports most Fusion macros, except the following: AB, CLKDIVDLY, CLKDIVDLY1, DYNCCC, NGMUX, NVM, PLL, UFROM, UFROMH, ULSICC, VRPSM, and XTLOSC.

Actel Support for Libero/Designer 9.0

This version of the software supports Actel's latest design environment.

New Features and Enhancements

This section contains a summary of the new features and enhancements for version D-2009.12A. Topics include:

Continue on Error Mode

The Compile Point Synthesis flows support the Continue on Error mode in the Synplify Pro tool. The synthesis software *automatically* creates a black box for the compile point when it encounters any software or design error, and continues to synthesize the design. Note that if the software continues on error, the timing and resource usage reports may not be accurate. The Continue on Error mode is supported for certain Actel technologies.

Use the Continue on Error mode when:

- You set up an initial design. Perhaps you want to synthesize most of the design to determine its design size, but some modules still have technology mapper errors.

  Note that the Continue on Error mode is only applicable for mapper errors. Compiler errors from RTL coding must be corrected for synthesis to proceed.
- A compile point synthesis error occurs either with the design or the software.

However, you can also *manually* create a black box compile point to avoid a top-level design error and ensure synthesis completes successfully. See *Compile Point Type black_box* on page 3 for more information.

Compile Point Type black_box

With type black_box, the compile point is treated as a black box. Therefore, the contents of the compile point are ignored and only its ports exist during the synthesis flow. Black box compile point modules only write port definitions to the netlist files.

For details on complete compile point support, see online help or `user_guide.pdf->`*Running Compile Points* or specifically, *Running Compile Points->Using Continue on Error Mode*.

Create Image Command

Select File->Create Image to create a capture image from the following views:

- HDL Analyst Views
- FSM Viewer

Once you create the image you want to capture, the Create Image dialog box appears. Then you can copy the image, save to a file, or print this image.

Note: This command replaces the Copy Image and Print Image commands.

For more information, see online help or `reference.pdf->`*User Interface Commands->File Menu->Create Image Command*.

SYNCore Enhancements

This release includes support for the SYNCore byte-enable RAM component.

The SYNCore byte-enable RAM compiler generates SystemVerilog code describing byte-enabled RAMs. The data width of each byte is calculated by dividing the total data width by the write enable width. The byte-enable RAM compiler supports both single- and dual-port configurations.

For details on this component, see online help or `user_guide.pdf->`*Working with IP Input ->Generating IP with SYNCore* or `reference.pdf->`*Utilities->SYNCore Byte-Enable RAM Compiler.*

VHDL 2008 Enhancements

This release includes support for the following VHDL 2008 functions:

- Generics in Packages
- Context Declarations
- Else/Elsif Clauses
- All Keyword

For details, see online help or `reference.pdf->`*VHDL 2008 Language Support*.

Verilog Enhancements

The following Verilog enhancements are available in the release.

Verilog Library Support

Verilog libraries are used to compile design units; this is similar to VHDL libraries. Use the libraries in Verilog to support mixed-HDL designs, where the VHDL design includes instances of a Verilog module that is compiled into a specific library. Library support in Verilog can be used with Verilog 2001 and SystemVerilog designs.

For details, see online help or `reference.pdf->`*Verilog Language Support->Verilog Synthesis Guidelines->Library Support in Verilog*.

Verilog Generate Enhancement — Hierarchical Access in Generate

The newer Verilog 2005 generate statement is now supported in Verilog and SystemVerilog. Generate statements conform to the Verilog 2005 LRM. Defparams, parameters, and function and task declarations within generate statements are supported. In addition, the naming scheme for registers and instances is enhanced to include closer correlation to specified generate symbolic hierarchies. Generated data types have unique identifier names and can be referenced hierarchically. Generate statements are created using one of the following three methods: generate-loop, generate-conditional, or generate-case.

For details on complete support, see online help or `reference.pdf->`*SystemVerilog Language Support->Generate Statement*.

Start and Stop Addresses for RAM Initialization

You can specify initial values for a RAM in a data file and then include the appropriate task enable statement, $readmemb or $readmemh, in the initial statement of the RTL code for the module. This release adds the capability to specify start and stop addresses for RAM initialization.

For details, see online help or `reference.pdf->`*Verilog Language Support->Verilog Synthesis Guidelines->Initial Values in Verilog*.

SystemVerilog Enhancements

The following SystemVerilog capabilities are available in the release:

- Packed Union
- Parameter Data Types
- Streaming Operator
- Extern Module
- Array Querying Function

For details on complete support, see online help or `reference.pdf->`*SystemVerilog Language Support->SystemVerilog Constructs->Union Constructs,* `reference.pdf->`*SystemVerilog Language Support->Data Types,* `reference.pdf->`*SystemVerilog Language Support->Streaming Operator*, `reference.pdf->`*SystemVerilog Language Support->Extern Module*, or `reference.pdf->`*SystemVerilog Language Support->SystemVerilog Constructs->Array Querying Functions*.

Multiple File Compilation Unit Option

To use the compilation unit for modules defined in multiple files, enable the Multiple File Compilation Unit switch on the Verilog tab of the Implementation Options dialog box.

Documentation

The documentation set consists of the following:

Document	Format	Access
Online Help	HTML Help	See *Accessing Online Help* on page 7.
User Guide	PDF and HTML help	See *Accessing PDF Documents* on page 6.
Reference	PDF and HTML help	Same as above.
Release Notes	PDF	Same as above.
Errors, Warnings, and Notes Guide	HTML Help	Click on the error message in the log file or the Message Viewer.

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader 7.0. A copy of Acrobat Reader is available for installation on the Synplicity CD. You can also download Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

From within the software, you can open the PDF documents by selecting Help->Online Documents and selecting the appropriate PDF. You can also access PDF documents without running the software, as follows:

From Windows	Select either of the following: • From outside the software, select Start->Programs->Synopsys-> Synplify Actel Edition D-2009.12A • From inside the software, select Help->Online Documents In the Open dialog box, select the desired document: • Release Notes (`release_notes.pdf`) • User Guide (`user_guide.pdf`) • Reference Manual (`reference.pdf`) • Licensing User Guide (`license.pdf`)

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

You can access help from within the software or outside of the tool.

Accessing Help from inside the tool	
All platforms	Press F1 or select Help->Help. For context-sensitive help, click F1 in a dialog box.
Accessing Help from outside the tool	
On Windows	Select Start->Programs->Synopsys->Synplify Actel Edition D-2009.12A

Displaying Graphics

In some cases, the online help graphics do not display correctly. This is usually because your Display setting is 256-Color. Reset it to 16-bit Color, then reopen the online help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

- Text Editor Help Button is not Functional
- Crossprobing Source Code Files Created with Third-Party Editors
- Inout Port Inside a Compile Point
- Digital Line Detect Error Appears (Windows XP)

Text Editor Help Button is not Functional

The Help button at the bottom of the text editor GUI window is not functional. However, you can still use F1 for more information if you are within a text file.

Solution: This will be fixed in a future release.

Verilog Include Paths Missing from VCS Integration

If Verilog include paths have been added to your Project file, these paths are not automatically added to the VCS script.

Solution: You must add the Verilog include paths manually. To do this, use one of the following workarounds:

- From the Run VCS Simulator dialog box, add `+incdir+<include path>` in the Verilog Compile options field.
- Modify the VCS script file, adding the `+incdir+<include path>` to all or any relevant vlogan commands.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the Synplicity text editor.

Inout Port Inside a Compile Point

Currently, the software does not support some inout ports inside a compile point. If you have an inout port implemented in a compile point that drives a top-level port directly, the software reports the following error message:

> @E: Unable to insert correct pad for port <port name>. It is driven by a tristate in an unreachable hierarchy (Blackbox or Compile point).

Solution: Move the inout port implementation from the compile point to the top level.

Digital Line Detect Error Appears (Windows XP)

When launching the synthesis software, a Digital Line Detect error occasionally appears on a Dell PC running Windows XP.

Solution: Download the latest update from Dell Corporation. See the following URL for more information.

> http://support.dell.com/support/downloads/format.aspx?releaseid=r84541&c=us&l=en&s=gen&cs

Alternatively, you can deselect the Digital Line Detect entry in your system configuration. To do this:

1. Select Run from the Start menu.
2. Type `msconfig` in the open field and click OK.

   The System Configuration Utility dialog box appears.
3. Select the Startup tab and scroll down to the Digital Line Detect entry.
4. Deselect the checkbox to disable it.

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