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Synplify Pro® for Actel Edition Release Notes

Version F-2011.09M, September 2011

Publication Version 01

Release Note Topics

About this Release

This F-2011.09M release includes software improvements for the Synplify Pro® Actel Edition product. See *New Features and Enhancements* on page 2 for the summary of features and enhancements contained in the release.

Actel Support for Libero 10.0

This version of the software supports Actel's latest design environment. However, the following legacy devices will not be supported in Libero 10.0 and future releases:

Antifuse FPGAs		
ACT1	ACT2/1200XL	ACT3
3200DX	40MX	42MX
54SX (RTSX)	54SXA (RTSXS)	AX[1] (RTAXS and RTAXD)
eX		
Flash FPGAs		
500K (ProASiC)	PA (ProASIC^{PLUS})	

1. Also known as Axcelerator

New Features and Enhancements

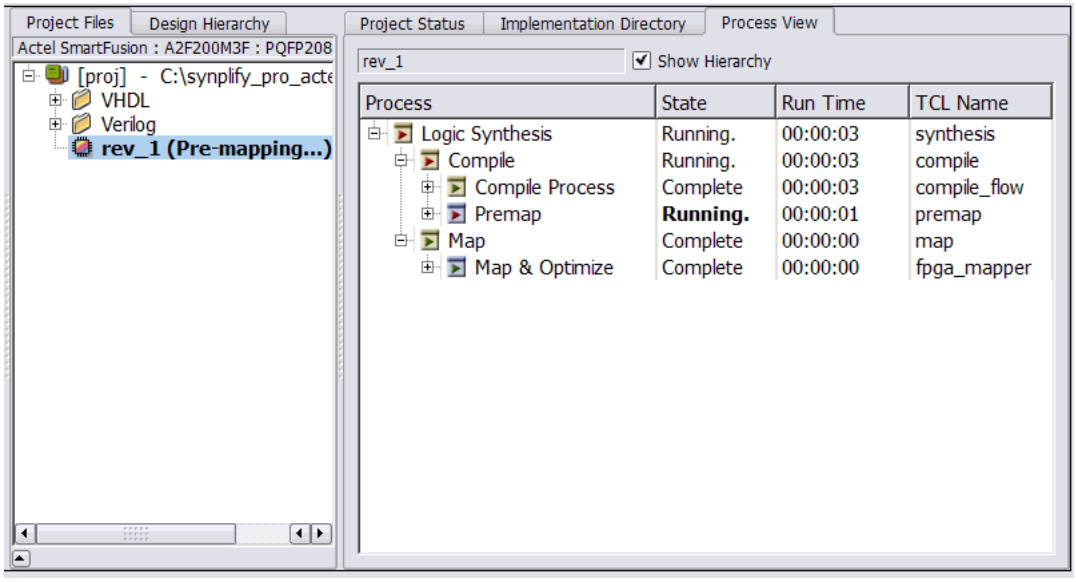
This section contains a summary of the features and enhancements that includes:

- Process View
- Project Status View
- Compile Point Timing Report
- Archive Utility Improvements
- Compiler Enhancements
- Synopsys Design Constraints

Process View

As process flow jobs become more complex, the benefits of exposing the underlying job flow is extremely valuable. The Process View gives you this visibility to track the design progress for the synthesis and place-and-route job flows.

Click the Process View tab on the right side of the Project Results view. This displays the job flow hierarchy run on the active implementation and is a function of this current implementation and its project settings.

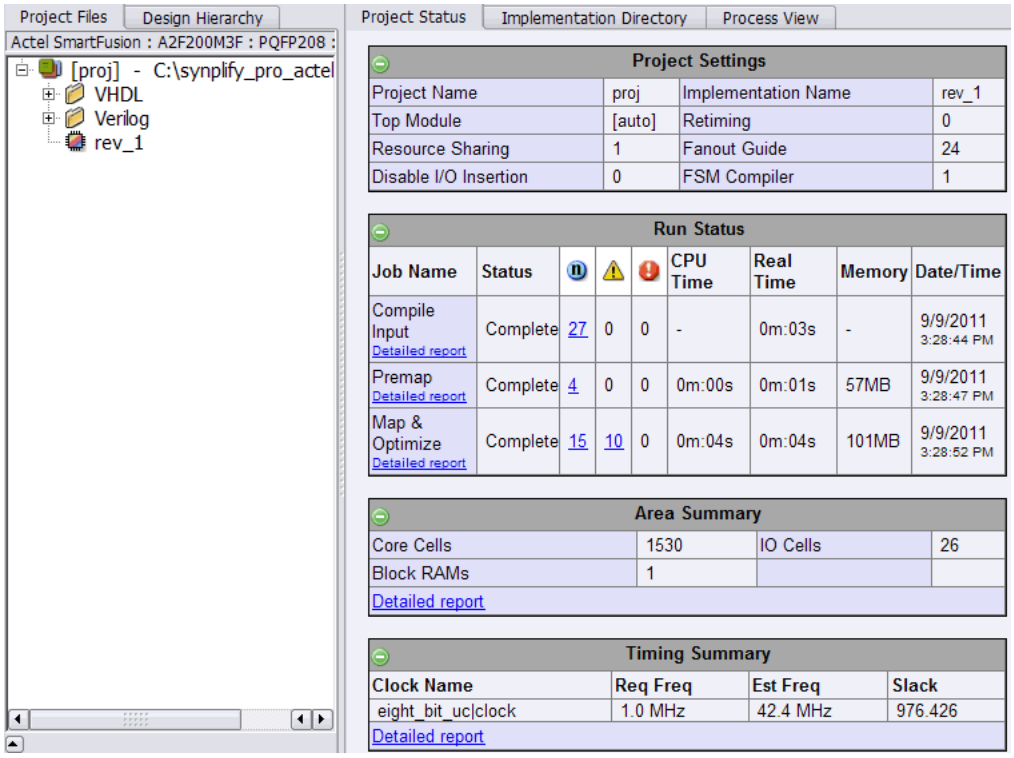


For more information, see the online help or reference.pdf->User Interface Overview->The Project Results View->Process View.

Project Status View

The Project Status view provides an overview of the project settings and at-a-glance summary of synthesis messages and reports such as an area or optimization summary for the active implementation. You can track the status and settings for your design and easily navigate to reports and messages in the Project view; this enhances usability of the synthesis tool.

To display this window, click on the Project Status tab in the Project view. An overview for the project is displayed in a spreadsheet format for each of the following sections: Project Settings, Run Status, and reports.



For more information about the Project Status view, see the online help or reference.pd->User Interface Overview->The Project Results View->Project Status View.

Compile Point Timing Report

In the Synplify Pro software, the Summary of Compile Points section of the log file (*projectName*.srr) lists each compile point, together with an indication of whether it was remapped during an incremental run, and if so, why the compile point changed. For this release, a timing report (*CPName*.srr) is generated for each compile point and is written to its respective result directory in the Implementation Directory view.

Archive Utility Improvements

The archive utility includes the following improvements:

- Supports batch/Tcl mode. For example:

```
project -archive -project test.prj -archive_file test.sar
```

For details about the syntax, see the online help or reference.pdf->Batch Commands and Scripts->Batch Commands for Synthesis->project.

- Can handle project files with long include paths.
- Compiler macro _SEARCHFILENAMEONLY_ can be used when the project file has include paths with absolute and relative paths.

  Note the following limitations:

  – Avoid using include files with the same name but different content.

  – The archived project might not translate the Tcl or environment variables correctly in the project file.

For more information, see the online help or reference.pdf->User Interface Commands->Implementation Options Command->Compiler Directives and Design Parameters.

Compiler Enhancements

Compiler enhancements for this release include:

- Beta Features – checkboxes have been added to both the VHDL and Verilog panels to enable the use of any Verilog or VHDL beta features included in the release. Enabling this checkbox is equivalent to including a set_option -hdl_define -set _BETA_FEATURES_ON_ directive in the project file.
- Default Verilog standard – the default Verilog standard for all new projects is now SystemVerilog (previously, the default standard for new Verilog projects was Verilog 2001).

VHDL Enhancements

The following features have been included in the VHDL compiler for this release:

Null Ranges

Null ranges (ranges that specify an empty subset of values) are now supported. A range specified as *m* to *n* is a null range when *m* is greater than *n*, and a range specified as *n* downto *m* is a null range when *n* is less than *m*. For examples of null ranges, see the online help or reference.pdf->VHDL Language Support->VHDL Language Constructs->Null Ranges.

Large Time Resolution (Beta)

Predefined physical time types now include the expanded range from –2147483647 to +2147483647 with units ranging from femtoseconds, and secondary units ranging up to an hour. Predefined physical time types allow selection of a wide number range representative of time type. The expanded time types are available as a beta feature and must be enabled by selecting the Beta Features for VHDL checkbox on the VHDL panel or by adding a set_option -hdl_define command to your project file (prj) as shown below:

```
set_option -hdl_define -set _BETA_FEATURES_ON_
```

For example time types, see the online help or reference.pdf->VHDL Language Support->VHDL Language Constructs->Large Time Resolution.

SystemVerilog Enhancements

SystemVerilog enhancements for this release include:

Enhanced Interface Construct Support (Beta)

SystemVerilog interface support has been extended to nested interfaces and array of interface instances. Additionally, access of the multi-dimensional data type and array type elements outside the interface is now supported. The new interface feature enhancements are available as a beta feature and must be enabled by selecting the Beta Features for Verilog checkbox on the Verilog panel or by adding a set_option -hdl_define command to your project file (prj) as shown below:

```
set_option -hdl_define -set _BETA_FEATURES_ON_
```

For detailed information, see the online help or reference.pdf->SystemVerilog Language Support->Interface->Interface Construct.

SVA System Functions

SystemVerilog assertion support now includes the $onehot, $onehot0, and $countones system functions. These functions check for specific characteristics on a particular signal. For detailed information, see the online help or reference.pdf->SystemVerilog Language Support->Assertions->SVA System Functions.

Conditional Generate Constructs

The if-generate and case-generate conditional generate constructs can now be used without the generate keyword to select, at most, one generate block from a set of alternative generate blocks based on constant expressions evaluated during elaboration. For detailed information, see the online help or reference.pdf->SystemVerilog Language Support->Generate Statement->Conditional Generate Constructs.

The following general enhancements have also been included in SystemVerilog:

- return statement within a task
- importing of multiple packages using comma separator
- package chaining
- data types accepted as arguments to array query function

Synopsys Design Constraints

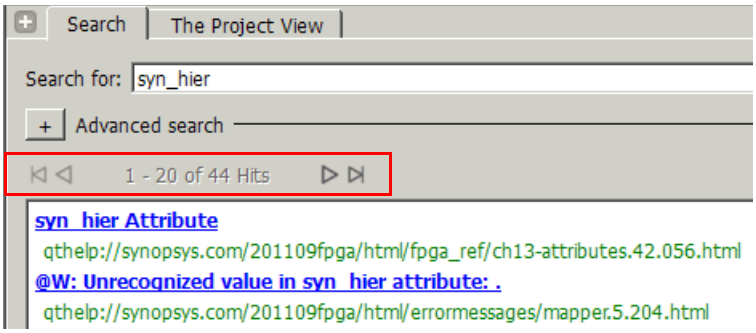
Support for the set_clock_latency Synopsys SDC constraint is included in this release. This constraint specifies the clock latency I/O delay applied to clock ports and clock aliases. In the FPGA synthesis tools, the set_clock_latency command accepts both clock objects and clock aliases. Applying a set_clock_latency constraint on a port can be used to model the off-chip clock delays in a multichip environment. Clock latency is forward annotated in the top-level constraint file as part of the time budgeting that takes place in the Certify/HAPS flow.

For detailed information and syntax, see reference.pdf->Timing Constraints->Synopsys Design Constraints->Supported Constraints.

Enhanced Online Help

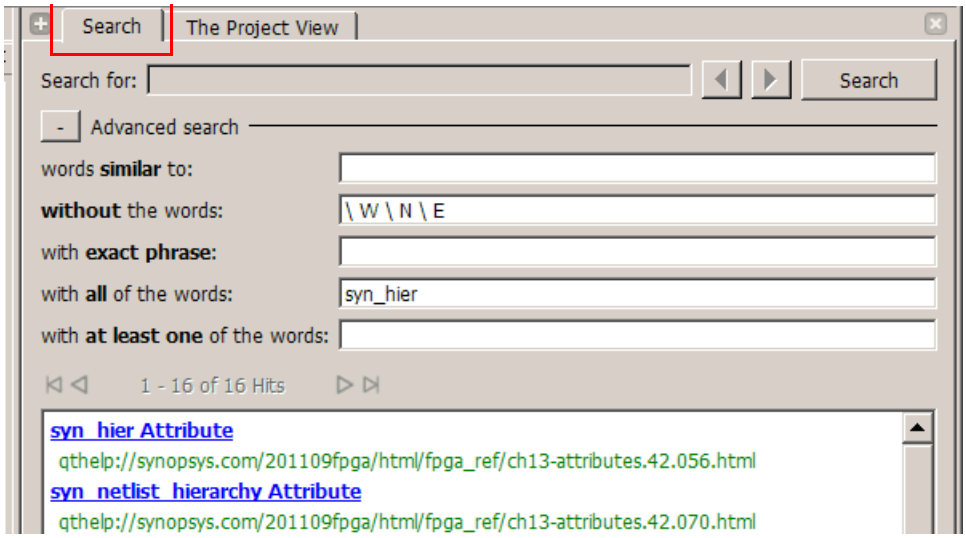
The F-2011.09M release provides an easier to use topic index and a new version of compiled help with faster search speeds and improved search capabilities:

- The index includes expanded links for a single-click entry. The Index locates information that is more focused and pertinent to a topic and is generally preferred over string search.
- The Search tab has been relocated within the help display and has been expanded to include all documented messages. The search function displays help in blocks of 20 targets; use the left/right arrows to display the next block.



To exclude a category of diagnostic messages (errors, warnings, or notes) from your search string, use the Advanced search option. To enable this option, click the adjacent + symbol. Enter the corresponding message identifier (\ E, \ W, or \ N) in the without the words field, and enter the search topic in the with all the words field. Click the Search button to initiate the search.

The following example illustrates a search for syn_hier that excludes warning, notes, and error messages to reduce the number of search hits:



- Clicking on a display target replaces the search list with the target information. Click the Search tab to return to the list of targets.
- The top of each help page includes the location within the help hierarchy. You can also use the Sync with Table of Contents icon to find your location in help.

Documentation

This section includes the following documentation topics:

- Accessing PDF Documents
- Accessing Online Help

The Synopsys FPGA Synthesis product documentation set consists of the following:

Document	Format	Access
Online Help	HTML Help	See *Accessing Online Help* on page 10.
Document Type • User Guide • Reference Manual • Release Notes	PDF and HTML help	See *Accessing PDF Documents* on page 9.
• Error Messages	HTML Help	Select Help->Error Messages. Click on the error message in the log file or the Message Viewer window.

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

To access PDF documents either from the software or without running the software, see the table below for details.

Synopsys FPGA Products

From Linux	From outside the software, select: • Open Acrobat Reader: `acroread` Open *`install_directory`*`/documents/`*`docfile`*

From Windows	• Start->Programs->Synopsys->Synplify Pro for Actel Edition F-2011.09M->Documents
	Then, select the desired document.
	• From inside the software for all platforms, select Help->Online Documents. In the Open dialog box, select the desired document:
	`- user_guide.pdf`
	`- reference.pdf`
	`- release_notes.pdf`

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

Topics include:

- Synopsys FPGA Products
- Displaying Graphics

Synopsys FPGA Products

For the FPGA products, you can access help from within the software or outside of the tool.

Accessing Help from inside the tool	
All platforms	Press F1 or select Help->Help. For context-sensitive help, click F1 in a dialog box.
Accessing Help from outside the tool	
On a Windows machine	Select Start->Programs->Synopsys->Synplify Pro Actel Edition F-2011.09M->Help.
From Linux	Run synplify_pro_help.

Displaying Graphics

In some cases, the online help graphics do not display correctly. This is usually because your Display setting is 256-Color. Reset the display to 16-bit Color, then reopen the online help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

Online Help—Page Could Not Be Found

After installing the latest product version, if you bring up the online help you might get the following message:

```
The Page Could Not Be Found
```

This indicates that there is a problem with the version number in your stored cached files. This could particularly be an issue for anyone who previously installed the beta version of this release. To correct this problem, you need to delete the cache files and restart the online help system.

Solution: Delete any `qhc` files and directories containing `qhc` files from the cache directory.

Windows 7:

C:\Users*userName***\AppData\Local\Synopsys\Synplify**

Windows XP:

C:\Documents and Settings*userName***\Local Settings\Application Data\Synopsys\Synplify**

Linux:

~/.local/share/data/Synopsys/Synplify/

This will be corrected in a future release.

Gated Clock Fixing and the create_generated_clock SDC Constraint

If the create_generated_clock constraint is used on the output of clock gating structures and the fixgatedclocks option is enabled, gated clock fixing does not occur for registers driven by the gated/generated clock because of issues with forward-annotation.

Solution: You can give up the use of generated clocks, enable gated clock fixing, and selectively specify timing exceptions from/to non-critical path start/end points in your design that are covered by the gated clock(s).

Enhancements are planned to address the forward-annotation issue in the future.

Manually Copy Compile Point Sub-directories to Identify Implementation

When compile points are included in an existing FPGA implementation and a new Identify implementation is created, the compile-point related data is not copied to the Identify implementation.

Solution: Manually copy the sub-directories in the FPGA implementation to the new Identify implementation directory. In addition to the sub-directories, the top-level constraint file and all of the compile-point constraint files for the related modules must be enabled on the Constraints panel of the Implementation Options.

Cannot Automatically Reorder VHDL Design with Verilog syn.dics File

When using a purely VHDL design within the Identify instrumentor, a Verilog version of the syn.dics file is automatically created which effectively makes the implementation a mixed-language design (VHDL design files plus Verilog syn.dics file). As a result, the compiler does not automatically reorder the VHDL design files which can cause some designs to fail when the file order is not correct in the project and the top-level module is not defined.

Solution: Manually re-order the source files in the project beginning with the VHDL packages and ending with the top-level file. Note that Arrange VHDL Files does not rearrange the files and that the files must be re-ordered manually.

Up-to-date Checking Not Applied for Mixed Language Designs

When a design includes mixed languages, the Synplify Pro tool re-synthesizes the design even though there are no changes to the input files. The up-to-date checking feature does not behave as expected.

Solution: This will be fixed in a future release.

Up-to-date Checking Limitation for Sourced Tcl Files in the SDC File

When a design is run, the up-to-date checking feature automatically determines if a design needs to be re-synthesized or not. This feature can provide significant runtime improvements especially for team designs.

However, when you modify constraints in a Tcl file sourced within the constraints file (sdc), the software is not aware of these changes and does not force the design to be re-synthesized.

Solution: This will be fixed in a future release.

Handling State Machines in Different Clock Domains

If a state machine defined in the code feeds sequential elements in a different clock domain, using any encoding value other than the "original" can cause metastability. By default, the synthesis tools choose the optimal encoding value based on the number of states in the state machine. This can introduce additional decode logic that may cause metastability when it feeds sequential elements in a different clock domain.

Solution: As a workaround, use syn_encoding = "original" to guide the synthesis tool for these cases.

Verilog Include Paths Missing from VCS Integration

If Verilog include paths have been added to your Project file, these paths are not automatically added to the VCS script.

Solution: You must add the Verilog include paths manually. To do this, use one of the following workarounds:

- From the Run VCS Simulator dialog box, add +incdir+<*include path*> in the Verilog Compile options field.
- Modify the VCS script file, adding the +incdir+<*include path*> to all or any relevant vlogan commands.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (.prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

Digital Line Detect Error Appears (Windows XP)

When launching the synthesis software, a Digital Line Detect error occasionally appears on a Dell PC running Windows XP.

Solution: Download the latest update from Dell Corporation. See the following URL for more information.

http://support.dell.com/support/downloads/format.aspx?releaseid=r84541&c=us&l=en&s=gen&cs

Alternatively, you can deselect the Digital Line Detect entry in your system configuration. To do this:

1. Select Run from the Start menu.
2. Type `msconfig` in the open field and click OK.

   The System Configuration Utility dialog box appears.
3. Select the Startup tab and scroll down to the Digital Line Detect entry.
4. Deselect the checkbox to disable it.

Invoking Tool can be Slow on Linux With Network Problems

Invoking the synthesis tools might be slow when you are experiencing network problems on Linux platforms, such as when a mounted drive is not accessible.

Solution: Delete the `$HOME/.config/Trolltech.conf` file to avoid caching. This might help to invoke the tool faster.

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