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Synplify Pro® for Actel Edition Release Notes

Version F-2012.03A-SP1, June 2012

Publication Version 01

Release Note Topics

About this Release

This F-2012.03A-SP1 release includes software improvements and enhancements for the Synplify Pro® Actel Edition product. See *New Features and Enhancements* on page 2 for the summary of features and enhancements contained in the release.

New Features and Enhancements

This release includes the compiler enhancement for *Internal Address Format for Initialization Data File* on page 2.

Internal Address Format for Initialization Data File

The initialization data file, read by the Verilog $readmemb and $readmemh tasks, now supports an embedded hexadecimal address format. Any number of address specifications can be included in the file, and in any order. When the $readmemb or $readmemh system task encounters an embedded address specification, it begins loading subsequent data at that memory location. For more information, see *Initialization Data File* on page 2.

Initialization Data File

The initialization data file, read by the $readmemb and $readmemh system tasks, contains the initial values to be loaded into the memory array. This initialization file can reside in the project directory or can be referenced by an include path relative to the project directory. The system $readmemb or $readmemh task first looks in the project directory for the named file and, if not found, searches for the file in the list of directories on the Verilog tab in include-path order.

If the initialization data file does not contain initial values for every memory address, the unaddressed memory locations are initialized to 0. Also, if a width mismatch exists between an initialization value and the memory width, loading of the memory array is terminated; any values initialized before the mismatch is encountered are retained.

Unless an internal address is specified (see *Internal Address Format* on page 3), each value encountered is assigned to a successive word element of the memory. If no addressing information is specified either with the $readmem task statement or within the initialization file itself, the default starting address is the lowest available address in the memory. Consecutive words are loaded until either the highest address in the memory is reached or the data file is completely read.

If a start address is specified without a finish address, loading starts at the specified start address and continues upward toward the highest address in the memory. In either case, loading continues upward. If both a start address and a finish address are specified, loading begins at the start address and continues until the finish address is reached (or until all initialization data is read).

For example:

```
initial
begin
//$readmemh ("mem.ini", ram_bank1)
   /* Initialize RAM with contents from locations 0 thru 31*/;

//$readmemh ("mem.ini", ram_bank1,0)
   /* Initialize RAM with contents from locations 0 thru 31*/;

$readmemh ("mem.ini", ram_bank1, 0, 31)
   /* Initialize RAM with contents from locations 0 thru 31*/;

$readmemh ("mem.ini", ram_bank2, 31, 0)
   /* Initialize RAM with contents from locations 31 thru 0*/;
```

The data initialization file can contain the following:

- White space (spaces, new lines, tabs, and form-feeds)
- Comments (both comment formats are allowed)
- Binary values for the $readmemb task, or hexadecimal values for the $readmemh tasks

In addition, the data initialization file can include any number of hexadecimal addresses (see *Internal Address Format* on page 3).

Internal Address Format

In addition to the binary and hex formats described above, the initialization file can include embedded hexadecimal addresses. These hexadecimal addresses must be prefaced with an at sign (@) as shown in the example below.

```
FFFFF37  /* data for address 0 */
FFFFF63  /* data for address 1 */
@0EA     /* memory address 234
FFFFFC2  /* data for address 234*/
FFFFF21  /* data for address 235*/
...
@0A7     /* memory address 137
FFFFF77  /* data for address 137*/
FFFFF7A  /* data for address 138*/
...
```

Either uppercase or lowercase characters can be used in the address. No white space is allowed between the @ and the hex address. Any number of address specifications can be included in the file, and in any order. When the $readmemb or $readmemh system task encounters an embedded address specification, it begins loading subsequent data at that memory location.

When addressing information is specified both in the system task and in the data file, the addresses in the data file must be within the address range specified by the system task arguments; otherwise, an error message is issued, and the load operation is terminated.

Platforms and Patches

This section includes platform support and other platform-specific information.

Platform Support

The software is supported on the following platforms and operating systems:

- Windows (x86_x64):
  - 7 Professional or Enterprise (32/64-bit)
  - Vista Enterprise or Business (32/64-bit)
  - XP Professional (32/64-bit)
- Linux (x86_x64):
  - Red Hat Enterprise Linux 4/5 (32/64-bit)

Required Operating System Patches

Running this software requires that the Linux operating system include specific patches. To determine whether your operating system requires patches, refer to the following procedure.

Checking the Installed Patches

All Linux-based FPGA synthesis applications include a script (syn_system_check) that is designed to check patches that have been installed and the patches that need to be installed or updated.

To use this script:

1. Install the product software.
2. Run the script by entering the following command in a shell:

   /*install_dir*/*product_version*/bin/syn_system_check

3. The script runs and generates a system check summary report that lists the patches and patch status (OK, Install, or Upgrade).
4. Consult the display and install or update any of the patches indicated.

Example

The following is a sample report.

```
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-

     Synplicity system check summary report for host 'synsun2'

 1.  /home/syn/user available size == 13728736 KB             [ OK ]
 2.  /tmp available size == 243192 KB                         [ OK ]
 3.  /var/tmp available size == 22069 KB                      [ OK ]
 4.  Current DISPLAY is set to 'user:0'                       [ Check user ]
 5.  Required Patch '106950-13'                               [ Install Patch ]
 6.  Upgrade from '106146-14'  to  '106146-31' Required       [ Upgrade Patch ]
 7.  Upgrade from '106327-08'  to  '106327-13' Required       [ Upgrade Patch ]
 8.  Upgrade from '106541-07'  to  '106541-19' Required       [ Upgrade Patch ]
 9.  Upgrade from '108376-12'  to  '108376-34' Required       [ Upgrade Patch ]
10.  sparc architecture                                       [ OK ]
11.  synsun2 solaris 5.7                                      [ OK ]

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Explanation of Operating system patches, following patches are
available at vendor's ftp site

[ 106146-31 ]    SunOS 5.7: M64 Graphics Patch
[ 106327-13 ]    32-Bit Shared library patch for C++
[ 106541-19 ]    SunOS 5.7: Kernel update patch
[ 106950-13 ]    SunOS 5.7: Linker Patch ( required by 106327-13 )
[ 108376-34 ]    OpenWindows 3.6.1: Xsun Patch

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```

Documentation

This section includes the following documentation topics:

- Accessing PDF Documents
- Accessing Online Help

The Synopsys FPGA Synthesis product documentation set consists of the following:

Document	Format	Access
Online Help	HTML Help	See *Accessing Online Help* on page 7.
Document Type • User Guide • Reference Manual • Release Notes	PDF and HTML help	See *Accessing PDF Documents* on page 6.
• Error Messages	HTML Help	Select Help->Error Messages. Click on the error message in the log file or the Message Viewer window.

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

To access PDF documents either from the software or without running the software, see the table below for details.

Synopsys FPGA Products

From Linux	From outside the software, select: • Open Acrobat Reader: `acroread` Open *`install_directory`*`/documents/`*`docfile`*
From Windows	• Start->Programs->Synopsys->Synplify Pro for Actel Edition F-2012.03A-SP1->Documents Then, select the desired document. • From inside the software for all platforms, select Help->Online Documents. In the Open dialog box, select the desired document: - `user_guide.pdf` - `reference.pdf` - `release_notes.pdf`

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

Topics include:

- Synopsys FPGA Products
- Displaying Graphics

Synopsys FPGA Products

For the FPGA products, you can access help from within the software or outside of the tool.

Accessing Help from inside the tool	
All platforms	Press F1 or select Help->Help. For context-sensitive help, click F1 in a dialog box.
Accessing Help from outside the tool	
On a Windows machine	Select Start->Programs->Synopsys->Synplify Pro Actel Edition F-2012.03A-SP1->Help.
From Linux	Run synplify_pro_help.

Displaying Graphics

In some cases, the online help graphics do not display correctly. This is usually because your Display setting is 256-Color. Reset the display to 16-bit Color, then reopen the online help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

VHDL Generics Documentation Syntax Clarification

The hdl_param command shows or sets VHDL parameter overrides for the top-level module of your design. In batch mode, to set generic values using the set_option command in a project file, specify the hdl_param generic with quotes and enclose it within {}. For example:

```
set_option -hdl_param -set ram_file {"init.mem"}
set_option -hdl_param -set simulation {"false"}
```

Solution: The documentation will be updated in a future release.

Gated Clock Fixing and the create_generated_clock SDC Constraint

If the create_generated_clock constraint is used on the output of clock gating structures and the fixgatedclocks option is enabled, gated clock fixing does not occur for registers driven by the gated/generated clock because of issues with forward-annotation.

Solution: You can give up the use of generated clocks, enable gated clock fixing, and selectively specify timing exceptions from/to non-critical path start/end points in your design that are covered by the gated clock(s).

Enhancements are planned to address the forward-annotation issue in the future.

Manually Copy Compile Point Sub-directories to Identify Implementation

When compile points are included in an existing FPGA implementation and a new Identify implementation is created, the compile-point related data is not copied to the Identify implementation.

Solution: Manually copy the sub-directories in the FPGA implementation to the new Identify implementation directory. In addition to the sub-directories, the top-level constraint file and all of the compile-point constraint files for the related modules must be enabled on the Constraints panel of the Implementation Options.

Cannot Automatically Reorder VHDL Design with Verilog syn.dics File

When using a purely VHDL design within the Identify instrumentor, a Verilog version of the syn.dics file is automatically created which effectively makes the implementation a mixed-language design (VHDL design files plus Verilog syn.dics file). As a result, the compiler does not automatically reorder the VHDL design files which can cause some designs to fail when the file order is not correct in the project and the top-level module is not defined.

Solution: Manually re-order the source files in the project beginning with the VHDL packages and ending with the top-level file. Note that Arrange VHDL Files does not rearrange the files and that the files must be re-ordered manually.

Up-to-date Checking Not Applied for Mixed Language Designs

When a design includes mixed languages, the Synplify Pro tool re-synthesizes the design even though there are no changes to the input files. The up-to-date checking feature does not behave as expected.

Solution: This will be fixed in a future release.

Up-to-date Checking Limitation for Sourced Tcl Files in the SDC File

When a design is run, the up-to-date checking feature automatically determines if a design needs to be re-synthesized or not. This feature can provide significant runtime improvements especially for team designs.

However, when you modify constraints in a Tcl file sourced within the constraints file (sdc), the software is not aware of these changes and does not force the design to be re-synthesized.

Solution: This will be fixed in a future release.

Handling State Machines in Different Clock Domains

If a state machine defined in the code feeds sequential elements in a different clock domain, using any encoding value other than the "original" can cause metastability. By default, the synthesis tools choose the optimal encoding value based on the number of states in the state machine. This can introduce additional decode logic that may cause metastability when it feeds sequential elements in a different clock domain.

Solution: As a workaround, use syn_encoding = "original" to guide the synthesis tool for these cases.

Verilog Include Paths Missing from VCS Integration

If Verilog include paths have been added to your Project file, these paths are not automatically added to the VCS script.

Solution: You must add the Verilog include paths manually. To do this, use one of the following workarounds:

- From the Run VCS Simulator dialog box, add `+incdir+<include path>` in the Verilog Compile options field.
- Modify the VCS script file, adding the `+incdir+<include path>` to all or any relevant vlogan commands.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (.prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

Digital Line Detect Error Appears (Windows XP)

When launching the synthesis software, a Digital Line Detect error occasionally appears on a Dell PC running Windows XP.

Solution: Download the latest update from Dell Corporation. See the following URL for more information.

http://support.dell.com/support/downloads/format.aspx?releaseid=r84541&c=us&l=en&s=gen&cs

Alternatively, you can deselect the Digital Line Detect entry in your system configuration. To do this:

1. Select Run from the Start menu.
2. Type `msconfig` in the open field and click OK.

   The System Configuration Utility dialog box appears.
3. Select the Startup tab and scroll down to the Digital Line Detect entry.
4. Deselect the checkbox to disable it.

Invoking Tool can be Slow on Linux With Network Problems

Invoking the synthesis tools might be slow when you are experiencing network problems on Linux platforms, such as when a mounted drive is not accessible.

Solution: Delete the `$HOME/.config/Trolltech.conf` file to avoid caching. This might help to invoke the tool faster.

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