Synopsys®, Inc.
700 East Middlefield Road
Mountain View, CA 94043 USA

Website: www.synopsys.com
Support: www.solvnet.com

Identify® Actel Edition Tool Set Release Notes

Version F-2011.09A, October 2011

Publication Version 01

Contents

About This Release

These release notes describe features and enhancements for the F-2011.09A release of the Identify Actel Edition tool set.

Release F-2011.09A Features and Enhancements

The following features and enhancements have been included in the F-2011.09A release:

- Expanded syntax for watchpoint expressions
- JTAG client/server configuration
- Data compression of sampled data
- Support for additional Actel SmartFusion device
- Compile-point support in Identify

Expanded Syntax for Watchpoint Expressions

Hexadecimal values can now be entered as watchpoint values in the GUI by introducing the value with an x character and enclosing the value in quotation marks. For more information, see *Setting a Watchpoint Expression* in Chapter 7 of the *User Guide*.

JTAG Client/Server Configuration

The client-server configuration can now be set from a dialog box available in the Identify debugger. The settings require changing only when the default server port address is already in use or when the Identify debugger is run from a machine other than the machine connected to the FPGA board/device. For more information, see *JTAG Client-Server Configuration* in Chapter 9 of the *User Guide*. Note that in the current release, the server address cannot be changed from “localhost.”

Data Compression of Sampled Data

Data compression of the sampled data is available in this release. Using this feature effectively increases the depth of the sample buffer without requiring any additional hardware resources. Data compression is enabled by a checkbox in the Identify debugger project view or can be enabled from the command prompt with an argument to the iice sampler command. For more information, see *Sampled Data Compression* in the *User Guide*.

Additional Actel SmartFusion Device

Device support for the Actel SmartFusion family has been expanded to include the A2F060M3E device.

Compile-point Support in Identify

Manual compile points are now supported in the Actel Edition of the Identify tool set. Using compile points in the Synplify FPGA-Identify flow offers the following advantages:

- reduction in synthesis runtimes when compile points defined in the FPGA implementation are used within the Identify implementation.
- reduction in synthesis runtimes for the incremental instrumentation flow.

Note that automatic compile points are not supported in the Identify tool set. For more information on manual compile points, see *Using Compile Points with the Identify Tool* in the *Running Post-Synthesis Operations* section of the *Synopsys FPGA Synthesis User Guide*.

Device Support

The F-2011.09A release supports the following device families. With this release, device selection is specified solely in the synthesis tool and passed to the Identify instrumentor in the synthesis project file. Specifying a library in the synthesis tool that is not supported in the Identify tool set results in a "device not supported" message when attempting to launch the Identify instrumentor.

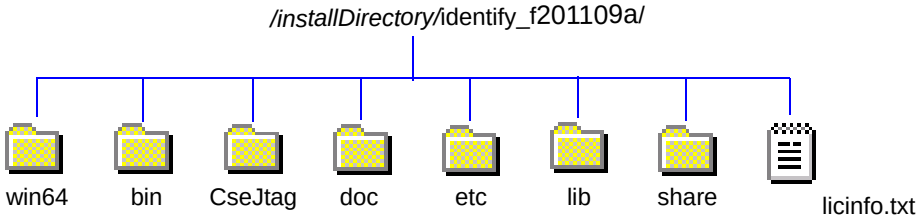
ProASIC	ProASIC PLUS	ProASIC3	ProASIC3E
ProASIC3L	Fusion	SmartFusion	IGLOO
IGLOOe	IGLOO PLUS		

Installation

The directory where Identify is installed is referred to as the *installDirectory*. The installation subdirectory name consists of the Identify product name and an associated version number, in the current case, identify_f201109a (for version F-2011.09A). This naming convention permits multiple versions to be installed in the same product directory. The start menus, desktop icons, and uninstall names have an associated version number, in the current case, Identify F-2011.09A. For a list of the compatible Windows-based platforms, see *Platform Support* on page 5.

Downloading the Software

The Identify Actel Edition software is normally downloaded from an FTP site and installed directly from the downloaded exe file. Installing the Identify software creates the identify_f201109a subdirectory in the installation directory. This directory contains the following files and subdirectories:



The contents of the files or sub-directories are as follows:

Directory	Contents
bin, win64	Executables for the Identify instrumentor and Identify debugger.
CseJtag	Drivers
doc	User documentation
etc	Location for user-defined startup scripts; template included
lib	Program data files
share	Includes the following subdirectories: • contrib – source directory for scripts executed on startup • vhdl – standard vhdl libraries • synthesis – program specific data files • demo_design – the bus_demo design
licinfo.txt	ASCII version of the Synopsys Software License and Maintenance Agreement for Actel-Synplicity Software Products.

Platform Support

The Identify F-2011.09A release is compatible with the following platforms and operating systems:

- Windows (x86/x64):
  - Windows 7 Professional or Enterprise (32/64-bit)
  - XP Professional (32-bit)

Synopsys FPGA Synthesis and Third-Party Tool Compatibility

The F-2011.09A release of the Identify Actel Edition software is compatible with the following Synopsys FPGA and third-party tools on the above platforms and operating systems.

Tool	Recommended Version
Synplify Pro (synthesis)	FPGA E-2011.09A (required)
Actel (place and route)	Libero 9.1

Machine Requirements

Machine memory requirements vary according to the size and complexity of your designs. At a minimum, 1 Gbyte of RAM is required (4 Gbytes are recommended). Your machine's virtual memory (swap space) should be set to at least two times the capacity of the RAM.

Location of the cfg File

The Windows platforms do not permit applications to write to the C:/Windows directory. Because the Identify tools must update the userprefs.cfg initialization file, this file is written to the following directory locations:

On Windows 7 platforms, the software stores the `cfg` file at the following location:

```
C:\Users\userName\AppData\Roaming\Identify
```

On Windows XP platforms, the software stores the `cfg` file at the following location:

```
C:\Documents and Settings\userName\Application Data\Identify
```

Windows Memory Configuration

For all memory configurations, Windows uses a default virtual address space of 4 GBytes; 2 GBytes allocated to user processes (applications) and 2GBytes allocated to the operating system and kernel-mode drivers. On Windows Server 2003 systems and Windows XP Pro systems (with Service Pack 2) that have 1 GByte or more of physical memory, the memory allocation between applications and operating system can be modified to increase the user-process memory allocation to 3 GBytes (and reduce the operating system memory allocation to 1 GByte). For the most up-to-date information for reconfiguring memory allocation on a compatible system, see *How to Set the /3GB Startup Switch in Windows* and related topics on the Microsoft TechNet (http://www.microsoft.com/technet).

Configuring the Windows Firewall for Client Access

Windows XP Service Pack 2 (SP2) and later enhance the security capabilities of the Windows operating system. If you are using a Windows XP machine with an SP2 or later update as your floating license server, you must configure the XP firewall application to allow client access to the floating license ports.

The license manager daemon (lmgrd) and the snpslmd license daemon are separate processes and each requires a separate port to run its associated driver. For floating licenses, you must define a PORT variable for the snpslmd license daemon and then add the ports to the the list of exceptions in the firewall application.

Do the following:

1. Open the license file and edit it to define the variable for the snpslmd license daemon by adding a PORT variable to the VENDOR line.

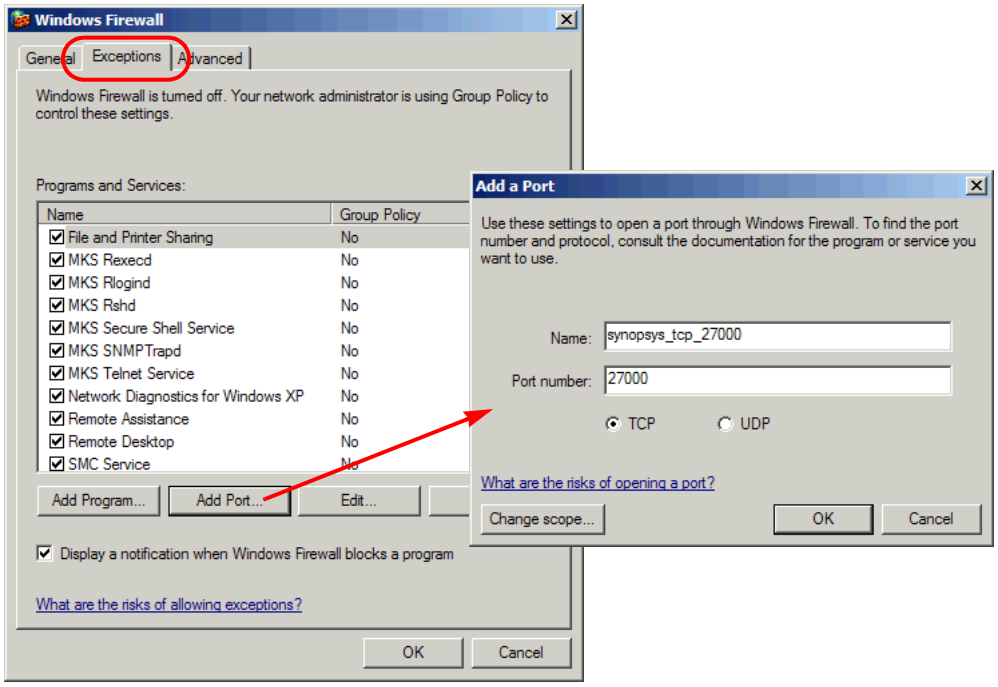
   The following is an example:

   ```
   SERVER <server_name> FLEXID=9-089Dxxxx 27000
   VENDOR snpslmd c:\synopsys\scl_11.1\windows\bin\snpslmd.exe PORT=27001
   INCREMENT synplifypro snpslmd 2010.12 31-dec-2011 1 \
   ...
   ```

   Next, you must add the port values to the Exceptions list in the Windows Firewall application.

2. From the Control Panel, open the Windows Firewall application.

3. Click the Exceptions tab, and then click the Add Port button to display the Add a Port dialog box.



4. Add the TCP port for the license manager daemon by doing the following in the Add a Port dialog box:
   - In the Name field, specify a name for the TCP port. For example, synopsys_tcp_27000.
   - In the Port number field, enter the assigned TCP port value from the license file. Using the sample license file as an example, enter 27000.
   - Click OK in the Add a Port dialog box to accept the entry and close the dialog box.
5. Specify the port for the snpslmd license daemon as follows:
   - Click the Add Port button to redisplay the Add a Port dialog box, and then set the following options.
   - In the Name field, specify a name for the snpslmd license daemon port. For example, synopsys_port_27001.
   - In the Port number field, enter the assigned PORT value from the license file. Using the sample license file as an example, enter 27001.
   - Click OK in the Add a Port dialog box to accept the entry and close the dialog box.
6. Verify that the port names you assigned are included in the Programs and Services list of the Exceptions pane.
7. Click OK in the Windows Firewall dialog box to exit the Windows Firewall application.

Identify Documentation

The following documentation is included with the F-2011.09A release of the Identify tool set:

- Identify Actel Edition User Guide
- Identify Actel Edition Reference Manual
- Identify Actel Edition Tutorial
- Identify Actel Edition Quick Start Guide
- Synopsys Software License and Maintenance Agreement

Accessing Documents using the Acrobat Reader

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online. From within the software, you can open the PDF documents by selecting Help->Online Documents and selecting the appropriate PDF. You can also access PDF documents without running the software by selecting Start->Programs->Synopsys->Identify F-2011.09A->Documents and then selecting the desired PDF document.

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Resolved Issues

The following issues have been resolved by the Identify F-2011.09A release:

Resolved Issue: On Windows platforms, the existing cable client/server architecture was responsible for a degradation in Identify debugger performance which was especially apparent on systems with limited memory or resources (STAR 9000459072).

Resolved Issue: When the RTL source files in a project included an ^M (end of line) character (due to editing across different platforms), loading the project into the Identify instrumentor resulted in a db_assert error (STAR 9000379248).

Resolved Issue: When a Synplify implementation name included any non-alphanumeric characters, Identify changed the implementation name by replacing the non-alphanumeric characters with underscores; the non-alphanumeric are now accepted (STAR 9000469618).

Resolved Issue: In a purely VHDL design, the compiler failed to not automatically reorder the VHDL design files which caused some designs to fail when the file order was not correct in the project and the top-level module was not defined (STAR 9000486136).

Resolved Issue: When invoking the Identify Instrumentor from the command line, including the location and type of synthesis tool command line arguments as described in *Synthesis Tool Pointers* in the *Reference Manual* opened the Identify Instrumentor in the GUI mode, but did not allow a project to be opened (Open Project button was disabled) (STAR 9000451295).

Important Issues and Workarounds

The following issues have been identified with the Identify F-2011.09A release:

Problem: When compile points are included in an existing FPGA implementation and a new Identify implementation is created, the compile-point related data is not copied to the Identify implementation.

Workaround: Manually copy the sub-directories in the FPGA implementation to the new Identify implementation directory. In addition to the sub-directories, the top-level constraint file and all of the compile-point constraint files for the related modules must be enabled on the Constraints panel of the Implementation Options.

Problem: When data compression is enabled in the Identify debugger, the precise trigger location indicated in the data samples may be incorrect. The amount of "trigger-shift" from the correct location varies according to the amount of data compression occurring during the trigger cycle. Since there is a maximum cycle compression of 64 clock cycles, the maximum incorrect shift can be up to 64 sample clocks (9000495203).

Problem: When using VHDL, if the trigger signal (scalar) is of type std_logic, the value must be enclosed in single quotes in both the UI and the shell as shown in the following command (STAR 9000483412):

```
watch enable -iice IICE -condition 0/my_signal {'0'}
```

Entering a scalar signal without quotes or in double quotes results in an error. Conversely, vectors must be entered without quotes as shown in the following command:

```
watch enable -iice IICE -condition 0/my_bus {1010}
```

Workaround: Make sure that all scalars are enclosed in single quotes and that vectors are entered without quotes.

Problem: The message suppression feature available with the synthesis tools cannot be used to suppress (or change the severity of) messages generated by Identify (STAR 9000484518).

Workaround: Be sure to disable message suppression when using an Identify implementation.

Problem: The -remote_trigger option for the run command is not functional (STAR 900415957).

Workaround: The functionality of remote triggering is essentially replaced with the current cross-triggering mechanism. Continued support for remote triggering is being discontinued in future releases.

Problem: If an implementation has an edf black-box module, the Identify instrumentor errors out complaining about an undefined module (STAR 9000315931).

Workaround: Replace the edf black box with some RTL or a functional edf module.

Problem: Use of external triggers via the import trigger mechanism causes an excessive use of internal block RAM due to sampling of the trigger as well as the creation of a look-up table. The problem is most notable when the maximum of eight imported triggers is selected. A better mechanism to import triggers that uses fewer resources will be available in a future release (STAR 9000462154).

Workaround: Add an extra input to the top-level RTL code and instrument the input as a trigger only.

Problem: Use of the SystemVerilog setting in Synplify can cause a compile error in Identify (STAR 9000426257).

Workaround: Disable the SystemVerilog switch for instrumentation and then turn it back on for synthesis. If the problem persists, contact Synopsys support.

Problem: Cross-triggering can cause Identify Debugger to crash if a trigger condition is not set for each IICE (STAR 9000359582).

Workaround: Set a trigger for each IICE (even a dummy trigger).

Synopsys, Inc.
700 East Middlefield Road, Mountain View, CA 94043 USA
www.solvnet.com