SmartFusion Customizable System-on-Chip (cSoC)

Microcontroller Subsystem (MSS)

- Hard 100 MHz 32-Bit ARM® Cortex™-M3
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth,[1] Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface[2]
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I²C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 from Data Transactions
- Clock Sources
  - 32 KHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; 1% Accurate
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA

- Based on proven ProASIC®3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog
Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
  - 500 Ksps in 12-Bit Mode
  - 550 Ksps in 10-Bit Mode
  - 600 Ksps in 8-Bit Mode
- Internal 2.56 V Reference or Optional External Reference
- One First-Order $\Sigma\Delta$ DAC (sigma-delta) per ADC
  - 8-Bit, 16-Bit, or 24-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
  - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5 V to −11.5/+14 V) with 1% Accuracy
  - High Gain Current Monitor, Differential Gain = 50, up to 14 V Common Mode
  - Temperature Monitor (Resolution = ¼°C in 12-Bit Mode; Accurate from −55°C to 150°C)
- Up to Ten High-Speed Voltage Comparators (t_{pd} = 15 ns)

Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® System-on-Chip (SoC) Software

I/Os and Operating Voltage

- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

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1 Theoretical maximum
2 A2F200 and larger devices

SmartFusion cSoC Family Product Table

FPGA Fabric	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			

Microcontroller Subsystem (MSS)	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	26-/16-bit address/data			26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^{2}C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			

Programmable Analog	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the *SmartFusion Programmable Analog User's Guide* for details.

Package I/Os: MSS + FPGA I/Os

Device	A2F060			A2F200				A2F500			
Package	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs[1]	4	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	15	15	15	24	24	24	24	24	24	24	32
Total Analog Outputs	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[2,3]	21[4]	28[4]	26[4]	22	31	25	41	22	31	25	41
FPGA I/Os	33	68	66	66	78	66	94	66[5]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
2. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
3. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
4. *10/100 Ethernet MAC is not available on A2F060.*
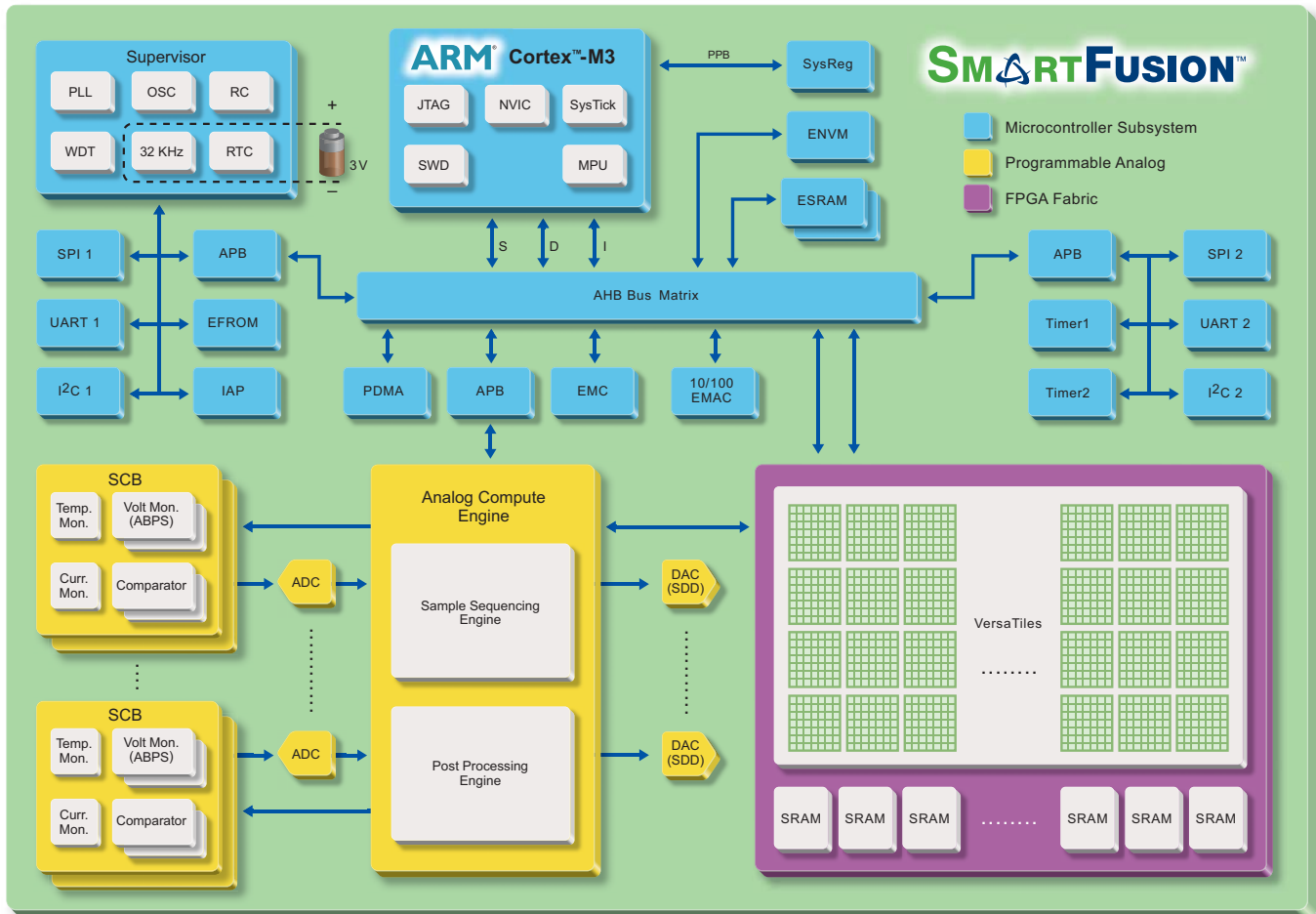5. *EMC is not available on the A2F500 PQ208 package.*

Table 1 • SmartFusion cSoC Package Sizes Dimensions

Package	TQ144	PQ208	CS288	FG256	FG484
Length × Width (mm\mm)	20 × 20	28 × 28		17 × 17	23 × 23
Nominal Area (mm^2)	400	784		289	529
Pitch (mm)	0.5	0.5		1.0	1.0
Height (mm)	1.40	3.40		1.60	2.23

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary: CS288, FG256, TQ144
A2F200	Production: CS288, FG256, FG484, PQ208
A2F500	Production: CS288, FG256, FG484, PQ208

SmartFusion cSoC Block Diagram

![SmartFusion cSoC Block Diagram]

Supervisor
PLL · OSC · RC
WDT · 32 KHz · RTC
+ 3V −

ARM® Cortex™-M3
JTAG · NVIC · SysTick
SWD · MPU

PPB · SysReg

ENVM

ESRAM

SMARTFUSION™
- Microcontroller Subsystem
- Programmable Analog
- FPGA Fabric

SPI 1 · APB
UART 1 · EFROM
I²C 1 · IAP

S · D · I

AHB Bus Matrix

PDMA · APB · EMC · 10/100 EMAC

APB · SPI 2
Timer1 · UART 2
Timer2 · I²C 2

SCB
Temp. Mon. · Volt Mon. (ABPS)
Curr. Mon. · Comparator

ADC

Analog Compute Engine
Sample Sequencing Engine

DAC (SDD)

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SCB
Temp. Mon. · Volt Mon. (ABPS)
Curr. Mon. · Comparator

ADC

Post Processing Engine

DAC (SDD)

SRAM · SRAM · SRAM .... SRAM · SRAM · SRAM

Legend:

SDD – Sigma-delta DAC

SCB – Signal conditioning block

PDMA – Peripheral DMA

IAP – In-application programming

ABPS – Active bipolar prescaler

WDT – Watchdog Timer

SWD – Serial Wire Debug

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