Military Grade SmartFusion Customizable System-on-Chip (cSoC)

Product Benefits
- 100% Military Temperature Tested and Qualified from –55°C to 125°C
- Not Susceptible to Neutron-Induced Configuration Loss

Microcontroller Subsystem (MSS)
- Hard 50 MHz 32-Bit ARM® Cortex™-M3
  - Fully Tested Across Military Temperature Range (–55°C to 125°C)
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth,¹ Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface²
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I²C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 from Data Transactions
- Clock Sources
  - 32 KHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; Up to 3% Accurate at Military Temperature
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA
- Based on proven ProASIC®3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
  - Secure ISP with 128-Bit AES via JTAG
  - FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog
- Analog Front-End (AFE)
  - Up to Three 12-Bit SAR ADCs
    - 500 Ksps in 12-Bit Mode
    - 550 Ksps in 10-Bit Mode
    - 600 Ksps in 8-Bit Mode
  - Internal 2.56 V Reference or Optional External Reference
  - One First-Order ΣΔ DAC (sigma-delta) per ADC
    - 12-Bit 500 Ksps Update Rate
  - Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
    - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5 V to –11.5/12 V) with 4% Accuracy
    - High Gain Current Monitor, Differential Gain = 50, up to 12 V Common Mode
    - Temperature Monitor (Resolution = ¼°C in 12-Bit Mode; Accurate from –55°C to 150°C)
  - Up to Ten High-Speed Voltage Comparators (t<sub>pd</sub> = 15 ns)

Analog Compute Engine (ACE)
- Offloads Cortex-M3-Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® Integrated Design (IDE) Software

I/Os and Operating Voltage
- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

¹ Theoretical maximum
² A2F500 devices

© 2012 Microsemi Corp.
# SmartFusion cSoC Family Product Table

<table>
<thead>
<tr>
<th>SmartFusion® cSoC</th>
<th>A2F060</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FPGA Fabric</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Gates</td>
<td>60,000</td>
<td>500,000</td>
</tr>
<tr>
<td>Tiles (D-flip-flops)</td>
<td>1,536</td>
<td>11,520</td>
</tr>
<tr>
<td>RAM Blocks (4,608 bits)</td>
<td>8</td>
<td>24</td>
</tr>
<tr>
<td><strong>Microcontroller Subsystem (MSS)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash (Kbytes)</td>
<td>128</td>
<td>512</td>
</tr>
<tr>
<td>SRAM (Kbytes)</td>
<td>16</td>
<td>64</td>
</tr>
<tr>
<td>Cortex-M3 with memory protection unit (MPU)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>10/100 Ethernet MAC</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>External Memory Controller (EMC)</td>
<td>24-bit address,16-bit data</td>
<td></td>
</tr>
<tr>
<td>DMA</td>
<td>8 Ch</td>
<td></td>
</tr>
<tr>
<td>I²C</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>SPI</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>16550 UART</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>32-Bit Timer</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>PLL</td>
<td>1</td>
<td>2¹</td>
</tr>
<tr>
<td>32 KHz Low Power Oscillator</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>100 MHz On-Chip RC Oscillator</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Main Oscillator (32 KHz to 20 MHz)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>Programmable Analog</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADCs (8-/10-/12-bit SAR)</td>
<td>1</td>
<td>3³</td>
</tr>
<tr>
<td>DACs (12-bit sigma-delta)</td>
<td>1</td>
<td>3³</td>
</tr>
<tr>
<td>Signal Conditioning Blocks (SCBs)</td>
<td>1</td>
<td>5³</td>
</tr>
<tr>
<td>Comparator²</td>
<td>2</td>
<td>10³</td>
</tr>
<tr>
<td>Current Monitors²</td>
<td>1</td>
<td>5³</td>
</tr>
<tr>
<td>Temperature Monitors²</td>
<td>1</td>
<td>5³</td>
</tr>
<tr>
<td>Bipolar High Voltage Monitors²</td>
<td>2</td>
<td>10³</td>
</tr>
</tbody>
</table>

**Notes:**
1. Two PLLs are available in FG484 (one PLL in FG256).
2. These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User’s Guide for details.
3. Available on FG484 only.
Package I/Os: MSS + FPGA I/Os

<table>
<thead>
<tr>
<th>Package</th>
<th>A2F060</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td>FG256</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Direct Analog Inputs</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>Shared Analog Inputs¹</td>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>Total Analog Inputs</td>
<td>15</td>
<td>24</td>
</tr>
<tr>
<td>Total Analog Outputs</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>MSS I/Os²,³</td>
<td>26⁴</td>
<td>25</td>
</tr>
<tr>
<td>FPGA I/Os</td>
<td>66</td>
<td>66</td>
</tr>
<tr>
<td>Total I/Os</td>
<td>108</td>
<td>117</td>
</tr>
</tbody>
</table>

Notes:
1. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.
2. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.
3. 9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.
4. 10/100 Ethernet MAC is not available on A2F060.

SmartFusion cSoC Device Status

<table>
<thead>
<tr>
<th>Device</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2F060</td>
<td>Preliminary</td>
</tr>
<tr>
<td>A2F500</td>
<td>Preliminary</td>
</tr>
</tbody>
</table>
Legend:

SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug
SmartFusion cSoC System Architecture

Note: Architecture for A2F200
### Product Ordering Codes

<table>
<thead>
<tr>
<th>A2F500</th>
<th>M3</th>
<th>F</th>
<th>1</th>
<th>FG</th>
<th>G</th>
<th>484</th>
<th>Y</th>
<th>M</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Application (junction temperature range)**
  - Blank = Commercial (0°C to +85°C)
  - I = Industrial (–40°C to +100°C)
  - M = Military (–55°C to 125°C)

- **Security Feature**
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

- **Part Number**

- **SmartFusion Devices**
  - A2F060 = 60,000 System Gates
  - A2F500 = 500,000 System Gates

- **Notes:**
  1. **C** = Commercial Temperature Range: 0°C to 85°C Junction
  2. **I** = Industrial Temperature Range: –40°C to 100°C Junction
  3. **M** = Military Temperature Range: –55°C to 125°C Junction

---

### Temperature Grade Offerings

<table>
<thead>
<tr>
<th>SmartFusion cSoC</th>
<th>A2F060</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td>FG256</td>
<td>C, I, M</td>
<td>C, I, M</td>
</tr>
<tr>
<td>FG484</td>
<td></td>
<td>C, I, M</td>
</tr>
</tbody>
</table>

---

**Notes:**

1. **C** = Commercial Temperature Range: 0°C to 85°C Junction
2. **I** = Industrial Temperature Range: –40°C to 100°C Junction
3. **M** = Military Temperature Range: –55°C to 125°C Junction

---

*Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*