Military Grade SmartFusion Customizable System-on-Chip (cSoC)

Product Benefits

- 100% Military Temperature Tested and Qualified from –55°C to 125°C
- Not Susceptible to Neutron-Induced Configuration Loss

Microcontroller Subsystem (MSS)

- Hard 50 MHz 32-Bit ARM® Cortex™-M3
  - Fully Tested Across Military Temperature Range (–55°C to 125°C)
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth,[1] Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface[2]
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I^2C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 from Data Transactions
- Clock Sources
  - 32 KHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; Up to 3% Accurate at Military Temperature
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA

- Based on proven ProASIC®3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog

Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
  - 500 Ksps in 12-Bit Mode
  - 550 Ksps in 10-Bit Mode
  - 600 Ksps in 8-Bit Mode
- Internal 2.56 V Reference or Optional External Reference
- One First-Order ΣΔ DAC (sigma-delta) per ADC
  - 12-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
  - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5 V to –11.5/12 V) with 4% Accuracy
  - High Gain Current Monitor, Differential Gain = 50, up to 12 V Common Mode
  - Temperature Monitor (Resolution = ¼°C in 12-Bit Mode; Accurate from –55°C to 150°C)
- Up to Ten High-Speed Voltage Comparators (t_{pd} = 15 ns)

Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® Integrated Design (IDE) Software

I/Os and Operating Voltage

- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

1 Theoretical maximum
2 A2F500 devices

SmartFusion cSoC Family Product Table

SmartFusion® cSoC		A2F060	A2F500
FPGA Fabric	System Gates	60,000	500,000
	Tiles (D-flip-flops)	1,536	11,520
	RAM Blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	512
	SRAM (Kbytes)	16	64
	Cortex-M3 with memory protection unit (MPU)	Yes	
	10/100 Ethernet MAC	No	Yes
	External Memory Controller (EMC)	24-bit address,16-bit data	
	DMA	8 Ch	
	I^2C	2	
	SPI	2	
	16550 UART	2	
	32-Bit Timer	2	
	PLL	1	2[1]
	32 KHz Low Power Oscillator	1	
	100 MHz On-Chip RC Oscillator	1	
	Main Oscillator (32 KHz to 20 MHz)	1	
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	3[3]
	DACs (12-bit sigma-delta)	1	3[3]
	Signal Conditioning Blocks (SCBs)	1	5[3]
	Comparator[2]	2	10[3]
	Current Monitors[2]	1	5[3]
	Temperature Monitors[2]	1	5[3]
	Bipolar High Voltage Monitors[2]	2	10[3]

Notes:

1. *Two PLLs are available in FG484 (one PLL in FG256).*
2. *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.*
3. *Available on FG484 only.*

Package I/Os: MSS + FPGA I/Os

Device	A2F060	A2F500	
Package	**FG256**	**FG256**	**FG484**
Direct Analog Inputs	11	8	12
Shared Analog Inputs[1]	4	16	20
Total Analog Inputs	15	24	32
Total Analog Outputs	1	2	3
MSS I/Os[2,3]	26[4]	25	41
FPGA I/Os	66	66	128
Total I/Os	108	117	204

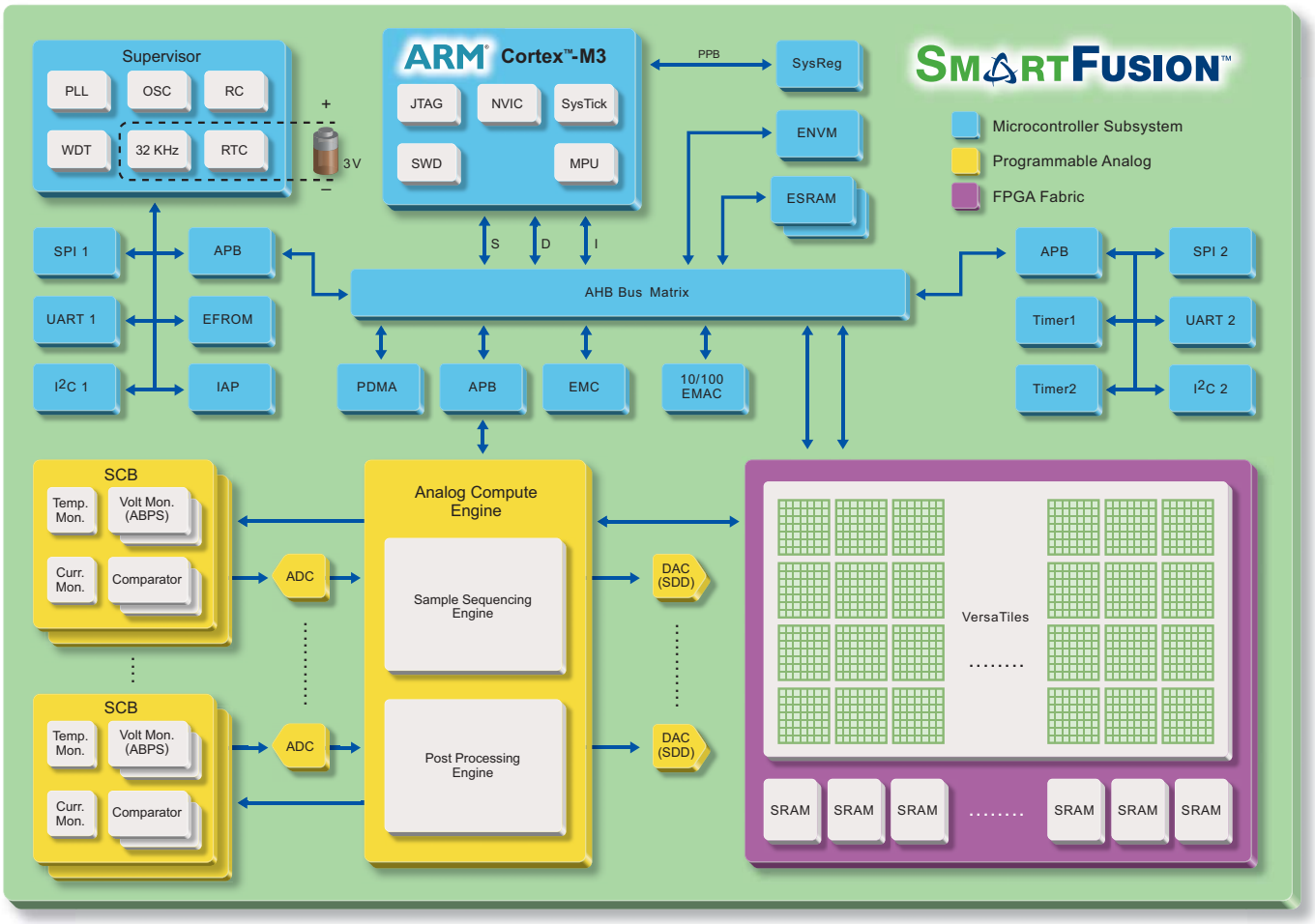
Notes:

1. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
2. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
3. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
4. *10/100 Ethernet MAC is not available on A2F060.*

SmartFusion cSoC Device Status

Device	Status
A2F060	Preliminary
A2F500	Preliminary

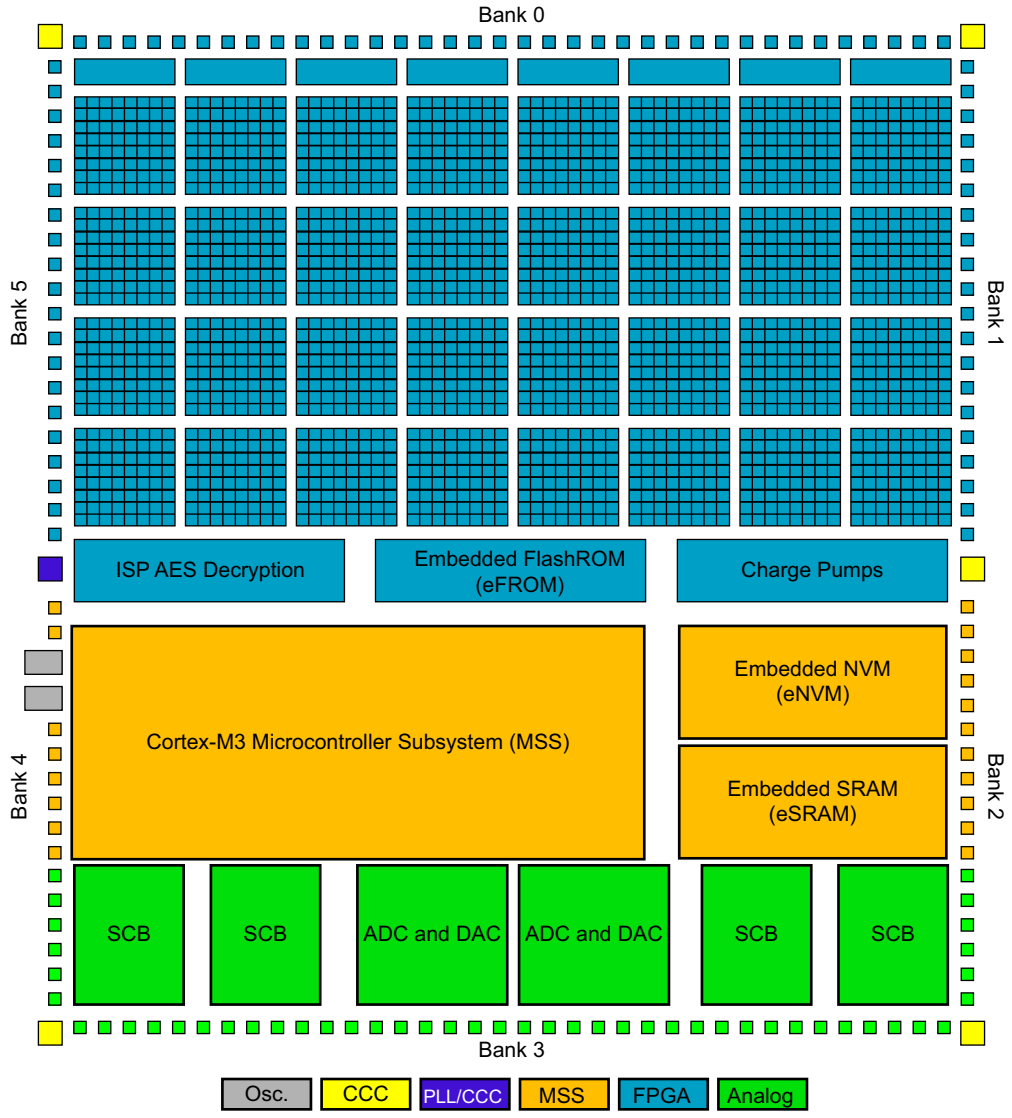
SmartFusion cSoC Block Diagram



Legend:

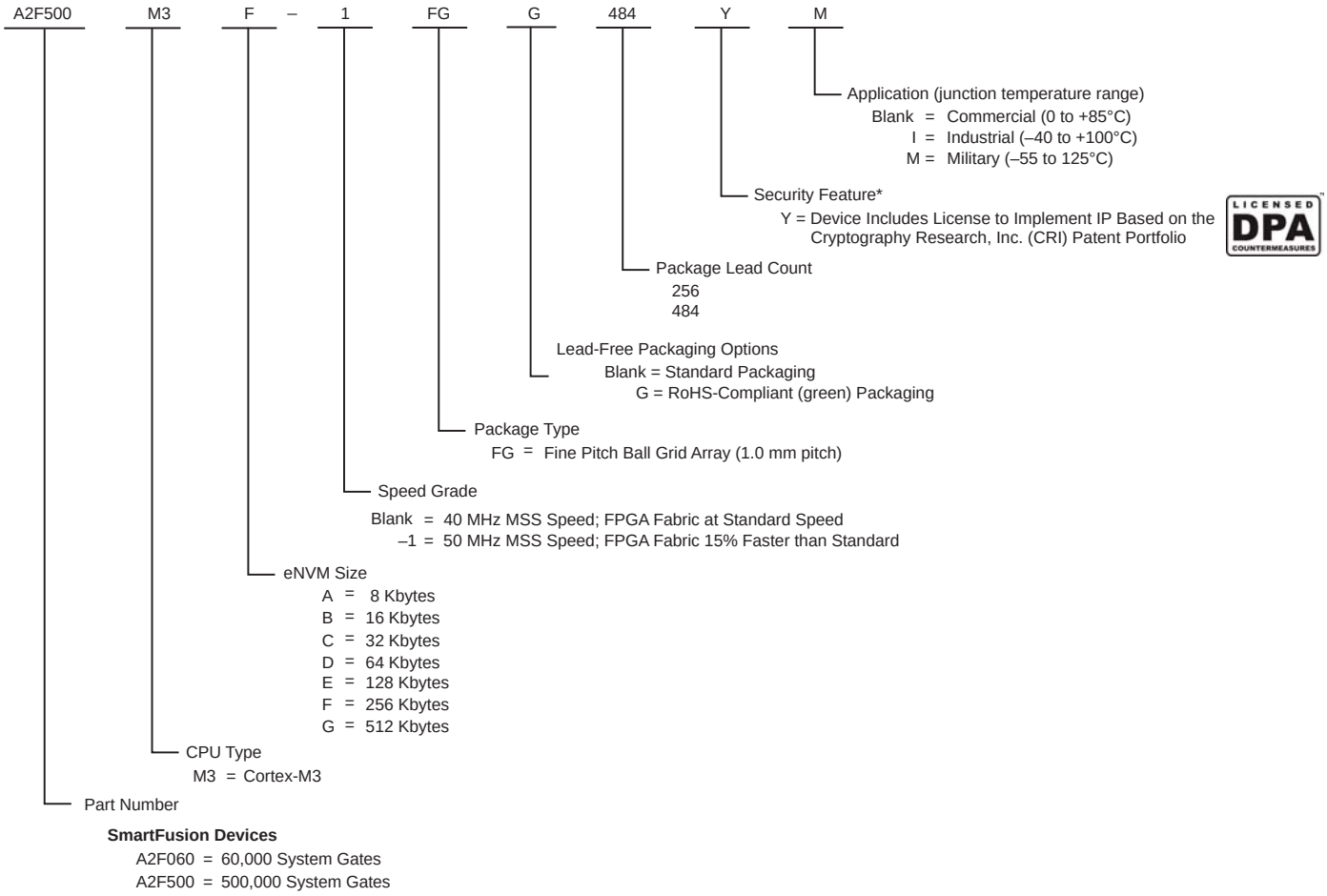
SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

SmartFusion cSoC System Architecture



Note: Architecture for A2F200

Product Ordering Codes



*Note: *Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*

Temperature Grade Offerings

SmartFusion cSoC	A2F060	A2F500
FG256	C, I, M	C, I, M
FG484	–	C, I, M

Notes:

1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*
3. *M = Military Temperature Range: –55°C to 125°C Junction*

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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