

# Technical Data for

# FS2 On-Chip Logic Navigator System for Actel FPGA Devices

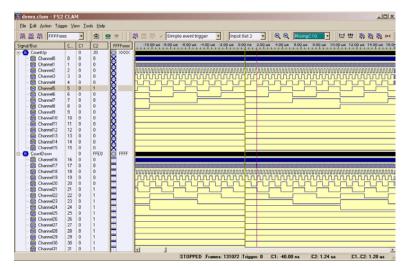
The FS2 Logic Navigator<sup>™</sup> is an On-Chip Instrumentation (OCI<sup>®</sup>) trace and debug tool that provides logic analysis capability to Actel FPGA internal logic. It supports Actel<sup>®</sup> Flash based FPGAs, including ProASIC and ProASIC<sup>PLUS</sup>, and Antifuse devices (MX, SX, and AX) providing an intuitive and easy way to view internal signals and debug the logic design. It can simultaneously trace and trigger on up to 256 signals in the FPGA fabric with support for up to 4096 total nodes during the debug session. Logic Navigator utilizes a FlashPro or FlashPro Lite programmer to interface with the Actel target system.

# Logic Navigator System Overview

The Logic Navigator system is highly configurable to allow the user to customize and balance features against available logic cells and on-chip resources. The user can easily generate the analyzer system logic using the FS2 OCI Generator tool that is included with the Logic Navigator product. OCI Generator automates creation of the OCI and integrates the code into the Verilog or VHDL design files that are then implemented in the FPGA. Logic Navigator is compatible with Actel Libero synthesis, place and route programming design flows for Actel devices. Up to 4096 signals (configured as 16 input sets of 256 channels each) can be defined for triggering and trace, depending on available on-chip logic resources. During the debug session, the user may select any one of the input sets for monitoring. The selected channels are fed into the triggering and trace capture system. Input set selection and trigger patterns can be easily selected in the graphical user interface (GUI) or in the Tcl/tk based command line interface. Trace capture results are displayed as a waveform in the GUI or output as text in the console.

#### Features Overview

- Based on FS2 On-Chip Instrumentation (OCI<sup>®</sup>) technology for trace and triggering on signals in the Actel FPGA device
- User configurable logic analysis of any nodes within the Actel ProASIC, ProASICPLUS, MX, SX, and AX devices
- Supports level or edge / level triggering. Trigger conditions include high, low, don't care, rising, falling.
- Pre, center, post, or user defined trigger positioning
- Trace storage qualification actions: trace on/off, trace single (one frame)
- Graphical User Interface (GUI) with logic analyzer style waveform display and text output options
- Command-line interface window with Tcl scripting
- Configurable trace and trigger options to optimize for device logic area utilization
- OCI JTAG interface with APA Flash based UJTAG or dedicated JTAG TAP interface for AX parts with TAP controller
- Uses Actel FlashPro or FlashPro Lite for target connection
- OCI Generator to quickly configure OCI logic block options and generate and instantiate analyzer logic code
- Analyze up to 4096 nodes
- Supports up to 16 input sets x 256 bits
- Up to 64K frames trace buffer based on available RAM
- Up to 16 triggers with up to 16 levels (states) of sequencing
- Optional variable width timestamp of up to 48 bits
- Up to 2 optional 32-bit counters
- Up to 32 optional external trigger interfaces
- Optional variable width general purpose register that can be wired to user logic



**Logic Navigator User Interface** 

# Triggering System

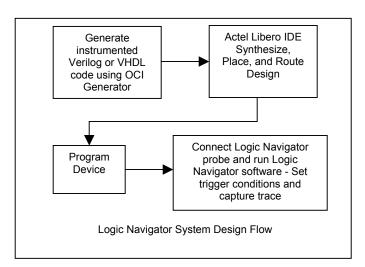
Events are defined by ANDing of up to 256 channels of pattern matching, where each channel can be programmed to recognize a high, low, don't care, rising, falling or either edge pattern. Complex sequential event recognition is supported using state and counter resources. If an event match occurs, user-selectable actions are taken. Available actions include: trigger; pulse or set level of output trigger; change trigger state; increment, clear, start, or stop the event counter; start/stop trace collection; or collect one trace frame for that event. The Logic Navigator supports up to 16 events with up to 16 levels (states) of triggering. Event matches can be combined with OR-IF statements. Trigger position is user adjustable.

#### Real Time Trace

The on-chip Logic Navigator supports up to 256 channels and a maximum of 64K frames. On-chip logic and RAM requirements will depend on width of the trace buffer (1-256 bits), number of events (2,4,8,16) and depth. As an example of RAM utilization, a 16-channel configuration of 1K frames depth would require 8 (256x9) RAM blocks.

# Typical Design Flow and Tools Required

Logic Navigator works seamlessly with the design flow and tools provided by the Actel Libero IDE.



## Graphical User Interface

Logic Navigator trace data is viewed in a logic analyzer style waveform or state display on the PC host. A tool bar and system of Windows panes and dialogs provide an intuitive and fast way to configure triggers and trace capture options.

# Command line interface

Logic Navigator also includes a command line interface (CLI). The CLI can be used to configure all functions and output data in ASCII format. It can also be used for writing automated sequences of functions for repetitive tests. The CLI is based on the widely used Tcl/tk command and scripting language.

# Software Supplied

Software provided includes the Logic Navigator User interface (GUI), command line interface (CLI), and OCI Generator for configuring, generating, and integrating the Logic Navigator OCI into user RTL. FS2 provides Logic Navigator IP and RTL design examples in Verilog and VHDL. A Simulation and Synthesis Guide, OCI Generator manual and Getting Started manual are included.

# Requirements

Requires Actel FlashPro or FlashPro Lite for interface to target system and Pentium class PC with minimum 32 M bytes of memory, parallel port or USB port depending on FlashPro configuration, and Windows® 98/NT/2000/XP operating system. Requires Actel Libero tools, which include Modeltech ModelSim and Synplicity Synplify Light.

# **Product Codes**

LNAV-ACTEL Logic Navigator System with on-chip trace support for use with Actel FlashPro or FlashPro Lite



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