Functional Failure Analysis Service

For Flash FPGAs

Failure Analysis Overview

Actel is committed to providing highly reliable FPGAs to commercial and HiRel customers, alike. This is achieved, in part, by performing very detailed analysis of failed products returned from users of Actel's FPGAs. Actel's failure analysis service has been engineered to find the root cause of failures efficiently and effectively.

Initiating a Failure Analysis

Failure analysis (FA) requests are first initiated through the Corporate Applications Group Technical Support hot line (tech@actel.com or (800) 262-1060). Once the case is confirmed to be a valid functional FA, it is escalated to the Applications Consulting Group, where a highly trained Applications Consulting Engineer (typically 5-15 years experience) works with the customer and Field Applications Engineer (FAE) to understand the failure mode completely.

Depending on the failure mode, the FAE may recommend using a logic debugger such as the FS2 Logic Navigator®, or Synplicity's Identify® to isolate the fault within the FPGA. The FAE will also evaluate the design implementation to check for potential timing errors and software bugs, verify the correct tool settings, and guide the customer in collecting important details about the failure mode. Flash FPGAs are reprogrammable (security settings permitting), so test designs can be programmed into the FPGA to further help isolate the failure.

If no timing, design, or usage errors are found in Applications Consulting, the issue is further escalated to a silicon FA specialist in Product Engineering.

Procedure to Initiate the FA Process

The steps for initiating an FA process are:

1. Contact Actel's Technical Support Team or your local Actel FAE or distributor to report the failure (www.actel.com/contact/info.html).
2. Complete a Functional Failure Checklist and provide all necessary design files and test vectors required to simulate the reported failure mode. (The Technical Support team will provide the Functional Failure Checklist. The checklist is also available on the FA web page at www.actel.com/custsup/fa.)

3. Devices can only be shipped back to Actel upon approval and issuance of a case number. Devices shipped to Actel prior to explicit approval by an Applications Engineer may be immediately shipped back to the customer. Shipping instructions can be found on the FA web page at www.actel.com/custsup/fa.

Failure Analysis Techniques

The following silicon FA techniques are employed to determine the root cause of the failure for Actel's flash-based FPGAs:

Visual Inspection

The device is inspected to check for signs of the following:

- Broken/bent/damaged leads
- Remains of solder
- Epoxy residue

Since most of the testing performed during the FA is done using adapter modules, the device package must be in excellent condition. Actel strongly recommends that users remove devices carefully from the PCB. The *Device Removal Instructions* Technical Brief (located at http://www.actel.com/documents/DeviceRemovalInst_AN.pdf) provided by Actel offers several suggestions to extract devices cleanly. In the case of units in Ceramic Quad (CQ) packages, field returns are generally removed from their lead frames and the additional step of soldering the device onto a new lead frame is required to facilitate testing. Pictures are taken of the failed device in the received condition. If necessary, the device is reworked before testing.

Images of a CQ device taken before and after re-work are shown in Figure 1.

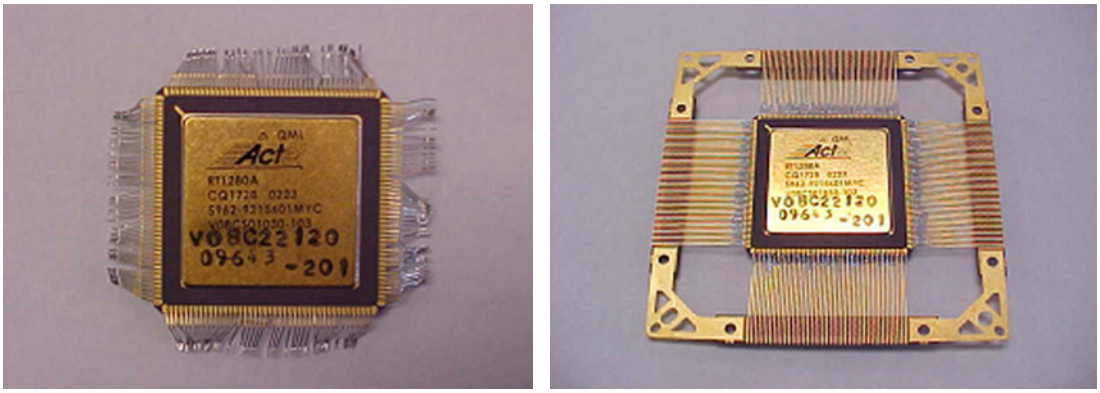

Figure 1: Images of a CQ Device Before and After Reworking

Programming Verification

All of Actel's devices have a unique checksum associated with each design. Actel's Silicon Sculptor and FlashPro programmers are used to read the checksum of the device to determine if the checksum read back corresponds with the expected design checksum. This step ensures that the returned device is programmed with the correct design. Actel then performs the Verify function to confirm all flash cells are properly programmed. This function checks erased and programmed cells against a particular voltage to ensure complete programming.

Margin Test

Margining is a process of sweeping the control gate voltage on each of the Non-Volatile Memory (NVM) switches within the FPGA. The control gate voltage level that turns on each NVM switch in the device is recorded across the entire voltage sweep. This data is then compared to margin data of a reference device for any differences. Differences between the subject device and the reference will indicate whether switches have lost or gained charge on the floating gate.

NVM Test

This test is performed by reprogramming the FPGA with various patterns to check the ability of all the flash cells to hold both programmed and erased states. This is performed in addition to the Verify function, which checks if the customer's design is programmed properly into the device.

Functional Verification and Fault Isolation

Devices are subject to a set of functional test patterns to achieve maximum test coverage. In each test pattern, the device is programmed with a different design, and outputs are compared to the expected results for the corresponding input vectors. This functional test routine is one of Actel's manufacturing tests, so a failure in one of the test patterns indicates a change in the silicon characteristics since the time of shipment.

While the functional test patterns may detect the presence of a silicon fault, they do not always identify location or cause of failure. Actel has the capability to apply a custom set of vectors to reproduce and debug failures on Automated Test Equipment (ATE) testers. This step of the Failure Analysis process requires test vectors for the customer's design. These test vectors are used to generate a functional test program that simulates a reported functional failure mode. Guidelines for generation of the test vectors in the format required by Actel's ATE are available in the application note *Test Vector Guidelines* (located at www.actel.com/documents/TestVector.pdf.

Final Test

Devices are later subjected to Final Test. This is the same test that is used to electrically screen devices prior to shipment. The Final Test is an Actel-specific screening process used in the regular production flow of flash products. It checks for DC parametric types of failures such as pin-to-pin continuity, shorts, excessive standby currents, gross IDD, and tri-state leakage. The device must be reprogrammed in order to perform Final Test.

Continuity (Both Open and Shorts):

Devices that fail continuity may have delamination, bond wire damage, or Electrostatic Discharge (ESD) damage to the I/O. Failures may be verified using CMode Scanning Acoustic Microscopy (CSAM) and X-Ray Analysis, and by Curve Tracing the failing I/O. Figure 2 shows delamination (observed using CSAM) caused by operation of a device outside Actel's recommended operating conditions. The color red indicates areas with large delamination.

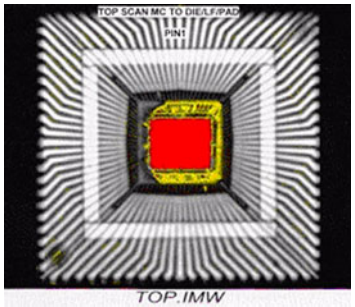

Figure 2: Example of Device Delamination Observed with CSAM

Standby Idd:

Devices failing this test generally exhibit failures caused either by ESD or Electrical Over Stress (EOS). Localization of circuitry generating the high standby Idd is done by Photo Emission, Liquid Crystal, or Thermally Induced Voltage Alteration (TIVA). Figure 3 shows high standby Idd regions localized using Photo Emission, Liquid Crystal, and TIVA.

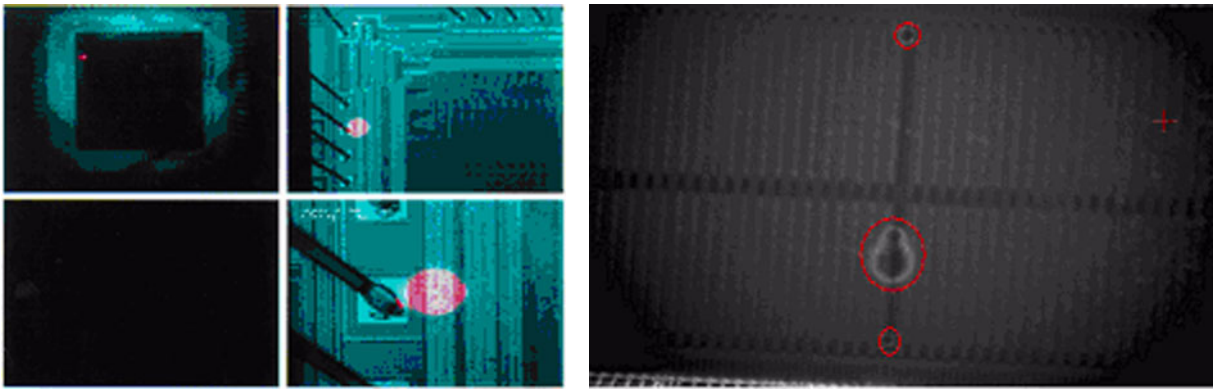

Figure 3: Photo Emission (Left) and Liquid Crystal (Right)

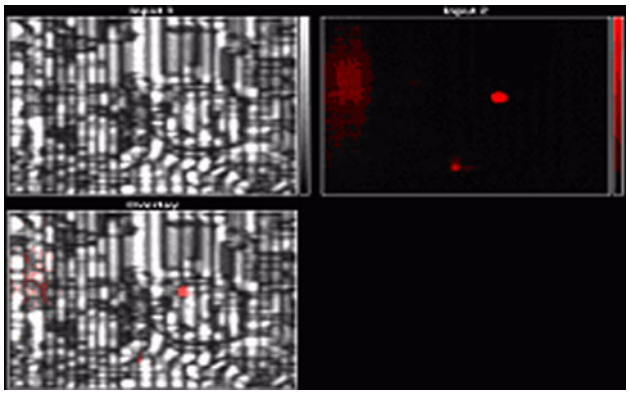

Figure 4: Failure Analysis Techniques Used to Localize Regions of High Standby Idd

Tri-State Leakage:

Indicates failure on an I/O, generally caused by EOS.

Micro Probing

After a functional failure is isolated to a particular logic module, additional localization of the failure may be performed using Focused Ion Beam (FIB) pads. The FIB pads facilitate micro- or pico-probing of a device and provide access to inputs and outputs of transistors within a suspect logic module. An image of a device after the addition of FIB pads is shown in figure Figure 5 on page 5.

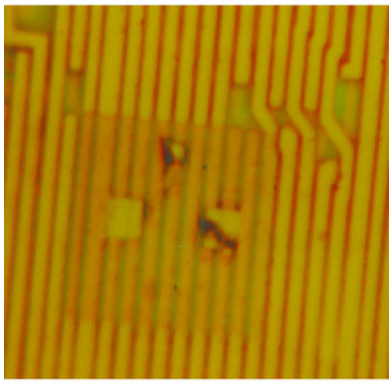

Figure 5: FIB Pads Added to Top Metal Layer of Device

Deprocessing

If a failure has been localized to a particular transistor or group of transistors using the steps outlined above, the failure region is deprocessed and the results correlated to the reported failure mechanism. Deprocessing images showing EOS-type damage induced by voltage spiking experiments are shown in figure Figure 6.

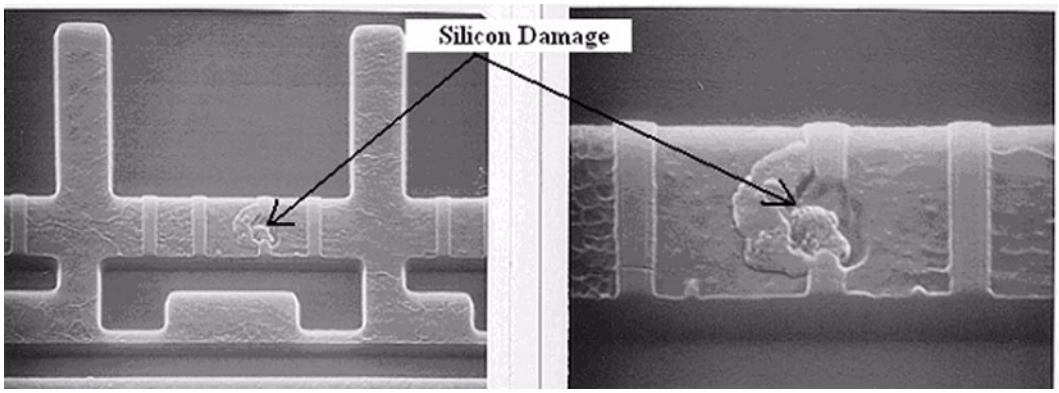

Figure 6: Deprocessing Images Showing Silicon Damage Induced by EOS

Completion of Failure Analysis

At the completion of the failure analysis, Actel will issue the customer a formal report providing details of the work that has been performed and any conclusions that can be made. Actel encourages questions to be asked and prefers to receive confirmation that the customer accepts the final report and conclusions. However, if no feedback is received within two weeks, the FA is automatically closed.

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