Functional Failure Analysis Service

For Antifuse FPGAs

Failure Analysis Overview

Actel is committed to providing highly reliable FPGAs to commercial and aerospace customers. This is partially achieved by performing very detailed analyses of product failure returns from users of Actel's FPGAs. Actel's failure analysis service has been engineered to find the root cause of failures efficiently and effectively.

Failure analysis (FA) requests are first initiated through the Technical Support Hotline (tech@actel.com). Once the case is confirmed to be a valid functional FA, it is escalated to the Applications Consulting Group, where a highly trained applications engineer (typically 5–15 years of experience) works with the customer and a field applications engineer (FAE) to understand the failure mode completely. The applications engineer will also evaluate the design implementation to check for potential timing errors or software bugs. He will also verify the correct tool settings, and will guide the customer to collect important details about the failure mode, such as the use of Silicon Explorer (www.actel.com/products/tools/siliexp/index.html.) The Silicon Explorer tool is unique to Actel antifuse FPGAs, and provides real-time observation of most internal nodes in the design while the device is being driven by its normal external inputs. No re-layout is necessary, and Silicon Explorer does not add any loading to the design (i.e., it does not affect timing).

If no timing, design, or usage errors are found by the Applications Consulting Group, the issue is further escalated to a silicon FA specialist in Product Engineering. The following silicon FA techniques are employed to determine the root cause of the failure for Actel's antifuse devices.

1. Visual Inspection

The device is inspected to check for signs of the following:

- Broken/ bent/ damaged leads
- Remains of solder
- Epoxy residue

Since most of the testing performed in the FA is done using adapter modules, the device package must be in excellent condition. Actel strongly recommends that users remove devices carefully from the PCB. The *Device Removal Instructions Technical Brief* provided by Actel offers several suggestions to extract devices cleanly. This document can be found on the FA web page at www.actel.com. The two package types that generally require rework at an outside laboratory prior to additional testing are the Ceramic Quad (CQ) packages and the Ball Grid Array (BGA) packages. In the case of units in Ceramic Quad (CQ)

packages, field returns are removed from their lead frames and the additional step of soldering the device onto a new lead frame is required to facilitate testing. Pictures are taken of the failure device in the received condition, and the device is reworked before testing. Images of a CQ device taken before and after reworking are shown in Figure 1. BGA devices removed from a PCB board tend to be in extremely poor condition after removal from a PCB board, and re-balling of the device is required before further testing. Figure 2 shows the bottom view of a BGA package before and after re-balling.

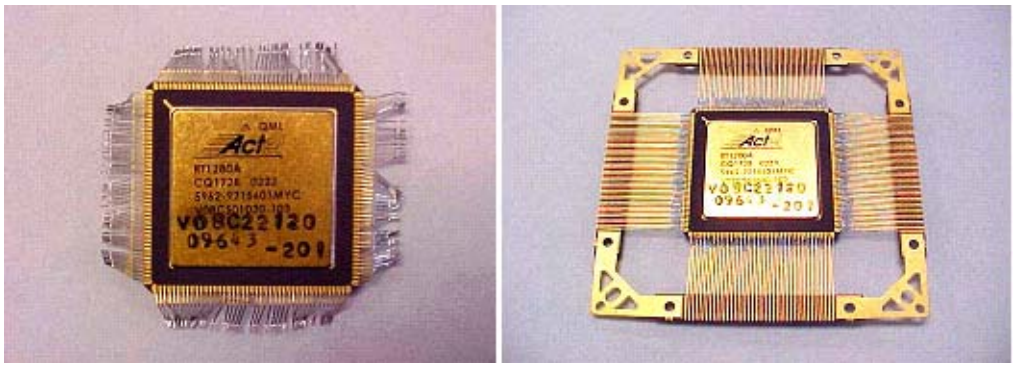

Figure 1: Images of a CQ Device before and after Reworking

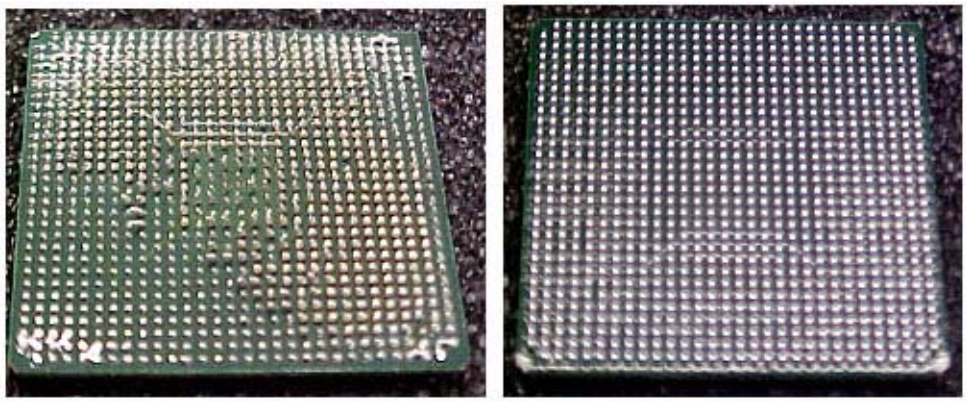

Figure 2: Bottom View of BGA Device before and after Re-Balling

2. Programming Verification

All of Actel's antifuse devices have a unique four-digit hexadecimal checksum associated with each design. Actel's Silicon Sculptor programmer is used to read the checksum of the device to ascertain whether the checksum that is read back corresponds with the expected design checksum. This step ensures that the returned device was programmed with the correct design.

3. DC Parametric Testing

All returned devices are subject to a post-programming test (PPT) that evaluates the following:

- **Continuity (both open and shorts):**

  Devices that fail continuity may have delamination, bond wire damage, or electrical overstress (EOS) damage to the I/O. Failures are verified using cmode scanning acoustic microscopy (CSAM) and x-ray analysis, and by curve-tracing the failing I/O. Figure 3 on page 3 shows delamination (observed using CSAM) caused by operation of the device outside of Actel's recommended operating conditions.

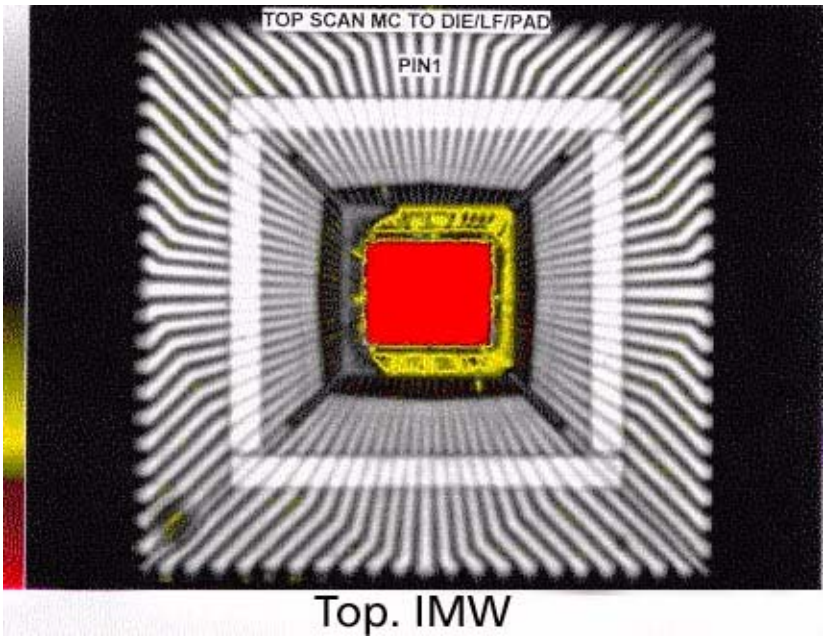

Figure 3: Delamination on Device Observed with CSAM

- **Standby IDD:**

  Devices failing this test generally exhibit failure caused either by electrical overstress (EOS) or electrostatic discharge (ESD). Localization of circuitry that generates high standby IDD is done by photoemission, liquid crystal, or thermally-induced voltage alteration (TIVA). Figure 4 on page 4 shows high standby IDD regions localized using photoemission, liquid crystal and TIVA.

- **Tristate leakage:**

  In this test, the pull-up and pull-down drivers are verified for leakage current. The I/Os are tristated, then the pins are externally pulled up and down, and corresponding leakage currents are measured. Failure on an I/O generally indicates EOS damage.

4. Functional Verification and Isolation of Failing Macro with Silicon Explorer

This step of the failure analysis process requires the customer's test vectors. These test vectors are used to generate a functional test program that stimulates a reported functional failure mode. Guidelines for generation of the test vectors in the format required by Actel's ATE are available at www.actel.com/documents/TestVector.pdf.

After isolating the functional failure to a single output or group of outputs, Actel's Silicon Explorer tool (www.actel.com/products/tools/siliexp/index.html) is utilized to isolate the failure to a single logic macro. Silicon Explorer provides real-time access to the internal nets of an Actel antifuse device. Internal nets can be accessed at any given time via the Silicon Explorer Probe A and Probe B circuitry unless the security fuse is programmed on the device.

Figure 5 on page 4 shows part of the schematic corresponding to a functionally failing output pin (pin #10 was confirmed to exhibit a stuck-at-low type fault using a functional test program generated from the customer's test vectors). The corresponding scope plots of the internal nets obtained on a control and failure unit via Probe A and Probe B of Silicon Explorer are provided in Figure 6 on page 5.

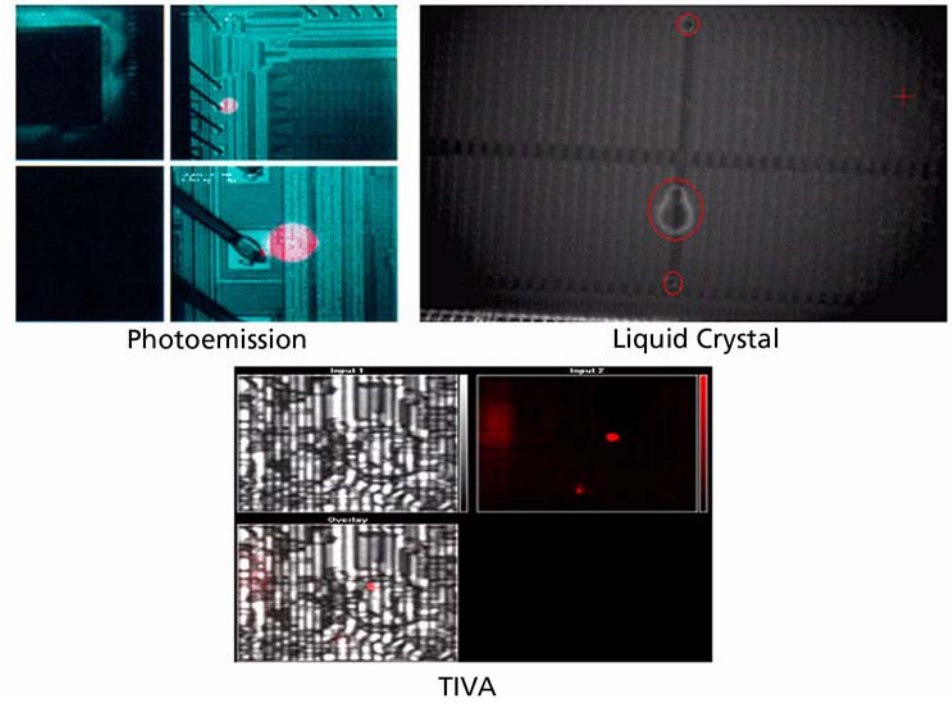

Figure 4: Failure Analysis Techniques Used to Localize Regions of High Standby IDD

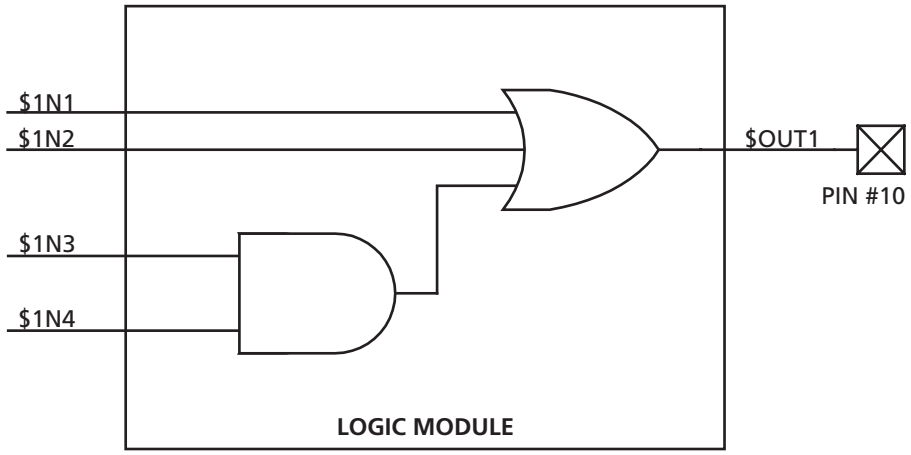

Figure 5: Example of Internal Nodes Accessible through Silicon Explorer

Using Silicon Explorer, it is possible to isolate a functional failure down to a single logic module.

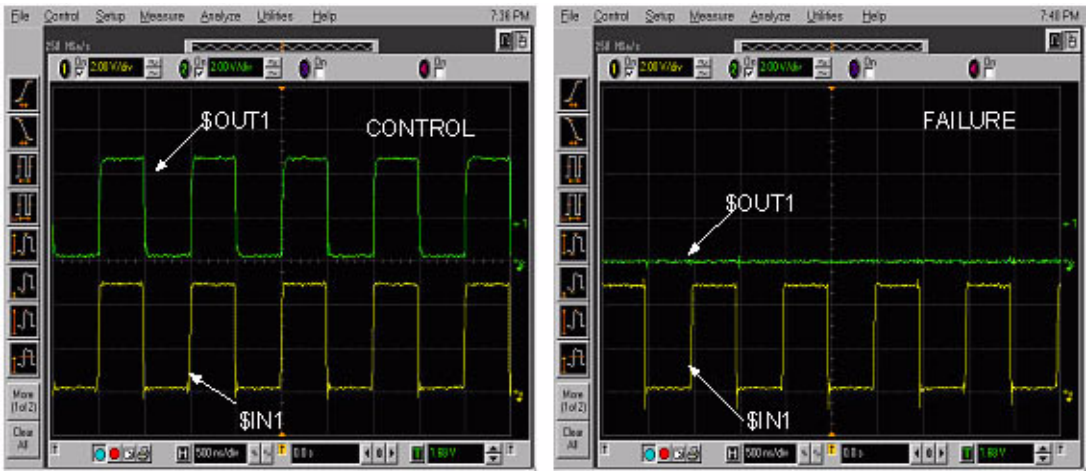

Figure 6: Typical Scope Plots Obtained with Silicon Explorer for the Design of Figure 5

5. Micro-Probing

After a functional failure is isolated down to a particular logic module using Silicon Explorer, additional localization of the failure is performed using focused ion beam (FIB) pads. The FIB pads facilitate micro- or pico-probing of a device and provide access to inputs and outputs of transistors within a suspect logic module. Images of a device after the addition of FIB pads are shown in Figure 7.

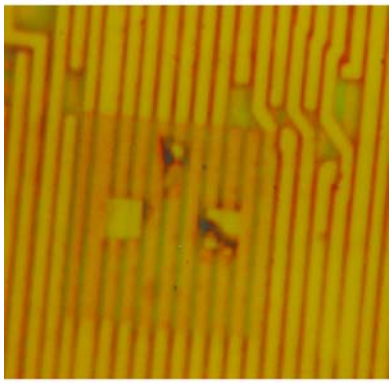

Figure 7: FIB Pads Added to Top Metal Layer of Device

6. De-Processing

When a failure has been localized down to a particular transistor or group of transistors using one or more of the steps outlined above, the failure region is de-processed and the results correlated to the reported failure mechanism. De-processing images showing EOS-type damage induced by voltage spiking experiments are shown in Figure 8 on page 6.

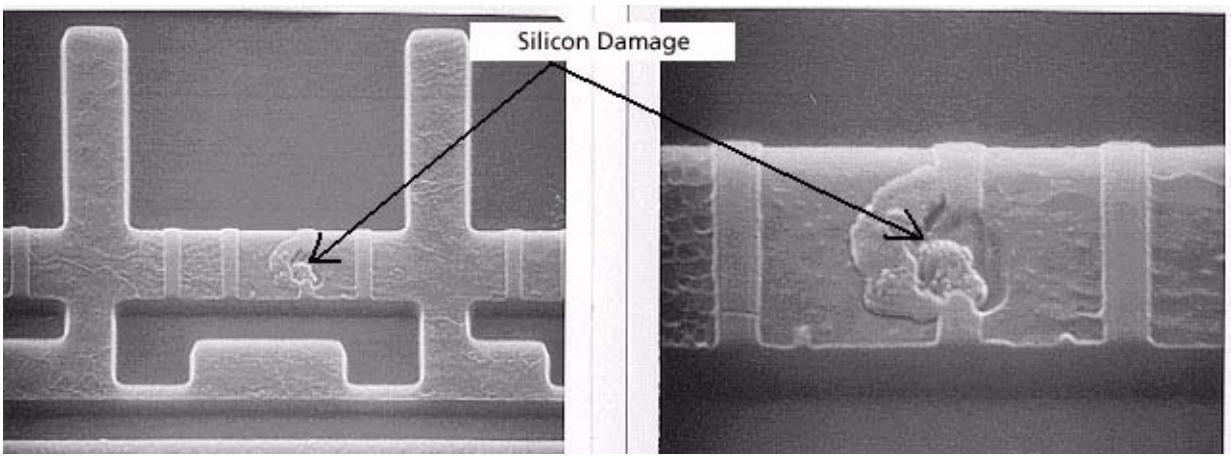

Figure 8: De-processing Images Showing Silicon Damaged Induced by EOS

Procedure for Initiation of FA Process

The list of steps for initiating an FA process is detailed below:

1. Contact Actel's Technical Support Team to report the failure (see www.actel.com/contact/info.html).
2. Complete a Functional Failure Checklist and provide all necessary design files and test vectors required to stimulate reported failure mode. Actel's technical support team will provide the checklist, or it can be printed from the FA web page at www.actel.com.
3. Devices can only be shipped back to Actel upon approval and issuance of a case or RMA number (RH/RT only). Shipping instructions can be found on the FA web page at www.actel.com.

For more information, visit our website at **http://www.actel.com**

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