Innovative Intelligent Integration

SmartFusion® System-on-Chip (SoC) devices integrate an FPGA, an Arm® Cortex®-M3 processor and programmable analog, offering full customization, IP protection and ease-of-use. Based on Microchip’s proprietary Flash process, SmartFusion SoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function Microcontrollers (MCU), without the excessive cost of soft processor cores on traditional FPGAs.

Key Benefits of SmartFusion SoCs

**Full Design Customization**
- Create a product with exactly the features you need
- Innovate and differentiate for a competitive edge
- Incorporate last-minute changes with an on-chip FPGA
- In-application Programming (IAP) capability for field upgrades
- Experiment with hardware acceleration for select algorithms in FPGA fabric

**Intellectual Property (IP) Protection**
- Interface between microcontroller and FPGA not exposed at board level
- No bitstream exposed at power-up
- Encrypted In-System Programming (ISP) with 128-bit AES via JTAG
- FlashLock® controls access to the security setting on the device
- Protection against overbuilding with customer programmable device key

**Ease-of-Use Increases Productivity**
- A single platform for your entire line of products
- Integrated design environment for both FPGA and embedded designers
- Simple GUI-based configuration of complex programmable analog
- Industry leading compile and debug from Keil, IAR and GNU
- Real-Time Operating System (RTOS) and middleware compo-
nents from Micrium, RoweBots, Emcraft and more
SmartFusion SoC FPGA offers 2K and 6K LE families with hard 100 MHz 32-bit Arm Cortex-M3. SmartFusion SoC FPGAs are ideal for hardware and embedded designers who need a true SoC solution that gives more flexibility than traditional fixed-function MCUs without the excessive cost of soft processor cores on traditional FPGAs.

**SmartFusion Architecture**

SmartFusion® SoC FPGA

- Supervisor
- PLL
- OSC
- RC
- WDT
- 32 kHz
- RTC
- Arm® Cortex®-M3
- JTAG
- NVIC
- SysTick
- SWD
- MPU
- SPI #1
- UART #1
- I2C #1
- APB
- EFRom
- PC #1
- IAP
- PDMA
- APB
- EMC
- 10/100 Ethernet MAC
- APB
- ESRAM
- Timer #1
- UART #2
- Timer #2
- PC #2

**Microcontroller Subsystem**

- Hardware industry-standard 100 MHz, 32-bit Arm Cortex-M3 CPU
- Multi-layer AHB communication matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC with RMII interface
- Two of each: SPI, I2C, UART, 32-bit timers
- Up to 512 KB Flash and 64 KB of SRAM
- External Memory Controller (EMC)
- 8-channel DMA controller
- Up to 41 MSS I/Os with Schmitt trigger inputs
- 25 I/Os can be used as FPGA I/Os

**Programmable Analog**

- High-performance analog Signal Conditioning Blocks (SCB) with voltage, current and temperature monitors
- Analog Compute Engine (ACE) offloads CPU from analog initialization and processing of Analog-to-Digital Conversion (ADC), Digital-to-Analog Conversion (DAC) and SCBs
- Integrated ADCs and DACs with 1% accuracy
- 12-/10-/8-bit mode ADCs with 500/550/600 Ksps sampling rate
- Up to ten 15 ns high-speed comparators
- Up to 32 analog inputs and 3 outputs

**FPGA Fabric**

- Based on proven ProASIC3 architecture
- 200,000 to 500,000 system gates with 350 MHz system performance
- Embedded SRAMs and FIFOs
- Variable aspect ratio 4,608-bit SRAM blocks
- ×1, ×2, ×4, ×9 and ×18 organizations
- True dual-port SRAM (including ×18)
- Up to 128 FPGA I/Os supporting LVDS, PCI, PCI-X and LVTTL/LVC-MOS standards

**No-Compromise**

**Microcontroller Subsystem (MSS)**

- Hardware industry-standard 100 MHz, 32-bit Arm Cortex-M3 CPU
- Multi-layer AHB communication matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC with RMII interface
- Two of each: SPI, I2C, UART, 32-bit timers
- Up to 512 KB Flash and 64 KB of SRAM
- External Memory Controller (EMC)
- 8-channel DMA controller
- Up to 41 MSS I/Os with Schmitt trigger inputs
- 25 I/Os can be used as FPGA I/Os
Designing with SmartFusion cSoCs

Designing with SmartFusion SoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity. Microchip has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project.

- **FPGA Design**—Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with low-power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.

- **Embedded Design**—Microchip offers FREE SoftConsole Eclipse-based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microchip also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

- **Analog Design**—The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA and embedded designers so device configuration can be easily shared between multiple developers.

**MSS Configuration**

- Configure the MSS peripherals and I/Os during embedded system design.
- Create or view hardware configuration in FPGA design flow.
- Create or import hardware configuration in embedded design flow.
- Automatically generate drivers for peripherals or soft IP.
- Configure programmable analog components.
- Connect FPGA fabric designs and IP to MSS.

---

**Microcontroller Subsystem (MSS)**

- **Clock Management**
- **Cortex®-M3**
- **ESRAM**
- **ENV**
- **External Memory Controller**
- **AHB Bus Matrix**
- **ACE**
- **PDMA**
- **UART_0**
- **UART_1**
- **SPT_0**
- **SPT_1**
- **T2C_0**
- **T2C_1**
- **GPIO**
- **MAC**
- **GPD**
- **EE PROM**
- **RTC**

**MSS Interface to SmartFusion FPGA Fabric Blocks**

**Hardware Interfaces**

FlashPro4, ULINK, J-LINK
Microchip has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver optimum usability and productivity to customers. Taking the same approach with processor development, Microchip has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microchip is partnering with Keil and IAR to provide software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by existing embedded developers. The learning path is straightforward for FPGA designers.

As an Arm processor was chosen for SmartFusion SoCs, you can benefit from the extensive Arm ecosystem. By building on supplied HAL and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion devices.

The diagram above shows the SmartFusion stack with examples of drivers, RTOS and middleware from Microchip and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

---

### Operating System

**Micrium**

Offers their μC/OS-III™ and μC/OS-II™ to support SmartFusion devices and includes a TCP/IP stack.

**Keil**

Includes the RTX Kernel in their standard MDK software and sources can also be purchased in an additional module along with TCP/IP.

**RoweBots**

Delivers their ultra tiny Linux® compatible RTOS Unison, consisting of a set of modular software components.

**Emcraft**

Developed the first uCLinux® offering for SmartFusion, along with their own embedded development platform.

**FreeRTOS**

Microchip has ported the FreeRTOS Kernel to SmartFusion and demonstrates this as a webserver reference design, included with both the SmartFusion evaluation and development kits.
Industrial Automation

The range of peripherals offered for the Cortex-M3 processor and the flexibility of SmartFusion FPGA fabric make the device ideal for industrial automation. The SmartFusion Development Kit supports Ethernet, EtherCAT, CAN, UART, I2C and SPI hardware, while firmware can be used for various other interface standards such as Modbus® and PROFIBUS for industrial networking. With the availability of programmable analog for sensing and analog outputs, SmartFusion SoCs can also be used in industrial control applications, including gateways, sensing, actuators and I/O devices. The list below describes how the various sections of the device could be used in industrial automation.

Microcontroller Subsystem
- Arm Cortex-M3 running Fieldbus protocol stack
- Ethernet MAC – standard protocols

FPGA Fabric
- Multiple RS485 capable UARTs
- PROFIBUS, Modbus, WorldFIP, P-NET
- High speed Manchester encoding/decoding
- CAN

Analog
- ADC for sensing
- DAC for excitation
System Management
System management continues to gain importance in the design of all electronic systems, since smaller process geometries drive more multi-volt devices and are more susceptible to voltage and temperature fluctuations. System management tasks focus on maximizing system uptime, identifying and communicating alert conditions and logging data and alarm conditions. This can be combined with in-system diagnostics and prognostics, not only to help debug systems that have failed, but also to identify potential failures before they arise. Thus, using a SmartFusion device as a system manager provides the designer maximum implementation flexibility.

- Use the sample sequence engine in the ACE to manage system health data collection.
- Use the post-processing engine in the ACE to manage alert condition flag generation.
- Cortex-M3 only needs to make requests to the ACE and respond to interrupts; no processing cycles needed.
- Use FPGA gates for control algorithms when needed.
- Communicate through I2C, UART, SPI or Ethernet for updates and reporting.

Power Management
Microchip’s system management solution significantly reduces the cost and complexity of board-level power management by integrating power converter functions including sequencing, trimming, margining, monitoring and control as well as system management functions like reset generation, event logging and “green” power algorithm support. Targeted to the SmartFusion SoC, there is an abundance of uncommitted analog and FPGA resources available to the user allowing the creation of a true custom solution.

Microchip’s Mixed Signal Power Manager (MPM) reference design version 4.0 further distances itself from the competition by now including support for PMBus based POL converters. No other power management solution seamlessly supports a mix of analog and PMBus based power converters. Now you can sequence, monitor and manage a mixed set of DC/DC converters including LDOs, analog style and the highly efficient PMBus based converters from a single management device.

- Manage up to 64 DC/DC Converters
- Full support for analog and digital POL converters
- Sequence, monitor, margin, trim converters

Leveraging the considerable processing power of the ACE leaves the Cortex-M3 and FPGA gates available for running the actual application or communicating with the outside world. This not only eliminates the need for multiple ASSP devices to perform system management, but prevents system management from being an unnecessary burden on the Bill-of-Materials (BOM) cost. Selecting SmartFusion devices for system management provides flexibility and reliability at the lowest Total Cost of Ownership (TCO).
Hardware Platform Management

nVent Schrroff with their Pigeon Point products, a Microchip partner, helped refine the architecture of SmartFusion devices for hardware platform management. The following SmartFusion-based Board Management Reference (BMR) solutions for the ATCA and VPX board as well as AMC module controller are examples of offerings from nVent Schrroff:

- BMR-A2F-ATCA: IPM Controllers (IPMCs) for ATCA boards
- BMR-A2F-AMCc: Carrier IPMCs for ATCA AMC carrier boards
- BMR-A2F-AMCm: Module Management Controllers for AMC modules
- BMR-A2F-VPX: IPM Controllers (IPMCs) for VPX boards

nVent Schrroff with its Pigeon Point products is the dominant supplier of hardware and firmware solutions for the mandatory hardware platform management controllers that are part of every Telecommunications Computing Architecture board or module and are optional for VITA46/VPX boards.

Key Features of the Hardware Management Solutions

- Advanced Ethernet attachment via built-in Ethernet MAC, supporting serial port access and fast firmware upgrades over LAN
- Optimizations for xTCA/VPX management via the flash FPGA fabric, with the option to integrate additional board- and module-specific functionality
- Advanced analog monitoring using SmartFusion programmable analog
- Complete offloading from the Cortex-M3 of xTCA/VPX-aware analog threshold processing via ACE
- Integration of flexible power management functions eliminating the use of external power devices
- Benchtop implementations for familiarization and as a known good reference during bring-up of a new xTCA/VPX board or module

Medical Systems

Microchip’s system management solution significantly reduces the cost and complexity of board-level power management by integrating power converter functions including sequencing, trimming, margining, monitoring and control as well as system management functions like reset generation, event logging and “green” power algorithm support. Targeted to the Microchip SmartFusion SoC, there is an abundance of uncommitted analog and FPGA resources available to the user allowing the creation of a true custom solution.

Microchip’s Mixed Signal Power Manager (MPM) reference design further distances itself from the competition by now including support for PMBus based POL converters. No other power management solution seamlessly supports a mix of analog and PMBus based power converters. Now you can sequence, monitor and manage a mixed set of DC/DC converters including LDO’s, analog style and the highly efficient PMBus based converters from a single management device.

- Manage up to 64 DC/DC Converters
- Full support for analog and digital POL converters
- Sequence, monitor, margin, trim converters
Design and Data Security

Microchip’s Flash SoCs and FPGAs have always been known for their design security and IP protection. SmartFusion devices bring an even higher level of security to embedded systems.

- Microcontroller and FPGA interface not exposed at board level
- No bitstream to transfer at boot-up
- FlashLock protects against tampering and reprogramming
- AES-encrypted in-system programming
- Protects against overbuilding with programmable device key

Microchip is the first major FPGA company to address the threats caused by side-channel analysis. Side-channel attacks such as Differential Power Analysis (DPA) can endanger the security of the design IP configured into a SoC or FPGA and the security of the end application itself.

Microchip has obtained a license from Cryptograph Research, Inc. (CRI) for the DPA patent portfolio, consisting of more than fifty patents. Contact Microchip sales to order devices that include a license to implement IP based on these patents.

Intellectual Property for SmartFusion SoCs

SmartFusion devices are composed of hard Intellectual Property (IP) blocks, such as an Arm Cortex-M3 processor, UART, SPI, I²C and 10/100 Ethernet interface, as well as standard peripherals, such as ADC, DAC, timers, watchdog timer (WDT) and RTC. Beyond these hard cores you can select from Microchip’s IP Catalog within SmartDesign to add additional free IP to the FPGA fabric of your SmartFusion device, or choose from a wide range of partner cores. Microchip has more than 180 intellectual property products designed and optimized to support communications, consumer, military, industrial, automotive and aerospace markets. Microchip IP solutions streamline your designs, enable faster time-to-market and minimize design costs and risk. The table below shows some examples of the IP available. A complete list of cores is available on the Microchip SoC Products Group website: https://www.microsemi.com/product-directory/design-resources/5092-ip-cores

<table>
<thead>
<tr>
<th>General Purpose</th>
<th>Cryptography</th>
<th>Communication</th>
<th>MIL-STD-1553B</th>
<th>DSP IP Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 16550</td>
<td>CoreUART</td>
<td>CoreAES128</td>
<td>CorePCIF</td>
<td>Core1553BRM</td>
</tr>
<tr>
<td>CoreGPIO</td>
<td>Core2C</td>
<td>CoreDES</td>
<td>CoreSDR/DDR</td>
<td>Core1553BRT</td>
</tr>
<tr>
<td>CoreTimer</td>
<td>CoreSPI</td>
<td>Core3DES</td>
<td>Core429</td>
<td>Core1553BRT-EBR</td>
</tr>
<tr>
<td>CoreSDR</td>
<td>CorePWM</td>
<td>Fast SHA-256 Hash1</td>
<td>InCAN2</td>
<td>Core1553BBC</td>
</tr>
</tbody>
</table>

1. For more information, see the Helion Technology partner page: www.microsemi.com/soc/products/partners/companioncore/helion.aspx.
2. For more information, see the Inicore partner page: www.microsemi.com/soc/products/partners/companioncore/inicore.aspx.

Microchip IP cores can be accessed through Libero SoC via the SmartDesign IP catalog. Drivers for the processor supported IP cores are available through the Firmware Catalog and are extracted automatically for SmartFusion designs through the MSS Configurator dialog.

For more details on the Microchip IP Core offerings, please refer IP DirectCores webpage: https://www.microsemi.com/products/fpga-soc/design-resources/ip-cores/direct-cores
SmartFusion Evaluation Kit

- Supports SmartFusion evaluation, including Arm Cortex-M3, FPGA and programmable analog
- Two USB cables
- Online user's guide, tutorial and design examples
- Printed Circuit Board (PCB) schematics, layout files and Bill-of-Materials (BOM)
- Board features
- Ethernet interface

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Supported Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2F-EVAL-KIT-2</td>
<td>A2F200M3F-FGG484</td>
</tr>
</tbody>
</table>

SmartFusion Development Kit

- Supports SmartFusion development, including Arm Cortex-M3, FPGA and programmable analog
- 5V power supply and international adapters
- Two USB cables
- Online user's guide, tutorial and design examples
- PCB schematics, layout files and BOM
- Board features
- Ethernet, CAN, UART, i²C and SPI interfaces
- USB port for HyperTerminal
- J-Link header for debug
- Mixed signal header
- SPI Flash – off-chip memory
- Reset and 2 user switches, 8 LEDs
- POT for voltage/current monitor
- Temperature monitor

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Supported Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2F500-DEV-KIT-2</td>
<td>A2F500M3G-FGG484</td>
</tr>
</tbody>
</table>

Digital Mixed-Signal Power Manager (DMPM) Daughter Card Kit

- Supports power management design with the SmartFusion Evaluation Kit and SmartFusion Development Kit
- MPM 4.0 design example implements configurable power management in SmartFusion
- Graphical configuration dialog
- In-system reconfigurable
- 9V power supply
- Board features
- 2 analog PoL
- 3 digital PoL with PMB support
- 5 power supply regulator interrupt switches
- 5 power supply regulator status LEDs
- Mixed signal header connector connects to SmartFusion board

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Supported Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMPM-DC-KIT</td>
<td>No Microchip Device on Daughtercard</td>
</tr>
</tbody>
</table>
## SmartFusion Family Product Table

<table>
<thead>
<tr>
<th>SmartFusion® Devices</th>
<th>A2F200</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FPGA Fabric</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Gates</td>
<td>200,000</td>
<td>500,000</td>
</tr>
<tr>
<td>Tiles (D-flip-flops)</td>
<td>4,608</td>
<td>11,520</td>
</tr>
<tr>
<td>RAM Blocks (4,608 bits)</td>
<td>8</td>
<td>24</td>
</tr>
<tr>
<td><strong>Microcontroller Subsystem (MSS)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash (Kbytes)</td>
<td>256</td>
<td>512</td>
</tr>
<tr>
<td>SRAM (Kbytes)</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>Cortex®-M3 with Memory Protection Unit (MPU)</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>10/100 Ethernet MAC</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>External Memory Controller (EMC)</td>
<td>26-bit address, 16-bit data</td>
<td>26-bit address, 16-bit data</td>
</tr>
<tr>
<td><strong>Microcontroller Subsystem (MSS)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA</td>
<td>8 Ch</td>
<td>8 Ch</td>
</tr>
<tr>
<td>I²C</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>SPI</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>16550 UART</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>32-bit Timer</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>PLL</td>
<td>1</td>
<td>22</td>
</tr>
<tr>
<td>32 KHz Low Power Oscillator</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>100 MHz On-Chip RC Oscillator</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Main Oscillator (32 KHz to 20 MHz)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Programmable Analog</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADCs (8-/10-/12-bit SAR)</td>
<td>2</td>
<td>34</td>
</tr>
<tr>
<td>DACs (12-bit sigma-delta)</td>
<td>2</td>
<td>34</td>
</tr>
<tr>
<td>Signal Conditioning Blocks (SCBs)</td>
<td>4</td>
<td>54</td>
</tr>
<tr>
<td>Comparators³</td>
<td>8</td>
<td>104</td>
</tr>
<tr>
<td>Current Monitors³</td>
<td>4</td>
<td>54</td>
</tr>
<tr>
<td>Temperature Monitors³</td>
<td>4</td>
<td>54</td>
</tr>
<tr>
<td>Bipolar High Voltage Monitors³</td>
<td>8</td>
<td>104</td>
</tr>
</tbody>
</table>

### 1. Not available on A2F500 for the PQ208 package.  
### 2. Two PLLs are available in CS288 and FG484 (one PLL in FG256 and PQ208).  
### 3. These functions share I/O pins and may not all be available at the same time.  
### 4. Available on FG484 only. PQ208, FG256, and CS288 packages offer the same programmable analog capabilities as A2F200.

### Package I/Os: MSS + FPGA I/Os

<table>
<thead>
<tr>
<th>Device</th>
<th>A2F200</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PQ208</td>
<td>CS288</td>
</tr>
<tr>
<td>Direct Analog Input</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Shared Analog Input¹</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Total Analog Input</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Total Analog output</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>MSS I/Os²³</td>
<td>22</td>
<td>31</td>
</tr>
<tr>
<td>FPGA I/Os</td>
<td>66</td>
<td>78</td>
</tr>
<tr>
<td>Total I/Os</td>
<td>113</td>
<td>135</td>
</tr>
</tbody>
</table>

### 1. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.  
### 2. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for the MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, 3.3V) standards.  
### 3. 9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, 3.3V) standards.  
### 4. EMC is not available on the A2F500 PQ208 package.  
### 5. Military temperature grade (−55°C to +125°C) devices are offered in some density and package combinations as noted.
Support
Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit www.microchip.com:
- Technical Support: www.microchip.com/support
- Evaluation samples of any Microchip device: www.microchip.com/sample
- Knowledge base and peer help: www.microchip.com/forums
- Sales and Global Distribution: www.microchip.com/sales

Training
If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.
- Overview of Technical Training Resources: www.microchip.com/training
- MASTERS Conferences: www.microchip.com/mastrs
- Developer Help Website: www.microchip.com/developerhelp
- Technical Training Centers: www.microchip.com/seminars