April 26, 2006

PCN Number: 0606

PCN Change level: Major

Subject: A3P400 Pinout Changes

Dear Customer,

This PCN provides information on changes in the pinouts for A3P400-PQ208, A3P400-FG256, and A3P400-FG484 (Table 1 through Table 3 on page 3). The pinout changes will be incorporated in Actel Libero® Integrated Design Environment (IDE) v7.2, which will be available June 12th. The datasheet for the product family will be changed by April 28th. Following is a summary of the changes.

Device: A3P400-PQ208

Changes include the following:

- I/O differential pair moved from pins 37-38 to pins 38-39

- Single-ended I/O moved from pin 39 to pin 37

- Second VMV2 was added to pin 53 (previously NC)

- I/O differential pair was added to pins 127 and 128 (previously two separate single-ended I/Os)

- Second VMV0 was added to pin 157 (previously NC)

Note: Since an I/O differential pair can be used as two individual single-ended I/Os, the change on pins 127-128 allows an additional differential I/O without changing the number of single-ended I/Os.

Table 1. Pinout Changes for A3P400-PQ208

OLD		NEW	
Pin#	**Pin Name**	**Pin#**	**Pin Name**
37	IO14PDB3	37	IO141PSB3
38	IO141NDB3	38	IO140PDB3
39	IO140PSB3	39	IO140NDB3
53	NC	53	VMV2
127	IO73PSB1	127	IO72NDB1
128	GCC2/IO72PSB1	128	GCC2/IO72PDB1
157	NC	157	VMV0

Device: A3P400-FG256

Changes include the following:

- Bank change was made to maximize I/O compatibility in east/west banks with larger devices

- Second VMV0 was added to pin C14 (previously user I/O)

- Second VMV2 was added to pin P3 (previously user I/O)

- Additional user I/Os were added to pins F3 and F14 (previously NC)

Table 2. Pinout Changes for A3P400-FG256

OLD		NEW	
Pin#	Pin Name	Pin#	Pin Name
C2	IO08RSB0	C2	IO155VDB3
C14	IO52RSB0	C14	VMV0
C15	IO53RSB0	C15	IO61NPB1
D15	IO63NDB1	D15	IO53RSB0
E4	IO11RSB0	E4	IO152VDB3
E15	IO63PDB1	E15	IO52RSB0
F3	NC	F3	IO09RSB0
F14	NC	F14	IO49RSB0
K4	IO138PDB3	K4	IO120RSB2
L3	IO139RSB3	L3	IO125RSB2
M2	IO140PDB3	M2	IO130RSB2
M3	IO127RSB2	M3	IO138NPB3
N2	IO131RSB2	N2	IO138PPB3
P3	IO130RSB2	P3	VMV2

Device: A3P400-FG484

Changes include the following:

- Bank change was made to maximize I/O compatibility in east/west banks with larger devices

- Second VMV0 was added to pin F17 (previously user I/O)

- Second VMV2 was added to pin U6 (previously user I/O)

- Added user I/Os were added to pins J6 and J17 (previously NC)

Table 3. Pinout Changes for A3P400-FG484

OLD		NEW	
Pin#	**Pin Name**	**Pin#**	**Pin Name**
E19	IO50RSB0	E19	IO60NDB1
F17	IO52RSB0	F17	VMV0
F18	IO53RSB0	F18	IO61NPB1
F5	IO08RSB0	F5	IO155VDB3
G18	IO63NDB1	G18	IO53RSB0
H18	IO63PDB1	H18	IO52RSB0
H5	IO152PPB3	H5	IO08RSB0
H7	IO11RSB0	H7	IO152VDB3
N7	IO138PDB3	N7	IO120RSB2
P6	IO139RSB3	P6	IO125RSB2
R6	IO127RSB2	R6	IO138NPB3
T5	IO131RSB2	T5	IO138PPB3
U6	IO130RSB2	U6	VMV2
J6	NC	J6	IO09RSB0
J17	NC	J17	IO49RSB0

If you have questions, please contact the Actel Corporate Application hotline at tech@actel.com.

Regards,

Actel Corporation