Actel®

PCN Number: 0605

PCN Change Level: Minor

April 13, 2006

Subject: Changes to the ProASIC^{PLUS}® Specification

Dear Customer,

This letter is to inform you that there are two minor specification changes to all devices in ProASIC^{PLUS} family. These changes pertain to the ProASIC^{PLUS} Phase-Locked Loop (PLL) and Clock Conditioning Circuits (CCC).

Please note: NO CHANGE has been made to the devices themselves. The purpose of this notification is to clarify device operation.

The first change refers to the phase select output on the GLB output. ProASIC^{PLUS} family will only support 0° and 180° phase shift between output clock GLA and GLB. As an alternative to using the 90° and 270° phase shift functions, you can set specific PLL delays manually using SmartGen. This change will be reflected in the Libero® Integrated Design Environment (IDE) v7.2 release. Existing designs in conflict with the revised specification will have the phase select changed to the default setting of 0°.

The second issue involves the output clock dividers (OADIV and OBDIV) of the CCC blocks. When the value of either one of these dividers is not equal to 1, then the phase shift of the corresponding signal is indeterminate. Libero IDE v7.2 will issue a warning and a note in the log file, indicating that the output clock may not have the desired phase.

For further information, please contact the Actel applications department by emailing tech@actel.com.

Regards

Actel Corporation