April 9, 2010

Customer Alert

Subject: ProASIC®3 nano Datasheet update

Dear Customer,

This notice is to inform you that the ProASIC3 nano datasheet has been updated. The updated datasheet can be downloaded from the Actel website: http://www.actel.com/documents/PA3_nano_DS.pdf.

A list of changes are described in the table below.

Changes	Page
References to differential inputs were removed from the datasheet, since ProASIC3 nano devices do not support differential inputs (SAR 21449).	N/A
The "ProASIC3 nano Device Status" table is new.	II
The JTAG DC voltage was revised in Table 2-2 • Recommended Operating Conditions (SAR 24052). The maximum value for VPUMP programming voltage (operation mode) was changed from 3.45 V to 3.6 V (SAR 25220).	2-2
The highest temperature in Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was changed to 100ºC.	2-5
The typical value for A3PN010 was revised in Table 2-7 • Quiescent Supply Current Characteristics. The note was revised to remove the statement that values do not include I/O static contribution.	2-6

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Changes	Page
The following tables were updated with available information: Table 2-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Table 2-10 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 nano Devices Table 2-14 • Summary of Maximum and Minimum DC Input and Output Levels Table 2-18 • Summary of I/O Timing Characteristics—Software Default Settings (at 35 pF) Table 2-19 • Summary of I/O Timing Characteristics—Software Default Settings (at 10 pF)	2-6 through 2-18
Table 2-22 • I/O Weak Pull-Up/Pull-Down Resistances was revised to add wide range data and correct the formulas in the table notes (SAR 21348).	2-19
The text introducing Table 2-24 • Duration of Short Circuit Event before Failure was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table.	2-20
Table 2-26 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was revised to give values with Schmitt trigger disabled and enabled (SAR 24634). The temperature for reliability was changed to 100ºC.	2-21
Table 2-33 • Minimum and Maximum DC Input and Output Levels for 3.3 V LVCMOS Wide Range and the timing tables in the "Single-Ended I/O Characteristics" section were updated with available information. The timing tables for 3.3 V LVCMOS wide range are new.	2-22
The following sentence was deleted from the "2.5 V LVCMOS" section: "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-30
Values for $t_{DDRISUD}$ and $F_{DDRIMAX}$ were updated in Table 2-62 • Input DDR Propagation Delays. Values for F_{DDOMAX} were added to Table 2-64 • Output DDR Propagation Delays (SAR 23919).	2-46, 2-48
Table 2-67 • A3PN010 Global Resource through Table 2-70 • A3PN060 Global Resource were updated with available information.	2-54 through 2-55
Table 2-73 • ProASIC3 nano CCC/PLL Specification was revised (SAR 79390).	2-57
Table 2-2 • Recommended Operating Conditions was revised to add VMV to the VCCI row. The following table note was added: "VMV pins must be connected to the corresponding VCCI pins."	2-2
The values in Table 2-7 • Quiescent Supply Current Characteristics were revised for A3PN010, A3PN015, and A3PN020.	2-6

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Changes	Page
A table note, “All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification,” was added to Table 2-14 • Summary of Maximum and Minimum DC Input and Output Levels, Table 2-18 • Summary of I/O Timing Characteristics—Software Default Settings (at 35 pF), and Table 2-19 • Summary of I/O Timing Characteristics—Software Default Settings (at 10 pF).	2-16, 2-18
3.3 V LVCMOS Wide Range was added to Table 2-21 • I/O Output Buffer Maximum Resistances and Table 2-23 • I/O Short Currents I_{OSH}/I_{OSL}.	2-19, 2-20
The “48-Pin QFN” pin diagram was revised.	3-2
Note 2 for the “48-Pin QFN”, “68-Pin QFN”, and “100-Pin VQFP” pin diagrams was added/changed to “The die attach paddle of the package is tied to ground (GND).”	3-2, 3-5, 3-9
The “100-Pin VQFP” pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner.	3-9

For questions please contact the Actel Technical Support hotline at tech@actel.com.

Regards,

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