April 9, 2010

Customer Alert

Subject: IGLOO® nano Datasheet update

Dear Customer,

This notice is to inform you that the IGLOO nano datasheet has been updated. The updated datasheet can be downloaded from the Actel website: http://www.actel.com/documents/IGLOO_nano_DS.pdf.

A list of changes are described in the table below.

Change	Page
References to differential inputs were removed from the datasheet, since IGLOO nano devices do not support differential inputs (SAR 21449).	N/A
A parenthetical note, "hold previous I/O state in Flash*Freeze mode," was added to each occurrence of bus hold in the datasheet (SAR 24079).	N/A
The “In-System Programming (ISP) and Security” section was revised to add 1.2 V programming.	I
The note connected with the “IGLOO nano Ordering Information” table was revised to clarify features not available for Z feature grade devices.	III
The “IGLOO nano Device Status” table is new.	II
The definition of C in the “Temperature Grade Offerings” table was changed to “extended commercial temperature range.”	IV
1.2 V wide range was added to the list of voltage ranges in the “I/Os with Advanced I/O Standards” section.	1-8
A note was added to Table 2-2 • Recommended Operating Conditions regarding switching from 1.2 V to 1.5 V core voltage for in-system programming. The VJTAG voltage was changed from “1.425 to 3.6" to “1.4 to 3.6" (SAR 24052). The note regarding voltage for programming V2 and V5 devices was revised (SAR 25213). The maximum value for VPUMP programming voltage (operation mode) was changed from 3.45 V to 3.6 V (SAR 25220).	2-2

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Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated. Table 2-8 • Power Supply State per Mode is new.	2-6, 2-7
The tables in the "Quiescent Supply Current" section were updated (SAR 24882 and SAR 24112).	2-7
VJTAG was removed from Table 2-10 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO nano Sleep Mode* (SARs 24112, 24882, and 79503).	2-8
The note stating what was included in I_{DD} was removed from Table 2-11 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO nano Shutdown Mode. The note, "per VCCI or VJTAG bank" was removed from Table 2-12 • Quiescent Supply Current (I_{DD}), No IGLOO nano Flash*Freeze Mode[1]. The note giving I_{DD} was changed to "$I_{DD} = N_{BANKS} * I_{CCI} + I_{CCA}$."	2-8
The values in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] were updated. Wide range support information was added.	2-9
The following tables were updated with current available information. The equivalent software default drive strength option was added. Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-28 • I/O Output Buffer Maximum Resistances [1] Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances Table 2-30 • I/O Short Currents IOSH/IOSL Timing tables in the "Single-Ended I/O Characteristics" section, including new tables for 3.3 V and 1.2 V LVCMOS wide range. Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Table 2-63 • Minimum and Maximum DC Input and Output Levels Table 2-67 • Minimum and Maximum DC Input and Output Levels (new)	2-19 through 2-40
The formulas in the notes to Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised (SAR 21348).	2-24
The text introducing Table 2-31 • Duration of Short Circuit Event before Failure was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table.	2-25

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The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5-V tolerant input buffer and push-pull output buffer."	2-32
The $F_{DDRIMAX}$ and F_{DDOMAX} values were added to tables in the "DDR Module Specifications" section (SAR 23919). A note was added stating that DDR is not supported for AGLN010, AGLN015, and AGLN020.	2-51
Tables in the "Global Tree Timing Characteristics" section were updated with new information available.	2-64
Table 2-101 • IGLOO nano CCC/PLL Specification and Table 2-102 • IGLOO nano CCC/PLL Specification were revised (SAR 79390).	2-70, 2-71
Tables in the SRAM "Timing Characteristics" section and FIFO "Timing Characteristics" section were updated with new information available.	2-77, 2-84
Table 3-3 • TRST and TCK Pull-Down Recommendations is new.	3-5
A note was added to the "81-Pin CS" pin tables for AGLN060, AGLN060Z, AGLN125, AGLN125Z, AGLN250, and AGLN250Z indicating that pins F1 and F2 must be grounded (SAR 25007).	3-9, through 3-14
A note was added to the "81-Pin CS" and "100-Pin VQFP" pin tables for AGLN060 and AGLN060Z stating that bus hold is not available for pin H7 or pin 45 (SAR 24079).	3-9, 3-24
The AGLN250 function for pin C8 in the "81-Pin CS" table was revised (SAR 22134).	3-13

For questions please contact the Actel Technical Support hotline at tech@actel.com.

Regards,

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